SST25VF016B

16-Mbit SPI Serial Flash

Features

- Single Voltage Read and Write Operations:
  - 2.7V-3.6V
- Serial Interface Architecture:
  - SPI Compatible: Mode 0 and Mode 3
- High-Speed Clock Frequency:
  - Up to 50 MHz
- Superior Reliability:
  - Endurance: 100,000 cycles (typical)
  - Greater than 100 years data retention
- Low Power Consumption:
  - Active Read Current: 10 mA (typical)
  - Standby Current: 5 µA (typical)
- Flexible Erase Capability:
  - Uniform 4-KByte sectors
  - Uniform 32-KByte overlay blocks
  - Uniform 64-KByte overlay blocks
- Fast Erase and Byte Program:
  - Chip Erase time: 35 ms (typical)
  - Sector/Block Erase time: 18 ms (typical)
  - Byte Program time: 7 µs (typical)
- Auto Address Increment (AAI) Programming:
  - Decrease total chip programming time over Byte Program operations
- End-of-Write Detection:
  - Software polling the BUSY bit in STATUS register
  - Busy Status readout on SO pin in AAI Mode
- Hold Pin (HOLD#):
  - Suspends a serial sequence to the memory without deselecting the device
- Write Protection (WP#):
  - Enables/Disables the Lock-Down function of the STATUS register
- Software Write Protection:
  - Write protection through Block Protection bits in STATUS register
- Temperature Range:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
- All devices are RoHS compliant

Packages

- 8-Lead SOIC (200 mils) and 8-Contact WSON (6 mm x 5 mm)

Product Description

The 25 Series Serial Flash family features a four-wire, SPI-compatible interface that allows for a low pin count package which occupies less board space and ultimately lowers total system costs. The SST25VF016B devices are enhanced with improved operating frequency and even lower power consumption than the original SST25VFxxxA devices. SST25VF016B SPI Serial Flash memories are manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

SST25VF016B devices significantly improve performance and reliability while lowering power consumption. The devices write (Program or Erase) with a single power supply of 2.7V-3.6V for SST25VF016B. The total energy consumed is a function of the applied voltage, current and time of application. For any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time. As a result, the total energy consumed during any Erase or Program operation is less than alternative Flash memory technologies.

See Figure 2-1 for pin assignments.

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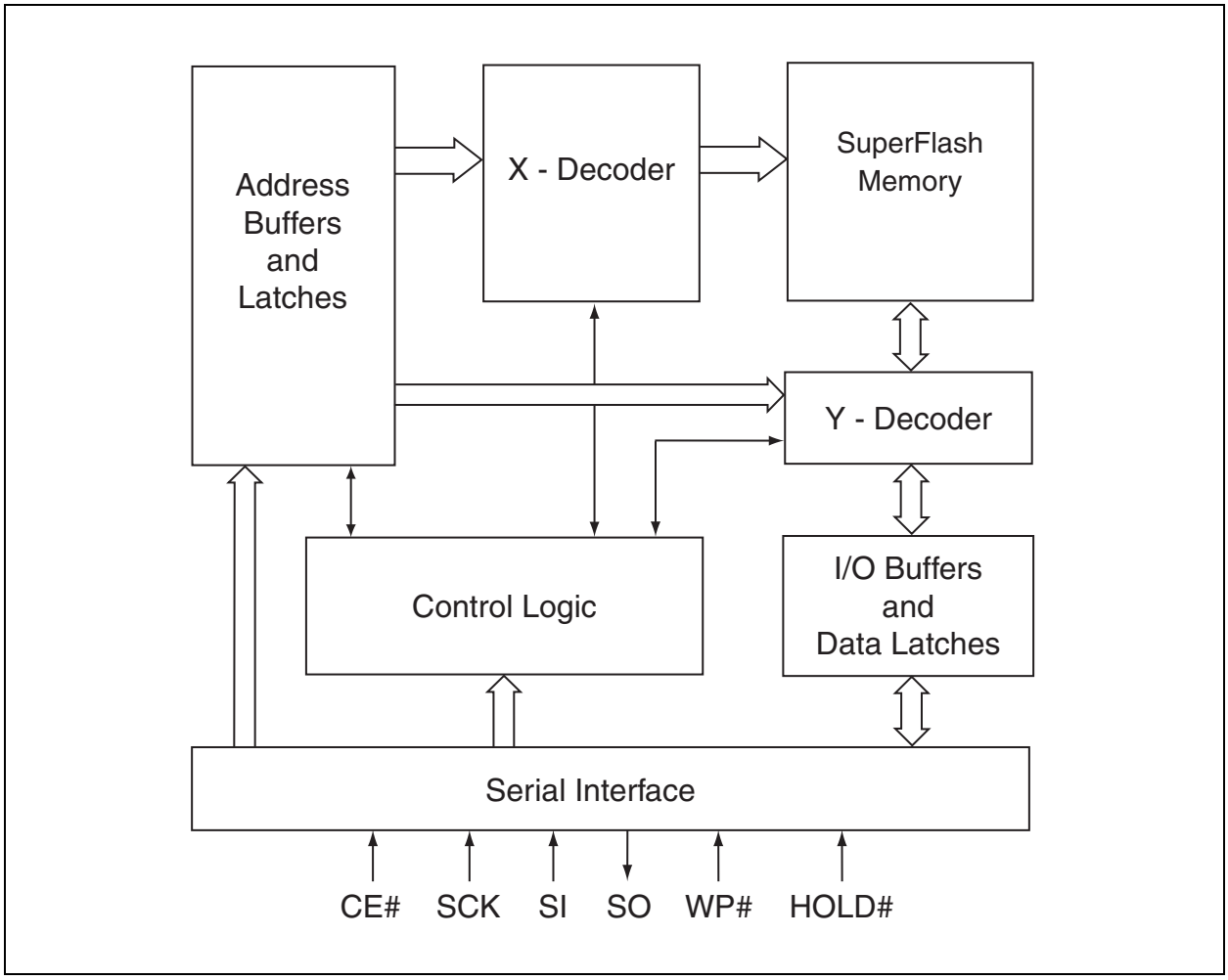
1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION

FIGURE 2-1: PIN ASSIGNMENTS

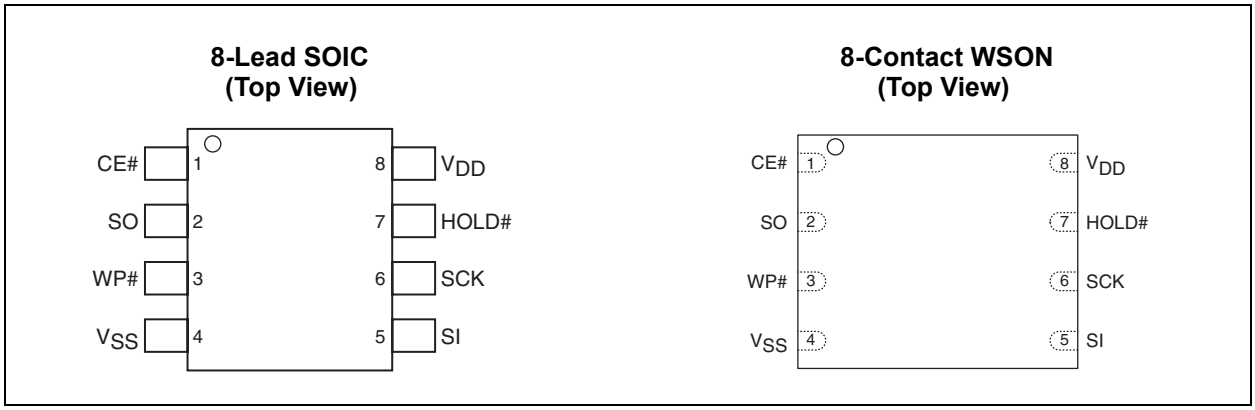


TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses or input data are latched on the rising edge of the clock input, while output data are shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data are shifted out on the falling edge of the serial clock. Outputs Flash busy status during AAI Programming when reconfigured as RY/BY# pin. See **Section 4.4.6 "Hardware End-of-Write Detection"** for details.
CE#	Chip Enable	The device is enabled by a high-to-low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	The Write-Protect (WP#) pin is used to enable/disable the BPL bit in the STATUS register.
HOLD#	Hold	To temporarily stop serial communication with SPI Flash memory without resetting the device.
V_{DD}	Power Supply	To provide power supply voltage: 2.7V-3.6V for SST25VF016B
V_{SS}	Ground	

3.0 MEMORY ORGANIZATION

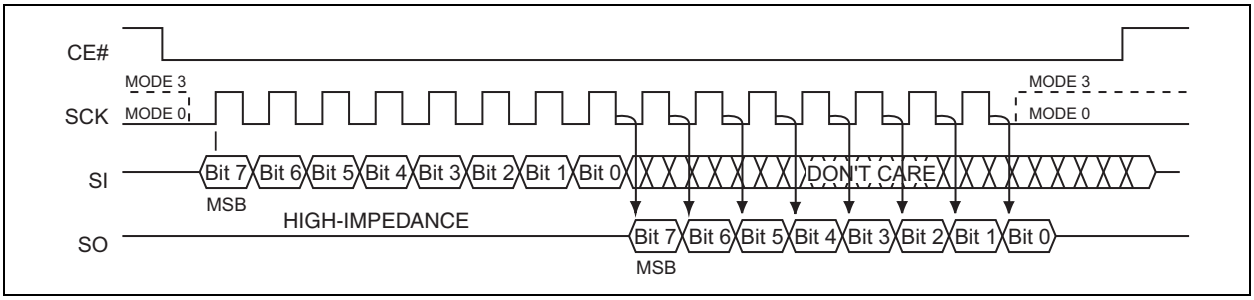
The SST25VF016B SuperFlash memory array is organized in uniform 4-KByte erasable sectors with 32-KByte overlay blocks and 64-KByte overlay erasable blocks.

4.0 DEVICE OPERATION

The SST25VF016B is accessed through the Serial Peripheral Interface (SPI) bus compatible protocol. The SPI bus consists of four control lines: Chip Enable (CE#) is used to select the device, and data are accessed through the Serial Data Input (SI), Serial Data Output (SO) and Serial Clock (SCK).

The SST25VF016B supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 4-1, is the state of the SCK signal when the bus host is in Standby mode and no data are being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

FIGURE 4-1: SPI PROTOCOL



4.1 Hold Operation

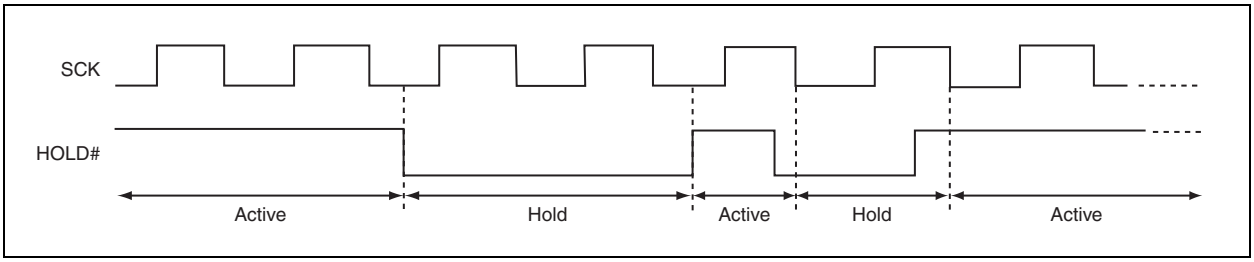
The HOLD# pin is used to pause a serial sequence underway with the SPI Flash memory without resetting the clocking sequence. To activate HOLD# mode, CE# must be in active-low state. Hold mode begins when the SCK active-low state coincides with the falling edge of the HOLD# signal. Hold mode ends when the HOLD# signal's rising edge coincides with the SCK active-low state.

If the falling edge of the HOLD# signal does not coincide with the SCK active-low state, then the device enters Hold mode when the SCK next reaches the active-low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active-low state, then the device exits in Hold mode when the SCK next reaches the active-low state. See Figure 4-2 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven active-high during a Hold condition, it resets the internal logic of the device. As long as the HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active-high and CE# must be driven active-low. See Figure 5-3 for Hold timing.

FIGURE 4-2: HOLD CONDITION WAVEFORM



4.2 Write Protection

The SST25VF016B device provides software Write protection. The Write-Protect pin (WP#) enables or disables the lock-down function of the STATUS register. The Block Protection bits (BP3, BP2, BP1, BP0 and BPL) in the STATUS register provide Write protection to the memory array and the STATUS register. See Table 4-3 for the Block Protection description.

4.2.1 WRITE PROTECT PIN (WP#)

The Write-Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the STATUS register. When WP# is driven low, the execution of the Write Status Register (WRSR) instruction is determined by the value of the BPL bit (see Table 4-1). When WP# is high, the lock-down function of the BPL bit is disabled.

TABLE 4-1: CONDITIONS TO EXECUTE WRITE STATUS REGISTER (WRSR) INSTRUCTION

WP#	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

4.3 STATUS Register

The software STATUS register provides status on whether the Flash memory array is available for any Read or Write operation, whether the device is write enabled, and the state of the memory write protected. During an internal Erase or Program operation, the STATUS register may be read only to determine the completion of an operation in progress. Table 4-2 describes the function of each bit in the software STATUS register.

TABLE 4-2: SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (see Table 4-3)	1	R/W
3	BP1	Indicate current level of block write protection (see Table 4-3	1	R/W
4	BP2	Indicate current level of block write protection (see Table 4-3)	1	R/W
5	BP3	Indicate current level of block write protection (see Table 4-3)	0	R/W
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte Program mode	0	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are read/writable	0	R/W

4.3.1 BUSY

The Busy bit determines whether there is an internal Erase or Program operation in progress. A '1' for the Busy bit indicates the device is busy with an operation in progress. A '0' indicates the device is ready for the next valid operation.

4.3.2 WRITE ENABLE LATCH (WEL)

The Write Enable Latch (WEL) bit indicates the status of the internal memory Write Enable Latch. If the Write Enable Latch bit is set to '1', it indicates the device is write enabled. If the bit is set to '0' (Reset), it indicates the device is not write enabled and does not accept any memory Write (Program/Erase) commands. The Write Enable Latch bit is automatically reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Byte Program instruction completion
- Auto Address Increment (AAI) programming is completed or reached its highest unprotected memory address
- Sector Erase instruction completion
- Block Erase instruction completion
- Chip Erase instruction completion
- Write Status Register instruction completion

4.3.3 AUTO ADDRESS INCREMENT (AAI)

The Auto Address Increment Programming Status bit provides status on whether the device is in Auto Address Increment (AAI) programming mode or Byte Program mode. The default at power-up is Byte Program mode.

4.3.4 BLOCK PROTECTION (BP3, BP2, BP1, BP0)

The Block Protection (BP3, BP2, BP1, BP0) bits define the size of the memory area, as defined in Table 4-3, to be software protected against any memory Write (Program or Erase) operation. The Write Status Register (WRSR) instruction is used to program the BP3, BP2, BP1 and BP0 bits as long as WP# is high or the Block Protect Lock (BPL) bit is '0'. Chip Erase can only be executed if Block Protection bits are all '0'. After power-up, BP3, BP2, BP1 and BP0 are set to '1'.

4.3.5 BLOCK PROTECTION LOCK-DOWN (BPL)

WP# pin driven low (V_{IL}) enables the Block Protection Lock-Down (BPL) bit. When BPL is set to '1', it prevents any further alteration of the BPL, BP3, BP2, BP1, and BP0 bits. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect and its value is "don't care". After power-up, the BPL bit is reset to '0'.

TABLE 4-3: SOFTWARE STATUS REGISTER BLOCK PROTECTION FOR SST25VF016B

Protection Level	STATUS Register Bit(1)				Protected Memory Address
	BP3	BP2	BP1	BP0	16 Mbit
None	X(2)	0	0	0	None
Upper 1/32	X(2)	0	0	1	1F0000H-1FFFFFH
Upper 1/16	X(2)	0	1	0	1E0000H-1FFFFFH
Upper 1/8	X(2)	0	1	1	1C0000H-1FFFFFH
Upper 1/4	X(2)	1	0	0	180000H-1FFFFFH
Upper 1/2	X(2)	1	0	1	100000H-1FFFFFH
All Blocks	X(2)	1	1	0	000000H-1FFFFFH
All Blocks	X(2)	1	1	1	000000H-1FFFFFH

Note 1: Default at power-up for BP2, BP1 and BP0 is '111'. (all blocks protected).

2: X = "don't care" (Reserved) default is '0'.

4.4 Instructions

Instructions are used to read, write (Erase and Program) and configure the SST25VF016B. The instruction bus cycles are 8 bits each for commands (Op Code), data and addresses. Prior to executing any Byte Program, Auto Address Increment (AAI) programming, Sector Erase, Block Erase, Write Status Register or Chip Erase instructions, the Write Enable (WREN) instruction must be executed first. The complete list of instructions is provided in Table 4-4. All instructions are synchronized off a high-to-low transition of CE#.

Inputs will be accepted on the rising edge of SCK starting with the Most Significant bit (MSb). CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read ID and Read Status Register instructions). Any low-to-high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and

return the device to Standby mode. Instruction commands (Op Code), addresses and data are all input from the Most Significant bit (MSb) first.

TABLE 4-4: DEVICE OPERATION INSTRUCTIONS

Instruction	Description	Op Code Cycle(1)	Address Cycle(s)(2)	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
Read	Read Memory at 25 MHz	0000 0011b (03H)	3	0	1 to ∞	25 MHz
High Speed Read	Read Memory at 50 MHz	0000 1011b (0BH)	3	1	1 to ∞	50 MHz
4-KByte Sector Erase(3)	Erase 4 KBytes of Memory Array	0010 0000b (20H)	3	0	0	50 MHz
32-KByte Block Erase(4)	Erase 32-KByte Block of Memory Array	0101 0010b (52H)	3	0	0	50 MHz
64-KByte Block Erase(5)	Erase 64-KByte Block of Memory Array	1101 1000b (D8H)	3	0	0	50 MHz
Chip Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0	50 MHz
Byte Program	Program One Data Byte	0000 0010b (02H)	3	0	1	50 MHz
AAI Word Program(6)	Auto Address Increment Programming	1010 1101b (ADH)	3	0	2 to ∞	50 MHz
RDSR(7)	Read Status Register	0000 0101b (05H)	0	0	1 to ∞	50 MHz
EWSR	Enable Write Status Register	0101b 0000b (50H)	0	0	0	50 MHz
WRSR	Write Status Register	0000 0001b (01H)	0	0	1	50 MHz
WREN	Write Enable	0000 0110b (06H)	0	0	0	50 MHz
WRDI	Write Disable	0000 0100b (04H)	0	0	0	50 MHz
RDID(8)	Read ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞	50 MHz
JEDEC ID	JEDEC ID Read	1001 1111b (9FH)	0	0	3 to ∞	50 MHz
EBSY	Enable SO to output RY/BY# status during AAI programming	0111 0000b (70H)	0	0	0	50 MHz
DBSY	Disable SO as RY/BY# status during AAI programming	1000 0000b (80H)	0	0	0	50 MHz

Note 1: One bus cycle is eight clock periods.

2: Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.

3: 4-KByte Sector Erase addresses: use A_{MS}-A_{12}, remaining addresses are “don’t care” but must be set either at V_{IL} or V_{IH}.

4: 32-KByte Block Erase addresses: use A_{MS}-A_{15}, remaining addresses are “don’t care” but must be set either at V_{IL} or V_{IH}.

5: 64-KByte Block Erase addresses: use A_{MS}-A_{16}, remaining addresses are “don’t care” but must be set either at V_{IL} or V_{IH}.

6: To continue programming to the next sequential address location, enter the 8-bit command, ADH, followed by 2 bytes of data to be programmed. Data Byte 0 will be programmed into the initial address [A_{23}-A_1] with A_0 = 0, Data Byte 1 will be programmed into the initial address [A_{23}-A_1] with A_0 = 1.

7: The Read Status Register is continuous with ongoing clock cycles until terminated by a low-to-high transition on CE#.

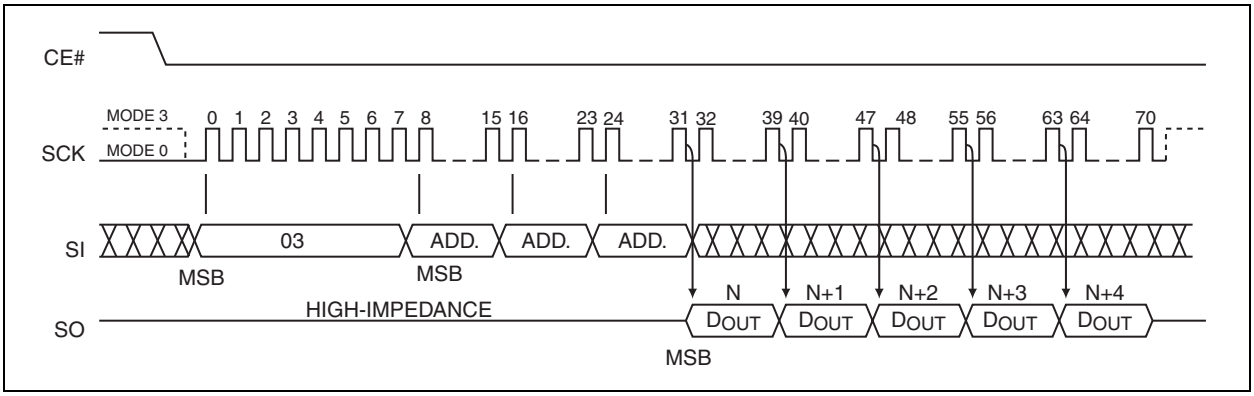
8: Manufacturer’s ID is read with A_0 = 0, and Device ID is read with A_0 = 1. All other address bits are 00H. The Manufacturer’s ID and device ID output stream is continuous until terminated by a low-to-high transition on CE#.

4.4.1 READ (25 MHZ)

The Read instruction, 03H, supports up to 25 MHz Read. The device outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer will automatically increment to the beginning (wrap-around) of the address space. Once the data from address location 1FFFFFH have been read, the next output will be from address location 000000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits [A_{23}-A_0]. CE# must remain active-low for the duration of the Read cycle. See Figure 4-3 for the Read sequence.

FIGURE 4-3: READ SEQUENCE



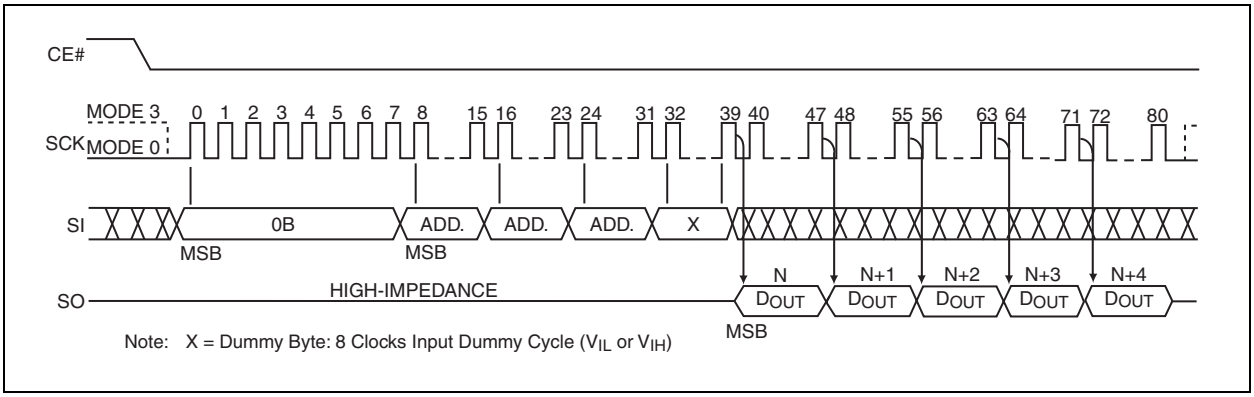
4.4.2 HIGH-SPEED READ (50 MHZ)

The High-Speed Read instruction supporting up to 50 MHz Read is initiated by executing an 8-bit command, 0BH, followed by address bits [A_{23}-A_0] and a dummy byte. CE# must remain active-low for the duration of the High-Speed Read cycle. See Figure 4-4 for the High-Speed Read sequence.

Following a dummy cycle, the High-Speed Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer will automatically increment to the beginning (wrap-around) of the address space. Once the data from address location 1FFFFFH have been read, the next output will be from address location 000000H.

FIGURE 4-4: HIGH-SPEED READ SEQUENCE



Note: X = Dummy Byte: 8 Clocks Input Dummy Cycle (V_{IL} or V_{IH})

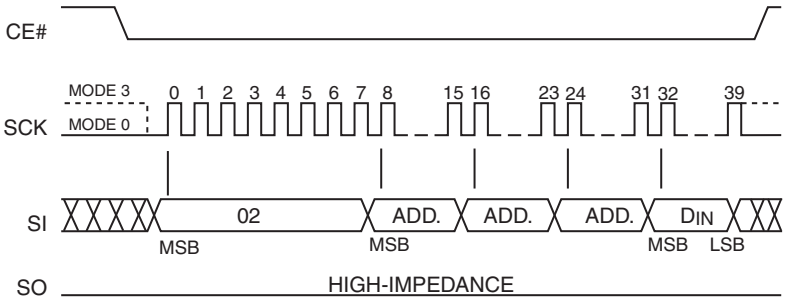
4.4.3 BYTE PROGRAM

The Byte Program instruction programs the bits in the selected byte to the desired data. The selected byte must be in the erased state (FFH) when initiating a program operation. A Byte Program instruction applied to a protected memory area will be ignored.

Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Byte Program instruction.

The Byte Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits [A_{23}-A_0]. Following the address, the data are input in order from MSb (bit 7) to LSb (bit 0). CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software STATUS register or wait T_{BP} for the completion of the internal self-timed Byte Program operation. See Figure 4-5 for the Byte Program sequence.

FIGURE 4-5: BYTE PROGRAM SEQUENCE



4.4.4 AUTO ADDRESS INCREMENT (AAI) WORD PROGRAM

The AAI program instruction allows multiple bytes of data to be programmed without re-issuing the next sequential address location. This feature decreases total programming time when multiple bytes or entire memory array is to be programmed. An AAI Word program instruction pointing to a protected memory area will be ignored. The selected address range must be in the erased state (FFH) when initiating an AAI Word Program operation. While within AAI Word Programming sequence, only the following instructions are valid: for software end-of-write detection — AAI Word (ADH), WRDI (04H) and RDSR (05H); for hardware end-of-write detection — AAI Word (ADH) and WRDI (04H). There are three options to determine the completion of each AAI Word program cycle: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the software STATUS register or wait T_{BP}. Refer to **Section 4.4.5 "End-of-Write Detection"** for details.

Prior to any write operation, the Write Enable (WREN) instruction must be executed. Initiate the AAI Word Program instruction by executing an 8-bit command, ADH, followed by address bits [A_{23}-A_0]. Following the addresses, two bytes of data are input sequentially, each one from MSb (bit 7) to LSb (bit 0). The first byte of data (D0) is programmed into the initial address [A_{23}-A_1] with A_0 = 0, the second byte of Data (D1) is programmed into the initial address [A_{23}-A_1] with A_0 = 1. CE# must be driven high before executing the AAI Word Program instruction. Check the BUSY status before entering the next valid command.

Once the device indicates it is no longer busy, data for the next two sequential addresses may be programmed, followed by the next two, and so on.

When programming the last desired word or the highest unprotected memory address, check the Busy status using either the hardware or software (RDSR instruction) method to check for program completion. Once programming is complete, use the applicable method to terminate AAI. If the device is in Software End-of-Write Detection mode, execute the Write Disable (WRDI) instruction, 04H. If the device is in AAI Hardware End-of-Write Detection mode, execute the Write Disable (WRDI) instruction, 04H, followed by the 8-bit DBSY command, 80H. There is no wrap mode during AAI programming once the highest unprotected memory address is reached. See Figure 4-8 and Figure 4-9 for the AAI Word programming sequence.

4.4.5 END-OF-WRITE DETECTION

There are three methods to determine completion of a program cycle during AAI Word programming:

- hardware detection by reading the Serial Output
- software detection by polling the BUSY bit in the Software Status Register,
- wait T_{BP}

The Hardware End-of-Write detection method is described in the section below.

4.4.6 HARDWARE END-OF-WRITE DETECTION

The Hardware End-of-Write detection method eliminates the overhead of polling the Busy bit in the Software Status Register during an AAI Word program operation. The 8-bit command, 70H, configures the Serial Output (SO) pin to indicate Flash Busy status during AAI Word programming (see Figure 4-6) The 8-bit command, 70H, must be executed prior to initiating an AAI Word Program instruction. Once an internal programming operation begins, asserting CE# will immediately drive the status of the internal Flash status on the SO pin. A '0' indicates the device is busy and a '1' indicates the device is ready for the next instruction. De-asserting CE# will return the SO pin to tri-state. While in AAI and Hardware End-of-Write detection mode, the only valid instructions are AAI Word (ADH) and WRDI (04H).

To exit AAI Hardware End-of-Write detection, first execute WRDI instruction, 04H, to reset the Write Enable Latch bit (WEL = 0) and AAI bit. Then execute the 8-bit DBSY command, 80H, to disable RY/BY# status during the AAI command. See Figure 4-7 and Figure 4-8.

FIGURE 4-6: ENABLE SO AS HARDWARE RY/BY# DURING AAI PROGRAMMING

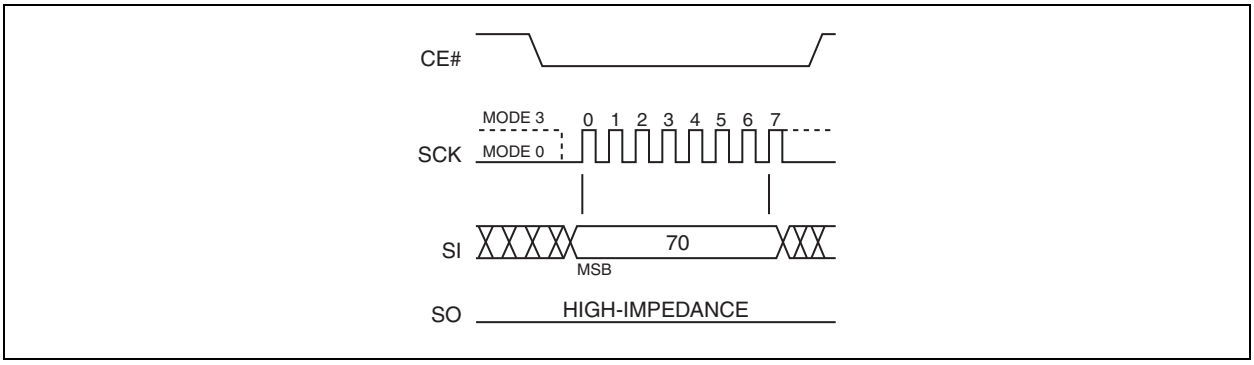


FIGURE 4-7: DISABLE SO AS HARDWARE RY/BY# DURING AAI PROGRAMMING

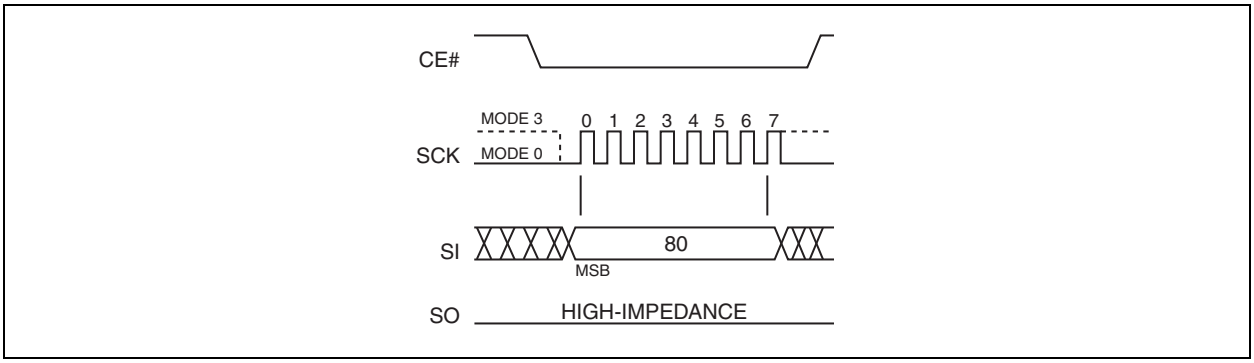
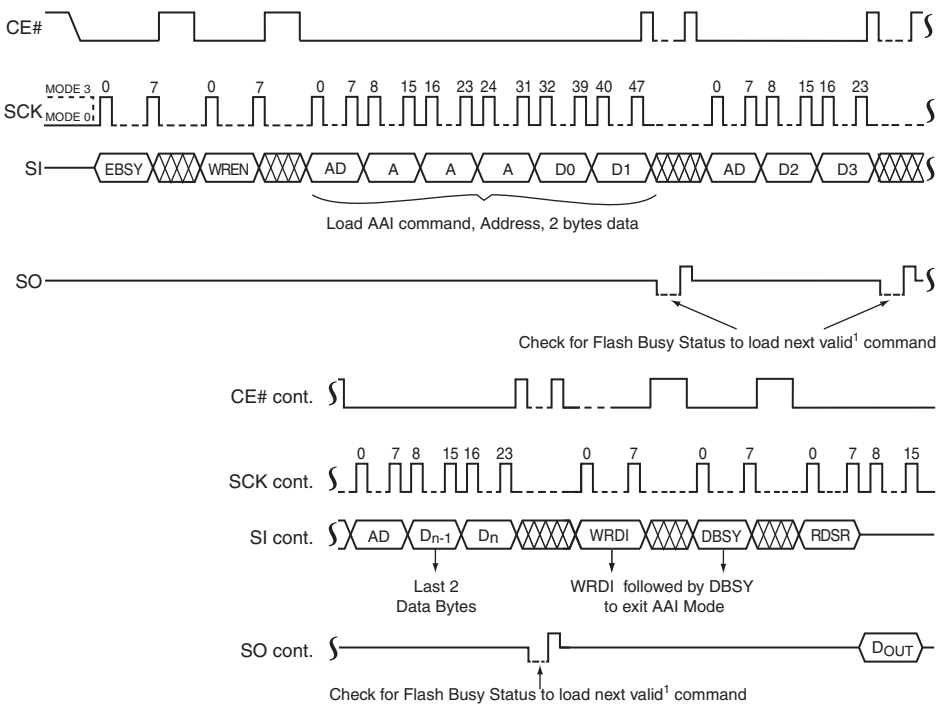
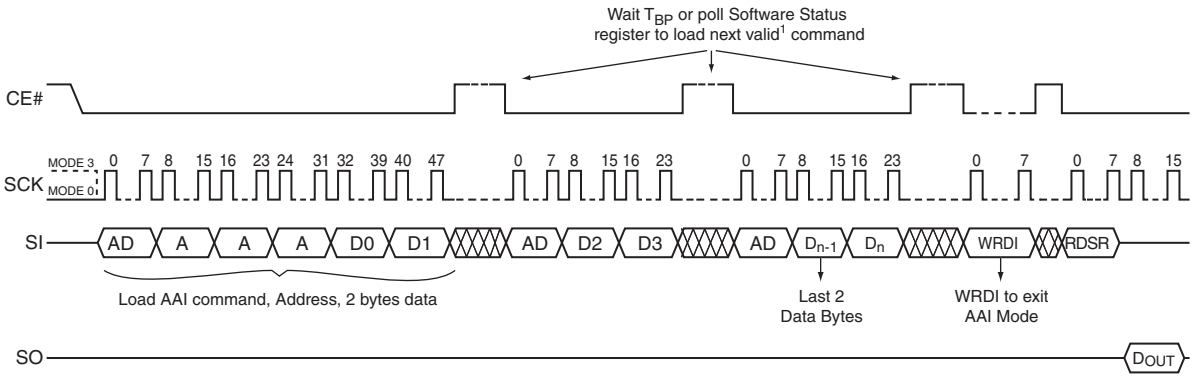


FIGURE 4-8: AUTO ADDRESS INCREMENT (AAI) WORD PROGRAM SEQUENCE WITH HARDWARE END-OF-WRITE DETECTION



Note: 1. Valid commands during AAI programming: AAI command or WRDI command
2. User must configure the SO pin to output Flash Busy status during AAI programming

FIGURE 4-9: AUTO ADDRESS INCREMENT (AAI) WORD PROGRAM SEQUENCE WITH SOFTWARE END-OF-WRITE DETECTION

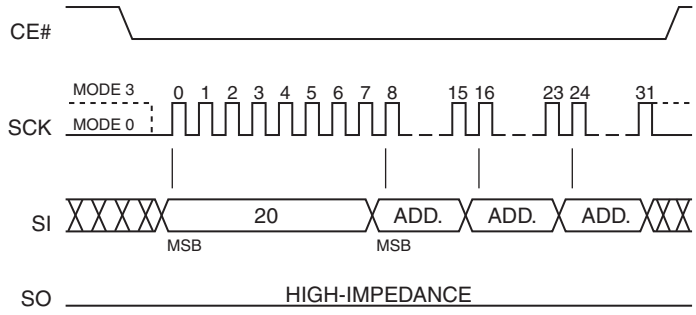


Note: 1. Valid commands during AAI programming: AAI command, RDSR command, or WRDI command

4.4.7 4-KBYTE SECTOR ERASE

The Sector Erase instruction clears all bits in the selected 4-KByte sector to FFH. A Sector Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of any command sequence. The Sector Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{12}] (A_{MS} = Most Significant address) are used to determine the sector address (SA$_X$). Remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software STATUS register or wait T_{SE} for the completion of the internal self-timed Sector Erase cycle. See Figure 4-10 for the Sector Erase sequence.

FIGURE 4-10: SECTOR ERASE SEQUENCE



4.4.8 32-KBYTE AND 64-KBYTE BLOCK ERASE

The 32-KByte Block Erase instruction clears all bits in the selected 32-KByte block to FFH. A Block Erase instruction applied to a protected memory area will be ignored. The 64-KByte Block Erase instruction clears all bits in the selected 64-KByte block to FFH. A Block Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of any command sequence. The 32-Kbyte Block Erase instruction is initiated by executing an 8-bit command, 52H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{15}] (A_{MS} = Most Significant Address) are used to determine block address (BA$_X$). Remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The 64-Kbyte Block Erase instruction is initiated by executing an 8-bit command D8H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{15}] are used to determine block address (BA$_X$). Remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software STATUS register or wait T_{BE} for the completion of the internal self-timed 32-KByte Block Erase or 64-KByte Block Erase cycles. See Figure 4-11 and Figure 4-12 for the 32-KByte Block Erase and 64-KByte Block Erase sequences.

FIGURE 4-11: 32-KBYTE BLOCK ERASE SEQUENCE

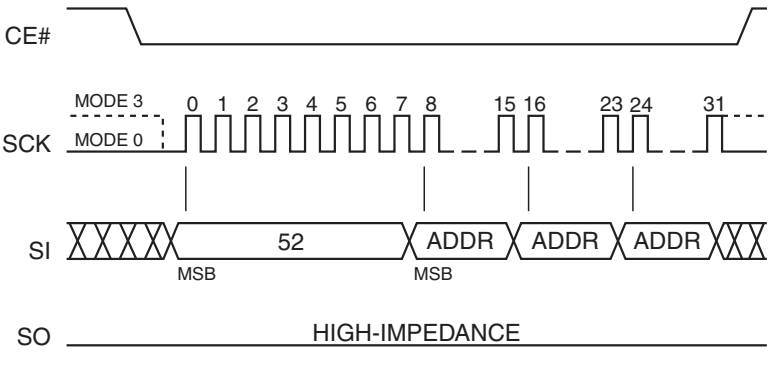
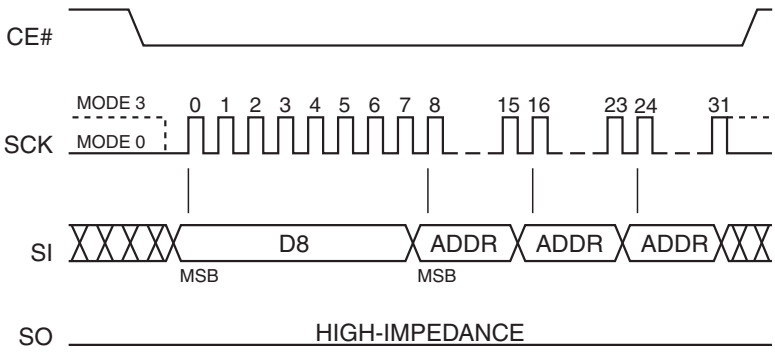


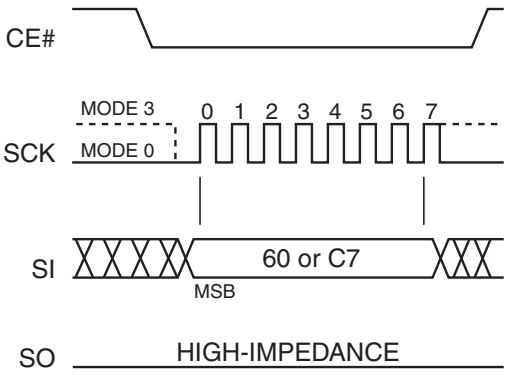
FIGURE 4-12: 64-KBYTE BLOCK ERASE SEQUENCE



4.4.9 CHIP ERASE

The Chip Erase instruction clears all bits in the device to FFH. A Chip Erase instruction will be ignored if any of the memory area is protected. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Chip Erase instruction sequence. The Chip Erase instruction is initiated by executing an 8-bit command, 60H or C7H. CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software STATUS register or wait TCE for the completion of the internal self-timed Chip Erase cycle. See Figure 4-13 for the Chip Erase sequence.

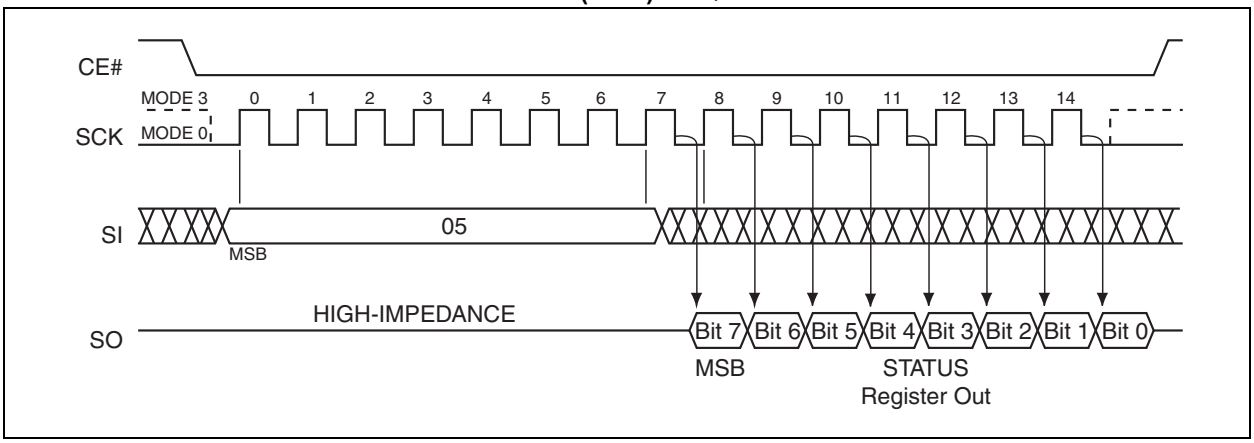
FIGURE 4-13: CHIP ERASE SEQUENCE



4.4.10 READ STATUS REGISTER (RDSR)

The Read Status Register (RDSR) instruction allows reading of the STATUS register. The STATUS register may be read at any time, even during a Write (Program/Erase) operation. When a Write operation is in progress, the Busy bit may be checked before sending any new commands to assure that the new commands are properly received by the device. CE# must be driven low before the RDSR instruction is entered and remain low until the status data are read. Read Status Register is continuous with ongoing clock cycles until it is terminated by a low-to-high transition of the CE#. See Figure 4-14 for the RDSR instruction sequence.

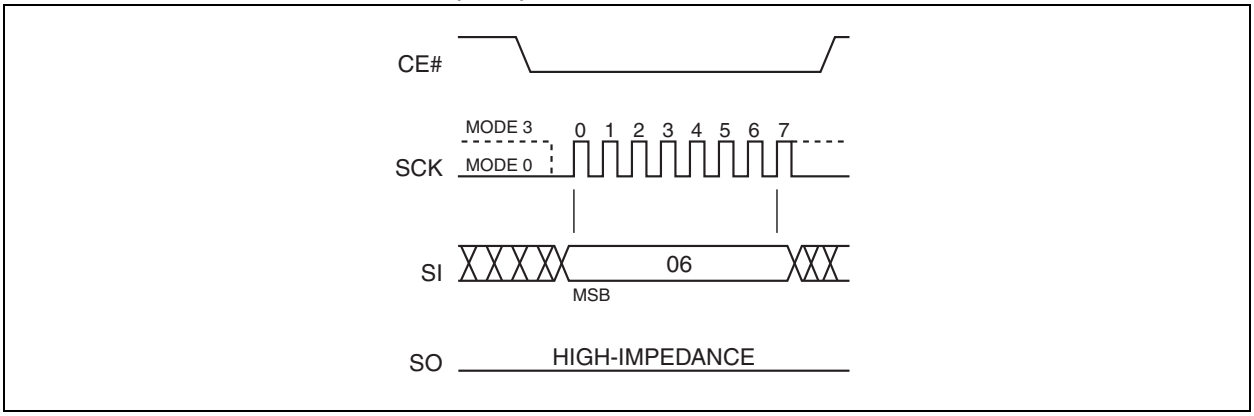
FIGURE 4-14: READ STATUS REGISTER (RDSR) SEQUENCE



4.4.11 WRITE ENABLE (WREN)

The Write Enable (WREN) instruction sets the Write Enable Latch bit in the STATUS register to '1', allowing write operations to occur. The WREN instruction must be executed prior to any Write (Program/Erase) operation. The WREN instruction may also be used to allow execution of the Write Status Register (WRSR) instruction; however, the Write Enable Latch bit in the STATUS register will be cleared upon the rising edge CE# of the WRSR instruction. CE# must be driven high before the WREN instruction is executed.

FIGURE 4-15: WRITE ENABLE (WREN) SEQUENCE

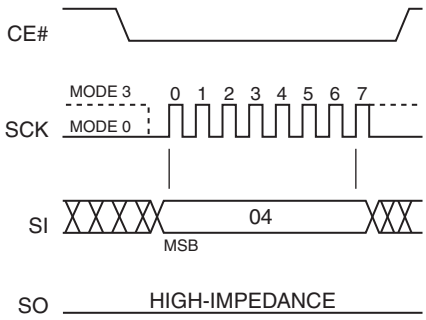


4.4.12 WRITE DISABLE (WRDI)

The Write Disable (WRDI) instruction resets the Write Enable Latch bit and AAI bit to '0', disabling any new write operations from occurring. The WRDI instruction will not terminate any programming operation in progress.

Any program operation in progress may continue up to TBP after executing the WRDI instruction. CE# must be driven high before the WRDI instruction is executed.

FIGURE 4-16: WRITE DISABLE (WRDI) SEQUENCE



4.4.13 ENABLE WRITE STATUS REGISTER (EWSR)

The Enable Write Status Register (EWSR) instruction arms the Write Status Register (WRSR) instruction and opens the STATUS register for alteration. The Write Status Register instruction must be executed immediately after the execution of the Enable Write Status Register instruction. This two-step instruction sequence of the EWSR instruction followed by the WRSR instruction works like software data protection (SDP) command structure, which prevents any accidental alteration of the STATUS register values. CE# must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.

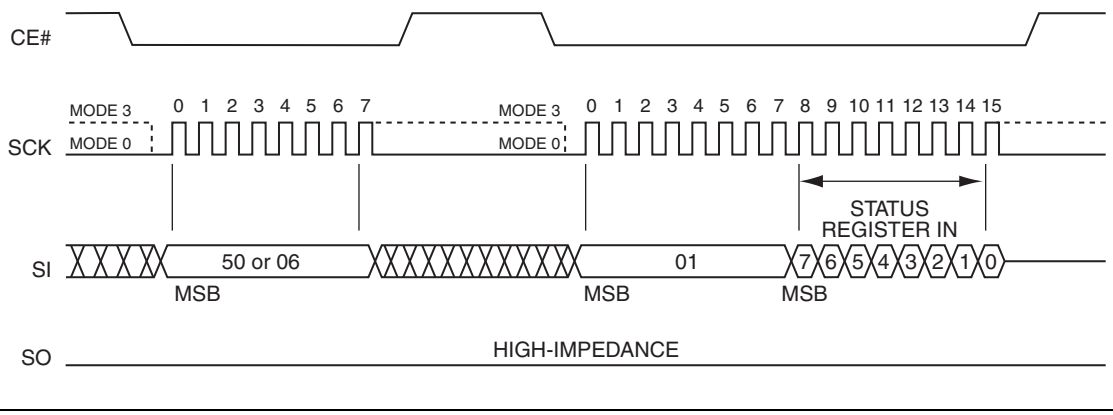
4.4.14 WRITE STATUS REGISTER (WRSR)

The Write Status Register instruction writes new values to the BP3, BP2, BP1, BP0 and BPL bits of the STATUS register.

CE# must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 4-17 for EWSR or WREN and WRSR instruction sequences.

Executing the Write Status Register instruction will be ignored when WP# is low and BPL bit is set to '1'. When the WP# is low, the BPL bit can only be set from '0' to '1' to lock down the STATUS register, but cannot be reset from '1' to '0'. When WP# is high, the lock-down function of the BPL bit is disabled and the BPL, BP0 and BP1 and BP2 bits in the STATUS register can all be changed. As long as BPL bit is set to '0' or the WP# pin is driven high (VIH) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the bits in the STATUS register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to '1' to lock down the STATUS register as well as altering the BP0, BP1 and BP2 bits at the same time. See Table 4-1 for a summary description of WP# and BPL functions.

FIGURE 4-17: ENABLE WRITE STATUS REGISTER (EWSR) OR WRITE ENABLE (WREN) AND WRITE STATUS REGISTER (WRSR) SEQUENCE



4.4.15 JEDEC READ D

The JEDEC Read ID instruction identifies the device as SST25VF016B and the manufacturer as Microchip. The device information can be read from executing the 8-bit command, 9FH. Following the JEDEC Read ID instruction, the 8-bit manufacturer's ID, BFH, is output from the device. After that, a 16-bit device ID is shifted out on the SO pin. Byte 1, BFH, identifies the manufacturer as Microchip. Byte 2, 25H, identifies the memory type as SPI Serial Flash. Byte 3, 41H, identifies the device as SST25VF016B. The instruction sequence is shown in Figure 4-18. The JEDEC Read ID instruction is terminated by a low-to-high transition on CE# at any time during data output. If no other command is issued after executing the JEDEC Read ID instruction, issue a 00H (NOP) command before going into Standby Mode (CE# = V_{IH}).

FIGURE 4-18: JEDEC READ ID SEQUENCE

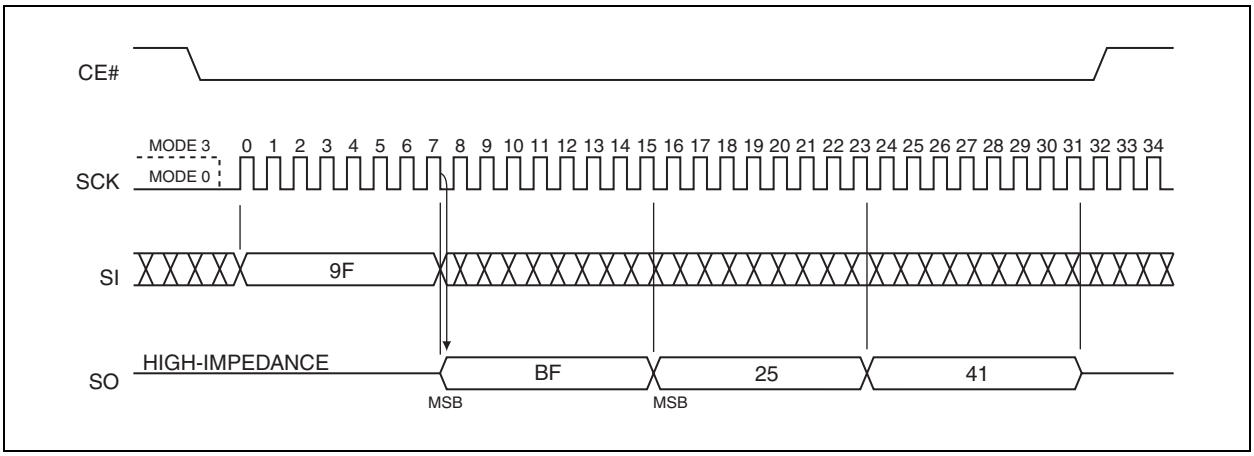


TABLE 4-5: JEDEC READ ID DATA

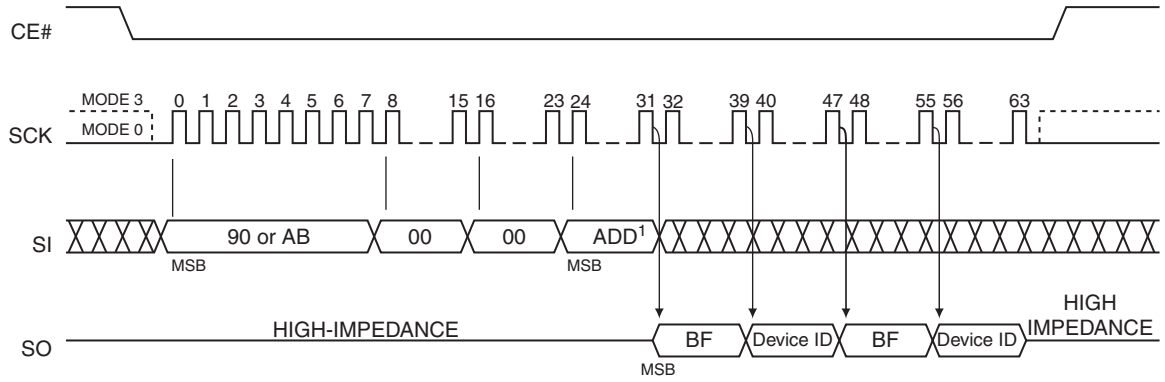
Manufacturer's ID	Device ID	
	Memory Type	Memory Capacity
Byte1	Byte 2	Byte 3
BFH	25H	41H

4.4.16 READ ID (RDID)

The Read ID instruction (RDID) identifies the device as SST25VF016B and manufacturer as Microchip. This command is backward compatible to all SST25xFxxxA devices and should be used as default device identification when multiple versions of SPI Serial Flash devices are used in a design. The device information can be read from executing an 8-bit command, 90H or ABH, followed by address bits [A_{23}-A_0]. Following the Read ID instruction, the manufacturer's ID is located in address 00000H and the device ID is located in address 00001H. Once the device is in Read ID mode, the manufacturer and device ID output data toggle between address 00000H and 00001H until terminated by a low-to-high transition on CE#.

Refer to Table 4-5 and Table 4-6 for device identification data.

FIGURE 4-19: READ ID SEQUENCE



Note: The manufacturer's and device ID output stream is continuous until terminated by a low to high transition on CE#.
Device ID = 41H for SST25VF016B
1. 00H will output the manfacturer's ID first and 01H will output device ID first before toggling between the two.

TABLE 4-6: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	00000H	BFH
Device ID		
SST25VF016B	00001H	41H

5.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

DC voltage on any pin to ground potential ..... -0.5V to V_{DD}+0.5V

Transient voltage (<20 ns) on any pin to ground potential ..... -2.0V to V_{DD}+2.0V

Package power dissipation capability (T_A = +25°C) 1.0W

Surface mount solder reflow temperature ..... +260°C for 10 seconds

Output short circuit current[1] ..... 50 mA

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 5-1: OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7V-3.6V
Industrial	-40°C to +85°C	2.7V-3.6V

TABLE 5-2: AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	Output Load
5 ns	C_L = 30 pF

Note 1: See Figure 5-5 and Figure 5-6.

TABLE 5-3: DC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{DDR}	Read Current	—	10	mA	CE# = 0.1 V_{DD}/0.9 V_{DD}@25 MHz, SO = open
I_{DDR2}	Read Current	—	15	mA	CE# = 0.1 V_{DD}/0.9 V_{DD}@50 MHz, SO = open
I_{DDR3}	Read Current	—	20	mA	CE# = 0.1 DD/0.9 V_{DD}@50 MHz, SO = open
I_{DDW}	Program and Erase Current	—	30	mA	CE# = V_{DD}
I_{SB}	Standby Current	—	20	µA	CE# = V_{DD}, V_{IN} = V_{DD} or V_{SS}
I_{LI}	Input Leakage Current	—	1	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max.
I_{LO}	Output Leakage Current	—	1	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} Max.
V_{IL}	Input Low Voltage	—	0.8	V	V_{DD} = V_{DD} Min.
V_{IH}	Input High Voltage	0.7 V_{DD}	—	V	V_{DD} = V_{DD} Max.
V_{OL}	Output Low Voltage	—	0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min.
V_{OL2}	Output Low Voltage	—	0.4	V	I_{OL} = 1.6 mA, V_{DD} = V_{DD} Min.
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH} = -100 µA, V_{DD} = V_{DD} Min.

TABLE 5-4: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}(1)	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 5-5: AC OPERATING CHARACTERISTICS

Symbol	Parameter	25 MHz		50 MHz		Units
		Min.	Max.	Min.	Max.	
F_{CLK}(1)	Serial Clock Frequency	—	25	—	50	MHz
T_{SCKH}	Serial Clock High Time	18	—	9	—	ns
T_{SCKL}	Serial Clock Low Time	18	—	9	—	ns
T_{SCKR}(2)	Serial Clock Rise Time (Slew Rate)	0.1	—	0.1	—	V/ns
T_{SCKF}	Serial Clock Fall Time (Slew Rate)	0.1	—	0.1	—	V/ns
T_{CES}(3)	CE# Active Setup Time	10	—	5	—	ns
T_{CEH}(3)	CE# Active Hold Time	10	—	5	—	ns
T_{CHS}(3)	CE# Not Active Setup Time	10	—	5	—	ns
T_{CHH}(3)	CE# Not Active Hold Time	10	—	5	—	ns
T_{CPH}	CE# High Time	100	—	50	—	ns
T_{CHZ}	CE# High to High-Z Output	—	15	—	8	ns
T_{CLZ}	SCK Low to Low-Z Output	0	—	0	—	ns
T_{DS}	Data In Setup Time	5	—	2	—	ns
T_{DH}	Data In Hold Time	5	—	5	—	ns
T_{HLS}	HOLD# Low Setup Time	10	—	5	—	ns
T_{HHS}	HOLD# High Setup Time	10	—	5	—	ns
T_{HLH}	HOLD# Low Hold Time	10	—	5	—	ns
T_{HHH}	HOLD# High Hold Time	10	—	5	—	ns
T_{HZ}	HOLD# Low to High-Z Output	—	20	—	8	ns
T_{LZ}	HOLD# High to Low-Z Output	—	15	—	8	ns
T_{OH}	Output Hold from SCK Change	0	—	0	—	ns
T_{V}	Output Valid from SCK	—	15	—	8	ns
T_{SE}	Sector Erase	—	25	—	25	ms
T_{BE}	Block Erase	—	25	—	25	ms
T_{SCE}	Chip Erase	—	50	—	50	ms
T_{BP}	Byte Program	—	10	—	10	µs

Note 1: Maximum clock frequency for Read instruction, 03H, is 25 MHz.

2: Maximum Rise and Fall time may be limited by T_{SCKH} and T_{SCKL} requirements.

3: Relative to SCK.

FIGURE 5-1: SERIAL INPUT TIMING DIAGRAM

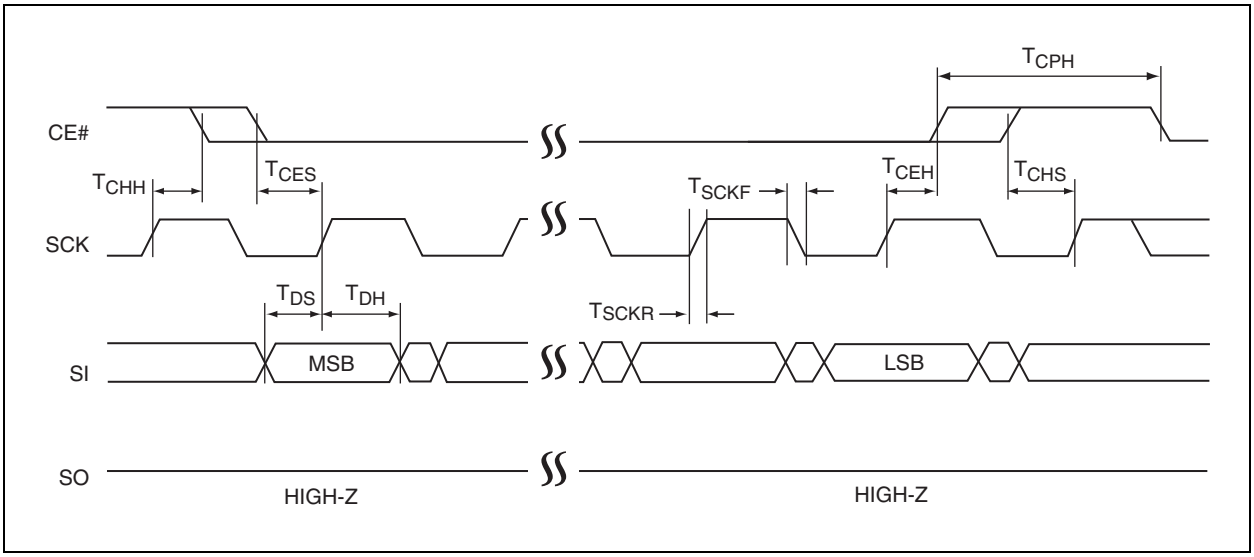


FIGURE 5-2: SERIAL OUTPUT TIMING DIAGRAM

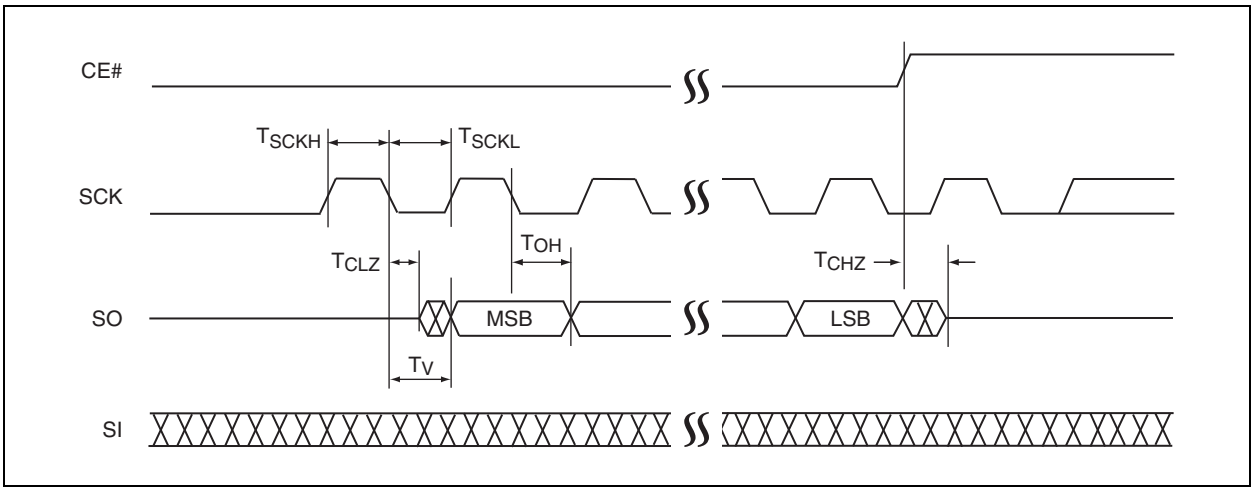
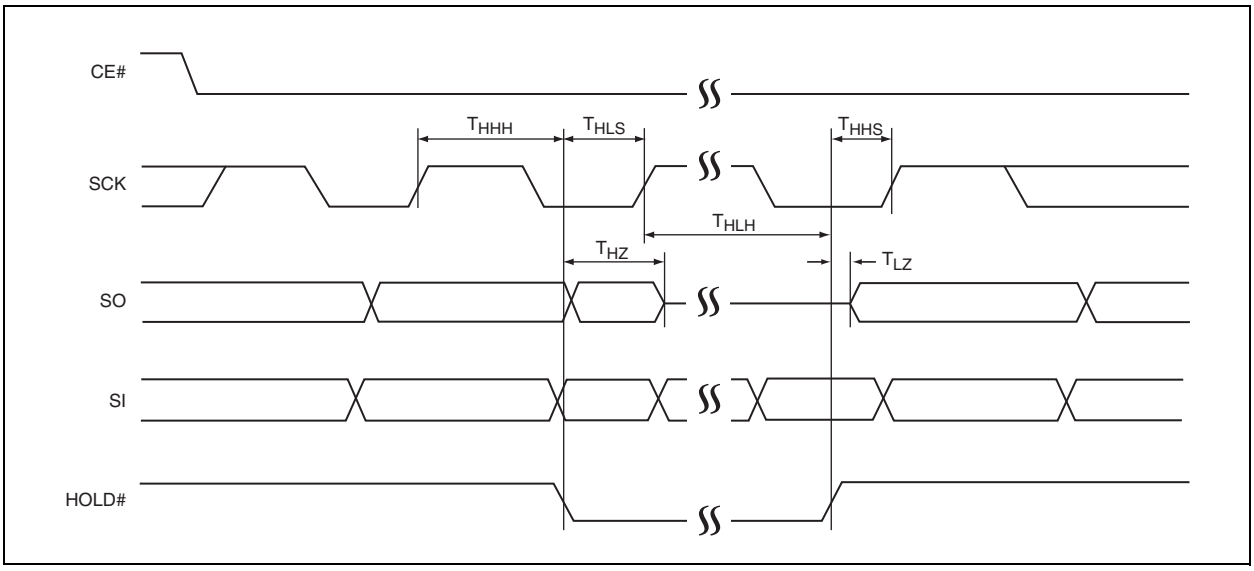


FIGURE 5-3: HOLD TIMING DIAGRAM



5.1 Power-Up Specifications

All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V – 3.0V in less than 300 ms). See Table 5-6 and Figure 5-4 for more information.

TABLE 5-6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$(1)	V_{DD} Min to Read Operation	100	µs
$T_{PU-WRITE}$(1)	V_{DD} Min to Write Operation	100	µs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 5-4: POWER-UP TIMING DIAGRAM

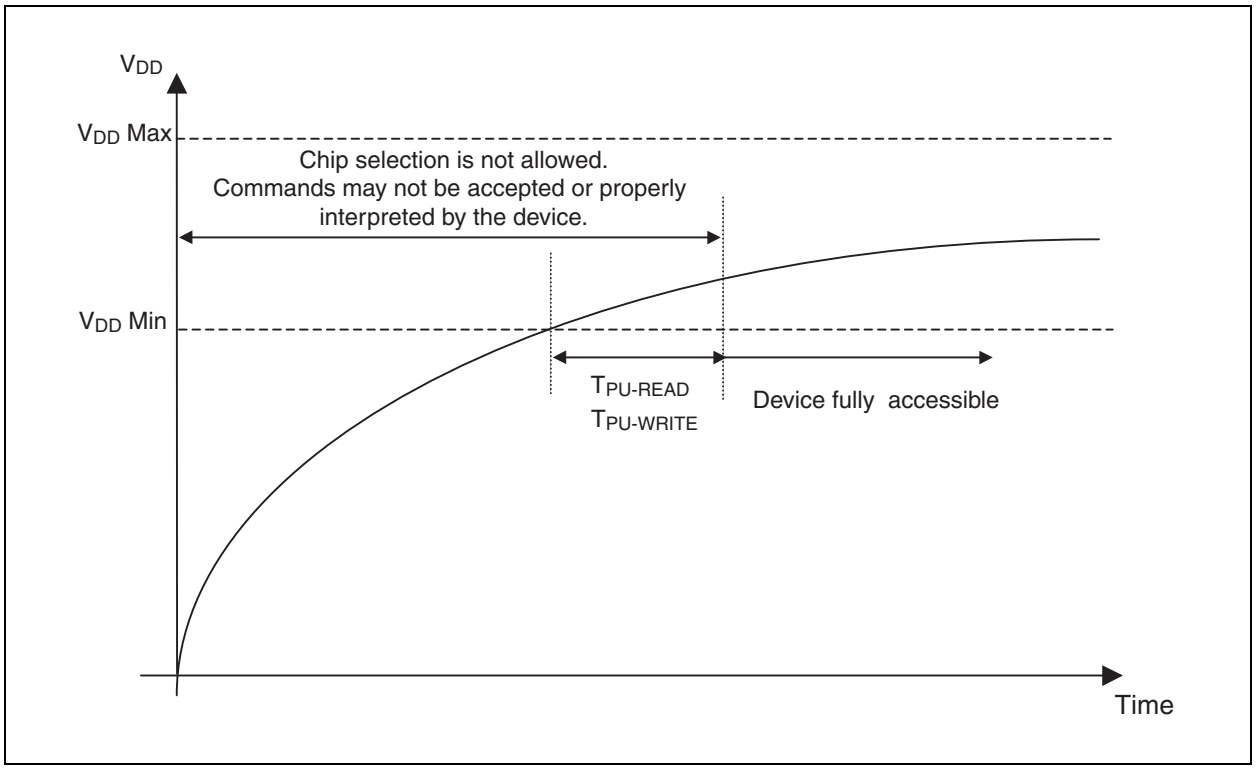
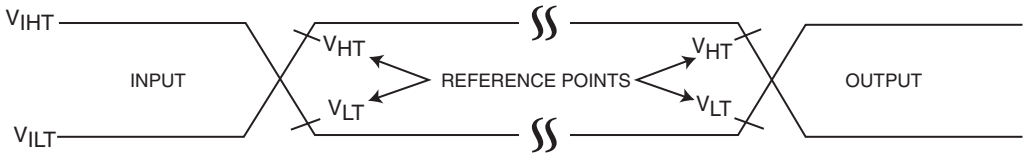


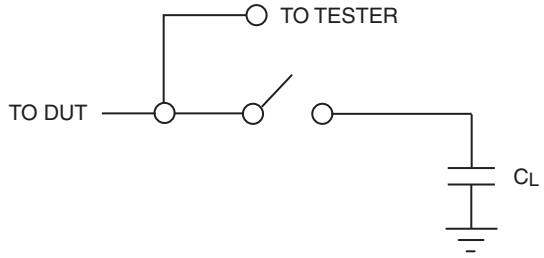
FIGURE 5-5: AC INPUT/OUTPUT REFERENCE WAVEFORMS



AC test inputs are driven at V_{IHT} (0.9V_{DD}) for a logic '1' and V_{ILT} (0.1V_{DD}) for a logic '0'. Measurement reference points for inputs and outputs are V_{HT} (0.6V_{DD}) and V_{LT} (0.4V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

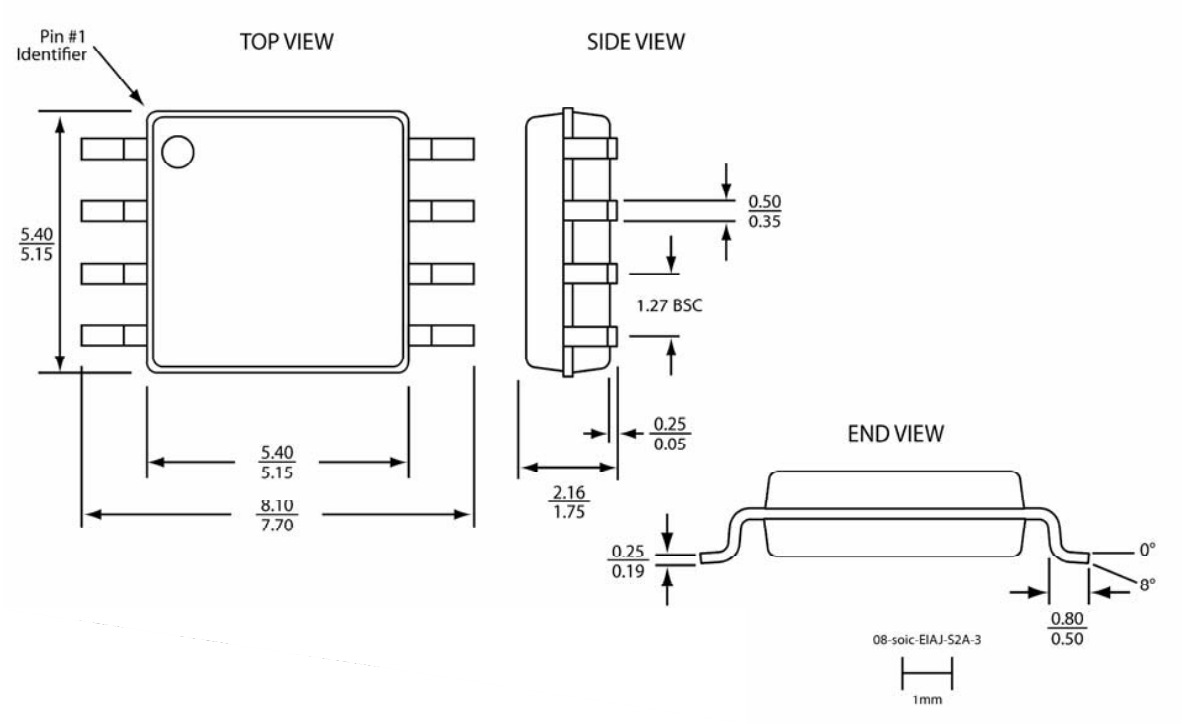
FIGURE 5-6: A TEST LOAD EXAMPLE



6.0 PACKAGING DIAGRAMS

8-Lead Small Outline Integrated Circuit (S2AE/F) - .208 Inch Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



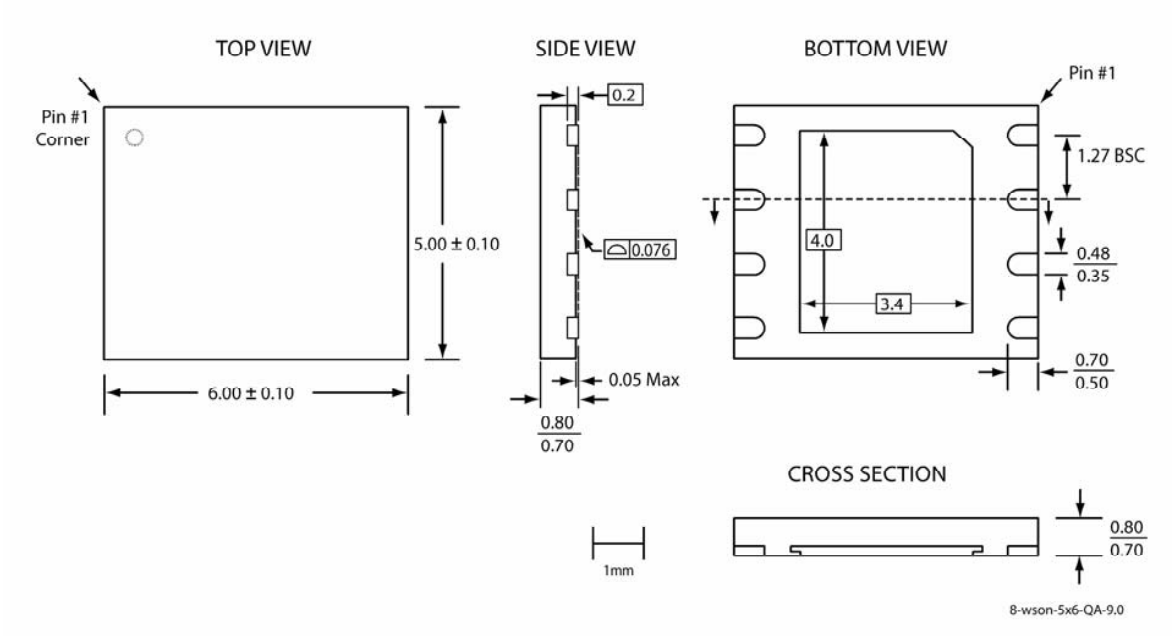
Note:

1. All linear dimensions are in millimeters (max/min).
2. Coplanarity: 0.1 mm
3. Maximum allowable mold flash is 0.15 mm at the package ends and 0.25 mm between leads.

Microchip Technology Drawing C04-14005A Sheet 1 of 1

8-Lead Very, Very Thin Small Outline No-Leads (QAE/F) - 5x6 mm Body [WSON]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Note:

1. All linear dimensions are in millimeters (max/min).
2. Untoleranced dimensions (shown with box surround) are nominal target dimensions.
3. The external paddle is electrically connected to the die back-side and possibly to certain VSS leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.

Microchip Technology Drawing C04-14008A Sheet 1 of 1

7.0 REVISION HISTORY

TABLE 7-1: REVISION HISTORY

Revision	Description	Date
00	• Initial release of data sheet	Apr. 2005
01	• Corrected Section 4.4.15 “JEDEC Read D” including timing diagram • Corrected V_{HT} and V_{LT} values in Figure 5-5	Sept. 2005
02	• Migrated document to a Data Sheet • Updated Surface Mount Solder Reflow Temperature information	Jan. 2006
03	• Edited Clock Frequency speed from 50 MHz to 80 MHz in Features • Revised Table 5 for 80 MHz • Edited High Speed Read for 80 MHz • Edited Table 8 • Added 80 MHz columns to Table 12 • Updated Product Ordering Information and Valid Combination	Sept. 2008
04	• Updated “Auto Address Increment (AAI) Word Program”, “End-of-Write Detection”, and “Hardware End-of-Write Detection” • Revised Figure 4-8 and Figure 4-9 • Updated document to new format	Jan. 2011
A	• Added “Power-Up Specifications” section • Updated Table 5-6 • Released document under letter revision system • Updated Spec number from S71271 to DS25044	Aug. 2011
B	• Updated document to new corporate format • EOL of all 75 MHz parts. Replacement parts are the 50 MHz parts found in this data sheet.	Jan. 2015
C	• Fixed an error in “Product Identification System” section.	July 2015
D	• Updated “Product Identification System” section; removed QAE and SAE options.	Oct. 2023

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. – XX – XX – XX – X	
Device	
Operating Frequency	
Minimum Endurance	
Temp Range	
Package	
Tape/Reel Indicator	

Device:	SST25VF016B	= 16-Mbit, 2.7V-3.6V, SPI Flash Memory
Operating Frequency:	50	= 50 MHz
Minimum Endurance	4	= 10,000 cycles
Temperature:	I C	= -40°C to +85°C = 0°C to +70°C
Package:	QAF(1) S2AF(1)	= WSON (6 mm x 5 mm Body), 8-lead = SOIC (200 mil Body), 8-lead
Tape and Reel Flag:	T	= Tape and Reel

Note 1: Suffix F = Nickel plating with Gold top (outer) layer finish or Matte Tin finish

Valid Combinations:

SST25VF016B-50-4C-S2AF
SST25VF016B-50-4C-S2AF-T
SST25VF016B-50-4I-S2AF
SST25VF016B-50-4I-S2AF-T

SST25VF016B-50-4C-QAF
SST25VF016B-50-4C-QAF-T
SST25VF016B-50-4I-QAF
SST25VF016B-50-4I-QAF-T

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