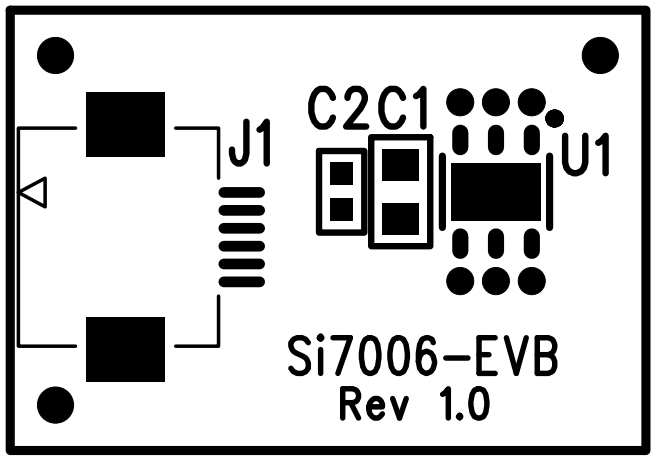
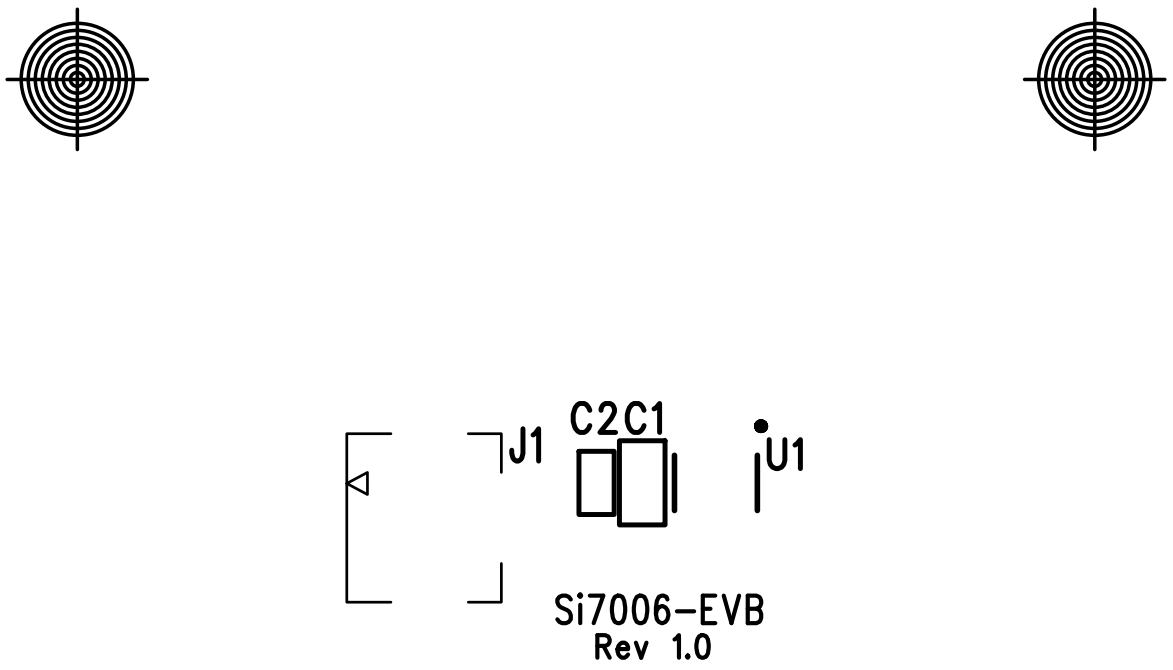
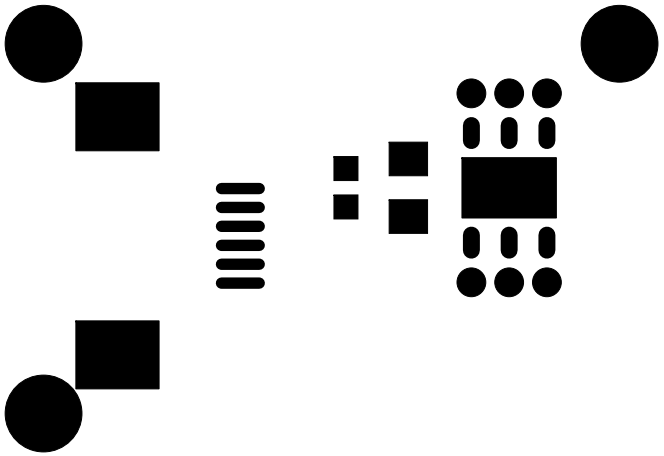


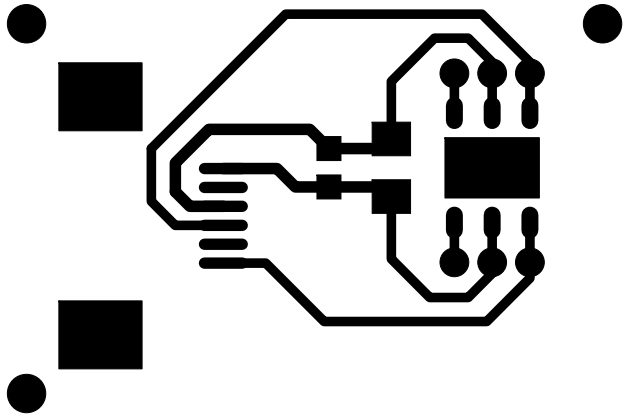

# PRIMARY SILKSCREEN



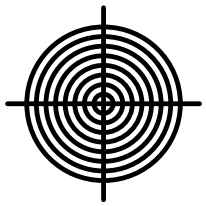
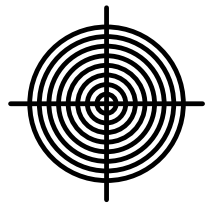
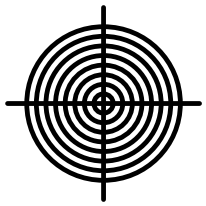

# PRIMARY SILKSCREEN



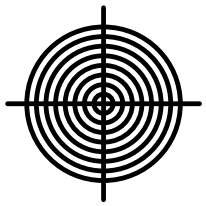
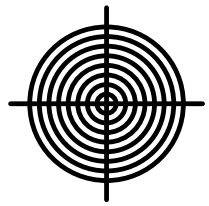
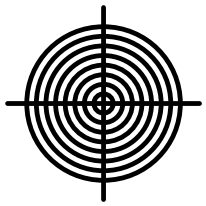
PRIMARY SOLDER MASK



PRIMARY SIDE

# SECONDARY SIDE

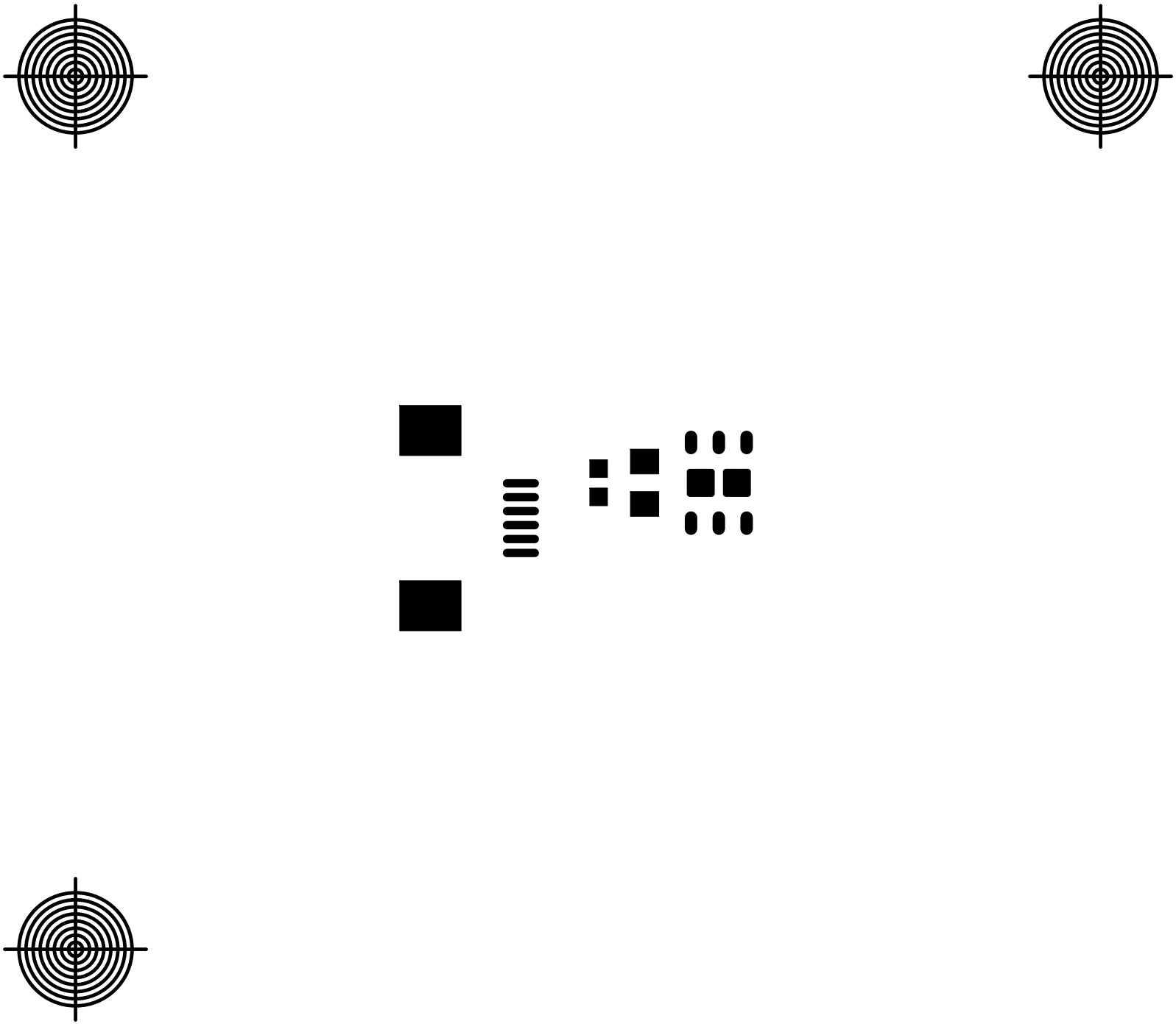




# SECONDARY SOLDER MASK

GND
SDA

ADD
SCL

# SECONDARY SILKSCREEN



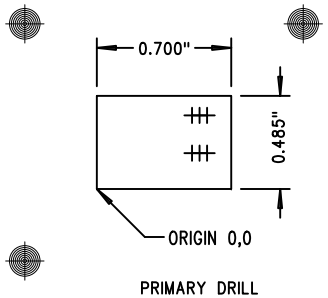
PRIMARY SOLDER PASTE

• • •

• • •

## NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345°C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ±0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" ±10%.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, GREEN S.M.O.B.C., BALANCE ENIG.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT




PRIMARY DRILL

| LAYER STACKUP | FILE NAMES |
|---|---|
| PRIMARY SILKSCREEN | Si7006_PSS.PHO |
| PRIMARY SOLDERMASK | Si702x_PSM.PHO |
| PRIMARY SIDE | Si702x_PRI.PHO |
| SECONDARY SIDE | Si702x_SEC.PHO |
| SECONDARY SOLDERMASK | Si702x_SSM.PHO |
| SECONDARY SILKSCREEN | Si702x_SSS.PHO |

SCALE: NONE

| SIZE | QTY | SYM | PLT | TOOL | TOL |
|---|---|---|---|---|---|
| 0.015 | 6 | + | P | 1 | +0/-0.015 |

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH
DIMENSIONS IN BRACKETS [ ] ARE IN MILLIMETERS
INTERPRET DRAWING PER MIL-D-1000

TOLERANCES

HOLE TOLERANCES PER 78027

| DECIMALS | ANGLES | SURFACES |
|---|---|---|
| .XX +/-<br>.XXX +/- | +/- | MICROINCHES |

PART TO BE FREE OF BURRS

| BREAK EDGES | BEND RADIUS | BEND RELIEF |
|---|---|---|
| MAX | MAX | MAX |



| | | |
|---|---|---|
| DESIGN | JG | 09MAY2014 |
| LAYOUT | CT | 13MAY2014 |

DO NOT SCALE DRAWING

COMPANY: SILICON LABORATORIES
400 W Cesar Chavez
AUSTIN, TX 78701
(512)416-8500
www.silabs.com

NAME: Si7006-EVB

REV : 1.0

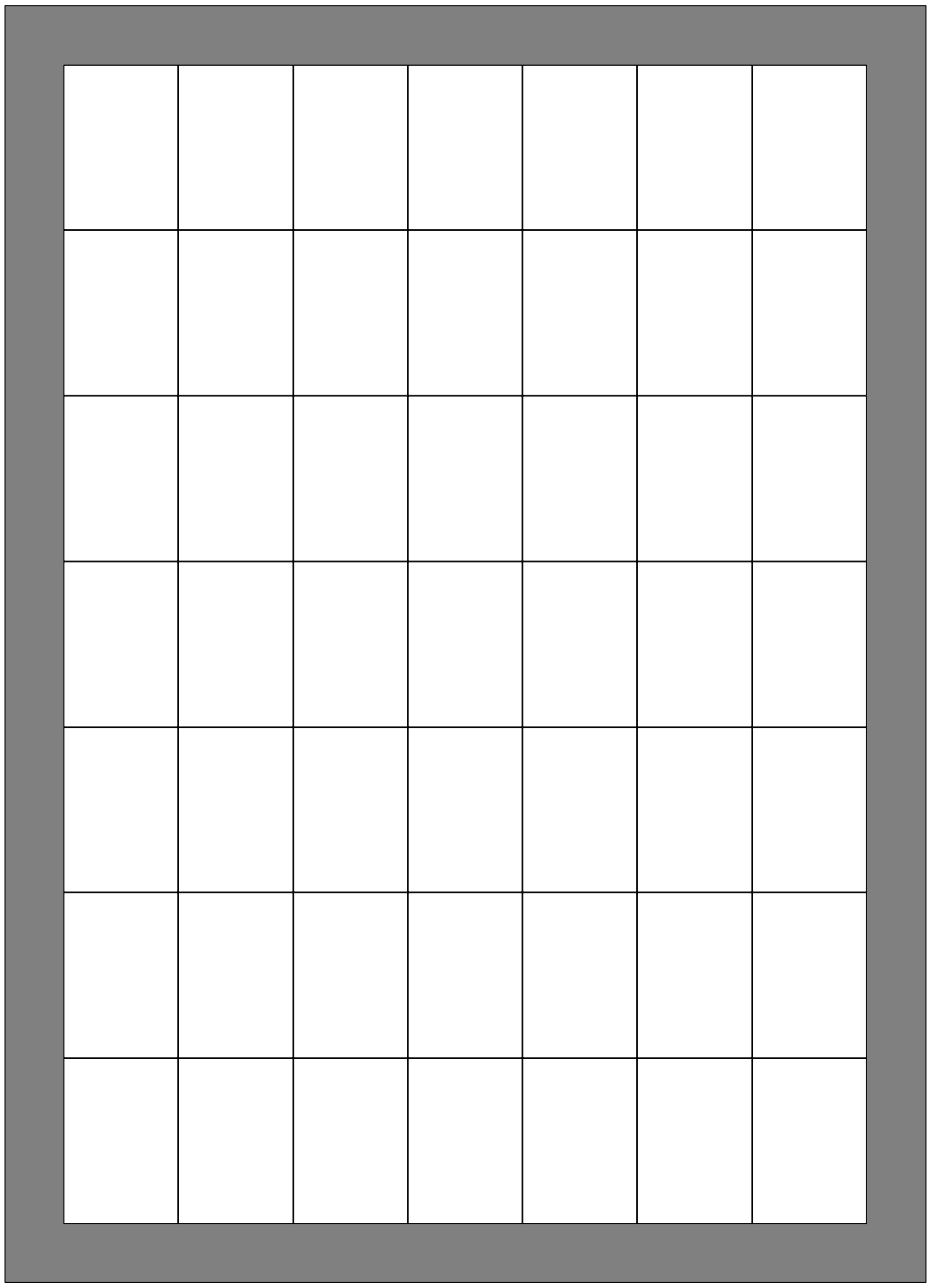
SIZE A

PART NUMBER:

SCALE 1:1

FABRICATION DRAWING

SHEET 1 OF 1



**Si702x-EVB Rev1.0**

**Size:**
Array: 3.895 x 5.4
Part: 0.485 x 0.7

**Parts On Array:**
49 Parts

**Matrix:**
7 x 7

**Spacing:**
0.0 x 0.0

**Array Borders:**
Left: 0.25 Right: 0.25
Top: 0.25 Bottom: 0.25

Notes:

Please add 4, 0.125" NP tooling holes located 0.125" from tab corners and 3, 40/120 fiduals to each side of array located 0.25" from tooling holes.