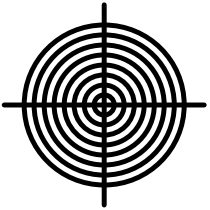
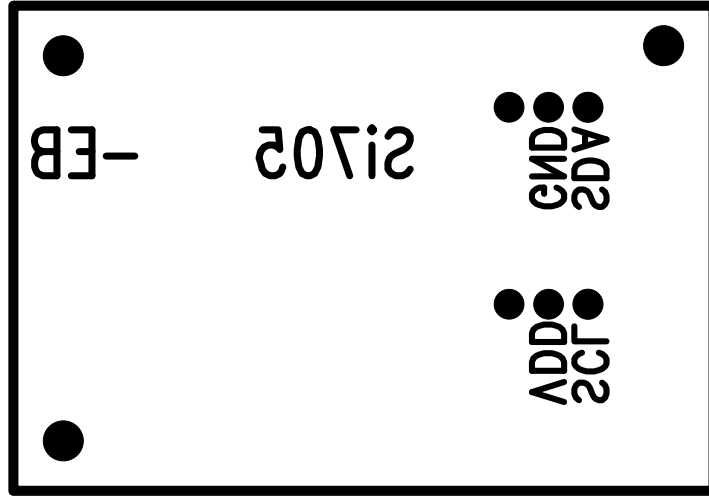
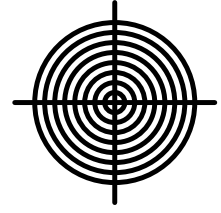
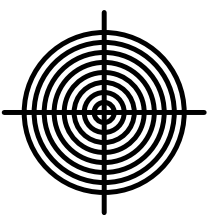
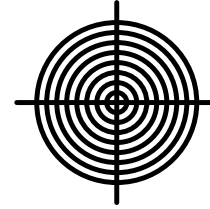
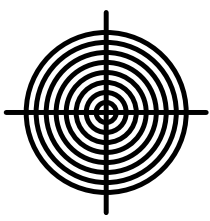


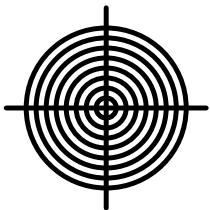
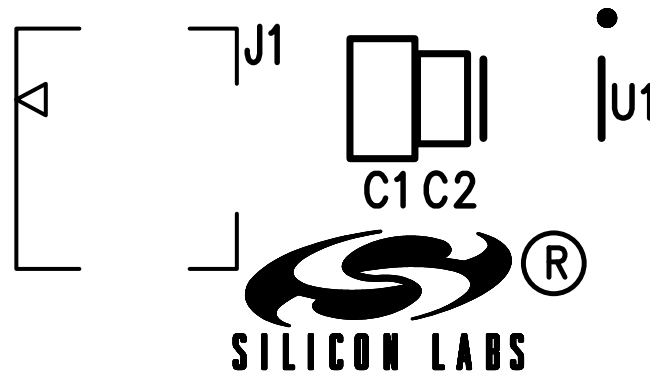
PRIMARY SILKSCREEN



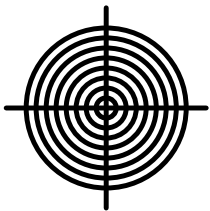
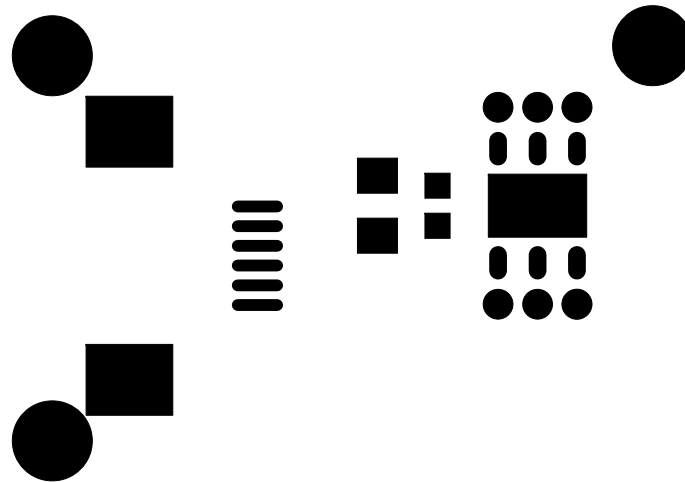
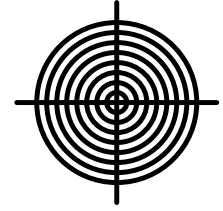
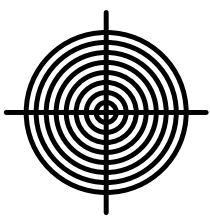
SECONDARY SILKSCREEN



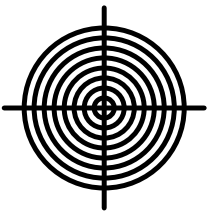
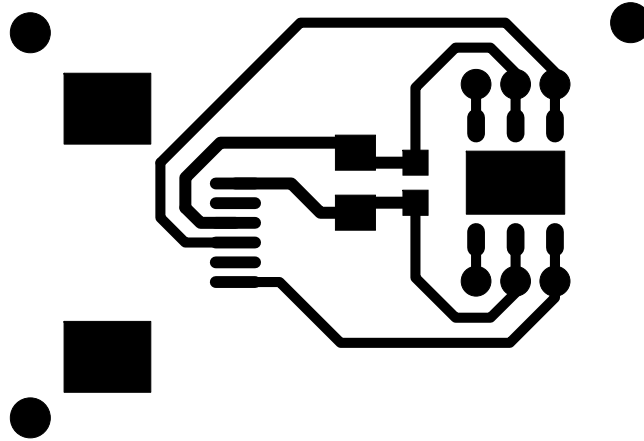
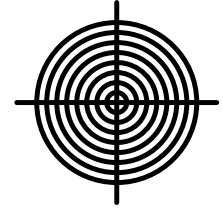
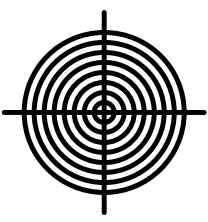
SiLabs® Si705x-EB
Rev 1.0



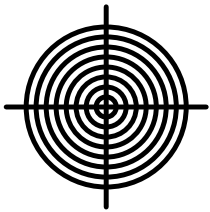
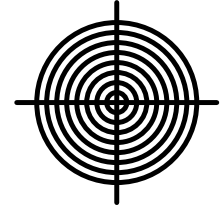
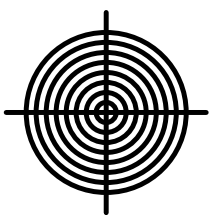
PRIMARY SILKSCREEN



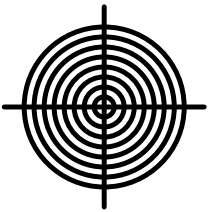
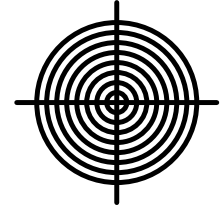
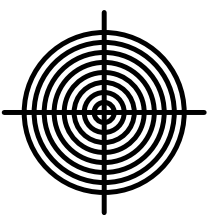
PRIMARY SOLDER MASK



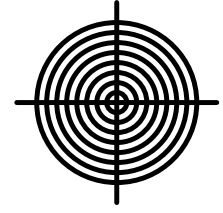
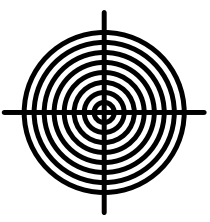
PRIMARY SIDE



SECONDARY SIDE



SECONDARY SOLDER MASK



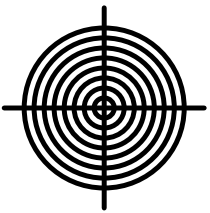
AD2
QND



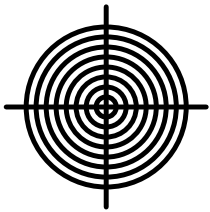
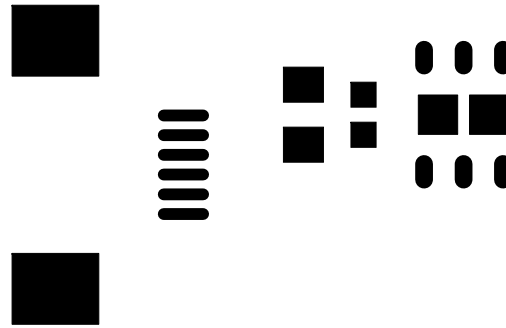
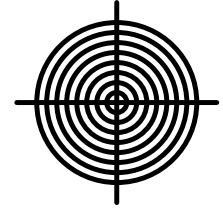
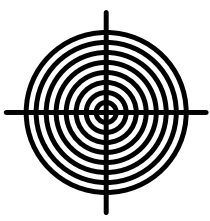
2i702

-EB

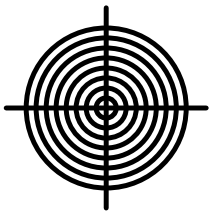
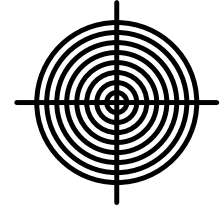
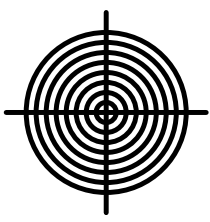
J32
ADD



SECONDARY SILKSCREEN



PRIMARY SOLDER PASTE



SECONDARY SOLDER PASTE



• • •

• • •

NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE $\geq 345^{\circ}\text{C}$, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ± 0.003 ".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" $\pm 10\%$.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, GREEN S.M.O.B.C., BALANCE ENIG.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

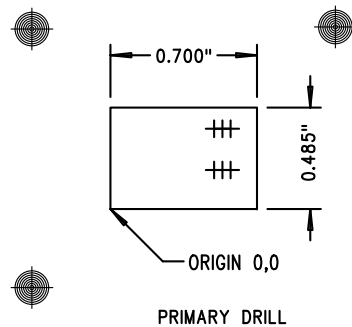
LAYER STACKUP


FILE NAMES

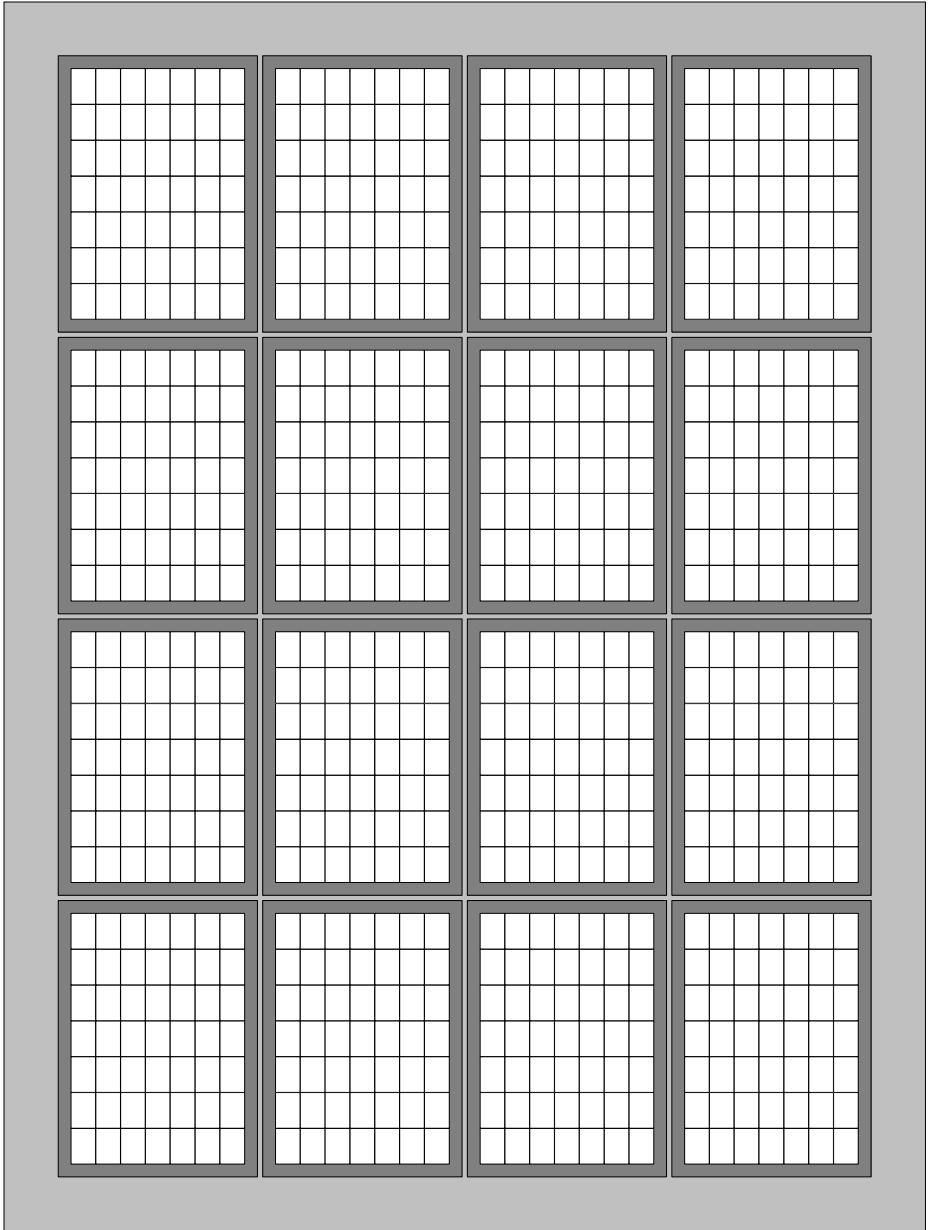
PRIMARY SILKSCREEN	Si705x_PSS.PHO
PRIMARY SOLDERMASK	Si705x_PSM.PHO
PRIMARY SIDE	Si705x_PRI.PHO
SECONDARY SIDE	Si705x_SEC.PHO
SECONDARY SOLDERMASK	Si705x_SSM.PHO
SECONDARY SILKSCREEN	Si705x_SSS.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.015	6	+	P	1	± 0.003



UNLESS OTHERWISE SPECIFIED		THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF SILICON LABORATORIES, INC..		COMPANY:  400 W Cesar Chavez AUSTIN, TX 78701 (512)416-8500 www.silabs.com	
DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH DIMENSIONS IN BRACKETS [] ARE IN MILLIMETERS INTERPRET DRAWING PER MIL-D-1000		TOLERANCES		NAME: Si705x-EVB	
HOLE TOLERANCES PER 78027		DESIGN		REV : 1.0	
DECIMALS .XX +/- .XXX +/-	ANGLES +/-	SURFACES MICROINCHES		SIZE A PART NUMBER:	
PART TO BE FREE OF BURRS		LAYOUT	AA	SCALE 1:1	
BREAK EDGES MAX	BEND RADIUS MAX	BEND RELIEF MAX		FABRICATION DRAWING	
DO NOT SCALE DRAWING				SHEET 1 OF 1	



Si705x-EVB Rev1.0

Size:

Panel: 18.0 x 24.0
Array: 3.895 x 5.4
Part: 0.485 x 0.7

Panel Yield:

16 Arrays of 49 Parts
784 Parts Total
77.9% Material Utilization

Matrix:

On Panel: 4 x 4, Origin: X1.06 Y1.05
On Array: 7 x 7

Spacing:

On Panel: 0.1 x 0.1
On Array: 0.0 x 0.0

Panel Borders:

Left: 1.06 Right: 1.06
Top: 1.05 Bottom: 1.05

Array Borders:

Left: 0.25 Right: 0.25
Top: 0.25 Bottom: 0.25

Notes:

Please add 4, 0.125" NP tooling holes located 0.125" from tab corners and 3, 40/120 fiducials to each side of array located 0.25" from tooling holes.