

# AP9974AGH-HF

**Halogen-Free Product**

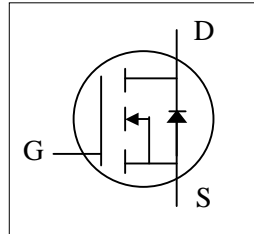


**Advanced Power  
Electronics Corp.**

*N-CHANNEL ENHANCEMENT MODE*

*POWER MOSFET*

- ▼ Low Gate Charge
- ▼ Simple Drive Requirement
- ▼ Surface Mount Package
- ▼ RoHS Compliant & Halogen-Free

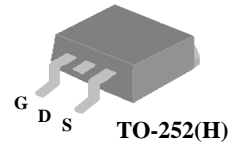


$BV_{DSS}$	60V
$R_{DS(ON)}$	12m $\Omega$
$I_D$	68A

## Description

AP9974A series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-252 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance.



## Absolute Maximum Ratings @ $T_J=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	+20	V
$I_D@T_C=25^\circ\text{C}$	Drain Current, $V_{GS}$ @ 10V	68	A
$I_D@T_C=100^\circ\text{C}$	Drain Current, $V_{GS}$ @ 10V	43	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	272	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	104	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1.2	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount) <sup>3</sup>	62.5	$^\circ\text{C}/\text{W}$



**Electrical Characteristics @T<sub>j</sub>=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =45A	-	-	12	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =30A	-	-	15	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	-	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =30A	-	71	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	10	uA
	Drain-Source Leakage Current (T <sub>j</sub> =125°C)	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V	-	-	250	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge	I <sub>D</sub> =30A	-	33	45	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =48V	-	5	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =4.5V	-	21	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =30V	-	10	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =30A	-	43	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω	-	47	-	ns
t <sub>f</sub>	Fall Time	V <sub>GS</sub> =10V	-	80	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	2680	3300	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =25V	-	260	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	180	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =45A, V <sub>GS</sub> =0V	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =10A, V <sub>GS</sub> =0V,	-	30	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	-	18	-	nC

**Notes:**

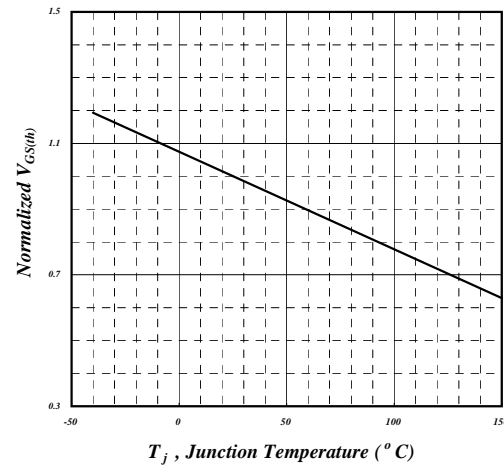
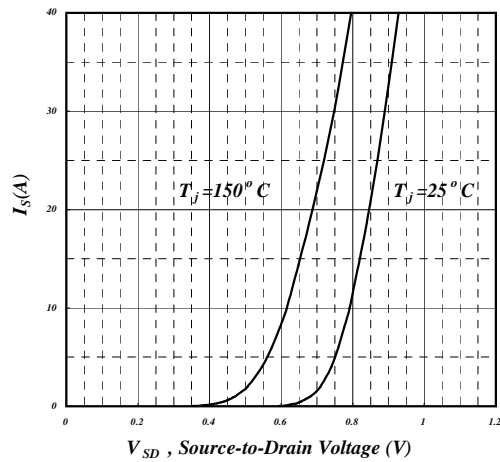
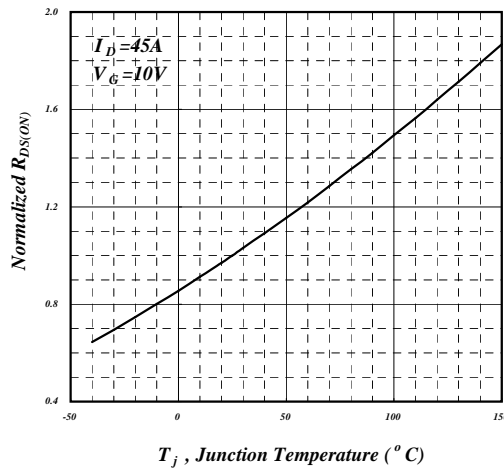
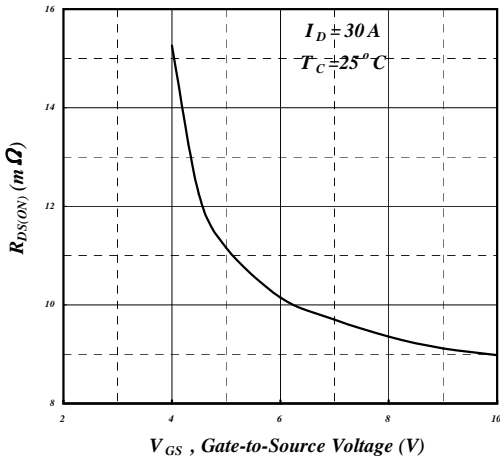
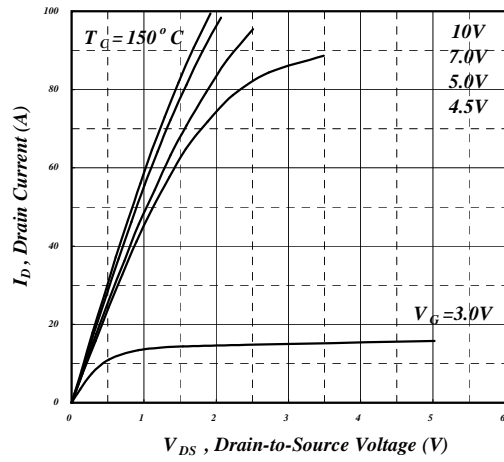
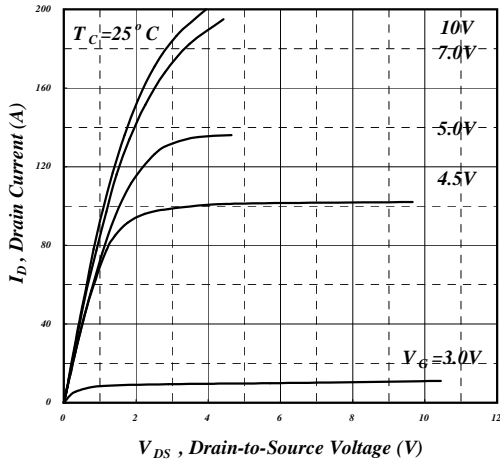
- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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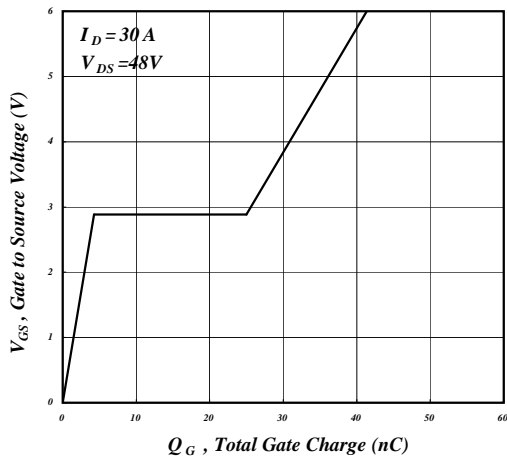


Fig 7. Gate Charge Characteristics

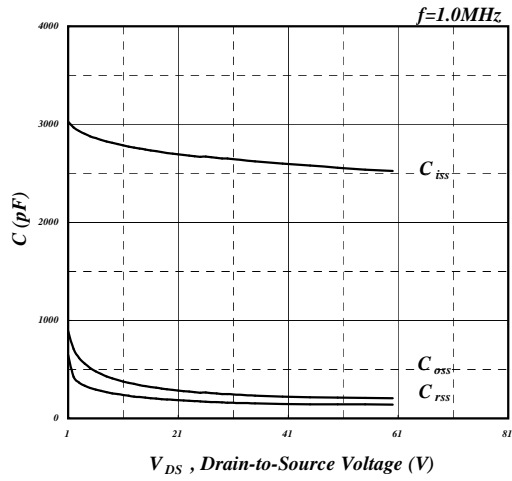


Fig 8. Typical Capacitance Characteristics

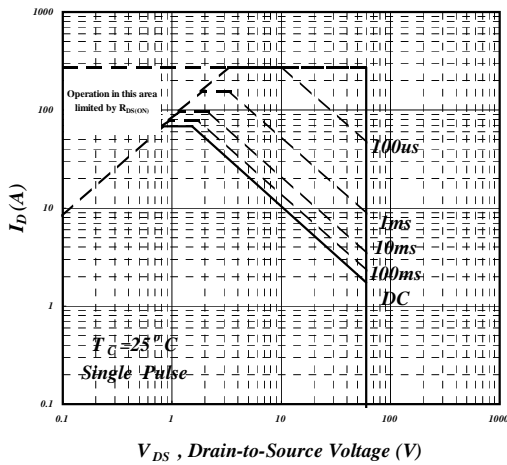


Fig 9. Maximum Safe Operating Area

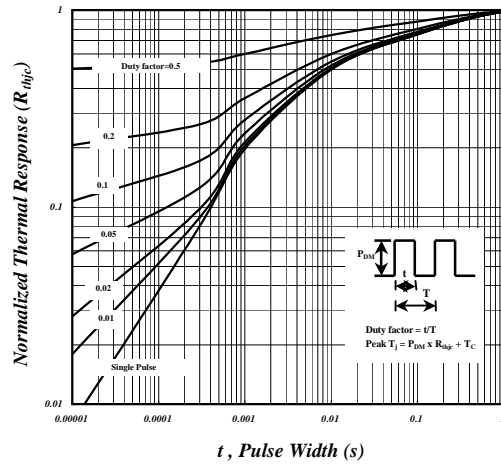


Fig 10. Effective Transient Thermal Impedance

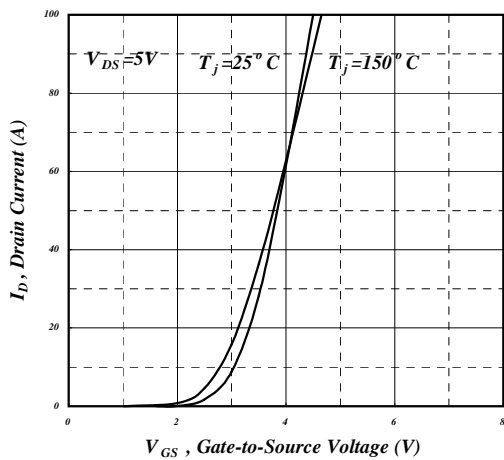


Fig 11. Transfer Characteristics

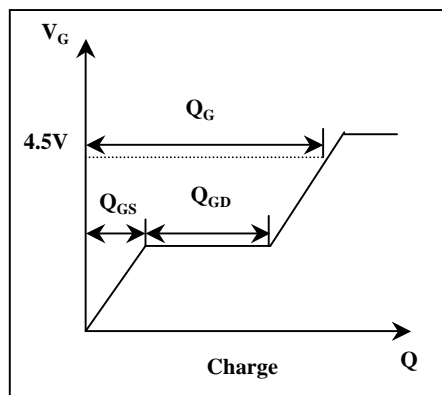


Fig 12. Gate Charge Waveform



# MARKING INFORMATION

