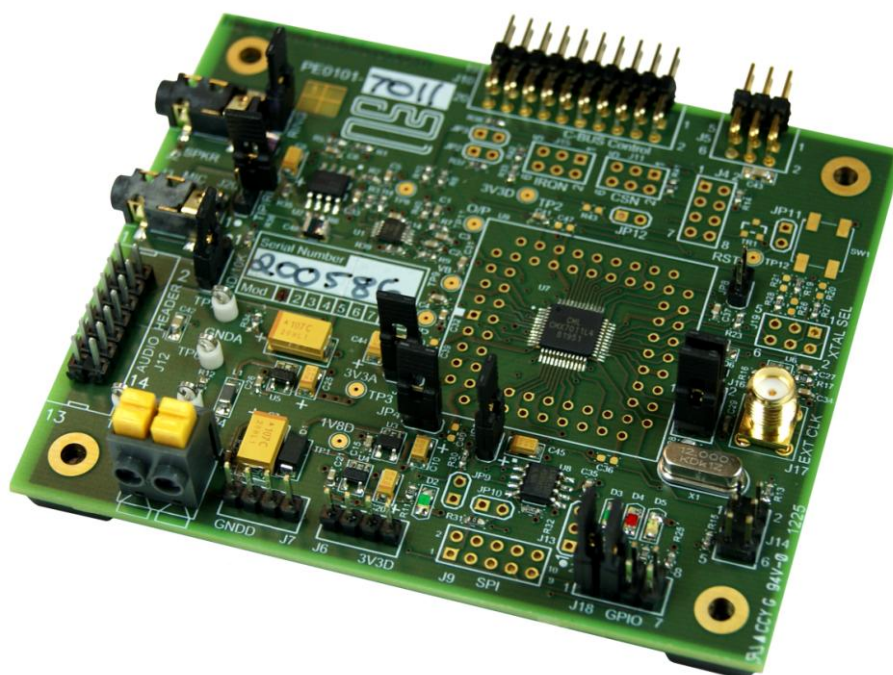


Features

- **CMX7x1x FirmASIC® Product Range Evaluation**
- **CMX188 Product Evaluation**
- **On-board Supply Regulators: Operation from a Single +5V Supply**
- **Command and Control by PC via:**
 - PE0002 Universal Interface Card or
 - User's μ C Development Application or
 - User's μ C Emulator



1 Brief Description

The PE0101 Platform Evaluation Kit is designed to assist in the demonstration, evaluation and application development of the CMX188¹ and CMX7x1x range of FirmASIC® products. The kit is in the form of a populated PCB comprising a CMX7x1x IC and appropriate supporting components and circuitry.

The board also incorporates all of the necessary power supply regulation facilities for operation from a single 5 volt supply.

The board is fitted with a C-BUS connector allowing the PE0101 to be operated by connection to either of the two C-BUS ports on a CML PE0002 Interface Card, and used with the associated PC GUI software, or by direct connection between the CMX7x1x C-BUS and the user's μ C development application or emulation system.

The CMX7x1x Function Image™ (FI) can be loaded, on power-up, directly into the on-board target IC (CMX7x1x) using the PE0002 interface or the user's system.

¹ Hereinafter, references to the CMX7x1x range of products should also include reference to the CMX188.

Function images suitable for the CMX7x1x range of products can be downloaded from the CML Technical Portal. A separate overlay is available for each product which can be evaluated with the PE0101, since the pin-names and jumper settings are dependent on the evaluation device which is fitted to this board. These overlays can be obtained from the CML Technical Portal [<http://www.cmlmicro.com/>].

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

Note that text shown in **pale grey** indicates features that will be supported in future versions of this Evaluation Kit.

1.1 History

Version	Changes	Date
3	Expanded product range to include CMX188 Mentioned the existence of product overlays for the PE0101 kit Details of TP8 (ext bias) added Added a reminder about jumper settings and the different device pin names	23 rd Oct '12
2	New photograph and PCB layout diagrams (top and bottom) Table 3 (Jumpers) – Jumper added to J14, pins 5 and 6 (to connect TEST (SYNC) pin to ground).	2 nd July '12
1	Original document.	11 th April '12

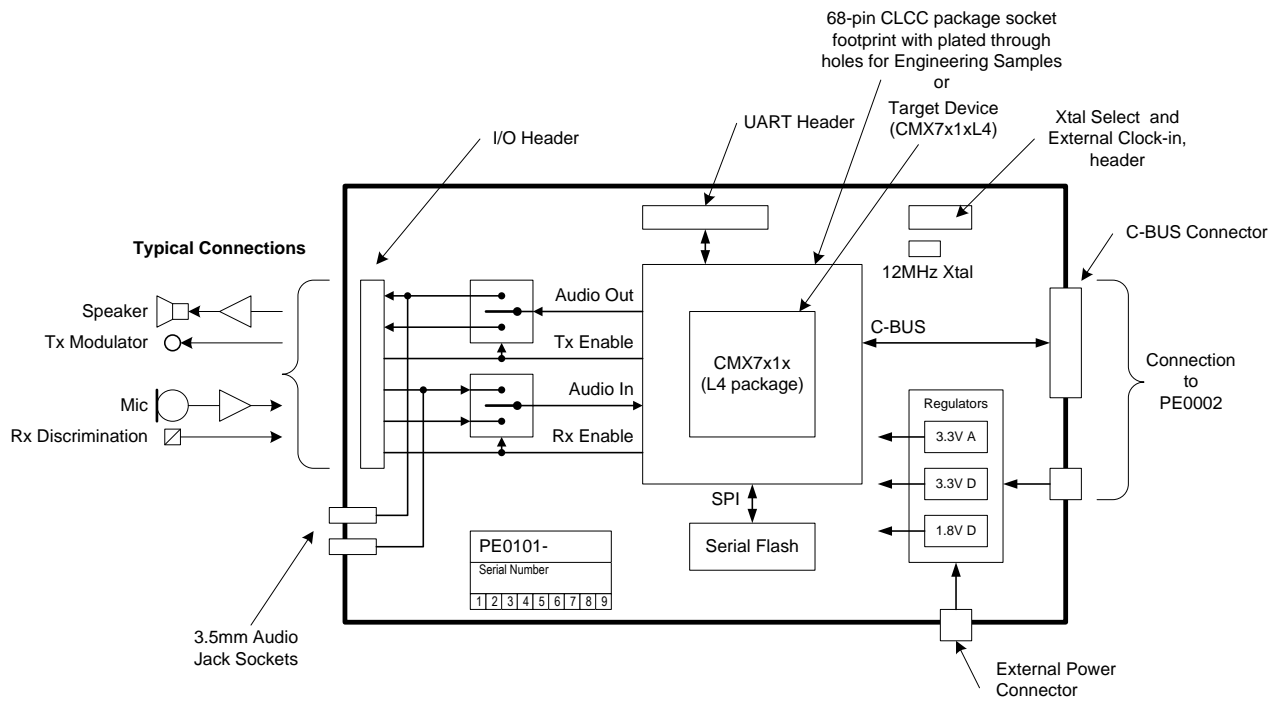


Figure 1 Block Diagram

2 Preliminary Information

The PE0101 is designed to support the CMX7x1x range of *FirmASIC*[®] devices using their respective Function Image[™].

The CMX7x1x IC fitted to the PE0101 is a special evaluation IC with the architecture of all CMX7x1x series ICs. The functionality of this evaluation IC is obtained from the relevant Function Image[™] (FI); evaluation FIs are downloaded from the CML Technical Portal. Each Function Image[™] can represent a different set of features.

2.1 Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

A 5V dc regulated power supply.

If the PE0101 is being used with the PE0002 Interface Card, the following items will also be required:

1. An IBM compatible PC with the following requirements:
 - One of the following Windows operating systems installed: Win7sp1, XPsp2 or 2000sp4.
 - USB port.
 - Minimum screen resolution of 800 x 600. Recommended resolution of 1024 x 768.
2. A USB type A male-to-mini B male cable.
3. Software application **ES000243.exe**, or later version, installed on the PC.

2.2 Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

2.2.1 Static Protection

This product uses low-power CMOS circuits that can be damaged by electrostatic discharge. Partially damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

2.2.2 Contents - Unpacking

Please ensure that all the items on the separate information sheet (EK0101) have been received and notify CML within seven working days if the delivery is incomplete.

2.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product.

3 Quick Start

This section is divided into two sub-sections. The first is for those users who are using the PE0101 with a PE0002 controller card and associated Windows PC GUI software. The second is for users who are using the PE0101 by itself, without a PE0002.

3.1 With PE0002

Note that the C-BUS connector J10 and the power connector J5 are both right-angle headers and are designed to plug directly into sockets J5 (C-BUS 1 port) and J9 respectively, or sockets J3 (C-BUS 2 port) and J7 respectively, of a PE0002. Power is supplied to the pair of boards either via connector J8 on the PE0101 or via connector J8 on the PE0002.

3.1.1 Setting-Up

Refer to the PE0002 user manual, and follow the instructions given in the quick start section. The basic arrangement, when used with the PE0002 is shown below:

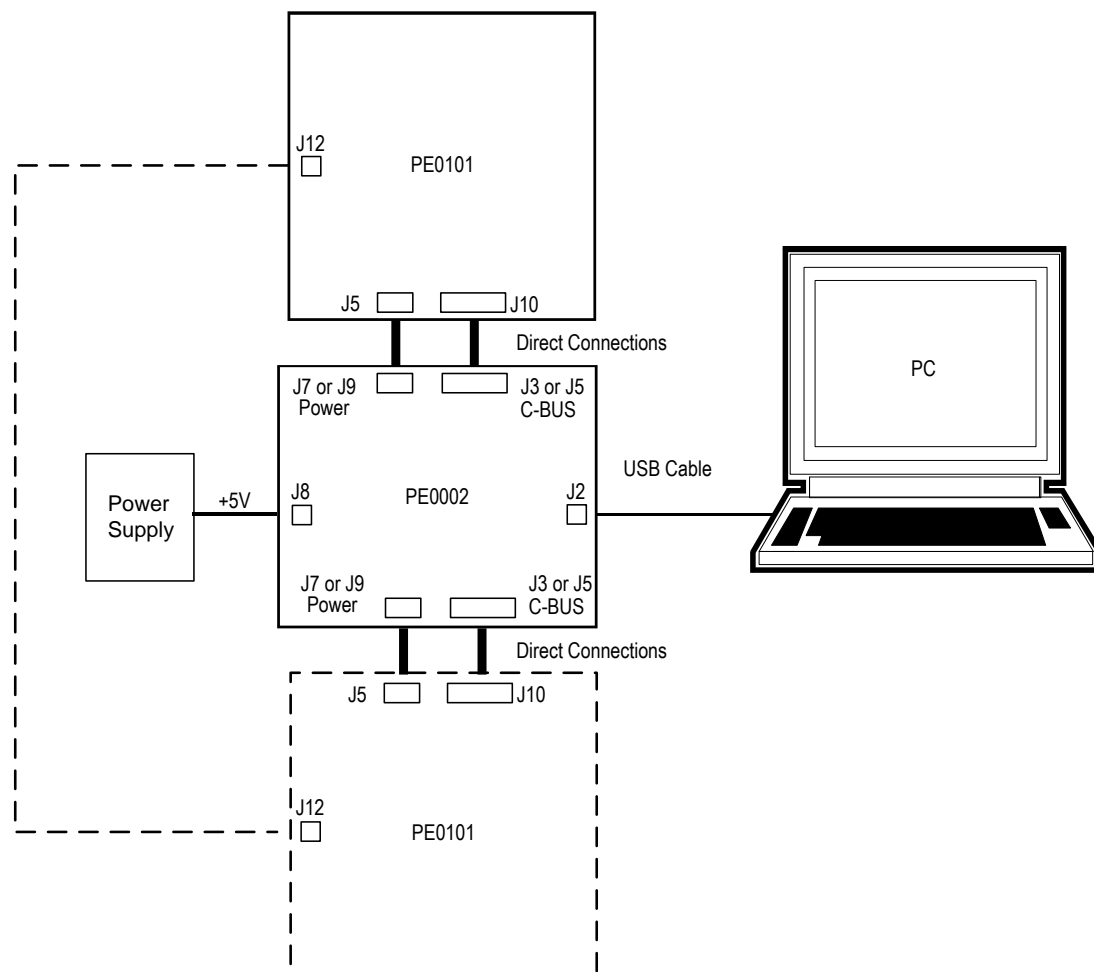


Figure 2 PE0101 used with PE0002

3.1.2 Jumper Settings

Check the jumper settings are correct by reference to Table 3, section 6.1 and Figure 5 before operating the board.

3.1.3 Operation

The Function Image™ (FI) must now be loaded into the CMX7x1x device. A FI is provided as a .ped type file and must be obtained from the CML Technical Portal after registration. A PE0002 script is provided to load the FI directly to the CMX7x1x, using the PE0002 script handler tab.

The PE0101 should now be ready for evaluation of the CMX7x1x.

3.2 Without PE0002

As an alternative to using the PE0002 controller kit, users may control the CMX7x1x target device with a user-supplied host controller card. C-BUS connections are made via connector J10 and the PE0101 should be powered via connector J8.

A FI for the CMX7x1x device must be either included in the customer's host system and loaded into the CMX7x1x device on power-up or programmed into the PE0101 on-board serial memory (U8) following the guidelines in the relevant datasheets and application notes.

Check the jumper settings are correct by reference to Table 3, section 6.1 and Figure 5 before operating the board.

4 Pin and Signal Lists

CONNECTOR PINOUT				
Connector Ref.	Connector Pin No.	Signal Name	Signal Type	Description
J2	-	SPKR	O/P	3.5mm Jack socket, speaker output
J3	-	MIC	I/P	3.5mm Jack socket, microphone input
J5	1, 2 3 to 6	GNDD +V	PWR PWR	Digital supply ground External supply voltage – Daisy chained from PE0002
J6	1 to 4	3V3D	PWR	Digital supply 3.3V
J7	1 to 4	GNDD	PWR	Digital supply ground
J8	1 2	0V +V	PWR PWR	External supply ground External supply voltage (5.0V)
J9 NOT POPULATED	1 2 3 4 5 6 7 8 9 10	SSOUT 3V3D SSIN MOSI GNDD SCLK OUT1 MISO OUT2 CSEL	O/P PWR I/P O/P PWR O/P O/P I/P O/P I/P	EPROM Chip select Digital supply 3.3V SSIN Master Out Slave in Digital supply ground Serial Clock Output 1 Master in serial Out Output 2 Chip select
J10	2 4 5 6 8 10 11, 12 16 17 18 1, 3, 7, 9, 13, 14, 15, 19, 20	CSN CDATA ENABLEXTAL CLK RDATA IRQN GNDD SOFT_RESET PEOUT1 PEOUT2	I/P I/P I/P I/P O/P O/P PWR I/P I/P I/P N/C	Chip select. Connects to host μ C, via R41 Serial Data input. Connects to host μ C Enable / disable XTAL Serial clock input. Connects to host μ C Serial data output. Connects to host μ C Interrupt request. Connects to host μ C, via R42 Digital supply ground PE0002 software reset Input to analogue switch for MIC/ RXDISC Input to analogue switch for SPKR/ TXMOD)) No connection)

CONNECTOR PINOUT				
Connector Ref.	Connector Pin No.	Signal Name	Signal Type	Description
J12	1	SPKR	O/P	Speaker output
	2	GNDA	PWR	Analogue supply ground
	3	TXMOD	O/P	TX Modulator output
	4	GNDA	PWR	Analogue supply ground
	5	MIC	I/P	Microphone input
	6	GNDA	PWR	Analogue supply ground
	7	RXDISC	I/P	RX discriminator input
	8	GNDA	PWR	Analogue supply ground
	9	OUT1	O/P	Output 1
	10	OUT2	O/P	Output 2
	11	OUT3	O/P	Output 3
	12, 13, 14		N/C	No connection
J17		EXT Clock	I/P	External Clk input (SMA connector)

Table 1 Signal List

TEST POINTS		
Test Point Ref.	Default Measurement	Description
TP1	1V8D	Pad – Power supply 1.8V digital
TP2	3V3D	Pad – Power supply 3.3V digital
TP3	3V3A	Pad – Power supply 3.3V analogue
TP4	GNDD	Pad – GNDD, digital ground
TP5	GNDD	Pad – GNDD, digital ground
TP6	GNDA	Pad – GNDA, analogue ground
TP7	GNDA	Pad – GNDA, analogue ground
TP8	EXT Bias	Pad – Externally generated V_{BIAS} output for audio circuits
TP9	VB	Pad – CMX7x1x V_{BIAS}
TP10	I/P	Pad – CMX7x1x AUDIO INPUT
TP11	O/P	Pad – CMX7x1x AUDIO OUTPUT
TP12	RST	Pad – CMX7x1x RESET INPUT

Table 2 Test Points

JUMPERS			
Link Ref.	Positions	Default Position	Description
JP1	1, 2	SHORT	Jumper to connect TIP to RING of 3.5mm jack J2
JP4	1, 2	SHORT	Jumper to enable 1.8V supply to CMX7x1x
JP5	1, 2	SHORT	Jumper to enable 3.3V digital supply to CMX7x1x
JP6	1, 2	SHORT	Jumper to enable 3.3V analogue supply to CMX7x1x
JP8	1, 2	OPEN	Jumper to disable crystal and clock input (open = enabled)
J1	1, 2 2, 3	OPEN SHORT	Jumper to connect MIC via 10k resistor to ground Jumper to connect MIC directly to ground (Connect the jumper to either 1, 2 or 2, 3).
J14	1, 2 3, 4 5, 6	OPEN OPEN SHORT)) Populated, but unused. Do not connect to these pins) Jumper to connect TEST pin to ground via 100k resistor (Connect the jumper to either 1, 2 or 3, 4 or 5, 6).
J16	1, 2 3, 4 5, 6	OPEN SHORT SHORT	Jumper to select External Clk operation Jumper to select 12MHz crystal operation Jumper to select 12MHz crystal operation (Connect a jumper to 1, 2 only or connect jumpers to 3, 4 and 5, 6 respectively, leaving 1, 2 unconnected).
J18	1, 2 3, 4 5, 6 7, 8	SHORT SHORT SHORT OPEN	Jumper to connect LED D3 to OUT1 Jumper to connect LED D4 to OUT2 Jumper to connect LED D5 to OUT3 Internal test input, which is pulled high via a 100k ohm resistor if no jumper is fitted, or pulled low if a jumper is fitted. The jumper setting is unimportant on CMX7011 and CMX188, as there is no internal connection to this pin.
J19	1, 2 3, 4 5, 6	OPEN OPEN OPEN)) Not populated. Do not connect to these XTALSEL pins.)
J20	1, 2 2, 3	OPEN OPEN	Jumper to connect powered mic supply to J3 Tip Jumper to connect powered mic supply to J3 Ring (Leave both jumpers unconnected for no mic power).

Table 3 Jumpers

LEDs	
LED Ref.	Description
D2	Indicates that the digital supply voltage is present (Green)
D3	Via Jumper J18 connection to OUT1 (Green)
D4	Via Jumper J18 connection to OUT2 (Red)
D5	Via Jumper J18 connection to OUT3 (Yellow)

Table 4 LEDs

Notes:

I/P	=	Input
O/P	=	Output
PWR	=	Power supply connection

5 Circuit Schematics and Board Layouts

For clarity, circuit schematics are available as separate high-resolution files. These can be obtained via the CML website.

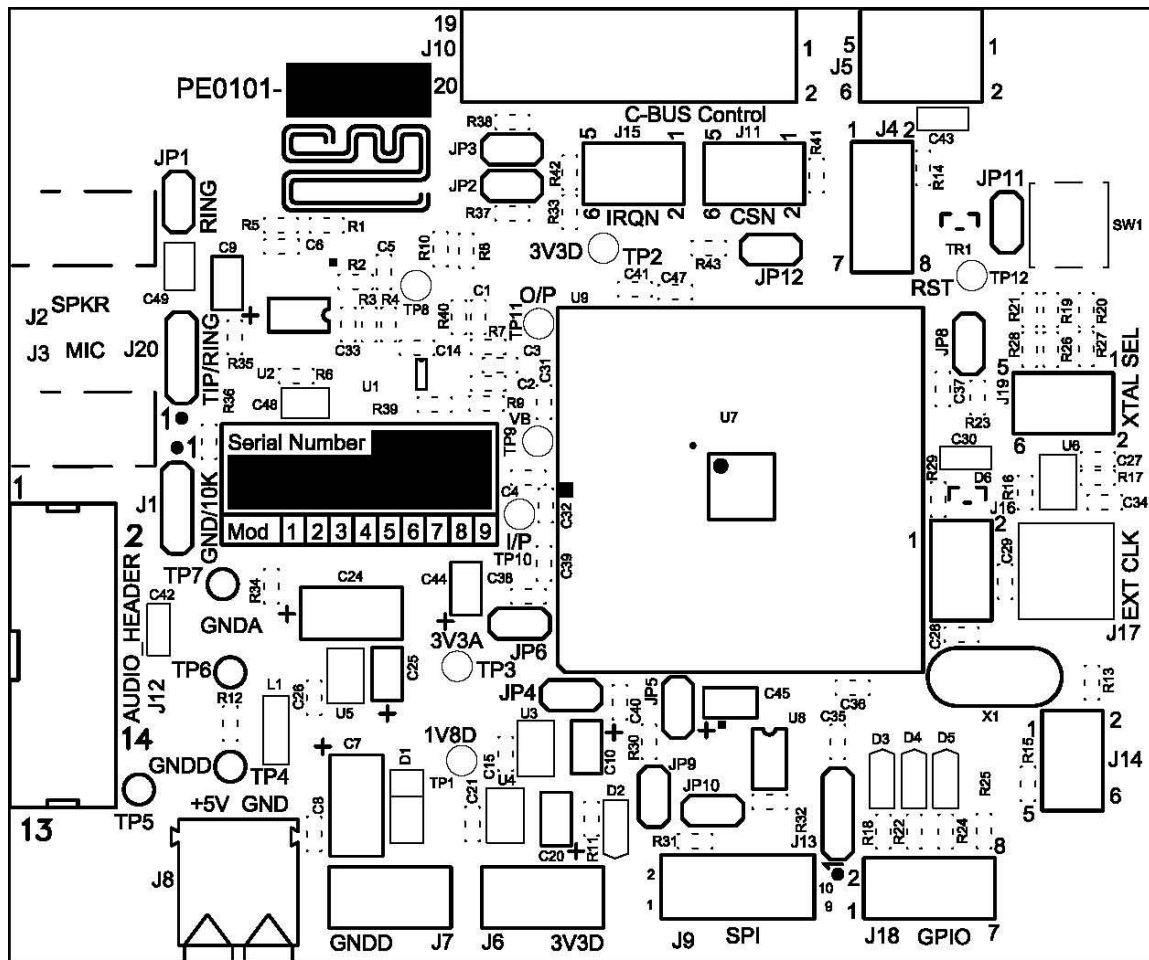


Figure 3 PCB Layout: Top

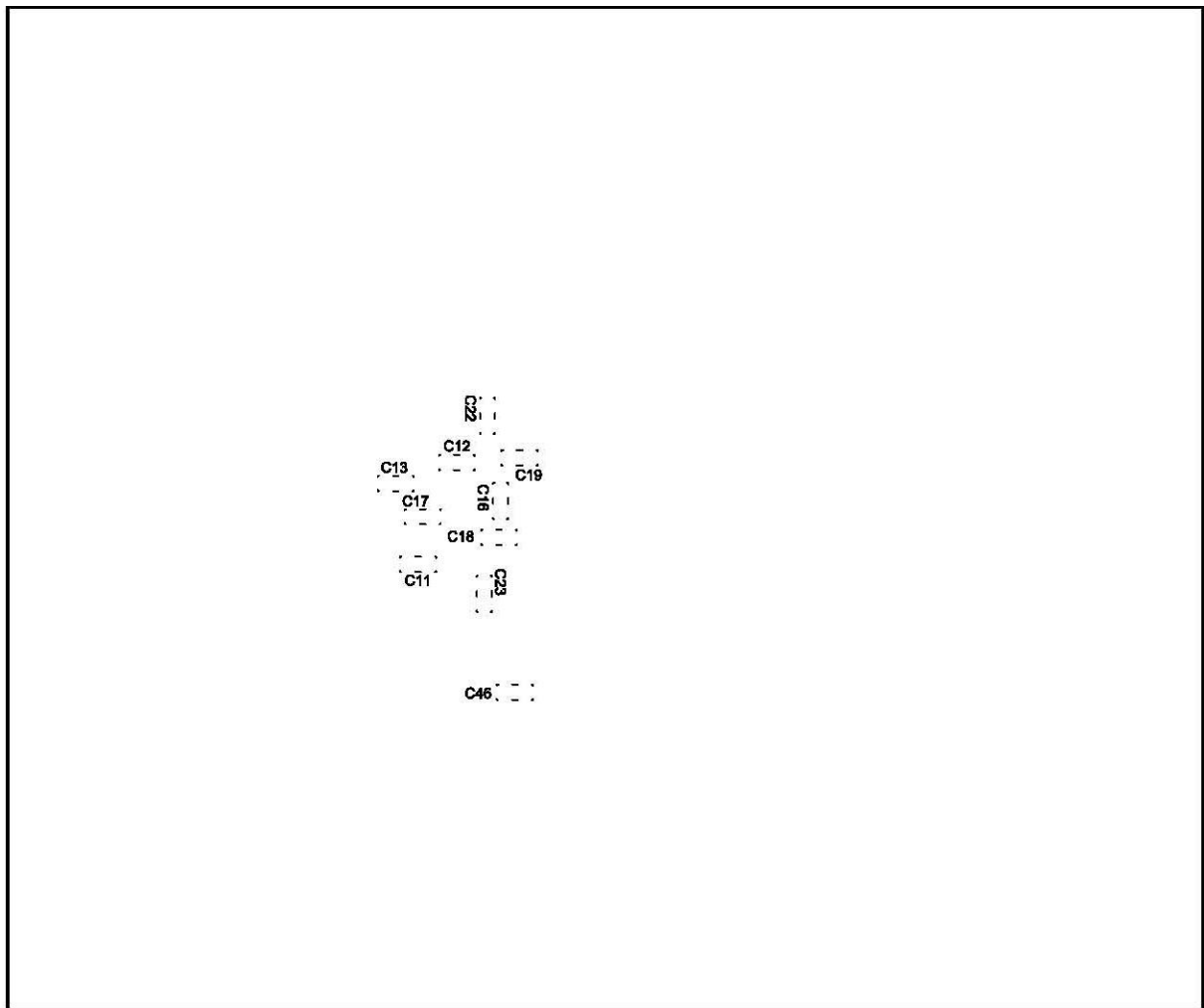


Figure 4 PCB Layout: Bottom

6 Detailed Description

6.1 Hardware Description

The PE0101 as shipped may not have the optimum configuration or component values for all Function Images™. Check the PE0101 schematic against recommendations in the specific CMX7x1x datasheet. Pin names differ between the board and the various CMX7x1x devices. Figure 5 shows the PE0101 board and CMX7011/CMX188 device pinouts.

6.1.1 Power Supplies

The board is fitted with three voltage regulators. U3, U4 and U6 provide the digital core, digital I/O and analogue supply rails respectively. The input to these three regulators should be provided by an external 5V dc regulated power supply, which can be daisy chained from the PE0002 or connected to the board via connector J8, a push type connector.

The digital and analogue supply voltage levels can be monitored on test points TP1 (1V8D), TP2 (3V3D) and TP3 (3V3A) respectively.

LED illumination confirms the on-board presence of the +3.3V dc digital voltage supply.

6.1.2 Clock Options

The PCB is designed to provide two CMX7x1x device clock options. The board is supplied with a 12MHz crystal fitted. The other option is an external clock source at J17.

Jumper block (Header) J16 is used to choose either 12MHz crystal or external clock.

Jumper block (Header) (Not Fitted) J19 can be used to change the clock or crystal frequency input to the CMX7x1x. The default setting, dictated by R27, R19, R28, is 12MHz. Other frequencies can be set by using the correct pull-up/pull-down combination of R20/R27, R19/R26 and R21/R28.

6.1.3 Control Interface

The C-BUS signals are brought out on connector J10. This is a right-angle male header designed to plug directly into the PE0002 interface card, that has a matching female header.

6.1.4 Serial Memory

The PE0101 is shipped with a blank serial memory (U8), type Atmel AT45DB041D.

6.1.5 Baseband Interfacing

Audio signals are routed for both input and output via an analogue switch block. The input is switchable between a Rx discriminator and a microphone input, the output is switchable between a Tx modulator and a speaker output. The analogue switches are controlled by outputs on the CMX7x1x (OUT1 and OUT2).

The CMX7x1x audio input is connected from the analogue switch via a single-pole low-pass filter with a 3dB cutoff of nominally 15kHz.

The CMX7x1x audio output is connected to the analogue switch via a single-pole low-pass filter. This filter will remove spurious high frequency signals. The 14-pin header J12 contains the analogue input and output interfaces and the OUT1 – OUT3 control outputs.

6.1.6 Digital Interfacing

Connector J12 also provides access to the three I/O lines (OUT1 – OUT3); two of these are used as control lines for the analogue switches discussed in section 6.1.5.

6.2 Configuration

PE0101 board pin-name			CMX7011 device pin-name																																									
		●	DVDD	VDD	IOVDD	IOVDD	IRQN	IRQN	CSN	CSN	RDATA	RDATA	CDATA	CDATA	CLK	CLK	VSS	VSS	TX	TX	RX	RX	RTS	RTS	RI	RI																		
AVDD	AVDD	1																								36	~ ~ ~ (n/c)	DCD																
AVSS	AVSS	2																								35	IOVDD	IOVDD																
BIAS	VBIAS	3																								34	ENABXTAL	ENABXTAL																
VSSREF	VSSREF	4																								33	XTALSEL3	XTALSEL3																
INPUTP	INPUTP	5																								32	XTALSEL2	XTALSEL2																
INPUTN	INPUTN	6																								31	XTALSEL1	XTALSEL1																
AVDD	AVDD	7																								30	RESETN	RESETN																
AVSS	AVSS	8																								29	IOVDD	IOVDDPLL																
VSSPA	VSSPA	9																								28	XTALN	XTALOUT																
OUTP	OUTP	10																								27	XTAL/CLK	XTALIN																
OUTN	OUTN	11																								26	DVSS	VSSPLL																
VDDPA	VDDPA	12																								25	TEST	SYNC																
			13	DVDD	VDD	14	(n/c)	~ ~ ~	OUT3	15	SDI	MOSI	16	SDO	MISO	17	SCLK	SCLK	18	(n/c)	~ ~ ~	SSIN	19	GPIO1	OUT1	20	GPIO2	OUT2	21	SSOUT	SSOUT	22	DVSS	VSS	23	(n/c)	~ ~ ~	CSEL	24	IOVDD	IOVDD			

Figure 5 Alternative Board/Device Pin Names for CMX7011/CMX188

An overlay diagram for the PE0101, for use when fitted with CMX7011 (loaded with FI-1.x) or CMX188, can be obtained from the CML Technical Portal [<http://www.cmlmicro.com/>]. The PE0101-7011 FI-1.x jumper settings are the default settings described in this document. Different CMX7x1x evaluation devices or Function Images™ may require the jumper settings to be changed. Details will be supplied with the Function Image™ or with an amendment to this document for alternative CMX7x1x evaluation devices.

6.3 Adjustments and Controls

None.

6.4 Download Protocol for Function Images™

Function Images™ can be downloaded into the CMX7x1x device by means of the script handler tab on the PE0002 GUI. Example scripts are provided for this purpose in the **ES0101xx.zip** software bundle.

New features and enhancements to existing functions are available as Function Images™. These are downloaded into the device over the C-BUS via the DECFRAME register (\$10). The data is sent in packets of 128 bytes. The Function Image™ will always be a whole multiple of 128 bytes. The following steps should be taken to download a Function Image™. Please check the documentation supplied with any Function Image™ which may detail a deviation from the following instructions.

1. Reset the device. This can be achieved by using either the RESETN pin (30), or by writing to the C-BUS RESET register (\$01).
2. Wait until the device indicates that it is ready. This can be done by either polling the STATUS register (\$40) and waiting for bit 15 (RDY) to be set to '1', or waiting until IRQN goes low, and then reading the STATUS register to reset it (bit 15 will have been set to '1').
3. If the process is to be interrupt driven (i.e. using IRQN to indicate a change in the STATUS register), then write the value of \$C000 to the IRQENAB register (\$1F). This will enable interrupts for the SVC bit (bit 14), which is used in the download protocol.
4. Write the value of \$01 to the SVCREQ register (\$0E). This indicates to the device that a Function Image™ is waiting to be downloaded.
5. Wait for bit 14 to be set to '1' in the STATUS register (either by polling or waiting for IRQN to go low).
6. Read the SVCACK register (\$2E) and check that bit 0 is set to '1'. This indicates that the device is able to accept a Function Image™.
7. Write 128 bytes of Function Image™ data to the DECFRAME register (\$10). This may be done as a single 128-byte streaming write, 128 single byte writes or 64 x 2-byte writes.
8. Wait for bit 14 to be set to '1' in the STATUS register (either by polling or waiting for IRQN to go low).
9. Read the SVCACK register (\$2E) and check that bit 0 is set to '1'. This indicates that the device has accepted the data packet.
10. If there is more data to send, go back to step 7.
11. Write the value of \$01 to the SVCREQ register (\$0E). This indicates to the device that all of the Function Image™ has now been sent.
12. Wait for bit 15 to be set to '1' in the STATUS register (either by polling or waiting for IRQN to go low).
13. Read the SVCACK register (\$2E) and check that bit 0 is set to '1'. This indicates that the device has accepted the Function Image™ and is now ready to be used.

The device should be reset, if at any time through the above sequence, when read, the SVCACK does not have bit 0 set to '1'.

Formats of the function image that can be used are:

- .h header format file
- .bfi binary file
- .ped one hexadecimal value per line
- .pes PE0002 file format.

Information on what features the Function Image™ provides, and instructions on how to use them, will be included with the Function Image™.

6.5 Troubleshooting

The CMX7x1x is a complex audio processor. If incorrectly programmed or modified, results will be at variance from datasheet performance. Please study the CMX7x1x datasheet, this manual and the associated schematics and layout drawings carefully when troubleshooting.

This section provides suggestions to help users resolve application issues they might encounter.

6.5.1 General

Error Observed	Possible Cause	Remedy
ES000243.exe software fails to run correctly and reports an error during start up.	Faulty USB port or cable.	Check USB cable to your PC.
	PE0002 or PE0101 is not powered up during start up.	Power up PE0002 (5.0V) and PE0101 (5.0V).
	Incorrect software for PE0002.	Contact: techsupport@cmlmicro.com
Programming data to PE0101 does not appear to work.	The data is being programmed to the wrong C-BUS port on PE0002.	Check whether the PE0101 is connected to PE0002 Port 1 (J5) or Port 2 (J3) and ensure that the correct window is used for programming data. (See PE0002 user manual for further information).

Table 5 Possible General Errors

6.5.2 Modification State

The modification state (mod state) of the PE0101 can be determined from the 'Board Mod' box printed on the PCB silkscreen. The highest number in the box that is blacked out gives the mod state. The following examples indicate a mod state of 3.

Board Mod			
●	●	●	4
5	6	7	8

Board Mod			
■	■	■	4
5	6	7	8

Figure 6 Examples of Mod State Identification

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply (+V – 0V)	-0.3	9.0	V
Voltage on any connector pin to V _{SS}	-0.3	3.6	V
Current into or out of +V and V _{SS} pins	0	+0.45	A
Current into or out of any other connector pin	-20	+20	mA

7.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (+V – 0V)		4.5	5.5	V
External Clock Frequency		3.0	24.576	MHz

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Evaluation Device Clock Frequency = 12MHz, +V = 5.0V, $T_{AMB} = +25^{\circ}\text{C}$.

For CMX7x1x parameters, see relevant CMX7x1x data sheet.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1, 2	–	15	–	mA
+3V3A on-board supply voltage		3.0	3.3	3.6	V
+3V3D on-board supply voltage		3.0	3.3	3.6	V
+1V8D on-board supply voltage		1.7	1.8	1.9	V
Analogue Parameters					
Impedances					
MIC or Disc Input Impedance	3	–	5	–	k Ω
Modulator Output Impedance	3	–	1	–	k Ω
SPKR Output Impedance	3	–	100	–	Ω
Signal Levels					
MIC or Disc Input Level		–	–	2.0	Vp-p
SPKR or Modulator Output Level		–	2.6	–	Vp-p
External Clock Input					
'High' pulse width		21	–	–	ns
'Low' pulse width		21	–	–	ns
Input Impedance (J17) – Resistance		–	150	–	k Ω
Input Impedance (J17) – Capacitance		–	20	–	pF

- Notes:**
1. PCB current consumption, not current consumption of the CMX7x1x.
 2. Not including any current drawn from pins by external circuitry.
 3. Small signal impedance.

7.1.4 Operating Characteristics – Timing Diagrams and Other Parameters

Please refer to relevant CMX7x1x Datasheet for details.



About FirmASIC®

CML's proprietary FirmASIC® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. FirmASIC® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a FirmASIC® device are determined by uploading its Function Image™ during device initialization. New function images may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. FirmASIC® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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