晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR
LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM-240320D4TNQW-00H(R)
APPROVED BY	
DATE	

☑Approved For Specifications
☐Approved For Specifications & Sample

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APPROVED BY	CHECKED BY	ORGANIZED BY

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2007/11/29	-	New Release.	Emil
2007/12/13	38	Modified Mechanical drawing.	Emil
2007/12/18	6	Addition the Color chromaticity (CIE1931).	Emil
2008/01/07	3	Correction the viewing angle to 9 O'clock.	Emil
2009/5/20	6	Update the Color chromaticity (CIE1931)	Edward
	34	Add guarantee declaration	Edward
2009/06/08	10	Addition the recommend connecter.	Emil
2009/11/17	--	Change to use 12 o'clock TFT LCD	Edward
	5	Update the contrast of LCD to 350 : 1	Edward
		Update viewing angle	
	--	Rename to AM-240320D4TNQW-00H(R)	Edward
2009/11/18	2	Update Features	Edward
	5	Update Brightness of module	Edward

1 Features

This single-display module is suitable for hand-held application. The LCD adopts one backlight with High brightness 6-lamps white LED and Touch panel

(1) LCD: 1.1 Amorphous-TFT 3.2 inch display, transmissive, Normally white type.
1.2 240(RGB)×320 dots Matrix
1.3 LCD Driver IC: ILI9320
1.4 Full 262,144 colors display.
Back ground: black (Back-Light, Red, Green, Blue dots are off state)
1.5 Viewing Direction 12 o'clock
(2) Low cross talk by frame rate modulation
(3) Direct data display with display RAM
(4) Partial display function: You can save power by limiting the display space.
(5) MPU 8,9,16, and18-bit interface selectable.

IM3	IM2	IM1	IM0	MPU mode	DB Pin in use	Remark
PIN9	JP2	PIN8	PIN7			
0	0 (2,3Short)	1	0	80-16BIT	DB[17:10],DB[8:1]	Default Selectable
0	0 (2,3Short)	1	1	80-8BIT	DB[17:10]	Default Selectable
1	0 (2,3Short)	1	0	80-18BIT	DB[17:0]	Default Selectable
1	0 (2,3Short)	1	1	80-9BIT	DB[17:9]]	Default Selectable
0	1 (1,2Short)	0	ID	SPI	SDI ,SDO	Must change JP2

* Others setting invalid

(6) ROHS compliant.
(7) Abundant command functions:
Area scroll function
Display direction switching function
Power saving function

(8) Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
Active Display Size		3.2 inch diagonal(81.28mm)	mm
Main LCD	Outline Dimension	55.64 (H) x 77.3(V)	mm
	Pixel pitch	0.2025 (H) x 0.2025(V)	mm
	Active area	48.6 (H) x 64.8 (V)	mm
	Number of Pixels	240(H)x320(V) pixels	mm

2 Absolute max. ratings and environment

2-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+4.0	V	
Power voltage	VBAT	-0.5	+6	V	
Input voltage	VIN	-0.5	VDD+0.5	V	

2-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +70°C Min. -20°C	Note 1: Non-condensing
Operating temperature	Max. +60°C Min. -10°C	Note 1: Non-condensing

Note 1：Ta≦+40°C・・・・Max.85%RH

Ta＞+40°C・・・・The max. humidity should not exceed the humidity with 40°C 85%RH.

3 Electrical specifications

3-1 Electrical characteristics of LCM

(V_{DD}=3.0V, Ta=25°C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{DD}		2.5	3.0	3.3	V
High-level input voltage	V_{IHC}		$0.8V_{DD}$		V_{DD}	V
Low-level input voltage	V_{ILC}		0		$0.2V_{DD}$	V
Consumption current of VDD	I_{DD}	LED OFF	-	(6)		mA

3-2 LED back light specification

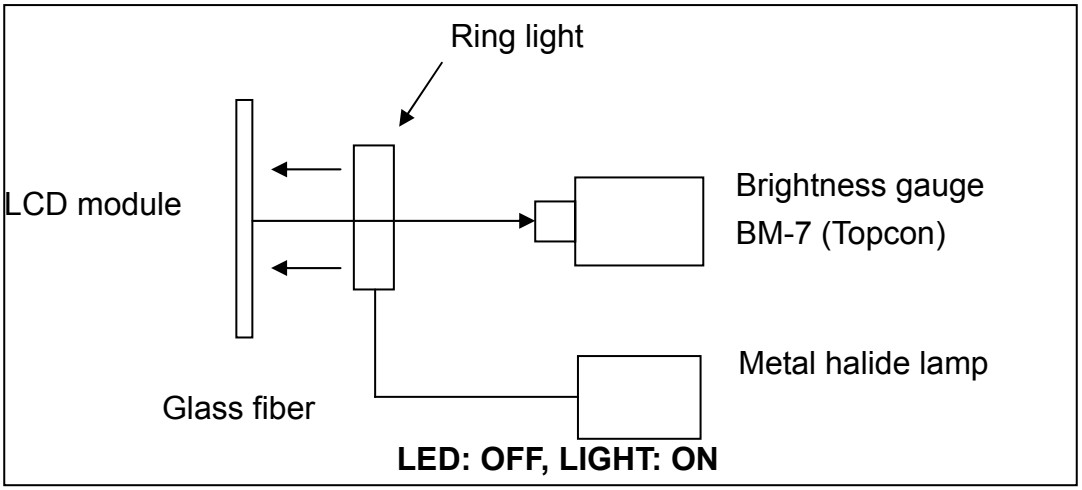
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =15mA	-	(19)	-	V
Forward current	I_f	Vf=19V	-	(15)	(20)	mA
Uniformity (with L/G)	-	I_f=15mA	70%	-	-	
C.I.E.	X		0.265	0.30	0.335	
	Y		0.275	0.31	0.345	
Luminous color	White					
Chip connection	6 chip serial connection					

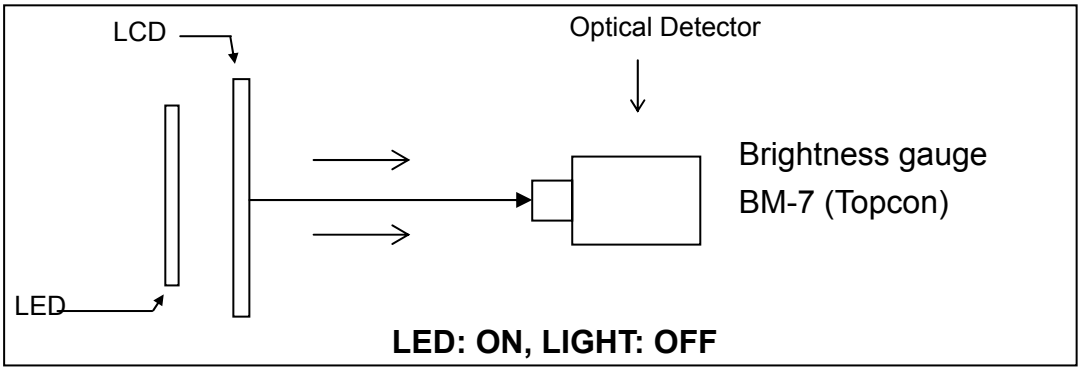
4 Optical characteristics

Item		Symbol	Min.	Std.	Max.	Unit	Conditions
Contrast ratio		CR	-	350	-	-	θ=0° Φ=0° Normal viewing angle
Response time	Rising	Tr	-	(15)	-	ms	
	Faling	Tf	-	(35)	-		
White luminance (center of screen)		YL		200		cd/m2	
Color chromaticity (CIE1931)	Red	Rx	0.54	0.59	0.63		
		RY	0.30	0.34	0.38		
	Green	GX	0.29	0.33	0.37		
		GY	0.56	0.60	0.64		
	Blue	Bx	0.10	0.14	0.18		
		BY	0.02	0.06	0.10		
	White	WX	0.26	0.30	0.34		
		WY	0.27	0.31	0.35		
Viewing angle	Hor.	θL	(60)			Degree	CR>10
		θR	(60)				
	Ver.	θF	(60)				
		θB	(50)				

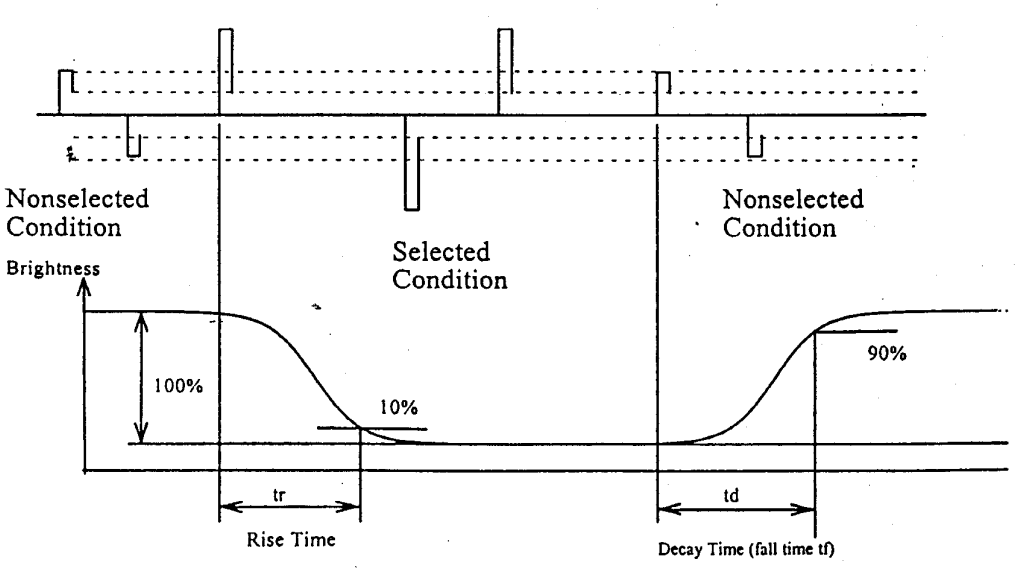
Note : ( )For reference only.

NOTE 1: Optical characteristic measurement system

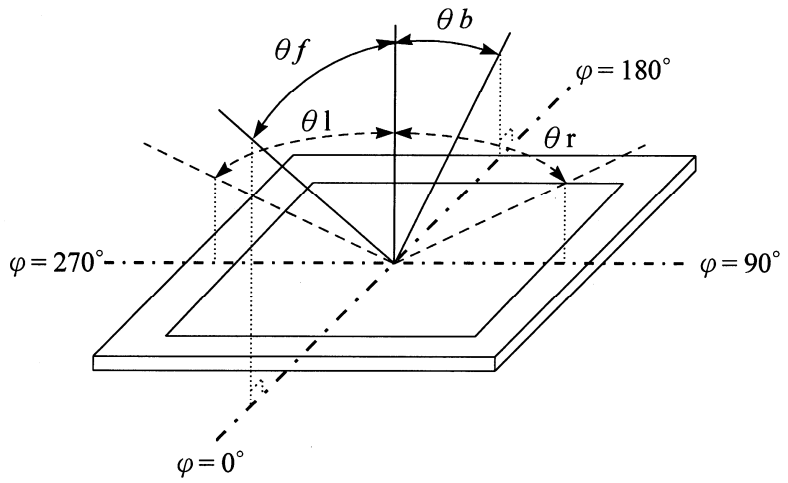




NOTE 2: Response tome definition

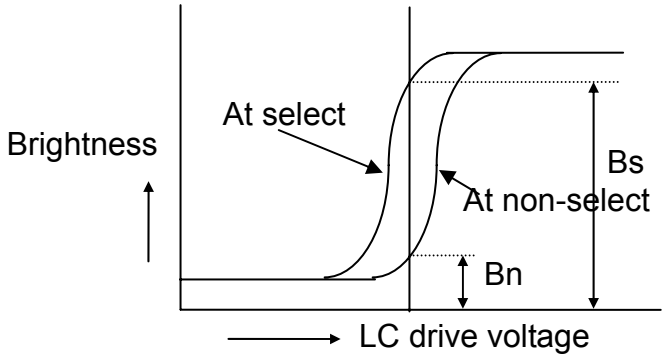


NOTE 3: φ、θ definition

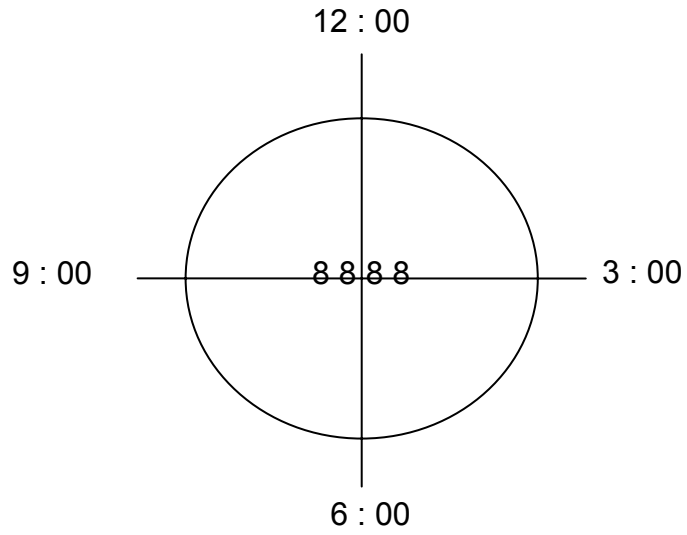


NOTE 4: Contrast definition

CR = Brightness in select (Bs)／Brightness in non-select (Bns)

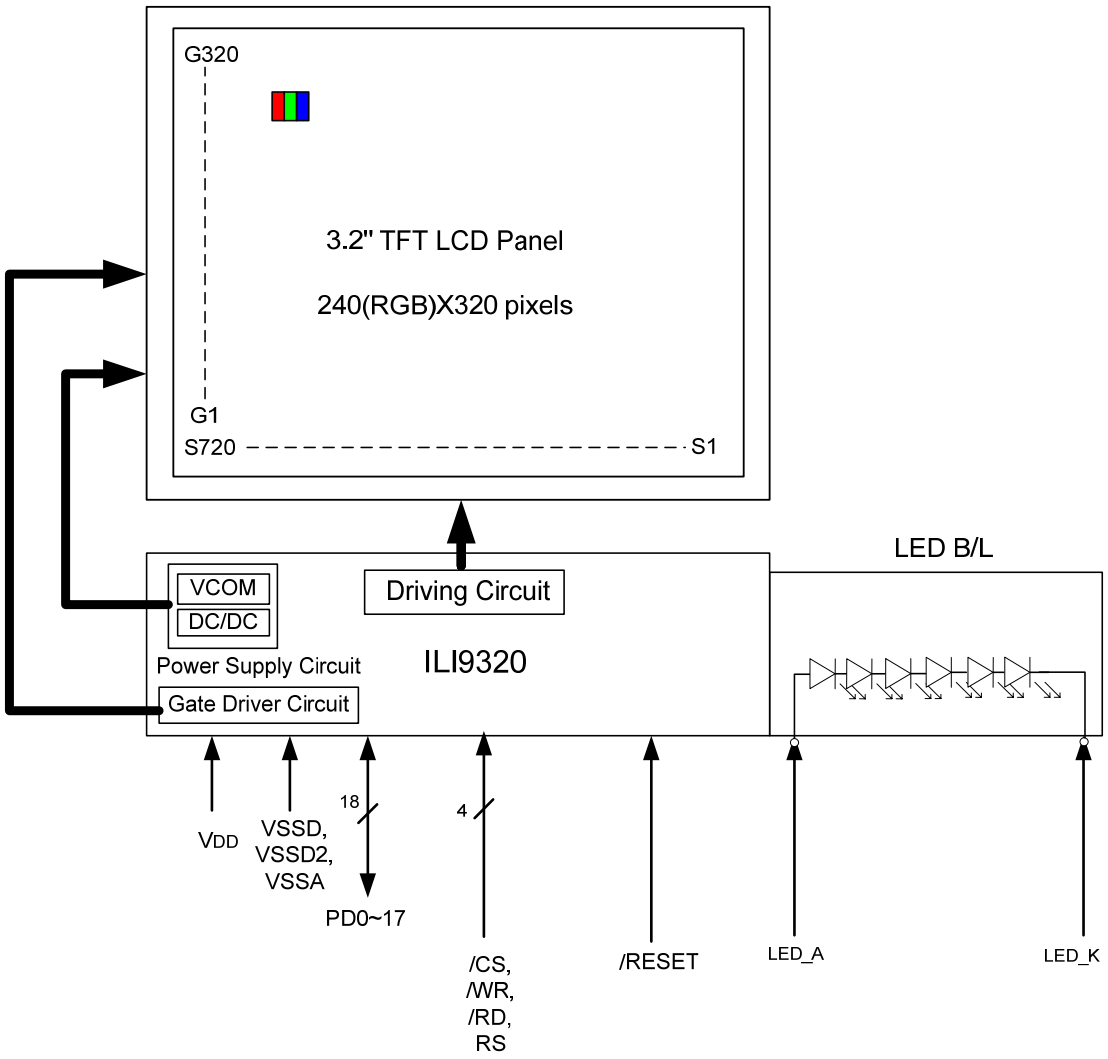


NOTE 5: Visual angle direction priority



5 Block Diagram

Display format: A-Si TFT transmissive, Normally white type.
Display composition: 240(RGB) x 320 dots
LCD Driver: ILI9320
Back light: White LED x 6 (I_{LED}=15mA)



6 Interface specifications

Connecter pitch:0.3mm

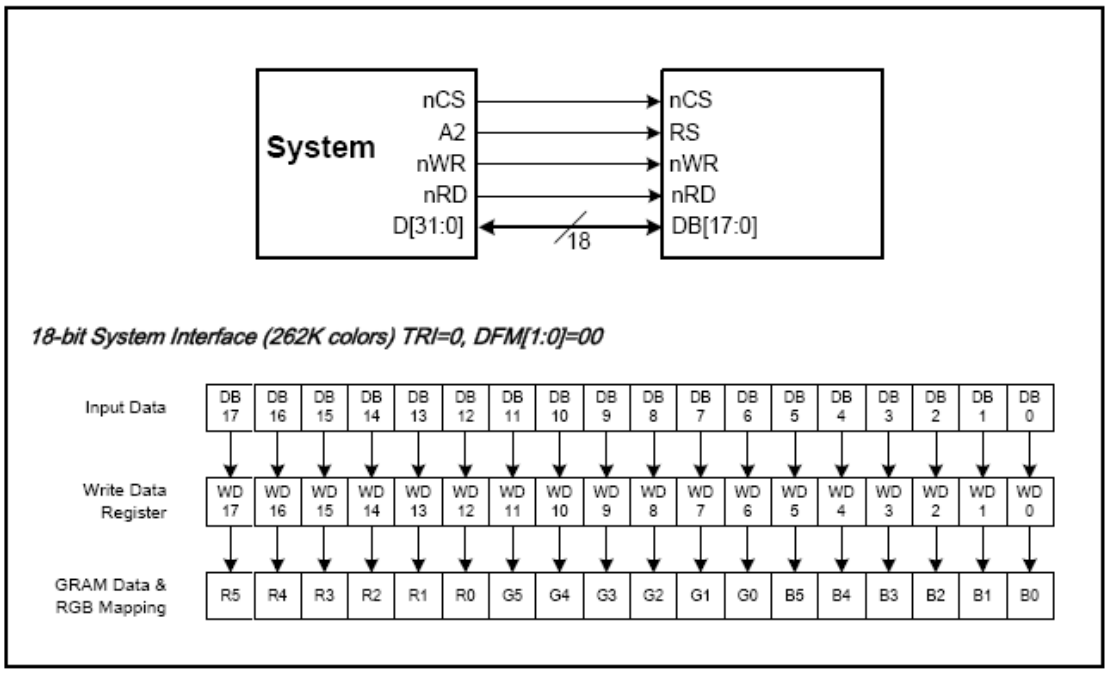
Recommend Connecter: JAE FF0245S

<table>
<tr><th>Pin No.</th><th>Terminal</th><th>Functions</th></tr>
<tr><td>1</td><td>VSS</td><td>Ground pins.</td></tr>
<tr><td>2</td><td>XL</td><td>Touch Panel Left Side.</td></tr>
<tr><td>3</td><td>XR</td><td>Touch Panel Right Side.</td></tr>
<tr><td>4</td><td>YD</td><td>Touch Panel Down Side.</td></tr>
<tr><td>5</td><td>YU</td><td>Touch Panel Up Side.</td></tr>
<tr><td>6</td><td>VSS</td><td>Ground pins.</td></tr>
<tr><td>7</td><td>IM0/ID</td><td rowspan="6"><table>
<tr><th>IM3</th><th>IM1</th><th>IM0/ID</th><th>MPU-Interface Mode</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>i80-system 16-bit interface</td><td>DB[17:10], DB[8:1]; (JP1 2-3short)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>i80-system 8-bit interface</td><td>DB[17:10]; (JP1 2-3short)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>i80-system 18-bit interface</td><td>DB[17:0]; (JP1 2-3short)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>i80-system 9-bit interface</td><td>DB[17:9]; (JP1 2-3short)</td></tr>
<tr><td>0</td><td>0</td><td>ID</td><td>Serial Peripheral Interface</td><td>SDI, SDO; (JP1 1-2short)</td></tr>
</table></td></tr>
<tr><td>8</td><td>IM1</td></tr>
<tr><td>9</td><td>IM3</td></tr>
<tr><td>10</td><td>SDO</td><td>Serial bus interface data output pin.</td></tr>
<tr><td>11</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>12</td><td>SDI</td><td>Serial bus interface data input pin.</td></tr>
<tr><td>13-30</td><td>D17-D0</td><td>18-bit bidirectional bus
Connect to VSS when the serial interface is selected.</td></tr>
<tr><td>31</td><td>/CS</td><td>Chip selection pin.
The “L” level enables inputting commands and reading /writing data.</td></tr>
<tr><td>32</td><td>/RESET</td><td>Switching to “L” initializes internally.
Must be reset after the power is supplied.</td></tr>
<tr><td>33</td><td>RS</td><td>Command/display Data Selection.</td></tr>
<tr><td>34</td><td>WR/SCL</td><td>Write enable signal/Serial bus interface clock input pin.</td></tr>
<tr><td>35</td><td>/RD</td><td>Read enable signal.</td></tr>
<tr><td>36</td><td>VSYNC</td><td>Frame synchronizing signal in RGB I/F mode. (JP1 1-2short)</td></tr>
<tr><td>37</td><td>HSYNC</td><td>Frame synchronizing signal in RGB I/F mode. (JP1 1-2short)</td></tr>
<tr><td>38</td><td>DOTCLK</td><td>Dot clock signal in RGB I/F mode. (JP1 1-2short)</td></tr>
<tr><td>39</td><td>ENABLE</td><td>A data ENABLE signal in RGB I/F mode. (JP1 1-2short)</td></tr>
<tr><td>40</td><td>VCC</td><td rowspan="2">Power supply for Step-up circuit. (VCI=2.5~3.3V).</td></tr>
<tr><td>41</td><td>VCC</td></tr>
<tr><td>42</td><td>VSS</td><td>Ground pins.</td></tr>
<tr><td>43</td><td>LED_K</td><td>Power supply for LED (Cathode).</td></tr>
<tr><td>44</td><td>LED_A</td><td>Power supply for LED (Anode).</td></tr>
<tr><td>45</td><td>VSS</td><td>Ground pins.</td></tr>
</table>

7 System Interface

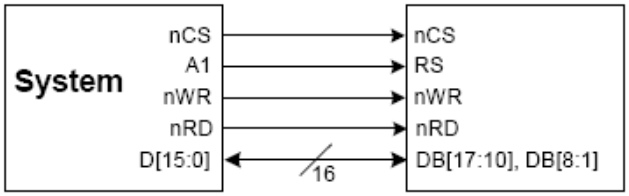
7.1 80-system 18-bit interface

The i80/18-bit system interface is selected by setting the IM[3:0] as "1010" levels.



7.2 80-system 16-bit interface

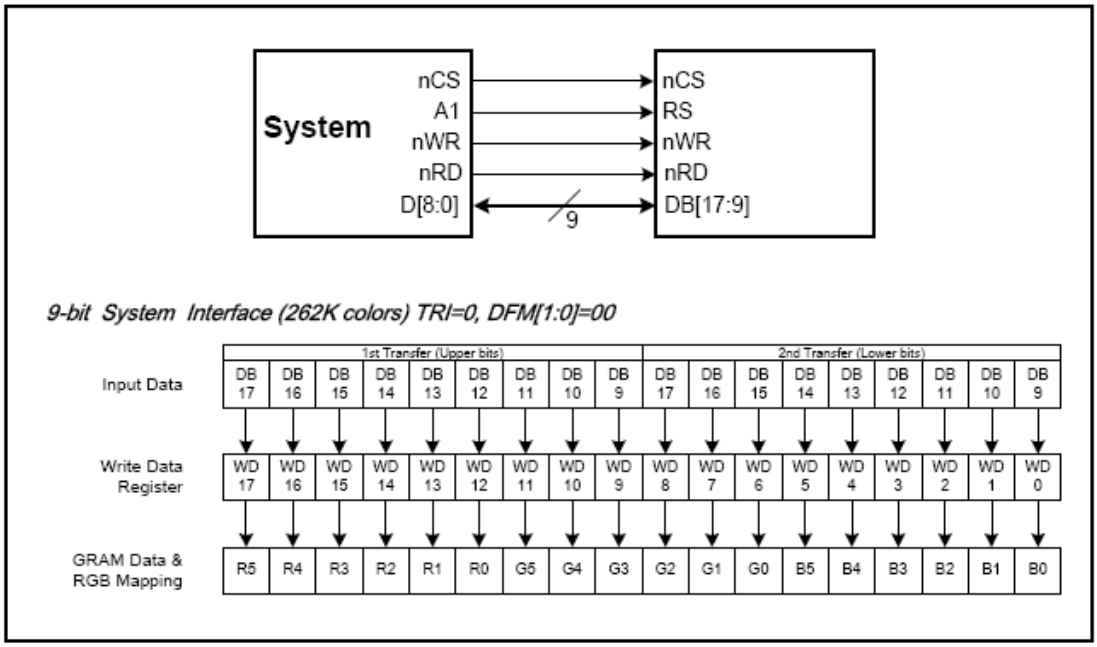
The i80/16-bit system interface is selected by setting the IM[3:0] as "0010" levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1st transfer: 2 bits, 2nd transfer: 16 bits or 1st transfer: 16 bits, 2nd transfer: 2 bits) are necessary for the 16-bit CPU interface.



TRI	DFM	16-bit MPU System Interface Data Format
0	*	system 16-bit interface (1 transfers/pixel) 65,536 colors
1	0	80-system 16-bit interface (2 transfers/pixel) 262,144 colors
1	1	80-system 16-bit interface (2 transfers/pixel) 262,144 colors

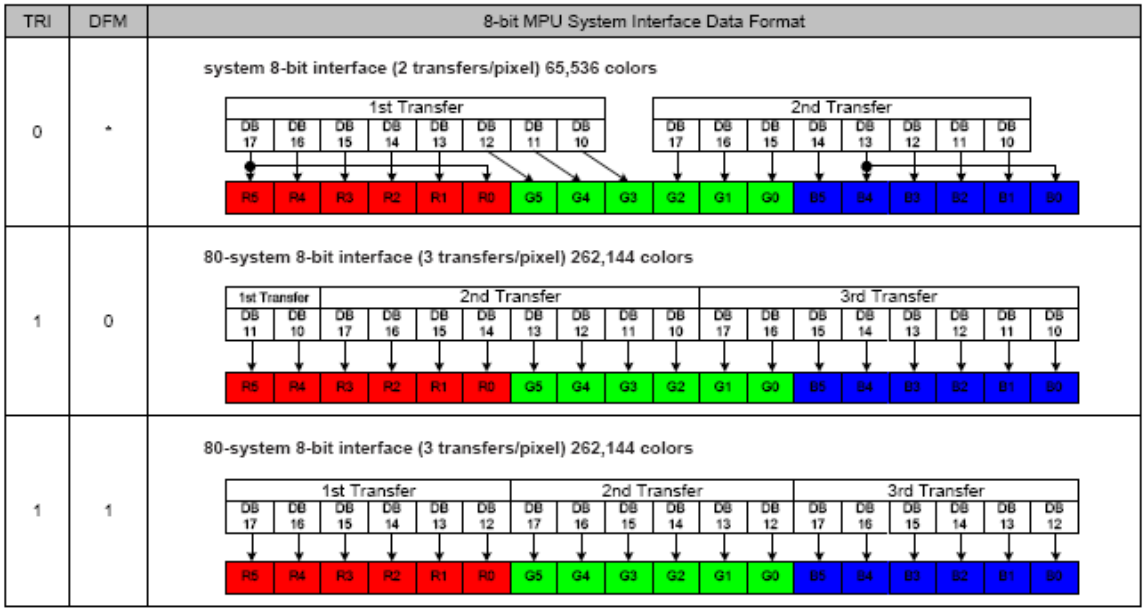
7.3 80-system 9-bit interface

The i80/9-bit system interface is selected by setting the IM[3:0] as "1011" and the DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to either Vcc or AGND.



7.4 80-system 8-bit interface

The i80/8-bit system interface is selected by setting the IM[3:0] as "0011" and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to either Vcc or AGND.



Data transfer synchronization in 8/9-bit bus interface mode

ILI9320 supports a data transfer synchronization function to reset upper and lower counters which count the transfers numbers of upper and lower byte in 8/9-bit interface mode. If a mismatch arises in the numbers of transfers between the upper and lower byte counters due to noise and so on, the "00"h register is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper byte. This synchronization function can effectively prevent display error if the upper/lower counters are periodically reset.

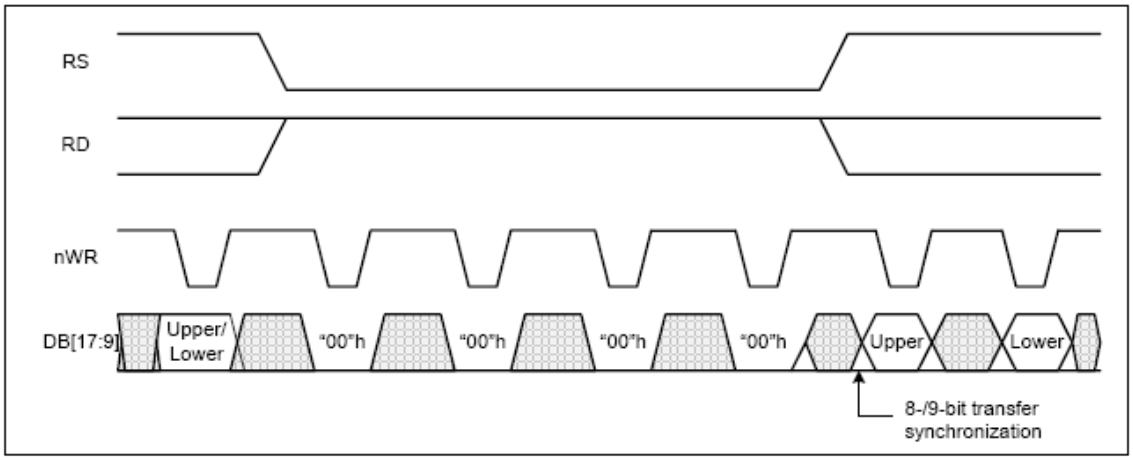


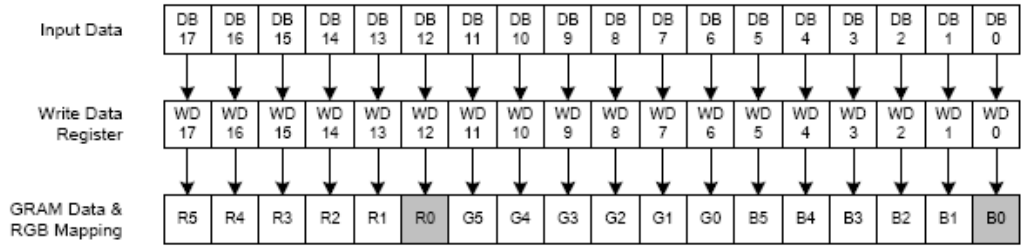
Figure6 Data Transfer Synchronization in 8/9-bit System Interface

7.5 RGB interface

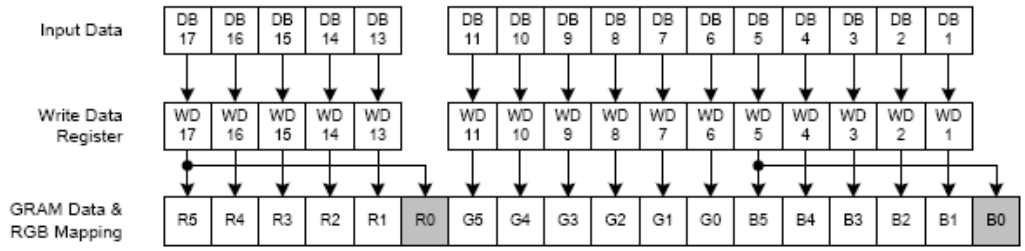
The RGB Interface mode is available for ILI9320 and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

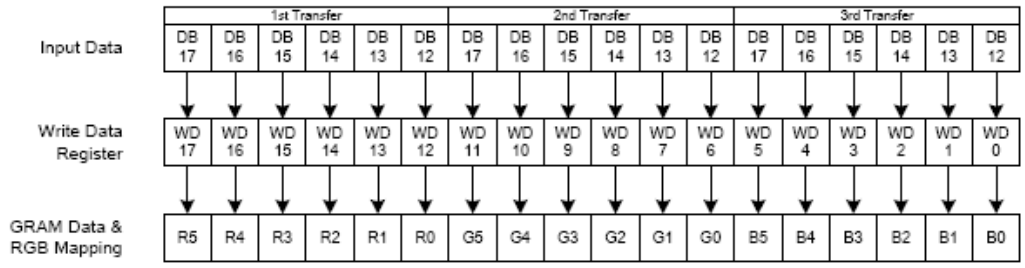
18-bit RGB Interface (262K colors)



16-bit RGB Interface (65K colors)

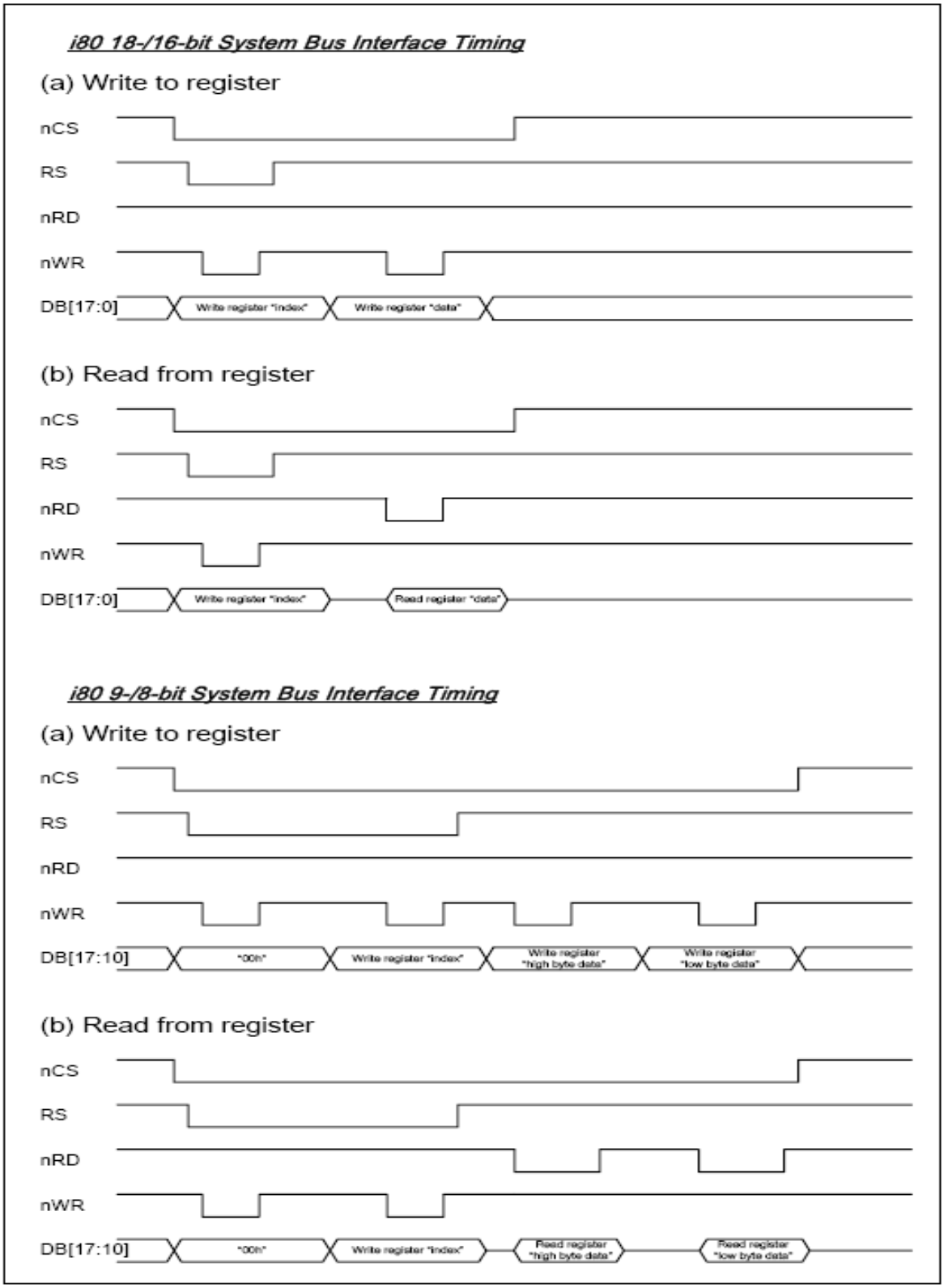


6-bit RGB Interface (262K colors)



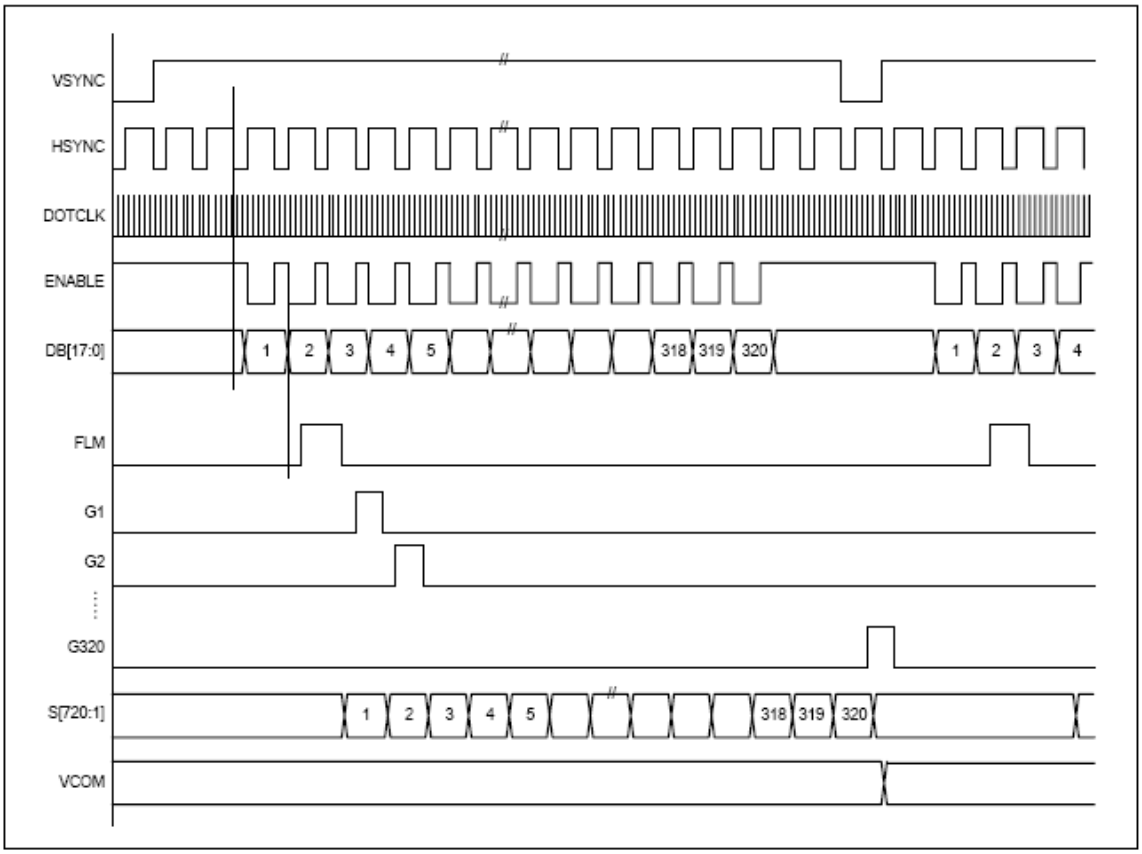
7.6 Timing of System Interface and RGB Interface

a. System Interface



b. RGB Interface

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.



8 INSTRUCTION DESCRIPTIONS

8.1 Instruction List

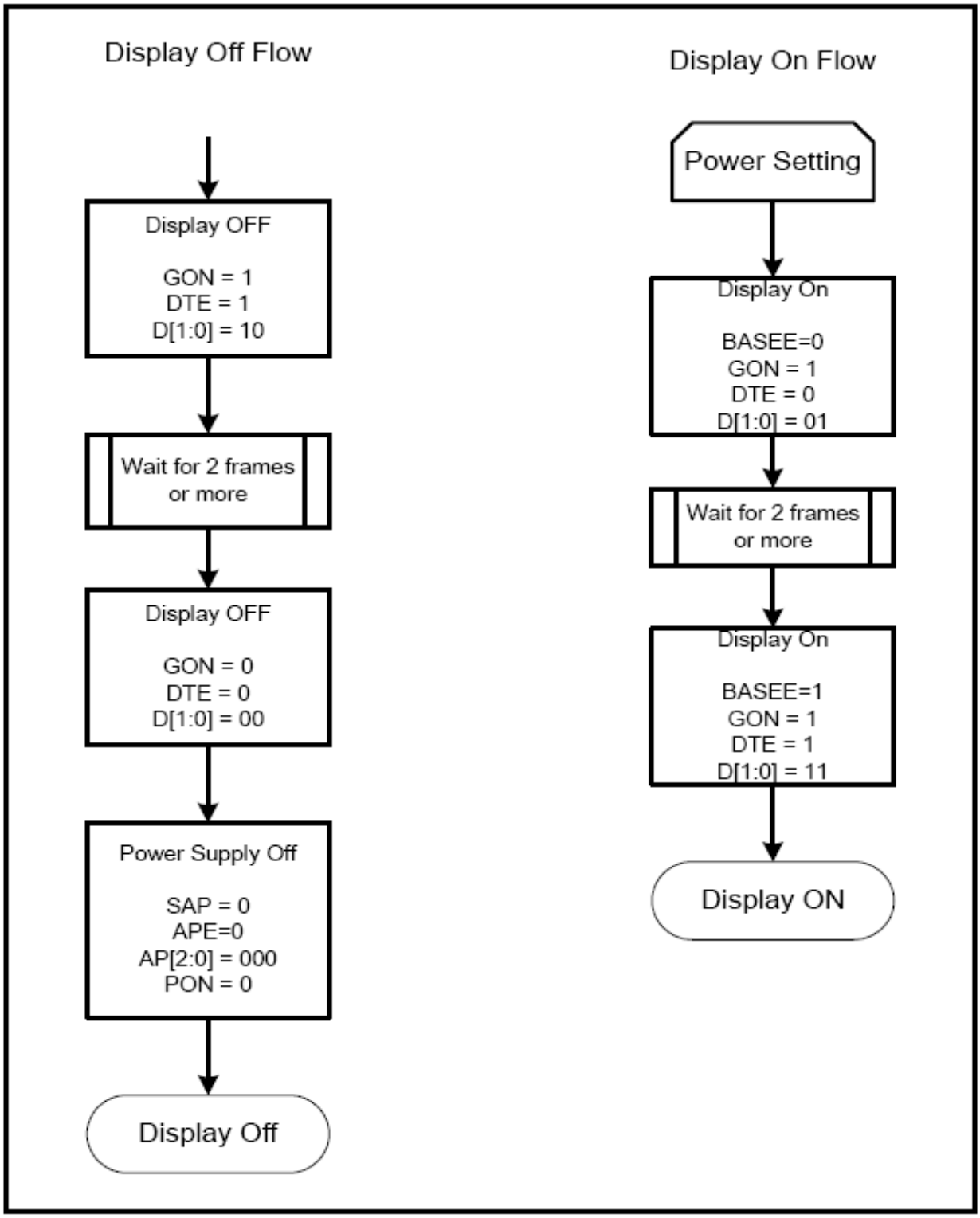
Main LCD Driver IC:ILI9320

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
00h	Driver Code Read	R	1	1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0
00h	Start Oscillation	W	1	-	-	-	-	-		-	-		-	-	-	-	-	-	OSC
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0
04h	Resize Control	W	1	0	0	0	0	0	0	RCV 1	RCV 0	0	0	RCH 1	RCH 0	0	0	RSZ1	RSZ0
07h	Display Control 1	W	1	0	0	PTD E1	PTD E0	0	0	0	BAS EE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMA RKO E	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	ENC 2	ENC 1	ENC 0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP 8	FMP 7	FMP 6	FMP 5	FMP 4	FMP 3	FMP 2	FMP 1	FMP 0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSP L	0	DPL	EPL
10h	Power Control 1	W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DST B	SLP	0
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	VCM R	0	0	0	PON	VRH 3	VRH 2	VRH 1	VRH 0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	0	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	EXT_ R	0	FR_S EL1	FR_S EL0	0	0	0	0
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1 [4]	VRP1 [3]	VRP1 [2]	VRP1 [1]	VRP1 [0]	0	0	0	VRP0 [4]	VRP0 [3]	VRP0 [2]	VRP0 [1]	VRP0 [0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]

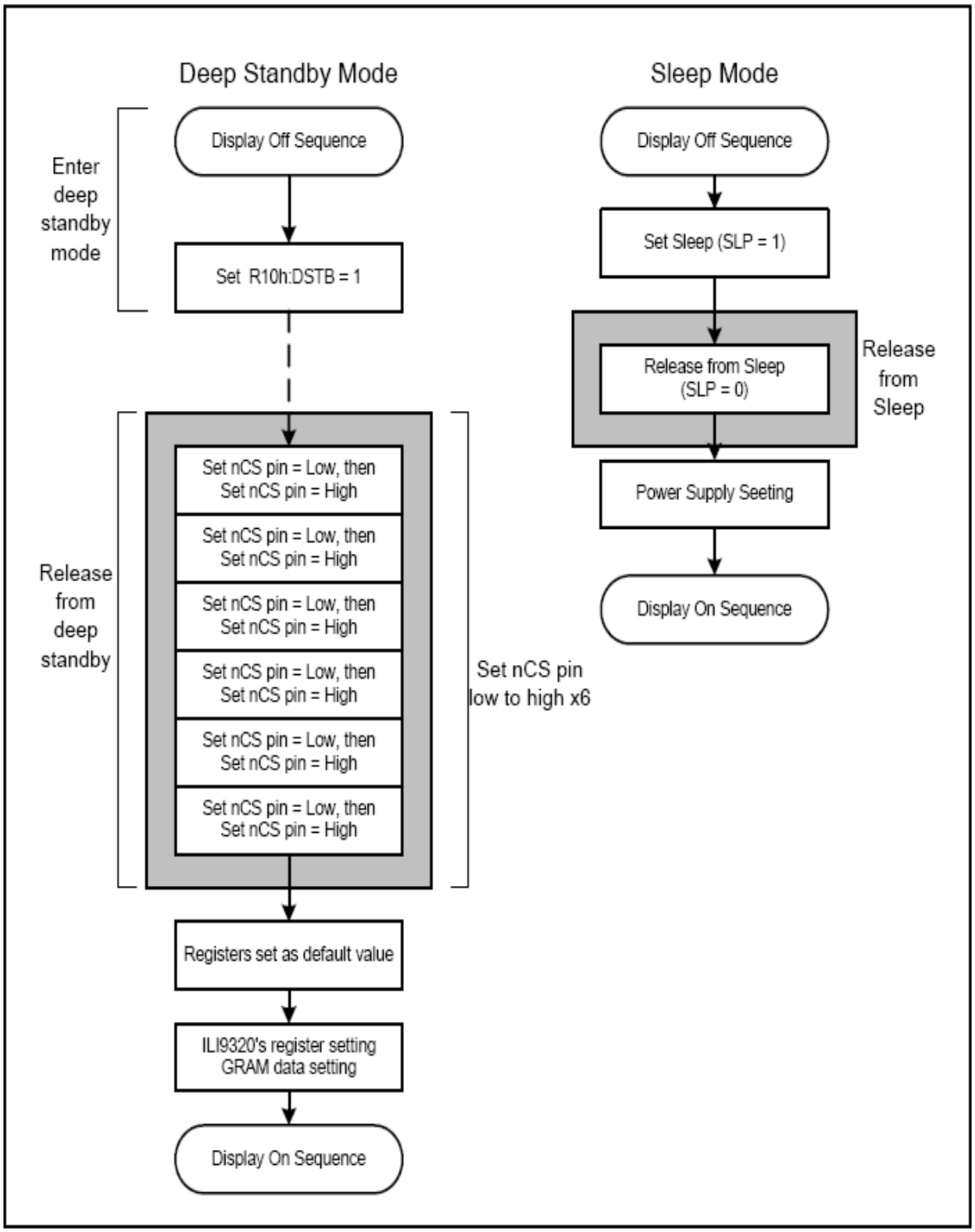
No.	Registers	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38h	Gamma Control 7	**W**	**1**	**0**	**0**	**0**	**0**	**0**	**KN3[2]**	**KN3[1]**	**KN3[0]**	**0**	**0**	**0**	**0**	**0**	**KN2[2]**	**KN2[1]**	**KN2[0]**
39h	Gamma Control 8	**W**	**1**	**0**	**0**	**0**	**0**	**0**	**KN5[2]**	**KN5[1]**	**KN5[0]**	**0**	**0**	**0**	**0**	**0**	**KN4[2]**	**KN4[1]**	**KN4[0]**
3Ch	Gamma Control 9	**W**	**1**	**0**	**0**	**0**	**0**	**0**	**RN1[2]**	**RN1[1]**	**RN1[0]**	**0**	**0**	**0**	**0**	**0**	**RN0[2]**	**RN0[1]**	**RN0[0]**
3Dh	Gamma Control 10	W	1	0	0	0	VRN 1[4]	VRN 1[3]	VRN 1[2]	VRN 1[1]	VRN 1[0]	0	0	0	VRN 0[4]	VRN 0[3]	VRN 0[2]	VRN 0[1]	VRN 0[0]
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN 5	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI00	0	0	0	0	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0
93h	Panel Interface Control 3	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI2	MCPI1	MCPI0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
98h	Panel Interface Control 6	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2	MCPE1	

9 Application

9.1 Display ON / OFF

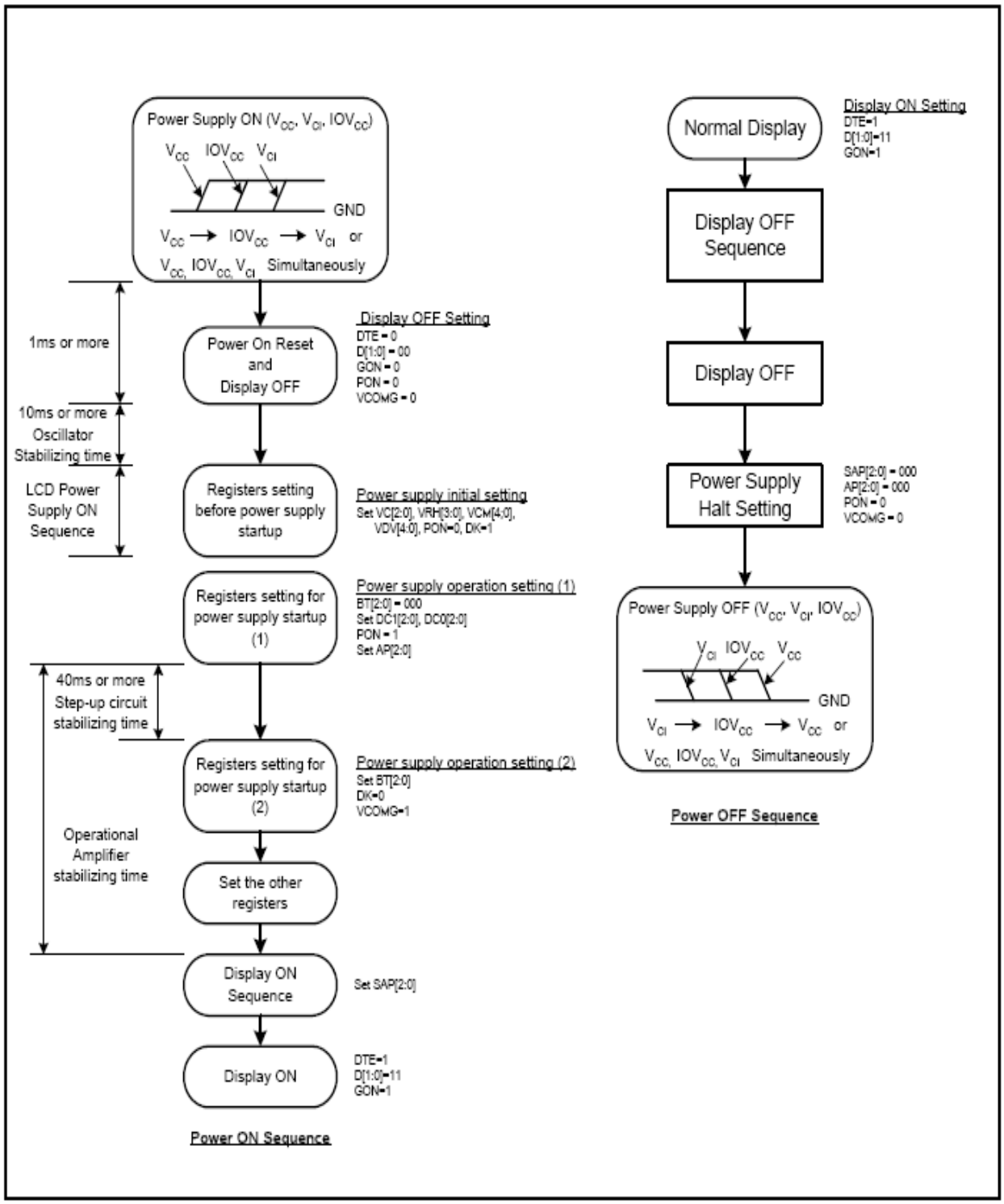


9.2 Deep Standby and Sleep Mode



9.3 Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.



10 Timing Characteristics

10.1 Clock Characteristics

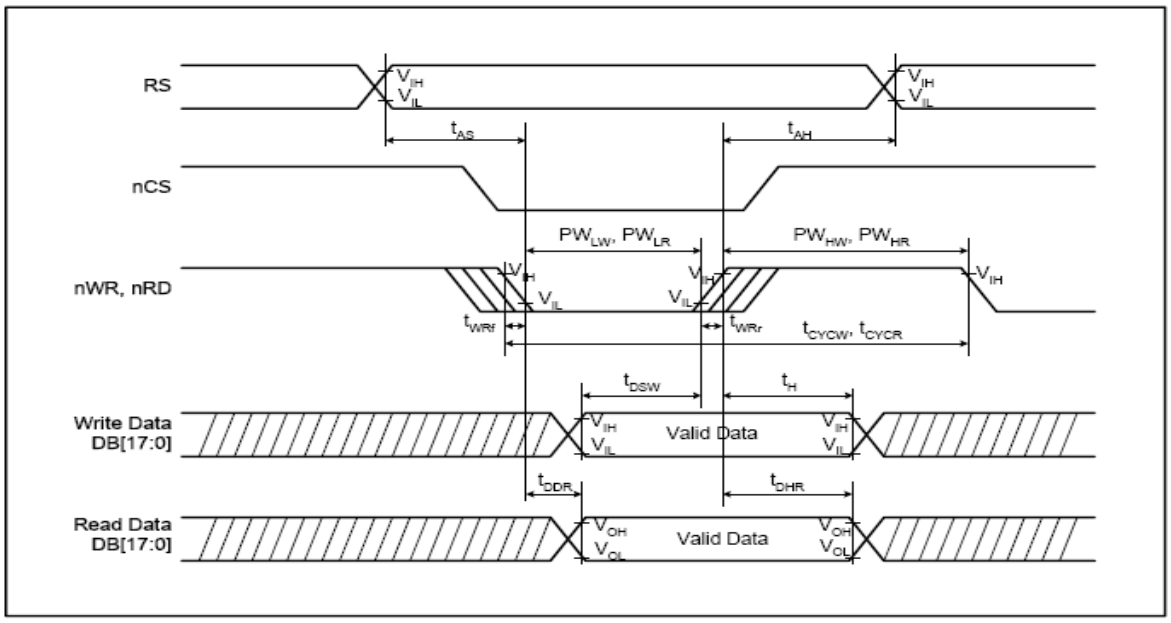
VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
External Clock Frequency	fcp	VCC = 2.4 ~ 3.3V	450	550	650	KHz
External Clock Duty	f_{Duty}	VCC = 2.4 ~ 3.3V	45	50	55	
External Clock Rising Time	Trcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
External Clock Falling Time	Tfcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
RC oscillation clock	f_{osc}	Rf = 100KΩ, VCC = 2.8V	450	550	650	KHz

10.2 AC Characteristics (i80 – system Interface Timing Characteristics)

Normal Write Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	100	-	-	-
	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	50	-	500	-
Write high-level pulse width		PW_{HW}	ns	50	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5	-	-	
Write data set up time		t_{DSW}	ns	10	-	-	
Write data hold time		t_H	ns	15	-	-	
Read data delay time		t_{DDR}	ns	-	-	100	
Read data hold time		t_{DHR}	ns	5	-	-	



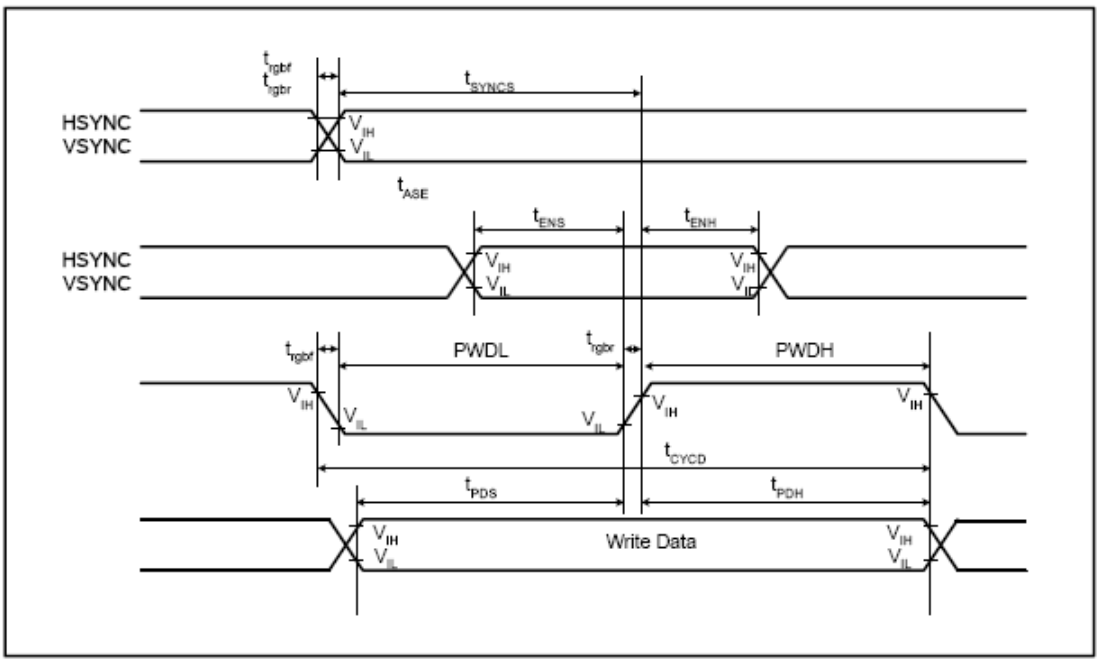
10.3 AC Characteristics (RGB Interface Timing Characteristics)

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-



11 QUALITY AND RELIABILITY

11.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

11.2 SAMPLING PLAN

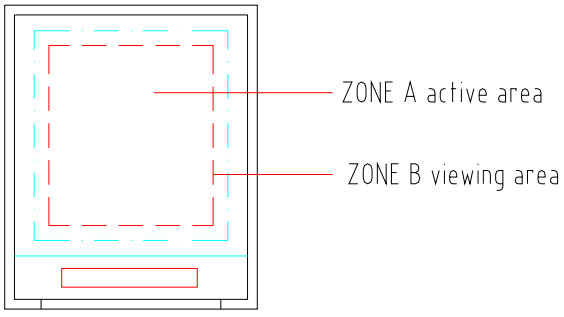
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

11.3 ACCEPTABLE QUALITY LEVEL

A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

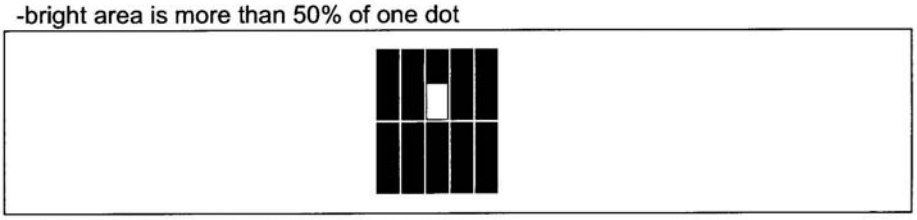
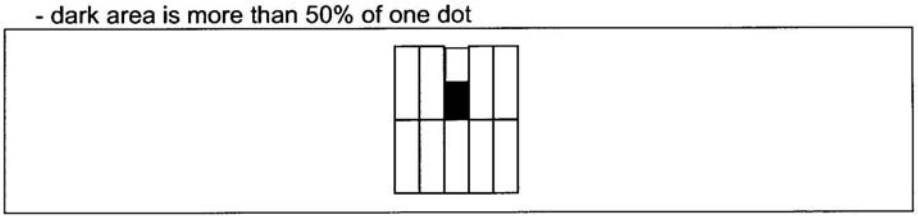
11.4 APPEARANCE

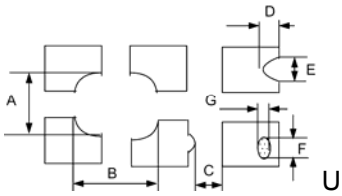
An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under fluorescent light. The inspection area of LCD panel shall be within the range of following limits.

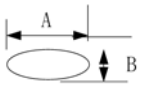


11.5 INSPECTION QUALITY CRITERIA

11.5.1 LCD

<table>
<tr><th>No.</th><th>Item</th><th colspan="2">Criterion for defects</th><th>Defect type</th></tr>
<tr><td>1</td><td>Non display</td><td colspan="2">No non display is allowed</td><td>Major</td></tr>
<tr><td>2</td><td>Irregular operation</td><td colspan="2">No irregular operation is allowed</td><td>Major</td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">Electrical defect</td><td>Bright dot</td><td>Not allowed</td><td>Major</td></tr>
<tr><td>Dark dot</td><td>2</td><td>Minor</td></tr>
<tr><td>Distance between Dark - dark</td><td>≧5mm</td><td>Minor</td></tr>
<tr><td colspan="5">Note 1. Bright,Dark dot defect description
-bright area is more than 50% of one dot
 
- dark area is more than 50% of one dot
  </td></tr>
<tr><td>4</td><td>Mura</td><td colspan="2">ND 8%</td><td>Minor</td></tr>
<tr><td>5</td><td>Black/White spot (I)</td><td colspan="2"><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr><tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr><tr><td>0.30 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>6</td><td>Black/White line (I)</td><td colspan="2"><table><tr><th>Length(mm)</th><th></th><th>Acceptable number</th></tr><tr><td>10 < L</td><td>0.03 < W ≤ 0.04</td><td>5</td></tr><tr><td>5.0 < L ≤10</td><td>0.04 < D ≤ 0.06</td><td>3</td></tr><tr><td>1.0 < L ≤ 5.0</td><td>0.06 < D ≤ 0.07</td><td>2</td></tr><tr><td>L ≤ 1.0</td><td>0.07 < D ≤ 0.09</td><td>1</td></tr></table></td><td>Minor</td></tr>
<tr><td>7</td><td>Black/White sport (II)</td><td colspan="2"><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.30</td><td>Ignore</td></tr><tr><td>0.30 < D ≤ 0.50</td><td>5</td></tr><tr><td>0.50 < D ≤ 1.20</td><td>3</td></tr><tr><td>1.20 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
</table>

<table>
<tr><td>8</td><td>Black/White line (II)</td><td>
<table>
<tr><th>Length (mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr>
<tr><td>20 < L</td><td>0.05 < W ≤ 0.07</td><td>5</td></tr>
<tr><td>10 < L ≤ 20</td><td>0.07 < D ≤ 0.09</td><td>3</td></tr>
<tr><td>5.0 < L ≤ 10</td><td>0.09 < D ≤ 0.10</td><td>2</td></tr>
<tr><td>L ≤ 5.0</td><td>0.10 < D ≤ 0.15</td><td>1</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>9</td><td>Back Light</td><td>1. No Lighting is rejectable
2. Flickering and abnormal lighting are rejectable</td><td>Major</td></tr>
<tr><td>10</td><td>Display pattern</td><td> 

Unit:mm
<table>
<tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr>
</table>
Note: 1. Acceptable up to 3 damages
2. NG if there're to two or more pinholes per dot</td><td>Minor</td></tr>
<tr><td>11</td><td>Blemish & Foreign matters
Size:
$D = \frac{A+B}{2}$</td><td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.15</td><td>Ignore</td></tr>
<tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr>
<tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr>
<tr><td>0.30 < D</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>12</td><td>Scratch on Polarizer
 
</td><td>
<table>
<tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr>
<tr><td>W≤0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.03<W≤0.05</td><td>L ≤ 2.0</td><td>Ignore</td></tr>
<tr><td></td><td>L > 2.0</td><td>1</td></tr>
<tr><td>0.05<W≤0.08</td><td>L > 1.0</td><td>1</td></tr>
<tr><td></td><td>L ≤ 1.0</td><td>Ignore</td></tr>
<tr><td>0.08<W</td><td>Note (1)</td><td>Note(1)</td></tr>
</table>
Note(1) Regard as a blemish</td><td>Minor</td></tr>
<tr><td>13</td><td>Bubble in polarizer</td><td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.20</td><td>Ignore</td></tr>
<tr><td>0.20 < D ≤ 0.50</td><td>3</td></tr>
<tr><td>0.50 < D ≤ 0.80</td><td>2</td></tr>
<tr><td>0.80 < D</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>14</td><td>Stains on LCD panel surface</td><td>Stains that cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable.</td><td>Minor</td></tr>
<tr><td>15</td><td>Rust in Bezel</td><td>Rust which is visible in the bezel is rejectable.</td><td>Minor</td></tr>
</table>

16	Defect of land surface contact (poor soldering)	Evident crevices which is visible are rejectable.	Minor
17	Parts mounting	1. Failure to mount parts 2. Parts not in the specifications are mounted 3. Polarity, for example, is reversed	Major Major Major
18	Parts alignment	1. LSI, IC lead width is more than 50% beyond pad outline. 2. Chip component is off center and more than 50% of the leads is off the pad outline.	Minor Minor
19	Conductive foreign matter (Solder ball, Solder chips)	1. 0.45<φ ,N≧1 2. 0.30<φ≦0.45 ,N≧1 φ:Average diameter of solder ball (unit: mm) 3. 0.50<L ,N≧1 L: Average length of solder chip (unit: mm)	Major Minor Minor
20	Faulty PCB correction	1. Due to PCB copper foil pattern burnout, the pattern is connected, using a jumper wire for repair; 2 or more places are corrected per PCB. 2. Short circuited part is cut, and no resist coating has been performed.	Minor Minor

11.5.2 Touch Panel

Cosmetic Limit Standard (suitable in view area, except dot spacer)

Quality inspection standard :

Inspect sampling standard : according to AQL MIL-STD-105E Level II
Serious defect (serious crack : possible expanding) 0.01
Major defect 0.65
Minor defect 1.5

Scope

The standard shall be applied to **view area only**

For the area outside the view area, shall be acceptable unless any scratch or irregularity which affects electrical performance.

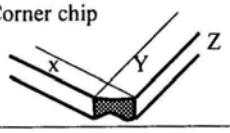
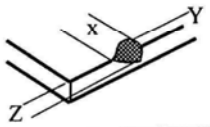
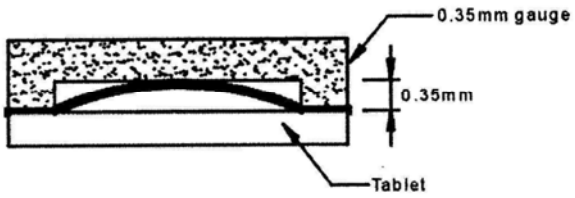
Criterion of visual inspection shall according to limit sample.
However, the chip and crack should be applied to the whole part of touch panel.

Inspection condition :
(A). The lightness of environment is 500 Lux
(B). The distance between product and eye is about 30cm
(C). The angle of 60° between eye
(D). Inspection method is under a ceiling fluorescent light (white color).
(E). Reference document of cosmetic inspection specification :
Item 8-3 ~ 8-9.
(F). W= width, L= length, D= diameter => (longest + shortest)/2
(G). Please find data below for your reference.

Newton Ring

Inspect criteria by limit sample.
(A). The lightness of environment is 500 Lux
(B). The distance between product and eye is about 30cm
(C). The angle of 60° between eye
(D). Please find data below for your reference.

(E).Newton Ring area be under 10% of to total display area.

Item	Specification	Judgment
8-3 **Dot-like foreign objects**	1. D≦0.1mm 2. 0.1mm＜D≦0.3mm 3. 0.3mm＜D	1. Acceptable 2. Three or less 3. Unacceptable
8-4 **Linear foreign objects**	1. W≦0.03mm、L ≦3mm 2. 0.03mm＜W≦0.1mm、L ≦5mm 3. 0.1mm<W、L> 5mm	1. Acceptable 2. Three or less 3. Unacceptable
8-5 **Chip and crack**	(1) Corner chip 	X≦3mm、Y≦3mm、Z＜ t(bottom glass thickness)
	(2) Side chip 	X≦3mm、Y≦3mm、Z＜ t(bottom glass thickness)
	(3) Bad crack(possibly expanding) 	Crack damage is not allowed to be existed in the viewing area or ITO。
8-6 **Scratch**	1. W≦0.03mm、L ≦3mm 2. 0.03mm＜W≦0.1mm、L ≦5mm 3. 0.1mm<W、L> 5mm	1. Acceptable 2. Three or less 3. Unacceptable
8-7 **Fish eyes**	1.D≦0.2mm 2.0.2mm<D≦0.4mm 3.0.4mm<D≦0.6mm 4.0.6mm<D 	1. Acceptable 2. Two or less (distance 5mm over) 3. One (distance 5mm over) 4. Unacceptable
8-8 **Dirt**	Acceptable if not noticeable	
8-9 **Blistering**	 Check through any 0.35mm gauge whether a panel surface film does not contact a measuring face.	

11.6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	60±3°C , t=96 hrs	
Low Temperature Operation	-10±3°C , t=96 hrs	
High Temperature Storage	70±3°C , t=96 hrs	1,2
Low Temperature Storage	-20±3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-20°C ~ 25°C ~ 70°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

12 Use precautions

12-1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

12-2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

12-3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

12-4 Operating precautions

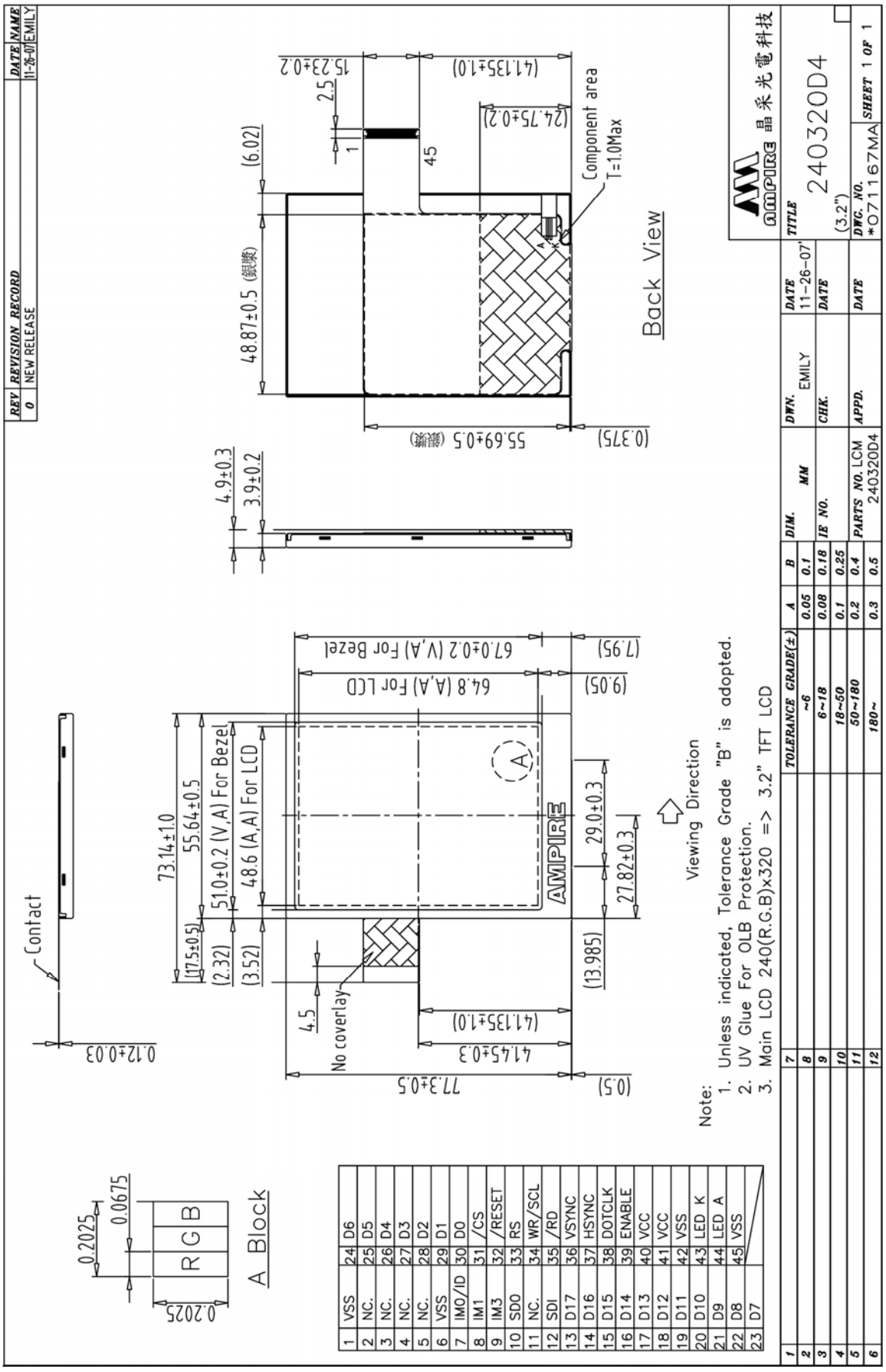
1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

12-5 Other

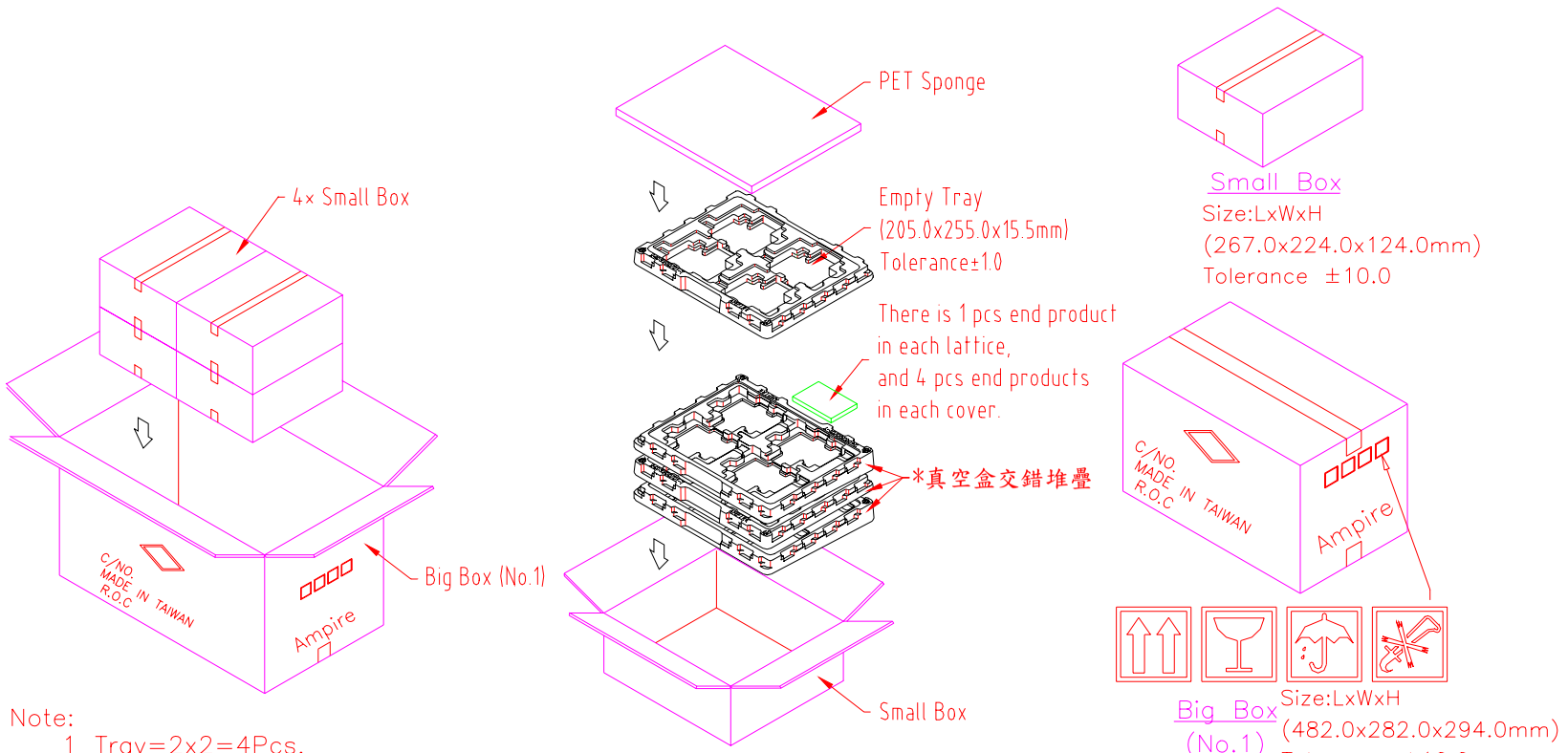
1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

13 Mechanic Drawing



1	VSS	24	D6																				
2	NC.	25	D5																				
3	NC.	26	D4																				
4	NC.	27	D3																				
5	NC.	28	D2																				
6	VSS	29	D1																				
7	IM0/ID	30	D0																				
8	IM1	31	/CS																				
9	IM3	32	/RESET																				
10	SDO	33	RS																				
11	NC.	34	WR/SCL																				
12	SDI	35	/RD																				
13	D17	36	VSYNC																				
14	D16	37	HSYNC																				
15	D15	38	DOTCLK																				
16	D14	39	ENABLE																				
17	D13	40	VCC																				
18	D12	41	VCC																				
19	D11	42	VSS																				
20	D10	43	LED K																				
21	D9	44	LED A																				
22	D8	45	VSS																				
23	D7																						

REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	07-13-06'	EMILY



Note:
1 Tray=2x2=4Pcs.
2 Small Box=9xTray=36Pcs.(10 Tray)
3 Big Box=4xSmall Box=144Pcs.

				TOLERANCE GRADE(±)	A	B	DIM.	DWN.	DATE
1		7					MM	EMILY	07-13-06'
2		8		~6	0.05	0.1			
3		9		6~18	0.08	0.18	IE NO.	CHK.	DATE
4		10		18~50	0.1	0.25			
5		11		50~180	0.2	0.4	PARTS NO. BOX 240320D1	APPD.	DATE
6		12		180~	0.3	0.5			

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TITLE: 240320D1

DWG. NO. *060724SA | SHEET 1 OF 1