Features

- **High Performance, Low Power 32-bit AVR® Microcontroller**
  - **Compact Single-cycle RISC Instruction Set Including DSP Instruction Set**
  - **Built-in Floating-Point Processing Unit (FPU)**
  - **Read-Modify-Write Instructions and Atomic Bit Manipulation**
  - **Performing 1.49 DMIPS / MHz**
    - **Up to 91 DMIPS Running at 66 MHz from Flash (1 Wait-State)**
    - **Up to 49 DMIPS Running at 33 MHz from Flash (0 Wait-State)**
  - **Memory Protection Unit**
- **Multi-hierarchy Bus System**
  - **High-Performance Data Transfers on Separate Buses for Increased Performance**
  - **16 Peripheral DMA Channels Improves Speed for Peripheral Communication**
- **Internal High-Speed Flash**
  - **512 Kbytes, 256 Kbytes, 128 Kbytes, 64 Kbytes Versions**
  - **Single Cycle Access up to 33 MHz**
  - **FlashVault™ Technology Allows Pre-programmed Secure Library Support for End User Applications**
  - **Prefetch Buffer Optimizing Instruction Execution at Maximum Speed**
  - **4ms Page Programming Time and 8ms Full-Chip Erase Time**
  - **100,000 Write Cycles, 15-year Data Retention Capability**
  - **Flash Security Locks and User Defined Configuration Area**
- **Internal High-Speed SRAM, Single-Cycle Access at Full Speed**
  - **64 Kbytes (512 KB and 256 KB Flash), 32 Kbytes (128 KB Flash), 16 Kbytes (64 KB Flash)**
  - **4 Kbytes on the Multi-Layer Bus System (HSB RAM)**
- **External Memory Interface on AT32UC3C0 Derivatives**
  - **SDRAM / SRAM Compatible Memory Bus (16-bit Data and 24-bit Address Buses)**
- **Interrupt Controller**
  - **Autovectored Low Latency Interrupt Service with Programmable Priority**
- **System Functions**
  - **Power and Clock Manager**
  - **Internal 115KHz (RCSYS) and 8MHz/1MHz (RC8M) RC Oscillators**
  - **One 32 KHz and Two Multipurpose Oscillators**
  - **Clock Failure detection**
  - **Two Phase-Lock-Loop (PLL) allowing Independent CPU Frequency from USB or CAN Frequency**
- **Windowed Watchdog Timer (WDT)**
- **Asynchronous Timer (AST) with Real-Time Clock Capability**
  - **Counter or Calendar Mode Supported**
- **Frequency Meter (FREQM) for Accurate Measuring of Clock Frequency**
- **Ethernet MAC 10/100 Mbps interface**
  - **802.3 Ethernet Media Access Controller**
  - **Supports Media Independent Interface (MII) and Reduced MII (RMII)**
- **Universal Serial Bus (USB)**
  - **Device 2.0 and Embedded Host Low Speed and Full Speed**
  - **Flexible End-Point Configuration and Management with Dedicated DMA Channels**
  - **On-chip Transceivers Including Pull-Ups**
- **One 2-channel Controller Area Network (CAN)**
  - **CAN2A and CAN2B protocol compliant, with high-level mailbox system**

32-bit AVR®
Microcontroller

AT32UC3C0512C
AT32UC3C0256C
AT32UC3C0128C
AT32UC3C064C
AT32UC3C1512C
AT32UC3C1256C
AT32UC3C1128C
AT32UC3C164C
AT32UC3C2512C
AT32UC3C2256C
AT32UC3C2128C
AT32UC3C264C

- – **Two independent channels, 16 Message Objects per Channel**
- **One 4-Channel 20-bit Pulse Width Modulation Controller (PWM)**
  - – **Complementary outputs, with Dead Time Insertion**
  - – **Output Override and Fault Protection**
- **Two Quadrature Decoders**
- **One 16-channel 12-bit Pipelined Analog-To-Digital Converter (ADC)**
  - – **Dual Sample and Hold Capability Allowing 2 Synchronous Conversions**
  - – **Single-Ended and Differential Channels, Window Function**
- **Two 12-bit Digital-To-Analog Converters (DAC), with Dual Output Sample System**
- **Four Analog Comparators**
- **Six 16-bit Timer/Counter (TC) Channels**
  - – **External Clock Inputs, PWM, Capture and Various Counting Capabilities**
- **One Peripheral Event Controller**
  - – **Trigger Actions in Peripherals Depending on Events Generated from Peripherals or from Input Pins**
  - – **Deterministic Trigger**
  - – **34 Events and 22 Event Actions**
- **Five Universal Synchronous/Asynchronous Receiver/Transmitters (USART)**
  - – **Independent Baudrate Generator, Support for SPI, LIN, IrDA and ISO7816 interfaces**
  - – **Support for Hardware Handshaking, RS485 Interfaces and Modem Line**
- **Two Master/Slave Serial Peripheral Interfaces (SPI) with Chip Select Signals**
- **One Inter-IC Sound (I2S) Controller**
  - – **Compliant with I2S Bus Specification**
  - – **Time Division Multiplexed mode**
- **Three Master and Three Slave Two-Wire Interfaces (TWI), 400 kbit/s I^{2}C-compatible**
- **QTouch® Library Support**
  - – **Capacitive Touch Buttons, Sliders, and Wheels**
  - – **QTouch® and QMatrix® Acquisition**
- **On-Chip Non-intrusive Debug System**
  - – **Nexus Class 2+, Runtime Control, Non-Intrusive Data and Program Trace**
  - – **aWire™ single-pin programming trace and debug interface muxed with reset pin**
  - – **NanoTrace™ provides trace capabilities through JTAG or aWire interface**
- **3 package options**
  - – **64-pin QFN/TQFP (45 GPIO pins)**
  - – **100-pin TQFP (81 GPIO pins)**
  - – **144-pin LQFP (123 GPIO pins)**
- **Two operating voltage ranges:**
  - – **Single 5V Power Supply**
  - – **Single 3.3V Power Supply**

1. Description

The AT32UC3C is a complete System-On-Chip microcontroller based on the AVR32UC RISC processor running at frequencies up to 66 MHz. AVR32UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high performance.

The processor implements a Memory Protection Unit (MPU) and a fast and flexible interrupt controller for supporting modern operating systems and real-time operating systems. Using the Secure Access Unit (SAU) together with the MPU provides the required security and integrity.

Higher computation capabilities are achievable either using a rich set of DSP instructions or using the floating-point instructions.

The AT32UC3C incorporates on-chip Flash and SRAM memories for secure and fast access. For applications requiring additional memory, an external memory interface is provided on AT32UC3C0 derivatives.

The Memory Direct Memory Access controller (MDMA) enables transfers of block of data from memories to memories without processor involvement.

The Peripheral Direct Memory Access (PDCA) controller enables data transfers between peripherals and memories without processor involvement. The PDCA drastically reduces processing overhead when transferring continuous and large data streams.

The AT32UC3C incorporates on-chip Flash and SRAM memories for secure and fast access. The FlashVault technology allows secure libraries to be programmed into the device. The secure libraries can be executed while the CPU is in Secure State, but not read by non-secure software in the device. The device can thus be shipped to end custumers, who are able to program their own code into the device, accessing the secure libraries, without any risk of compromising the proprietary secure code.

The Power Manager improves design flexibility and security. Power monitoring is supported by on-chip Power-On Reset (POR), Brown-Out Detectors (BOD18, BOD33, BOD50). The CPU runs from the on-chip RC oscillators, the PLLs, or the Multipurpose Oscillators. The Asynchronous Timer (AST) combined with the 32 KHz oscillator keeps track of the time. The AST can operate in counter or calendar mode.

The device includes six identical 16-bit Timer/Counter (TC) channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing, and pulse width modulation.

The PWM module provides four channels with many configuration options including polarity, edge alignment and waveform non overlap control. The PWM channels can operate independently, with duty cycles set independently from each other, or in interlinked mode, with multiple channels updated at the same time. It also includes safety feature with fault inputs and the ability to lock the PWM configuration registers and the PWM pin assignment.

The AT32UC3C also features many communication interfaces for communication intensive applications. In addition to standard serial interfaces like UART, SPI or TWI, other interfaces like flexible CAN, USB and Ethernet MAC are available. The USART supports different communication modes, like SPI mode and LIN mode.

The Inter-IC Sound Controller (I2SC) provides a 5-bit wide, bidirectional, synchronous, digital audio link with off-chip audio devices. The controller is compliant with the I2S bus specification.

The Full-Speed USB 2.0 Device interface supports several USB Classes at the same time thanks to the rich End-Point configuration. The On-The-GO (OTG) Host interface allows device like a USB Flash disk or a USB printer to be directly connected to the processor.

The media-independent interface (MII) and reduced MII (RMII) 10/100 Ethernet MAC module provides on-chip solutions for network-connected devices.

The Peripheral Event Controller (PEVC) allows to redirect events from one peripheral or from input pins to another peripheral. It can then trigger, in a deterministic time, an action inside a peripheral without the need of CPU. For instance a PWM waveform can directly trigger an ADC capture, hence avoiding delays due to software interrupt processing.

The AT32UC3C features analog functions like ADC, DAC, Analog comparators. The ADC interface is built around a 12-bit pipelined ADC core and is able to control two independent 8-channel or one 16-channel. The ADC block is able to measure two different voltages sampled at the same time. The analog comparators can be paired to detect when the sensing voltage is within or outside the defined reference window.

Atmel offers the QTouch library for embedding capacitive touch buttons, sliders, and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and included fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop, and debug your own touch applications.

AT32UC3C integrates a class 2+ Nexus 2.0 On-Chip Debug (OCD) System, with non-intrusive real-time trace, full-speed read/write memory access in addition to basic runtime control. The Nanotrace interface enables trace feature for aWire- or JTAG-based debuggers. The single-pin aWire interface allows all features available through the JTAG interface to be accessed through the RESET pin, allowing the JTAG pins to be used for GPIO or peripherals.

2. Overview

2.1 Block diagram

Figure 2-1. Block diagram
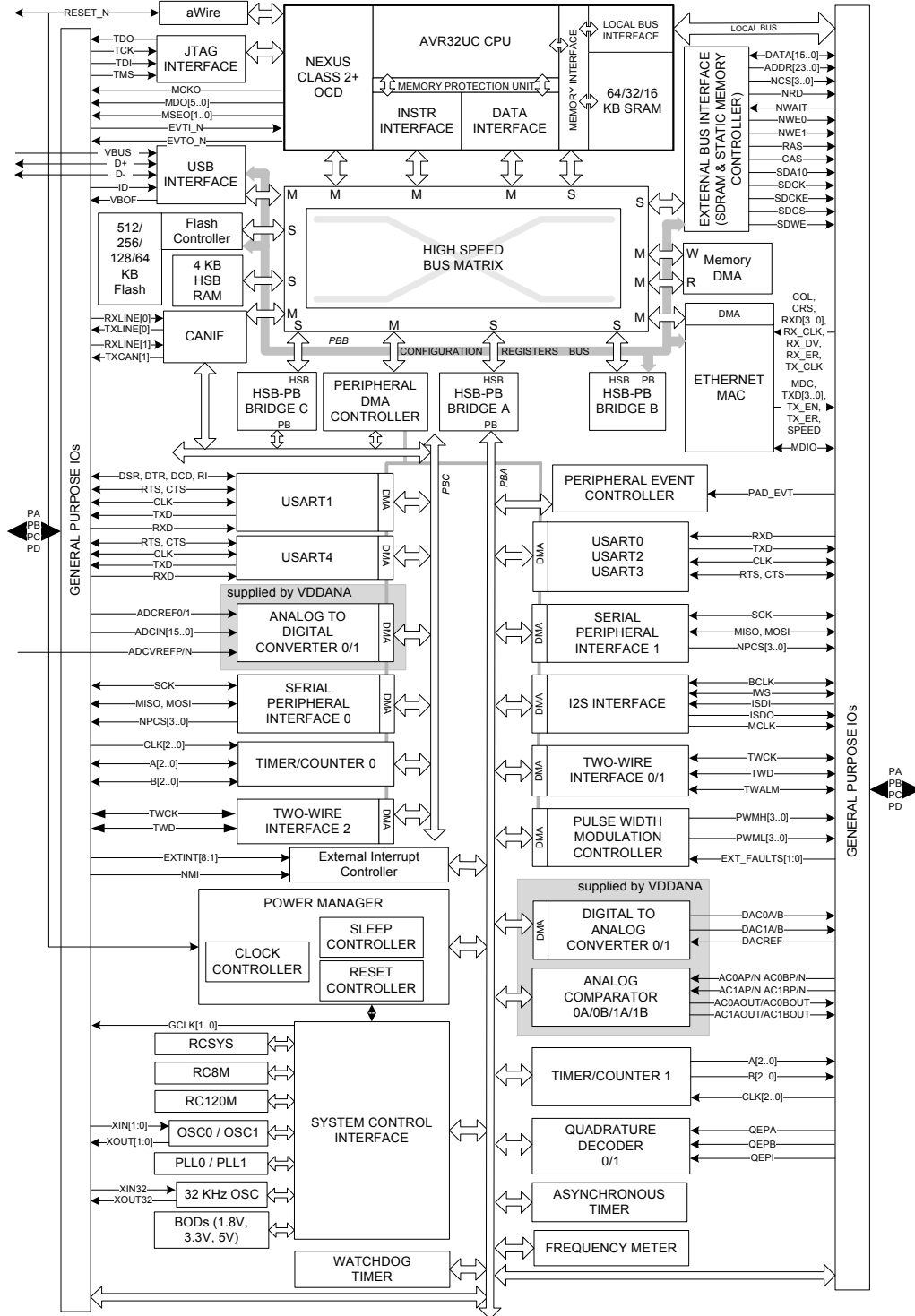
2.2 Configuration Summary

Table 2-1. Configuration Summary

Feature	AT32UC3C0512C/ AT32UC3C0256C/ AT32UC3C0128C/ AT32UC3C064C	AT32UC3C1512C/ AT32UC3C1256C/ AT32UC3C1128C/ AT32UC3C164C	AT32UC3C2512C/ AT32UC3C2256C/ AT32UC3C2128C/ AT32UC3C264C
Flash	512/256/128/64 KB	512/256/128/64 KB	512/256/128/64 KB
SRAM	64/64/32/16 KB	64/64/32/16 KB	64/64/32/16 KB
HSB RAM	4 KB		
EBI	1	0	0
GPIO	123	81	45
External Interrupts	8	8	8
TWI	3	3	2
USART	5	5	4
Peripheral DMA Channels	16	16	16
Peripheral Event System	1	1	1
SPI	2	2	1
CAN channels	2	2	2
USB	1	1	1
Ethernet MAC 10/100	1	1	1
I2S	1	1	1
Asynchronous Timers	1	1	1
Timer/Counter Channels	6	6	3
PWM channels	4x2		
QDEC	2	2	1
Frequency Meter	1		
Watchdog Timer	1		
Power Manager	1		
Oscillators	PLL 80-240 MHz (PLL0/PLL1) Crystal Oscillator 0.4-20 MHz (OSC0) Crystal Oscillator 32 KHz (OSC32K) RC Oscillator 115 kHz (RCSYS) RC Oscillator 8 MHz (RC8M) RC Oscillator 120 MHz (RC120M)		
	0.4-20 MHz (OSC1)		-
12-bit ADC number of channels	1 16	1 16	1 11
12-bit DAC number of channels	1 4	1 4	1 2

**Table 2-1.** Configuration Summary

Feature	AT32UC3C0512C/ AT32UC3C0256C/ AT32UC3C0128C/ AT32UC3C064C	AT32UC3C1512C/ AT32UC3C1256C/ AT32UC3C1128C/ AT32UC3C164C	AT32UC3C2512C/ AT32UC3C2256C/ AT32UC3C2128C/ AT32UC3C264C
Analog Comparators	4	4	2
JTAG	1		
aWire	1		
Max Frequency	66 MHz		
Package	LQFP144	TQFP100	TQFP64/QFN64

3. Package and Pinout

3.1 Package

The device pins are multiplexed with peripheral functions as described in Table 3-1 on page 10.

Figure 3-1. QFN64/TQFP64 Pinout
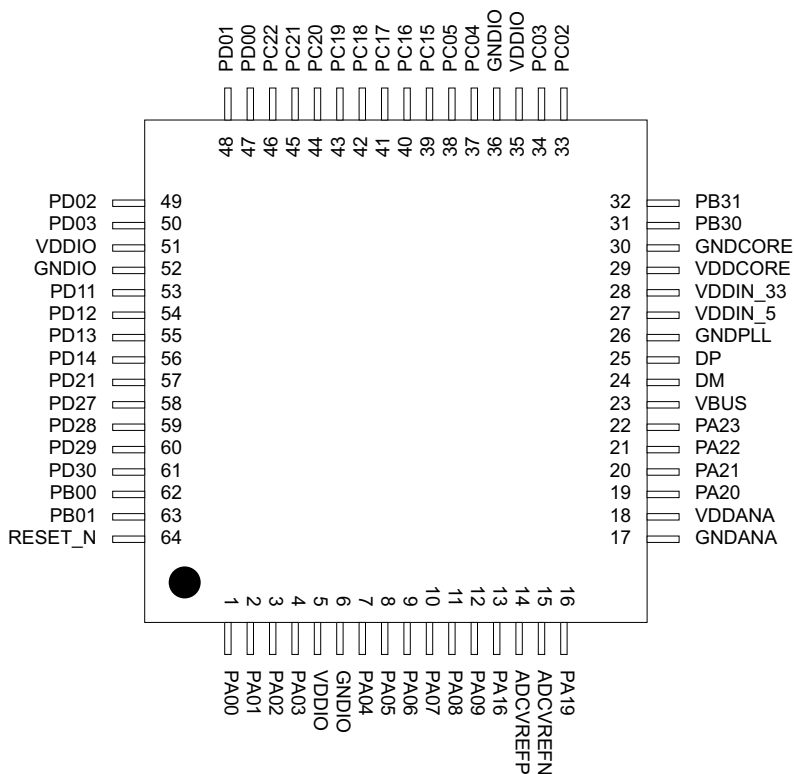
Note: on QFN packages, the exposed pad is unconnected.
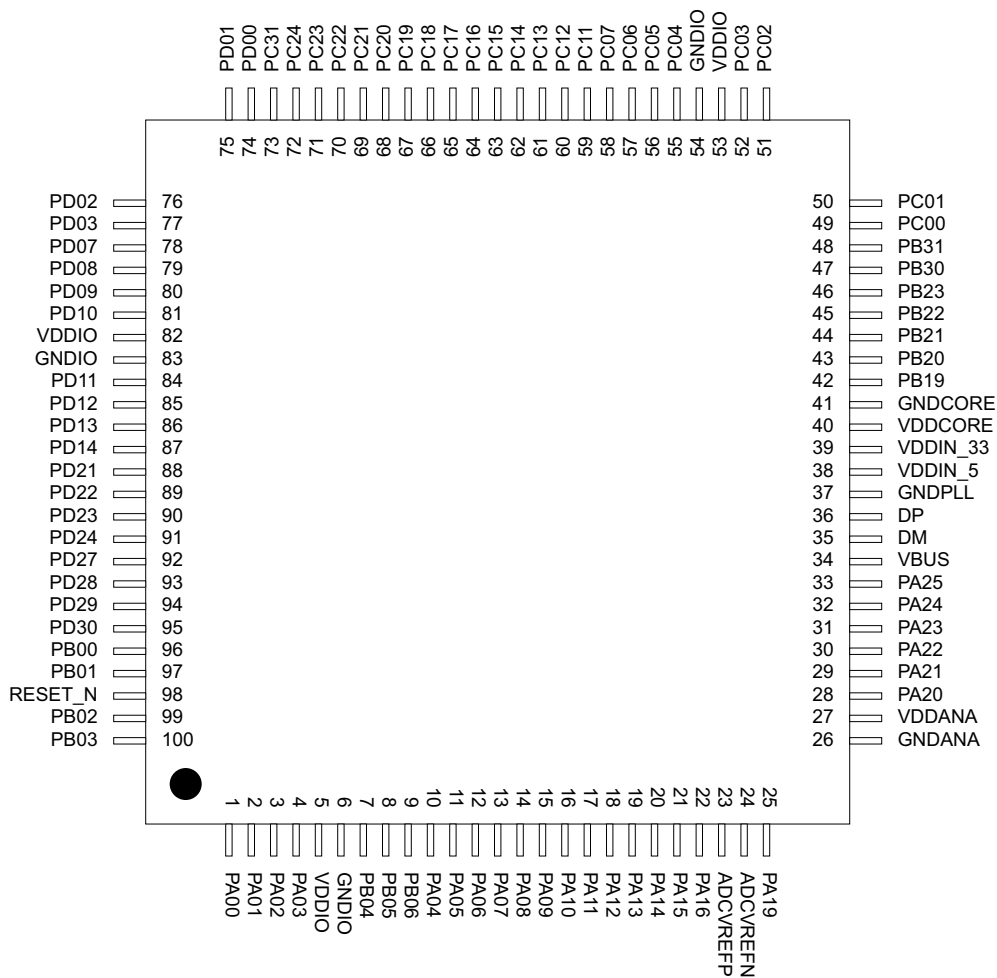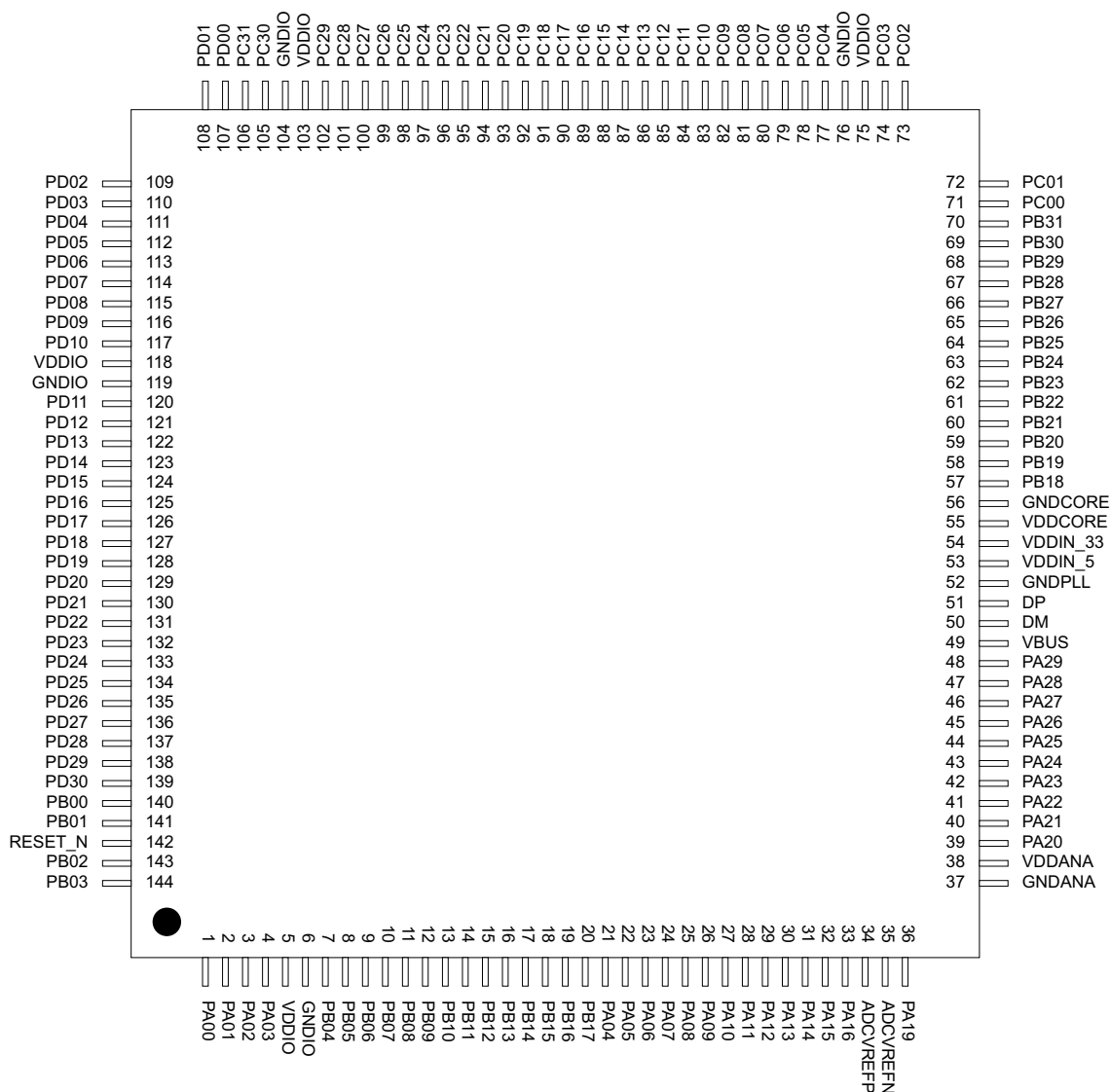
Figure 3-2. TQFP100 Pinout

Figure 3-3. LQFP144 Pinout

3.2 Peripheral Multiplexing on I/O lines

3.2.1 Multiplexed signals

Each GPIO line can be assigned to one of the peripheral functions.The following table describes the peripheral signals multiplexed to the GPIO lines.

Table 3-1. GPIO Controller Function Multiplexing

TQFP/ QFN64	TQFP 100	LQFP 144	Pad Type[1]	PIN	GPIO	GPIO function					
						A	B	C	D	E	F
1	1	1	x1/x2	PA00	0		CANIF - TXLINE[1]				

Table 3-1. GPIO Controller Function Multiplexing

2	2	2	x1/x2	PA01	1		CANIF - RXLINE[1]	PEVC - PAD_EVT[0]			
3	3	3	x1/x2	PA02	2	SCIF - GCLK[0]		PEVC - PAD_EVT[1]			
4	4	4	x1/x2	PA03	3	SCIF - GCLK[1]	EIC - EXTINT[1]				
7	10	21	x1/x2	PA04	4	ADCIN0	USBC - ID	ACIFA0 - ACAOUT			
8	11	22	x1/x2	PA05	5	ADCIN1	USBC - VBOF	ACIFA0 - ACBOUT			
9	12	23	x1/x2	PA06	6	ADCIN2	AC1AP1	PEVC - PAD_EVT[2]			
10	13	24	x1/x2	PA07	7	ADCIN3	AC1AN1	PEVC - PAD_EVT[3]			
11	14	25	x1/x2	PA08	8	ADCIN4	AC1BP1	EIC - EXTINT[2]			
12	15	26	x1/x2	PA09	9	ADCIN5	AC1BN1				
	16	27	x1/x2	PA10	10	ADCIN6	EIC - EXTINT[4]	PEVC - PAD_EVT[13]			
	17	28	x1/x2	PA11	11	ADCIN7	ADCREF1	PEVC - PAD_EVT[14]			
	18	29	x1/x2	PA12	12	AC1AP0	SPI0 - NPCS[0]	DAC1A			
	19	30	x1/x2	PA13	13	AC1AN0	SPI0 - NPCS[1]	ADCIN15			
	20	31	x1/x2	PA14	14	AC1BP0	SPI1 - NPCS[0]				
	21	32	x1/x2	PA15	15	AC1BN0	SPI1 - NPCS[1]	DAC1B			
13	22	33	x1/x2	PA16	16	ADCREF0		DACREF			
14	23	34		ADC REFP							
15	24	35		ADC REFN							
16	25	36	x1/x2	PA19	19	ADCIN8	EIC - EXTINT[1]				
19	28	39	x1/x2	PA20	20	ADCIN9	AC0AP0	DAC0A			
20	29	40	x1/x2	PA21	21	ADCIN10	AC0BN0	DAC0B			
21	30	41	x1/x2	PA22	22	ADCIN11	AC0AN0	PEVC - PAD_EVT[4]		MACB - SPEED	

Table 3-1. GPIO Controller Function Multiplexing

22	31	42	x1/x2	PA23	23	ADCIN12	AC0BP0	PEVC - PAD_EVT[5]		MACB - WOL
	32	43	x1/x2	PA24	24	ADCIN13	SPI1 - NPCS[2]			
	33	44	x1/x2	PA25	25	ADCIN14	SPI1 - NPCS[3]	EIC - EXTINT[0]		
		45	x1/x2	PA26	26	AC0AP1	EIC - EXTINT[1]			
		46	x1/x2	PA27	27	AC0AN1	EIC - EXTINT[2]			
		47	x1/x2	PA28	28	AC0BP1	EIC - EXTINT[3]			
		48	x1/x2	PA29	29	AC0BN1	EIC - EXTINT[0]			
62	96	140	x1	PB00	32	USART0 - CLK	CANIF - RXLINE[1]	EIC - EXTINT[8]	PEVC - PAD_EVT[10]	
63	97	141	x1	PB01	33		CANIF - TXLINE[1]		PEVC - PAD_EVT[11]	
	99	143	x1	PB02	34		USBC - ID	PEVC - PAD_EVT[6]	TC1 - A1	
	100	144	x1	PB03	35		USBC - VBOF	PEVC - PAD_EVT[7]		
	7	7	x1/x2	PB04	36	SPI1 - MOSI	CANIF - RXLINE[0]	QDEC1 - QEPI		MACB - TXD[2]
	8	8	x1/x2	PB05	37	SPI1 - MISO	CANIF - TXLINE[0]	PEVC - PAD_EVT[12]	USART3 - CLK	MACB - TXD[3]
	9	9	x2/x4	PB06	38	SPI1 - SCK		QDEC1 - QEPA	USART1 - CLK	MACB - TX_ER
		10	x1/x2	PB07	39	SPI1 - NPCS[0]	EIC - EXTINT[2]	QDEC1 - QEPB		MACB - RX_DV
		11	x1/x2	PB08	40	SPI1 - NPCS[1]	PEVC - PAD_EVT[11]	PWM - PWML[0]	EIC - SCAN[0]	MACB - RXD[0]
		12	x1/x2	PB09	41	SPI1 - NPCS[2]		PWM - PWMH[0]	EIC - SCAN[1]	MACB - RXD[1]
		13	x1/x2	PB10	42	USART1 - DTR	SPI0 - MOSI	PWM - PWML[1]	EIC - SCAN[2]	
		14	x1/x2	PB11	43	USART1 - DSR	SPI0 - MISO	PWM - PWMH[1]	EIC - SCAN[3]	
		15	x1/x2	PB12	44	USART1 - DCD	SPI0 - SCK	PWM - PWML[2]	EIC - SCAN[4]	
		16	x1/x2	PB13	45	USART1 - RI	SPI0 - NPCS[0]	PWM - PWMH[2]	EIC - SCAN[5]	MACB - RX_ER

Table 3-1. GPIO Controller Function Multiplexing

		17	x1/x2	PB14	46	USART1 - RTS	SPI0 - NPCS[1]	PWM - PWML[3]	EIC - SCAN[6]	MACB - MDC	
		18	x1/x2	PB15	47	USART1 - CTS	USART1 - CLK	PWM - PWMH[3]	EIC - SCAN[7]	MACB - MDIO	
		19	x1/x2	PB16	48	USART1 - RXD	SPI0 - NPCS[2]	PWM - EXT_FAULTS[0]		CANIF - RXLINE[0]	
		20	x1/x2	PB17	49	USART1 - TXD	SPI0 - NPCS[3]	PWM - EXT_FAULTS[1]		CANIF - TXLINE[0]	
		57	x1/x2	PB18	50	TC0 - CLK2		EIC - EXTINT[4]			
	42	58	x1/x2	PB19	51	TC0 - A0	SPI1 - MOSI	IISC - ISDO		MACB - CRS	
	43	59	x1/x2	PB20	52	TC0 - B0	SPI1 - MISO	IISC - ISDI	ACIFA1 - ACAOUT	MACB - COL	
	44	60	x2/x4	PB21	53	TC0 - CLK1	SPI1 - SCK	IISC - IMCK	ACIFA1 - ACBOUT	MACB - RXD[2]	
	45	61	x1/x2	PB22	54	TC0 - A1	SPI1 - NPCS[3]	IISC - ISCK	SCIF - GCLK[0]	MACB - RXD[3]	
	46	62	x1/x2	PB23	55	TC0 - B1	SPI1 - NPCS[2]	IISC - IWS	SCIF - GCLK[1]	MACB - RX_CLK	
		63	x1/x2	PB24	56	TC0 - CLK0	SPI1 - NPCS[1]				
		64	x1/x2	PB25	57	TC0 - A2	SPI1 - NPCS[0]	PEVC - PAD_EVT[8]			
		65	x2/x4	PB26	58	TC0 - B2	SPI1 - SCK	PEVC - PAD_EVT[9]		MACB - TX_EN	
		66	x1/x2	PB27	59	QDEC0 - QEPA	SPI1 - MISO	PEVC - PAD_EVT[10]	TC1 - CLK0	MACB - TXD[0]	
		67	x1/x2	PB28	60	QDEC0 - QEPB	SPI1 - MOSI	PEVC - PAD_EVT[11]	TC1 - B0	MACB - TXD[1]	
		68	x1/x2	PB29	61	QDEC0 - QEPI	SPI0 - NPCS[0]	PEVC - PAD_EVT[12]	TC1 - A0		
31	47	69	x1	PB30	62						
32	48	70	x1	PB31	63						
	49	71	x1/x2	PC00	64	USBC - ID	SPI0 - NPCS[1]	USART2 - CTS	TC1 - B2	CANIF - TXLINE[1]	
	50	72	x1/x2	PC01	65	USBC - VBOF	SPI0 - NPCS[2]	USART2 - RTS	TC1 - A2	CANIF - RXLINE[1]	
33	51	73	x1	PC02	66	TWIMS0 - TWD	SPI0 - NPCS[3]	USART2 - RXD	TC1 - CLK1	MACB - MDC	
34	52	74	x1	PC03	67	TWIMS0 - TWCK	EIC - EXTINT[1]	USART2 - TXD	TC1 - B1	MACB - MDIO	

Table 3-1. GPIO Controller Function Multiplexing

37	55	77	x1	PC04	68	TWIMS1 - TWD	EIC - EXTINT[3]	USART2 - TXD	TC0 - B1		
38	56	78	x1	PC05	69	TWIMS1 - TWCK	EIC - EXTINT[4]	USART2 - RXD	TC0 - A2		
	57	79	x1	PC06	70	PEVC - PAD_EVT[15]	USART2 - CLK	USART2 - CTS	TC0 - CLK2	TWIMS2 - TWD	TWIMS0 - TWALM
	58	80	x1	PC07	71	PEVC - PAD_EVT[2]	EBI - NCS[3]	USART2 - RTS	TC0 - B2	TWIMS2 - TWCK	TWIMS1 - TWALM
		81	x1/x2	PC08	72	PEVC - PAD_EVT[13]	SPI1 - NPCS[1]	EBI - NCS[0]		USART4 - TXD	
		82	x1/x2	PC09	73	PEVC - PAD_EVT[14]	SPI1 - NPCS[2]	EBI - ADDR[23]		USART4 - RXD	
		83	x1/x2	PC10	74	PEVC - PAD_EVT[15]	SPI1 - NPCS[3]	EBI - ADDR[22]			
	59	84	x1/x2	PC11	75	PWM - PWMH[3]	CANIF - RXLINE[1]	EBI - ADDR[21]	TC0 - CLK0		
	60	85	x1/x2	PC12	76	PWM - PWML[3]	CANIF - TXLINE[1]	EBI - ADDR[20]	USART2 - CLK		
	61	86	x1/x2	PC13	77	PWM - PWMH[2]	EIC - EXTINT[7]	EBI - SDCS	USART0 - RTS		
	62	87	x1/x2	PC14	78	PWM - PWML[2]	USART0 - CLK	EBI - SDCKE	USART0 - CTS		
39	63	88	x1/x2	PC15	79	PWM - PWMH[1]	SPI0 - NPCS[0]	EBI - SDWE	USART0 - RXD	CANIF - RXLINE[1]	
40	64	89	x1/x2	PC16	80	PWM - PWML[1]	SPI0 - NPCS[1]	EBI - CAS	USART0 - TXD	CANIF - TXLINE[1]	
41	65	90	x1/x2	PC17	81	PWM - PWMH[0]	SPI0 - NPCS[2]	EBI - RAS	IISC - ISDO		USART3 - TXD
42	66	91	x1/x2	PC18	82	PWM - PWML[0]	EIC - EXTINT[5]	EBI - SDA10	IISC - ISDI		USART3 - RXD
43	67	92	x1/x2	PC19	83	PWM - PWML[2]	SCIF - GCLK[0]	EBI - DATA[0]	IISC - IMCK		USART3 - CTS
44	68	93	x1/x2	PC20	84	PWM - PWMH[2]	SCIF - GCLK[1]	EBI - DATA[1]	IISC - ISCK		USART3 - RTS
45	69	94	x1/x2	PC21	85	PWM - EXT_FAULTS[0]	CANIF - RXLINE[0]	EBI - DATA[2]	IISC - IWS		
46	70	95	x1/x2	PC22	86	PWM - EXT_FAULTS[1]	CANIF - TXLINE[0]	EBI - DATA[3]		USART3 - CLK	
	71	96	x1/x2	PC23	87	QDEC1 - QEPB	CANIF - RXLINE[1]	EBI - DATA[4]	PEVC - PAD_EVT[3]		
	72	97	x1/x2	PC24	88	QDEC1 - QEPA	CANIF - TXLINE[1]	EBI - DATA[5]	PEVC - PAD_EVT[4]		

Table 3-1. GPIO Controller Function Multiplexing

		98	x1/x2	PC25	89		TC1 - CLK2	EBI - DATA[6]	SCIF - GCLK[0]	USART4 - TXD	
		99	x1/x2	PC26	90	QDEC1 - QEPI	TC1 - B2	EBI - DATA[7]	SCIF - GCLK[1]	USART4 - RXD	
		100	x1/x2	PC27	91		TC1 - A2	EBI - DATA[8]	EIC - EXTINT[0]	USART4 - CTS	
		101	x1/x2	PC28	92	SPI1 - NPCS[3]	TC1 - CLK1	EBI - DATA[9]		USART4 - RTS	
		102	x1/x2	PC29	93	SPI0 - NPCS[1]	TC1 - B1	EBI - DATA[10]			
		105	x1/x2	PC30	94	SPI0 - NPCS[2]	TC1 - A1	EBI - DATA[11]			
	73	106	x1/x2	PC31	95	SPI0 - NPCS[3]	TC1 - B0	EBI - DATA[12]	PEVC - PAD_EVT[5]	USART4 - CLK	
47	74	107	x1/x2	PD00	96	SPI0 - MOSI	TC1 - CLK0	EBI - DATA[13]	QDEC0 - QEPI	USART0 - TXD	
48	75	108	x1/x2	PD01	97	SPI0 - MISO	TC1 - A0	EBI - DATA[14]	TC0 - CLK1	USART0 - RXD	
49	76	109	x2/x4	PD02	98	SPI0 - SCK	TC0 - CLK2	EBI - DATA[15]	QDEC0 - QEPA		
50	77	110	x1/x2	PD03	99	SPI0 - NPCS[0]	TC0 - B2	EBI - ADDR[0]	QDEC0 - QEPB		
		111	x1/x2	PD04	100	SPI0 - MOSI		EBI - ADDR[1]			
		112	x1/x2	PD05	101	SPI0 - MISO		EBI - ADDR[2]			
		113	x2/x4	PD06	102	SPI0 - SCK		EBI - ADDR[3]			
	78	114	x1/x2	PD07	103	USART1 - DTR	EIC - EXTINT[5]	EBI - ADDR[4]	QDEC0 - QEPI	USART4 - TXD	
	79	115	x1/x2	PD08	104	USART1 - DSR	EIC - EXTINT[6]	EBI - ADDR[5]	TC1 - CLK2	USART4 - RXD	
	80	116	x1/x2	PD09	105	USART1 - DCD	CANIF - RXLINE[0]	EBI - ADDR[6]	QDEC0 - QEPA	USART4 - CTS	
	81	117	x1/x2	PD10	106	USART1 - RI	CANIF - TXLINE[0]	EBI - ADDR[7]	QDEC0 - QEPB	USART4 - RTS	
53	84	120	x1/x2	PD11	107	USART1 - TXD	USBC - ID	EBI - ADDR[8]	PEVC - PAD_EVT[6]	MACB - TXD[0]	
54	85	121	x1/x2	PD12	108	USART1 - RXD	USBC - VBOF	EBI - ADDR[9]	PEVC - PAD_EVT[7]	MACB - TXD[1]	
55	86	122	x2/x4	PD13	109	USART1 - CTS	USART1 - CLK	EBI - SDCK	PEVC - PAD_EVT[8]	MACB - RXD[0]	
56	87	123	x1/x2	PD14	110	USART1 - RTS	EIC - EXTINT[7]	EBI - ADDR[10]	PEVC - PAD_EVT[9]	MACB - RXD[1]	

Table 3-1. GPIO Controller Function Multiplexing

		124	x1/x2	PD15	111	TC0 - A0	USART3 - TXD	EBI - ADDR[11]			
		125	x1/x2	PD16	112	TC0 - B0	USART3 - RXD	EBI - ADDR[12]			
		126	x1/x2	PD17	113	TC0 - A1	USART3 - CTS	EBI - ADDR[13]	USART3 - CLK		
		127	x1/x2	PD18	114	TC0 - B1	USART3 - RTS	EBI - ADDR[14]			
		128	x1/x2	PD19	115	TC0 - A2		EBI - ADDR[15]			
		129	x1/x2	PD20	116	TC0 - B2		EBI - ADDR[16]			
57	88	130	x1/x2	PD21	117	USART3 - TXD	EIC - EXTINT[0]	EBI - ADDR[17]	QDEC1 - QEPI		
	89	131	x1/x2	PD22	118	USART3 - RXD	TC0 - A2	EBI - ADDR[18]	SCIF - GCLK[0]		
	90	132	x1/x2	PD23	119	USART3 - CTS	USART3 - CLK	EBI - ADDR[19]	QDEC1 - QEPA		
	91	133	x1/x2	PD24	120	USART3 - RTS	EIC - EXTINT[8]	EBI - NWE1	QDEC1 - QEPB		
		134	x1/x2	PD25	121	TC0 - CLK0	USBC - ID	EBI - NWE0		USART4 - CLK	
		135	x1/x2	PD26	122	TC0 - CLK1	USBC - VBOF	EBI - NRD			
58	92	136	x1/x2	PD27	123	USART0 - TXD	CANIF - RXLINE[0]	EBI - NCS[1]	TC0 - A0	MACB - RX_ER	
59	93	137	x1/x2	PD28	124	USART0 - RXD	CANIF - TXLINE[0]	EBI - NCS[2]	TC0 - B0	MACB - RX_DV	
60	94	138	x1/x2	PD29	125	USART0 - CTS	EIC - EXTINT[6]	USART0 - CLK	TC0 - CLK0	MACB - TX_CLK	
61	95	139	x1/x2	PD30	126	USART0 - RTS	EIC - EXTINT[3]	EBI - NWAIT	TC0 - A1	MACB - TX_EN	

Note: 1. Refer to "Electrical Characteristics" on page 50 for a description of the electrical properties of the pad types used.

See Section 3.3 for a description of the various peripheral signals.

Signals are prioritized according to the function priority listed in Table 3-2 on page 17 if multiple functions are enabled simultaneously.

3.2.2 Peripheral Functions

Each GPIO line can be assigned to one of several peripheral functions. The following table describes how the various peripheral functions are selected. The last listed function has priority in case multiple functions are enabled.

Table 3-2. Peripheral Functions

Function	Description
A	GPIO peripheral selection A
B	GPIO peripheral selection B
C	GPIO peripheral selection C
D	GPIO peripheral selection D
E	GPIO peripheral selection E
F	GPIO peripheral selection F

3.2.3 Oscillator Pinout

The oscillators are not mapped to the normal GPIO functions and their muxings are controlled by registers in the System Control Interface (SCIF). Please refer to the SCIF chapter for more information about this.

Table 3-3. Oscillator pinout

QFN64/ TQFP64 pin	TQFP100 pin	LQFP144 pin	Pad	Oscillator pin
31	47	69	PB30	xin0
	99	143	PB02	xin1
62	96	140	PB00	xin32
32	48	70	PB31	xout0
	100	144	PB03	xout1
63	97	141	PB01	xout32

3.2.4 JTAG port connections

If the JTAG is enabled, the JTAG will take control over a number of pins, irrespectively of the I/O Controller configuration.

Table 3-4. JTAG pinout

QFN64/ TQFP64 pin	TQFP100 pin	LQFP144 pin	Pin name	JTAG pin
2	2	2	PA01	TDI
3	3	3	PA02	TDO
4	4	4	PA03	TMS
1	1	1	PA00	TCK

3.2.5 Nexus OCD AUX port connections

If the OCD trace system is enabled, the trace system will take control over a number of pins, irrespectively of the GPIO configuration. Two different OCD trace pin mappings are possible,

depending on the configuration of the OCD AXS register. For details, see the AVR32UC Technical Reference Manual.

Table 3-5. Nexus OCD AUX port connections

Pin	AXS=0	AXS=1	AXS=2
EVTI_N	PA08	PB19	PA10
MDO[5]	PC05	PC31	PB06
MDO[4]	PC04	PC12	PB15
MDO[3]	PA23	PC11	PB14
MDO[2]	PA22	PB23	PA27
MDO[1]	PA19	PB22	PA26
MDO[0]	PA09	PB20	PA19
EVTO_N	PD29	PD29	PD29
MCKO	PD13	PB21	PB26
MSEO[1]	PD30	PD08	PB25
MSEO[0]	PD14	PD07	PB18

3.2.6 Other Functions

The functions listed in Table 3-6 are not mapped to the normal GPIO functions. The aWire DATA pin will only be active after the aWire is enabled. The aWire DATAOUT pin will only be active after the aWire is enabled and the 2_PIN_MODE command has been sent.

Table 3-6. Other Functions

QFN64/ TQFP64 pin	TQFP100 pin	LQFP144 pin	Pad	Oscillator pin
64	98	142	RESET_N	aWire DATA
3	3	3	PA02	aWire DATAOUT

3.3 Signals Description

The following table give details on the signal name classified by peripherals.

Table 3-7. Signal Description List

Signal Name	Function	Type	Active Level	Comments
		Power		
VDDIO	I/O Power Supply	Power Input		4.5V to 5.5V or 3.0V to 3.6 V
VDDANA	Analog Power Supply	Power Input		4.5V to 5.5V or 3.0V to 3.6 V

Table 3-7. Signal Description List

Signal Name	Function	Type	Active Level	Comments
VDDIN_5	1.8V Voltage Regulator Input	Power Input		Power Supply: 4.5V to 5.5V or 3.0V to 3.6 V
VDDIN_33	USB I/O power supply	Power Output/ Input		Capacitor Connection for the 3.3V voltage regulator or power supply: 3.0V to 3.6 V
VDDCORE	1.8V Voltage Regulator Output	Power output		Capacitor Connection for the 1.8V voltage regulator
GNDIO	I/O Ground	Ground		
GNDANA	Analog Ground	Ground		
GNDCORE	Ground of the core	Ground		
GNDPLL	Ground of the PLLs	Ground		
Analog Comparator Interface - ACIFA0/1				
AC0AN1/AC0AN0	Negative inputs for comparator AC0A	Analog		
AC0AP1/AC0AP0	Positive inputs for comparator AC0A	Analog		
AC0BN1/AC0BN0	Negative inputs for comparator AC0B	Analog		
AC0BP1/AC0BP0	Positive inputs for comparator AC0B	Analog		
AC1AN1/AC1AN0	Negative inputs for comparator AC1A	Analog		
AC1AP1/AC1AP0	Positive inputs for comparator AC1A	Analog		
AC1BN1/AC1BN0	Negative inputs for comparator AC1B	Analog		
AC1BP1/AC1BP0	Positive inputs for comparator AC1B	Analog		
ACAOUT/ACBOUT	analog comparator outputs	output		
ADC Interface - ADCIFA				
ADCIN[15:0]	ADC input pins	Analog		
ADCREF0	Analog positive reference 0 voltage input	Analog		
ADCREF1	Analog positive reference 1 voltage input	Analog		
ADCVREFP	Analog positive reference connected to external capacitor	Analog		
ADCVREFN	Analog negative reference connected to external capacitor	Analog		

Table 3-7. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Auxiliary Port - AUX				
MCKO	Trace Data Output Clock	Output		
MDO[5:0]	Trace Data Output	Output		
MSEO[1:0]	Trace Frame Control	Output		
EVTI_N	Event In	Output	Low	
EVTO_N	Event Out	Output	Low	
aWire - AW				
DATA	aWire data	I/O		
DATAOUT	aWire data output for 2-pin mode	I/O		
Controller Area Network Interface - CANIF				
RXLINE[1:0]	CAN channel rxline	I/O		
TXLINE[1:0]	CAN channel txline	I/O		
DAC Interface - DACIFB0/1				
DAC0A, DAC0B	DAC0 output pins of S/H A	Analog		
DAC1A, DAC1B	DAC output pins of S/H B	Analog		
DACREF	Analog reference voltage input	Analog		
External Bus Interface - EBI				
ADDR[23:0]	Address Bus	Output		
CAS	Column Signal	Output	Low	
DATA[15:0]	Data Bus	I/O		
NCS[3:0]	Chip Select	Output	Low	
NRD	Read Signal	Output	Low	
NWAIT	External Wait Signal	Input	Low	
NWE0	Write Enable 0	Output	Low	
NWE1	Write Enable 1	Output	Low	
RAS	Row Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
SDCK	SDRAM Clock	Output		

Table 3-7. Signal Description List

Signal Name	Function	Type	Active Level	Comments
SDCKE	SDRAM Clock Enable	Output		
SDCS	SDRAM Chip Select	Output	Low	
SDWE	SDRAM Write Enable	Output	Low	
External Interrupt Controller - EIC				
EXTINT[8:1]	External Interrupt Pins	Input		
NMI_N = EXTINT[0]	Non-Maskable Interrupt Pin	Input	Low	
General Purpose Input/Output - GPIOA, GPIOB, GPIOC, GPIOD				
PA[29:19] - PA[16:0]	Parallel I/O Controller GPIOA	I/O		
PB[31:0]	Parallel I/O Controller GPIOB	I/O		
PC[31:0]	Parallel I/O Controller GPIOC	I/O		
PD[30:0]	Parallel I/O Controller GPIOD	I/O		
Inter-IC Sound (I2S) Controller - IISC				
IMCK	I2S Master Clock	Output		
ISCK	I2S Serial Clock	I/O		
ISDI	I2S Serial Data In	Input		
ISDO	I2S Serial Data Out	Output		
IWS	I2S Word Select	I/O		
JTAG				
TCK	Test Clock	Input		
TDI	Test Data In	Input		
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		
Ethernet MAC - MACB				
COL	Collision Detect	Input		
CRS	Carrier Sense and Data Valid	Input		
MDC	Management Data Clock	Output		
MDIO	Management Data Input/Output	I/O		
RXD[3:0]	Receive Data	Input		

Table 3-7. Signal Description List

Signal Name	Function	Type	Active Level	Comments
RX_CLK	Receive Clock	Input		
RX_DV	Receive Data Valid	Input		
RX_ER	Receive Coding Error	Input		
SPEED	Speed	Output		
TXD[3:0]	Transmit Data	Output		
TX_CLK	Transmit Clock or Reference Clock	Input		
TX_EN	Transmit Enable	Output		
TX_ER	Transmit Coding Error	Output		
WOL	Wake-On-LAN	Output		
Peripheral Event Controller - PEVC				
PAD_EVT[15:0]	Event Input Pins	Input		
Power Manager - PM				
RESET_N	Reset Pin	Input	Low	
Pulse Width Modulator - PWM				
PWMH[3:0] PWML[3:0]	PWM Output Pins	Output		
EXT_FAULT[1:0]	PWM Fault Input Pins	Input		
Quadrature Decoder- QDEC0/QDEC1				
QEPA	QEPA quadrature input	Input		
QEPB	QEPB quadrature input	Input		
QEPI	Index input	Input		
System Controller Interface- SCIF				
XIN0, XIN1, XIN32	Crystal 0, 1, 32K Inputs	Analog		
XOUT0, XOUT1, XOUT32	Crystal 0, 1, 32K Output	Analog		
GCLK0 - GCLK1	Generic Clock Pins	Output		
Serial Peripheral Interface - SPI0, SPI1				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		

Table 3-7. Signal Description List

Signal Name	Function	Type	Active Level	Comments
NPCS[3:0]	SPI Peripheral Chip Select	I/O	Low	
SCK	Clock	Output		
Timer/Counter - TC0, TC1				
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		
A2	Channel 2 Line A	I/O		
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWIMS0, TWIMS1, TWIMS2				
TWALM	SMBus SMBALERT	I/O	Low	Only on TWIMS0, TWIMS1
TWCK	Serial Clock	I/O		
TWD	Serial Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3, USART4				
CLK	Clock	I/O		
CTS	Clear To Send	Input	Low	
DCD	Data Carrier Detect	Input	Low	Only USART1
DSR	Data Set Ready	Input	Low	Only USART1
DTR	Data Terminal Ready	Output	Low	Only USART1
RI	Ring Indicator	Input	Low	Only USART1
RTS	Request To Send	Output	Low	
RXD	Receive Data	Input		
TXD	Transmit Data	Output		
Universal Serial Bus Device - USB				
DM	USB Device Port Data -	Analog		

Table 3-7. Signal Description List

Signal Name	Function	Type	Active Level	Comments
DP	USB Device Port Data +	Analog		
VBUS	USB VBUS Monitor and OTG Negociation	Analog Input		
ID	ID Pin of the USB Bus	Input		
VBOF	USB VBUS On/off: bus power control port	output		

3.4 I/O Line Considerations

3.4.1 JTAG pins

The JTAG is enabled if TCK is low while the RESET_N pin is released. The TCK, TMS, and TDI pins have pull-up resistors when JTAG is enabled. The TCK pin always have pull-up enabled during reset. The TDO pin is an output, driven at VDDIO, and has no pull-up resistor. The JTAG pins can be used as GPIO pins and muxed with peripherals when the JTAG is disabled. Please refer to Section 3.2.4 for the JTAG port connections.

3.4.2 RESET_N pin

The RESET_N pin integrates a pull-up resistor to VDDIO. As the product integrates a power-on reset cell, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

The RESET_N pin is also used for the aWire debug protocol. When the pin is used for debugging, it must not be driven by external circuitry.

3.4.3 TWI pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as GPIO pins.

3.4.4 GPIO pins

All I/O lines integrate programmable pull-up and pull-down resistors. Most I/O lines integrate drive strength control, see Table 3-1. Programming of this pull-up and pull-down resistor or this drive strength is performed independently for each I/O line through the GPIO Controllers.

After reset, I/O lines default as inputs with pull-up/pull-down resistors disabled. After reset, output drive strength is configured to the lowest value to reduce global EMI of the device.

When the I/O line is configured as analog function (ADC I/O, AC inputs, DAC I/O), the pull-up and pull-down resistors are automatically disabled.

4. Processor and Architecture

Rev: 2.1.2.0

This chapter gives an overview of the AVR32UC CPU. AVR32UC is an implementation of the AVR32 architecture. A summary of the programming model, instruction set, and MPU is presented. For further details, see the *AVR32 Architecture Manual* and the *AVR32UC Technical Reference Manual*.

4.1 Features

- **32-bit load/store AVR32A RISC architecture**
  - **15 general-purpose 32-bit registers**
  - **32-bit Stack Pointer, Program Counter and Link Register reside in register file**
  - **Fully orthogonal instruction set**
  - **Privileged and unprivileged modes enabling efficient and secure operating systems**
  - **Innovative instruction set together with variable instruction length ensuring industry leading code density**
  - **DSP extension with saturating arithmetic, and a wide variety of multiply instructions**
- **3-stage pipeline allowing one instruction per clock cycle for most instructions**
  - **Byte, halfword, word, and double word memory access**
  - **Multiple interrupt priority levels**
- **MPU allows for operating systems with memory protection**
- **FPU enables hardware accelerated floating point calculations**
- **Secure State for supporting FlashVault™ technology**

4.2 AVR32 Architecture

AVR32 is a new, high-performance 32-bit RISC microprocessor architecture, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption and high code density. In addition, the instruction set architecture has been tuned to allow a variety of microarchitectures, enabling the AVR32 to be implemented as low-, mid-, or high-performance processors. AVR32 extends the AVR family into the world of 32- and 64-bit applications.

Through a quantitative approach, a large set of industry recognized benchmarks has been compiled and analyzed to achieve the best code density in its class. In addition to lowering the memory requirements, a compact code size also contributes to the core's low power characteristics. The processor supports byte and halfword data types without penalty in code size and performance.

Memory load and store operations are provided for byte, halfword, word, and double word data with automatic sign- or zero extension of halfword and byte data. The C-compiler is closely linked to the architecture and is able to exploit code optimization features, both for size and speed.

In order to reduce code size to a minimum, some instructions have multiple addressing modes. As an example, instructions with immediates often have a compact format with a smaller immediate, and an extended format with a larger immediate. In this way, the compiler is able to use the format giving the smallest code size.

Another feature of the instruction set is that frequently used instructions, like add, have a compact format with two operands as well as an extended format with three operands. The larger format increases performance, allowing an addition and a data move in the same instruction in a

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single cycle. Load and store instructions have several different formats in order to reduce code size and speed up execution.

The register file is organized as sixteen 32-bit registers and includes the Program Counter, the Link Register, and the Stack Pointer. In addition, register R12 is designed to hold return values from function calls and is used implicitly by some instructions.

4.3 The AVR32UC CPU

The AVR32UC CPU targets low- and medium-performance applications, and provides an advanced On-Chip Debug (OCD) system, no caches, and a Memory Protection Unit (MPU). A hardware Floating Point Unit (FPU) is also provided through the coprocessor instruction space. Java acceleration hardware is not implemented.

AVR32UC provides three memory interfaces, one High Speed Bus master for instruction fetch, one High Speed Bus master for data access, and one High Speed Bus slave interface allowing other bus masters to access data RAMs internal to the CPU. Keeping data RAMs internal to the CPU allows fast access to the RAMs, reduces latency, and guarantees deterministic timing. Also, power consumption is reduced by not needing a full High Speed Bus access for memory accesses. A dedicated data RAM interface is provided for communicating with the internal data RAMs.

A local bus interface is provided for connecting the CPU to device-specific high-speed systems, such as floating-point units and I/O controller ports. This local bus has to be enabled by writing a one to the LOCEN bit in the CPUCR system register. The local bus is able to transfer data between the CPU and the local bus slave in a single clock cycle. The local bus has a dedicated memory range allocated to it, and data transfers are performed using regular load and store instructions. Details on which devices that are mapped into the local bus space is given in the CPU Local Bus section in the Memories chapter.

displays the contents of AVR32UC.

Figure 4-1. Overview of the AVR32UC CPU
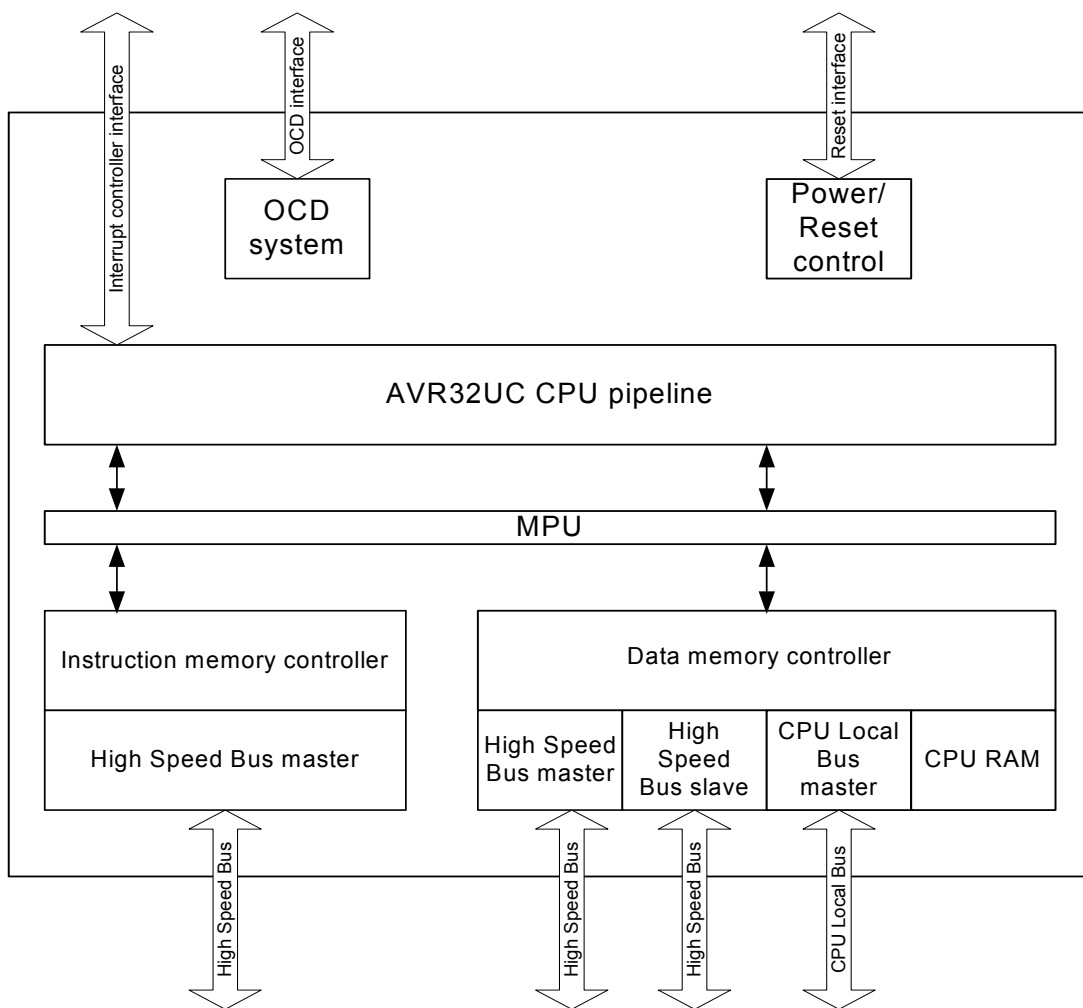
4.3.1 Pipeline Overview

AVR32UC has three pipeline stages, Instruction Fetch (IF), Instruction Decode (ID), and Instruction Execute (EX). The EX stage is split into three parallel subsections, one arithmetic/logic (ALU) section, one multiply (MUL) section, and one load/store (LS) section.

Instructions are issued and complete in order. Certain operations require several clock cycles to complete, and in this case, the instruction resides in the ID and EX stages for the required number of clock cycles. Since there is only three pipeline stages, no internal data forwarding is required, and no data dependencies can arise in the pipeline.

shows an overview of the AVR32UC pipeline stages.

Figure 4-2. The AVR32UC Pipeline
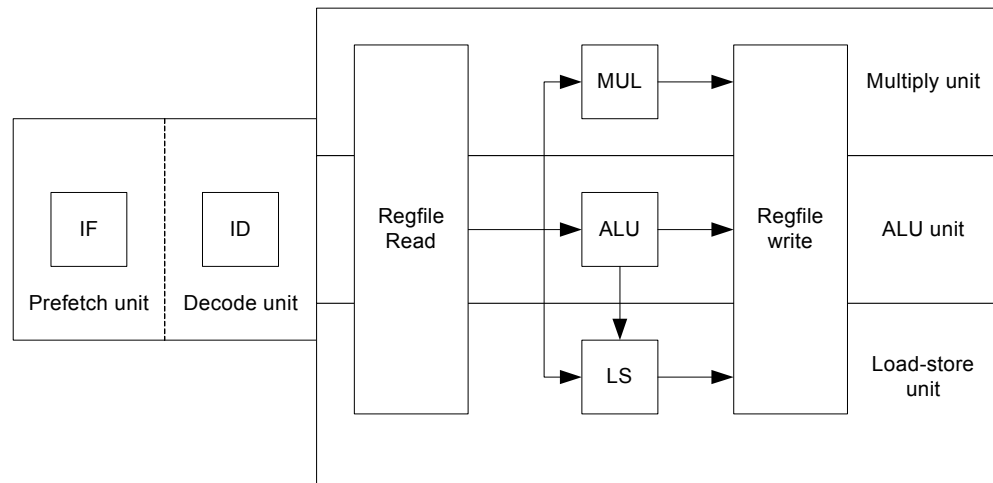
4.3.2 AVR32A Microarchitecture Compliance

AVR32UC implements an AVR32A microarchitecture. The AVR32A microarchitecture is targeted at cost-sensitive, lower-end applications like smaller microcontrollers. This microarchitecture does not provide dedicated hardware registers for shadowing of register file registers in interrupt contexts. Additionally, it does not provide hardware registers for the return address registers and return status registers. Instead, all this information is stored on the system stack. This saves chip area at the expense of slower interrupt handling.

4.3.2.1 Interrupt Handling

Upon interrupt initiation, registers R8-R12 are automatically pushed to the system stack. These registers are pushed regardless of the priority level of the pending interrupt. The return address and status register are also automatically pushed to stack. The interrupt handler can therefore use R8-R12 freely. Upon interrupt completion, the old R8-R12 registers and status register are restored, and execution continues at the return address stored popped from stack.

The stack is also used to store the status register and return address for exceptions and *scall*. Executing the *rete* or *rets* instruction at the completion of an exception or system call will pop this status register and continue execution at the popped return address.

4.3.2.2 Java Support

AVR32UC does not provide Java hardware acceleration.

4.3.2.3 Floating Point Support

A fused multiply-accumulate Floating Point Unit (FPU), performaing a multiply and accumulate as a single operation with no intermediate rounding, therby increasing precision is provided. The floating point hardware conforms to the requirements of the C standard, which is based on the IEEE 754 floating point standard.

4.3.2.4 Memory Protection

The MPU allows the user to check all memory accesses for privilege violations. If an access is attempted to an illegal memory address, the access is aborted and an exception is taken. The MPU in AVR32UC is specified in the AVR32UC Technical Reference manual.

4.3.2.5   Unaligned Reference Handling

AVR32UC does not support unaligned accesses, except for doubleword accesses. AVR32UC is able to perform word-aligned *st.d* and *ld.d*. Any other unaligned memory access will cause an address exception. Doubleword-sized accesses with word-aligned pointers will automatically be performed as two word-sized accesses.

The following table shows the instructions with support for unaligned addresses. All other instructions require aligned addresses.

Table 4-1.   Instructions with Unaligned Reference Support

Instruction	Supported Alignment
ld.d	Word
st.d	Word

4.3.2.6   Unimplemented Instructions

The following instructions are unimplemented in AVR32UC, and will cause an Unimplemented Instruction Exception if executed:

- All SIMD instructions
- All coprocessor instructions if no coprocessors are present
- retj, incjosp, popjc, pushjc
- tlbr, tlbs, tlbw
- cache

4.3.2.7   CPU and Architecture Revision

Three major revisions of the AVR32UC CPU currently exist. The device described in this datasheet uses CPU revision 3.

The Architecture Revision field in the CONFIG0 system register identifies which architecture revision is implemented in a specific device.

AVR32UC CPU revision 3 is fully backward-compatible with revisions 1 and 2, ie. code compiled for revision 1 or 2 is binary-compatible with revision 3 CPUs.

4.4 Programming Model

4.4.1 Register File Configuration

The AVR32UC register file is shown below.

Figure 4-3. The AVR32UC Register File

Application	Supervisor	INT0	INT1	INT2	INT3	Exception	NMI	Secure
PC	PC	PC	PC	PC	PC	PC	PC	PC
LR	LR	LR	LR	LR	LR	LR	LR	LR
SP_APP	SP_SYS	SP_SYS	SP_SYS	SP_SYS	SP_SYS	SP_SYS	SP_SYS	SP_SEC
R12	R12	R12	R12	R12	R12	R12	R12	R12
R11	R11	R11	R11	R11	R11	R11	R11	R11
R10	R10	R10	R10	R10	R10	R10	R10	R10
R9	R9	R9	R9	R9	R9	R9	R9	R9
R8	R8	R8	R8	R8	R8	R8	R8	R8
R7	R7	R7	R7	R7	R7	R7	R7	R7
R6	R6	R6	R6	R6	R6	R6	R6	R6
R5	R5	R5	R5	R5	R5	R5	R5	R5
R4	R4	R4	R4	R4	R4	R4	R4	R4
R3	R3	R3	R3	R3	R3	R3	R3	R3
R2	R2	R2	R2	R2	R2	R2	R2	R2
R1	R1	R1	R1	R1	R1	R1	R1	R1
R0	R0	R0	R0	R0	R0	R0	R0	R0
SR	SR	SR	SR	SR	SR	SR	SR	SR

SS_STATUS
SS_ADRF
SS_ADRR
SS_ADR0
SS_ADR1
SS_SP_SYS
SS_SP_APP
SS_RAR
SS_RSR

4.4.2 Status Register Configuration

The Status Register (SR) is split into two halfwords, one upper and one lower, see Figure 4-4 and Figure 4-5. The lower word contains the C, Z, N, V, and Q condition code flags and the R, T, and L bits, while the upper halfword contains information about the mode and state the processor executes in. Refer to the *AVR32 Architecture Manual* for details.

Figure 4-4. The Status Register High Halfword

Bit 31															Bit 16	
SS	-	-	-	DM	D	-	M2	M1	M0	EM	I3M	I2M	I1M	I0M	GM	Bit name
0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	Initial value

- Global Interrupt Mask
- Interrupt Level 0 Mask
- Interrupt Level 1 Mask
- Interrupt Level 2 Mask
- Interrupt Level 3 Mask
- Exception Mask
- Mode Bit 0
- Mode Bit 1
- Mode Bit 2
- Reserved
- Debug State
- Debug State Mask
- Reserved
- Secure State
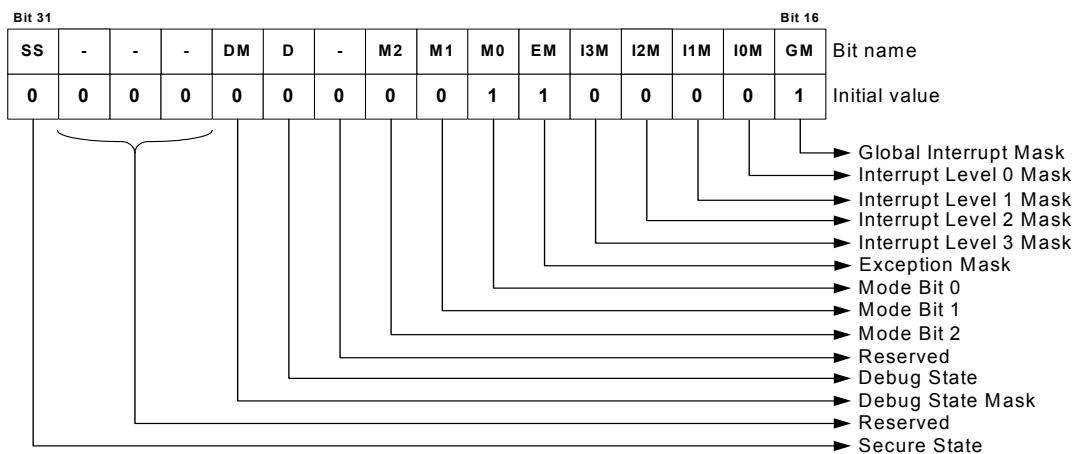
Figure 4-5. The Status Register Low Halfword
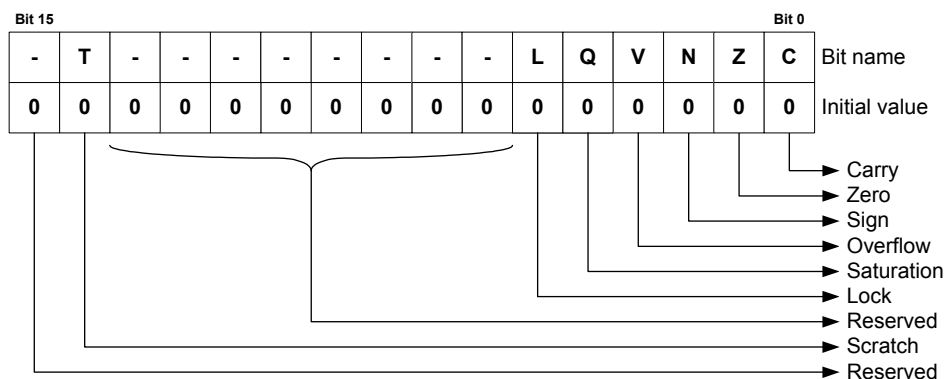
4.4.3 Processor States

4.4.3.1 Normal RISC State

The AVR32 processor supports several different execution contexts as shown in Table 4-2.

Table 4-2. Overview of Execution Modes, their Priorities and Privilege Levels.

Priority	Mode	Security	Description
1	Non Maskable Interrupt	Privileged	Non Maskable high priority interrupt mode
2	Exception	Privileged	Execute exceptions
3	Interrupt 3	Privileged	General purpose interrupt mode
4	Interrupt 2	Privileged	General purpose interrupt mode
5	Interrupt 1	Privileged	General purpose interrupt mode
6	Interrupt 0	Privileged	General purpose interrupt mode
N/A	Supervisor	Privileged	Runs supervisor calls
N/A	Application	Unprivileged	Normal program execution mode

Mode changes can be made under software control, or can be caused by external interrupts or exception processing. A mode can be interrupted by a higher priority mode, but never by one with lower priority. Nested exceptions can be supported with a minimal software overhead.

When running an operating system on the AVR32, user processes will typically execute in the application mode. The programs executed in this mode are restricted from executing certain instructions. Furthermore, most system registers together with the upper halfword of the status register cannot be accessed. Protected memory areas are also not available. All other operating modes are privileged and are collectively called System Modes. They have full access to all privileged and unprivileged resources. After a reset, the processor will be in supervisor mode.

4.4.3.2 Debug State

The AVR32 can be set in a debug state, which allows implementation of software monitor routines that can read out and alter system information for use during application development. This implies that all system and application registers, including the status registers and program counters, are accessible in debug state. The privileged instructions are also available.

All interrupt levels are by default disabled when debug state is entered, but they can individually be switched on by the monitor routine by clearing the respective mask bit in the status register.

Debug state can be entered as described in the *AVR32UC Technical Reference Manual*.

Debug state is exited by the *retd* instruction.

4.4.3.3   Secure State

The AVR32 can be set in a secure state, that allows a part of the code to execute in a state with higher security levels. The rest of the code can not access resources reserved for this secure code. Secure State is used to implement FlashVault technology. Refer to the *AVR32UC Technical Reference Manual* for details.

4.4.4   System Registers

The system registers are placed outside of the virtual memory space, and are only accessible using the privileged *mfsr* and *mtsr* instructions. The table below lists the system registers specified in the AVR32 architecture, some of which are unused in AVR32UC. The programmer is responsible for maintaining correct sequencing of any instructions following a *mtsr* instruction. For detail on the system registers, refer to the *AVR32UC Technical Reference Manual*.

Table 4-3.   System Registers

Reg #	Address	Name	Function
0	0	SR	Status Register
1	4	EVBA	Exception Vector Base Address
2	8	ACBA	Application Call Base Address
3	12	CPUCR	CPU Control Register
4	16	ECR	Exception Cause Register
5	20	RSR_SUP	Unused in AVR32UC
6	24	RSR_INT0	Unused in AVR32UC
7	28	RSR_INT1	Unused in AVR32UC
8	32	RSR_INT2	Unused in AVR32UC
9	36	RSR_INT3	Unused in AVR32UC
10	40	RSR_EX	Unused in AVR32UC
11	44	RSR_NMI	Unused in AVR32UC
12	48	RSR_DBG	Return Status Register for Debug mode
13	52	RAR_SUP	Unused in AVR32UC
14	56	RAR_INT0	Unused in AVR32UC
15	60	RAR_INT1	Unused in AVR32UC
16	64	RAR_INT2	Unused in AVR32UC
17	68	RAR_INT3	Unused in AVR32UC
18	72	RAR_EX	Unused in AVR32UC
19	76	RAR_NMI	Unused in AVR32UC
20	80	RAR_DBG	Return Address Register for Debug mode
21	84	JECR	Unused in AVR32UC
22	88	JOSP	Unused in AVR32UC
23	92	JAVA_LV0	Unused in AVR32UC

Table 4-3. System Registers (Continued)

Reg #	Address	Name	Function
24	96	JAVA_LV1	Unused in AVR32UC
25	100	JAVA_LV2	Unused in AVR32UC
26	104	JAVA_LV3	Unused in AVR32UC
27	108	JAVA_LV4	Unused in AVR32UC
28	112	JAVA_LV5	Unused in AVR32UC
29	116	JAVA_LV6	Unused in AVR32UC
30	120	JAVA_LV7	Unused in AVR32UC
31	124	JTBA	Unused in AVR32UC
32	128	JBCR	Unused in AVR32UC
33-63	132-252	Reserved	Reserved for future use
64	256	CONFIG0	Configuration register 0
65	260	CONFIG1	Configuration register 1
66	264	COUNT	Cycle Counter register
67	268	COMPARE	Compare register
68	272	TLBEHI	Unused in AVR32UC
69	276	TLBELO	Unused in AVR32UC
70	280	PTBR	Unused in AVR32UC
71	284	TLBEAR	Unused in AVR32UC
72	288	MMUCR	Unused in AVR32UC
73	292	TLBARLO	Unused in AVR32UC
74	296	TLBARHI	Unused in AVR32UC
75	300	PCCNT	Unused in AVR32UC
76	304	PCNT0	Unused in AVR32UC
77	308	PCNT1	Unused in AVR32UC
78	312	PCCR	Unused in AVR32UC
79	316	BEAR	Bus Error Address Register
80	320	MPUAR0	MPU Address Register region 0
81	324	MPUAR1	MPU Address Register region 1
82	328	MPUAR2	MPU Address Register region 2
83	332	MPUAR3	MPU Address Register region 3
84	336	MPUAR4	MPU Address Register region 4
85	340	MPUAR5	MPU Address Register region 5
86	344	MPUAR6	MPU Address Register region 6
87	348	MPUAR7	MPU Address Register region 7
88	352	MPUPSR0	MPU Privilege Select Register region 0
89	356	MPUPSR1	MPU Privilege Select Register region 1

Table 4-3.   System Registers (Continued)

Reg #	Address	Name	Function
90	360	MPUPSR2	MPU Privilege Select Register region 2
91	364	MPUPSR3	MPU Privilege Select Register region 3
92	368	MPUPSR4	MPU Privilege Select Register region 4
93	372	MPUPSR5	MPU Privilege Select Register region 5
94	376	MPUPSR6	MPU Privilege Select Register region 6
95	380	MPUPSR7	MPU Privilege Select Register region 7
96	384	MPUCRA	Unused in this version of AVR32UC
97	388	MPUCRB	Unused in this version of AVR32UC
98	392	MPUBRA	Unused in this version of AVR32UC
99	396	MPUBRB	Unused in this version of AVR32UC
100	400	MPUAPRA	MPU Access Permission Register A
101	404	MPUAPRB	MPU Access Permission Register B
102	408	MPUCR	MPU Control Register
103	412	SS_STATUS	Secure State Status Register
104	416	SS_ADRF	Secure State Address Flash Register
105	420	SS_ADRR	Secure State Address RAM Register
106	424	SS_ADR0	Secure State Address 0 Register
107	428	SS_ADR1	Secure State Address 1 Register
108	432	SS_SP_SYS	Secure State Stack Pointer System Register
109	436	SS_SP_APP	Secure State Stack Pointer Application Register
110	440	SS_RAR	Secure State Return Address Register
111	444	SS_RSR	Secure State Return Status Register
112-191	448-764	Reserved	Reserved for future use
192-255	768-1020	IMPL	IMPLEMENTATION DEFINED

4.5   Exceptions and Interrupts

In the AVR32 architecture, events are used as a common term for exceptions and interrupts. AVR32UC incorporates a powerful event handling scheme. The different event sources, like Illegal Op-code and interrupt requests, have different priority levels, ensuring a well-defined behavior when multiple events are received simultaneously. Additionally, pending events of a higher priority class may preempt handling of ongoing events of a lower priority class.

When an event occurs, the execution of the instruction stream is halted, and execution is passed to an event handler at an address specified in Table 4-4 on page 38. Most of the handlers are placed sequentially in the code space starting at the address specified by EVBA, with four bytes between each handler. This gives ample space for a jump instruction to be placed there, jumping to the event routine itself. A few critical handlers have larger spacing between them, allowing the entire event routine to be placed directly at the address specified by the EVBA-relative offset generated by hardware. All interrupt sources have autovectored interrupt service routine (ISR) addresses. This allows the interrupt controller to directly specify the ISR address as an address

relative to EVBA. The autovector offset has 14 address bits, giving an offset of maximum 16384 bytes. The target address of the event handler is calculated as (EVBA | event_handler_offset), not (EVBA + event_handler_offset), so EVBA and exception code segments must be set up appropriately. The same mechanisms are used to service all different types of events, including interrupt requests, yielding a uniform event handling scheme.

An interrupt controller does the priority handling of the interrupts and provides the autovector offset to the CPU.

4.5.1 System Stack Issues

Event handling in AVR32UC uses the system stack pointed to by the system stack pointer, SP_SYS, for pushing and popping R8-R12, LR, status register, and return address. Since event code may be timing-critical, SP_SYS should point to memory addresses in the IRAM section, since the timing of accesses to this memory section is both fast and deterministic.

The user must also make sure that the system stack is large enough so that any event is able to push the required registers to stack. If the system stack is full, and an event occurs, the system will enter an UNDEFINED state.

4.5.2 Exceptions and Interrupt Requests

When an event other than *scall* or debug request is received by the core, the following actions are performed atomically:

1. The pending event will not be accepted if it is masked. The I3M, I2M, I1M, I0M, EM, and GM bits in the Status Register are used to mask different events. Not all events can be masked. A few critical events (NMI, Unrecoverable Exception, TLB Multiple Hit, and Bus Error) can not be masked. When an event is accepted, hardware automatically sets the mask bits corresponding to all sources with equal or lower priority. This inhibits acceptance of other events of the same or lower priority, except for the critical events listed above. Software may choose to clear some or all of these bits after saving the necessary state if other priority schemes are desired. It is the event source's responsability to ensure that their events are left pending until accepted by the CPU.

2. When a request is accepted, the Status Register and Program Counter of the current context is stored to the system stack. If the event is an INT0, INT1, INT2, or INT3, registers R8-R12 and LR are also automatically stored to stack. Storing the Status Register ensures that the core is returned to the previous execution mode when the current event handling is completed. When exceptions occur, both the EM and GM bits are set, and the application may manually enable nested exceptions if desired by clearing the appropriate bit. Each exception handler has a dedicated handler address, and this address uniquely identifies the exception source.

3. The Mode bits are set to reflect the priority of the accepted event, and the correct register file bank is selected. The address of the event handler, as shown in Table 4-4 on page 38, is loaded into the Program Counter.

The execution of the event handler routine then continues from the effective address calculated.

The *rete* instruction signals the end of the event. When encountered, the Return Status Register and Return Address Register are popped from the system stack and restored to the Status Register and Program Counter. If the *rete* instruction returns from INT0, INT1, INT2, or INT3, registers R8-R12 and LR are also popped from the system stack. The restored Status Register contains information allowing the core to resume operation in the previous execution mode. This concludes the event handling.

4.5.3 Supervisor Calls

The AVR32 instruction set provides a supervisor mode call instruction. The *scall* instruction is designed so that privileged routines can be called from any context. This facilitates sharing of code between different execution modes. The *scall* mechanism is designed so that a minimal execution cycle overhead is experienced when performing supervisor routine calls from time-critical event handlers.

The *scall* instruction behaves differently depending on which mode it is called from. The behaviour is detailed in the instruction set reference. In order to allow the *scall* routine to return to the correct context, a return from supervisor call instruction, *rets*, is implemented. In the AVR32UC CPU, *scall* and *rets* uses the system stack to store the return address and the status register.

4.5.4 Debug Requests

The AVR32 architecture defines a dedicated Debug mode. When a debug request is received by the core, Debug mode is entered. Entry into Debug mode can be masked by the DM bit in the status register. Upon entry into Debug mode, hardware sets the SR.D bit and jumps to the Debug Exception handler. By default, Debug mode executes in the exception context, but with dedicated Return Address Register and Return Status Register. These dedicated registers remove the need for storing this data to the system stack, thereby improving debuggability. The Mode bits in the Status Register can freely be manipulated in Debug mode, to observe registers in all contexts, while retaining full privileges.

Debug mode is exited by executing the *retd* instruction. This returns to the previous context.

4.5.5 Entry Points for Events

Several different event handler entry points exist. In AVR32UC, the reset address is 0x80000000. This places the reset address in the boot flash memory area.

TLB miss exceptions and *scall* have a dedicated space relative to EVBA where their event handler can be placed. This speeds up execution by removing the need for a jump instruction placed at the program address jumped to by the event hardware. All other exceptions have a dedicated event routine entry point located relative to EVBA. The handler routine address identifies the exception source directly.

AVR32UC uses the ITLB and DTLB protection exceptions to signal a MPU protection violation. ITLB and DTLB miss exceptions are used to signal that an access address did not map to any of the entries in the MPU. TLB multiple hit exception indicates that an access address did map to multiple TLB entries, signalling an error.

All interrupt requests have entry points located at an offset relative to EVBA. This autovector offset is specified by an interrupt controller. The programmer must make sure that none of the autovector offsets interfere with the placement of other code. The autovector offset has 14 address bits, giving an offset of maximum 16384 bytes.

Special considerations should be made when loading EVBA with a pointer. Due to security considerations, the event handlers should be located in non-writeable flash memory, or optionally in a privileged memory protection region if an MPU is present.

If several events occur on the same instruction, they are handled in a prioritized way. The priority ordering is presented in . If events occur on several instructions at different locations in the pipeline, the events on the oldest instruction are always handled before any events on any younger instruction, even if the younger instruction has events of higher priority

than the oldest instruction. An instruction B is younger than an instruction A if it was sent down the pipeline later than A.

The addresses and priority of simultaneous events are shown in Table 4-4 on page 38. Some of the exceptions are unused in AVR32UC since it has no MMU, coprocessor interface, or floating-point unit.

Table 4-4. Priority and Handler Addresses for Events

Priority	Handler Address	Name	Event source	Stored Return Address
1	0x80000000	Reset	External input	Undefined
2	Provided by OCD system	OCD Stop CPU	OCD system	First non-completed instruction
3	EVBA+0x00	Unrecoverable exception	Internal	PC of offending instruction
4	EVBA+0x04	TLB multiple hit	MPU	PC of offending instruction
5	EVBA+0x08	Bus error data fetch	Data bus	First non-completed instruction
6	EVBA+0x0C	Bus error instruction fetch	Data bus	First non-completed instruction
7	EVBA+0x10	NMI	External input	First non-completed instruction
8	Autovectored	Interrupt 3 request	External input	First non-completed instruction
9	Autovectored	Interrupt 2 request	External input	First non-completed instruction
10	Autovectored	Interrupt 1 request	External input	First non-completed instruction
11	Autovectored	Interrupt 0 request	External input	First non-completed instruction
12	EVBA+0x14	Instruction Address	CPU	PC of offending instruction
13	EVBA+0x50	ITLB Miss	MPU	PC of offending instruction
14	EVBA+0x18	ITLB Protection	MPU	PC of offending instruction
15	EVBA+0x1C	Breakpoint	OCD system	First non-completed instruction
16	EVBA+0x20	Illegal Opcode	Instruction	PC of offending instruction
17	EVBA+0x24	Unimplemented instruction	Instruction	PC of offending instruction
18	EVBA+0x28	Privilege violation	Instruction	PC of offending instruction
19	EVBA+0x2C	Floating-point	UNUSED	
20	EVBA+0x30	Coprocessor absent	Instruction	PC of offending instruction
21	EVBA+0x100	Supervisor call	Instruction	PC(Supervisor Call) +2
22	EVBA+0x34	Data Address (Read)	CPU	PC of offending instruction
23	EVBA+0x38	Data Address (Write)	CPU	PC of offending instruction
24	EVBA+0x60	DTLB Miss (Read)	MPU	PC of offending instruction
25	EVBA+0x70	DTLB Miss (Write)	MPU	PC of offending instruction
26	EVBA+0x3C	DTLB Protection (Read)	MPU	PC of offending instruction
27	EVBA+0x40	DTLB Protection (Write)	MPU	PC of offending instruction
28	EVBA+0x44	DTLB Modified	UNUSED	

5. Memories

5.1 Embedded Memories

- **Internal High-Speed Flash (See Table 5-1 on page 40)**
  - **512 Kbytes**
  - **256 Kbytes**
  - **128 Kbytes**
  - **64 Kbytes**
    - **0 Wait State Access at up to 33 MHz in Worst Case Conditions**
    - **1 Wait State Access at up to 66 MHz in Worst Case Conditions**
    - **Pipelined Flash Architecture, allowing burst reads from sequential Flash locations, hiding penalty of 1 wait state access**
    - **Pipelined Flash Architecture typically reduces the cycle penalty of 1 wait state operation to only 15% compared to 0 wait state operation**
    - **100 000 Write Cycles, 15-year Data Retention Capability**
    - **4ms Page Programming Time and 8ms Full-Chip Erase Time**
    - **Sector Lock Capabilities, Bootloader Protection, Security Bit**
    - **64 Fuses, 32 Of Which Are Preserved During Chip Erase**
    - **User Page For Data To Be Preserved During Chip Erase**
- **Internal High-Speed SRAM, Single-cycle access at full speed (See Table 5-1 on page 40)**
  - **64 Kbytes**
  - **32 Kbytes**
  - **16 Kbytes**
- **Supplementary Internal High-Speed System SRAM (HSB RAM), Single-cycle access at full speed**
  - **Memory space available on System Bus for peripherals data.**
  - **4 Kbytes**

5.2   Physical Memory Map

The system bus is implemented as a bus matrix. All system bus addresses are fixed, and they are never remapped in any way, not even in boot. Note that AVR32UC CPU uses unsegmented translation, as described in the AVR32 Architecture Manual. The 32-bit physical address space is mapped as follows:

Table 5-1.   AT32UC3C Physical Memory Map

Device	Start Address	AT32UC3 Derivatives							
		C0512C	C1512C C2512C	C0256C	C1256C C2256C	C0128C	C1128C C2128C	C064C	C164C C264C
Embedded SRAM	0x0000_0000	64 KB	64 KB	64 KB	64 KB	32 KB	32 KB	16 KB	16 KB
Embedded Flash	0x8000_0000	512 KB	512 KB	256 KB	256 KB	128 KB	128 KB	64 KB	64 KB
SAU	0x9000_0000	1 KB	1 KB	1 KB	1 KB	1 KB	1 KB	1 KB	1 KB
HSB SRAM	0xA000_0000	4 KB	4 KB	4 KB	4 KB	4 KB	4 KB	4 KB	4 KB
EBI SRAM CS0	0xC000_0000	16 MB	-	16 MB	-	16 MB	-	16 MB	-
EBI SRAM CS2	0xC800_0000	16 MB	-	16 MB	-	16 MB	-	16 MB	-
EBI SRAM CS3	0xCC00_0000	16 MB	-	16 MB	-	16 MB	-	16 MB	-
EBI SRAM CS1 /SDRAM CS0	0xD000_0000	128 MB	-	128 MB	-	128 MB	-	128 MB	-
HSB-PB Bridge C	0xFFFD_0000	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB
HSB-PB Bridge B	0xFFFE_0000	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB
HSB-PB Bridge A	0xFFFF_0000	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB

Table 5-2. Flash Memory Parameters

Part Number	Flash Size (FLASH_PW)	Number of pages (FLASH_P)	Page size (FLASH_W)
AT32UC3C0512C AT32UC3C1512C AT32UC3C2512C	512 Kbytes	1024	128 words
AT32UC3C0256C AT32UC3C1256C AT32UC3C2256C	256 Kbytes	512	128 words
AT32UC3C0128C AT32UC3C1128C AT32UC3C2128C	128 Kbytes	256	128 words
AT32UC3C064C AT32UC3C164C AT32UC3C264C	64 Kbytes	128	128 words

5.3 Peripheral Address Map

Table 5-3. Peripheral Address Mapping

Address		Peripheral Name
0xFFFD0000	PDCA	Peripheral DMA Controller - PDCA
0xFFFD1000	MDMA	Memory DMA - MDMA
0xFFFD1400	USART1	Universal Synchronous/Asynchronous Receiver/Transmitter - USART1
0xFFFD1800	SPI0	Serial Peripheral Interface - SPI0
0xFFFD1C00	CANIF	Control Area Network interface - CANIF
0xFFFD2000	TC0	Timer/Counter - TC0
0xFFFD2400	ADCIFA	ADC controller interface with Touch Screen functionality - ADCIFA
0xFFFD2800	USART4	Universal Synchronous/Asynchronous Receiver/Transmitter - USART4
0xFFFD2C00	TWIM2	Two-wire Master Interface - TWIM2
0xFFFD3000	TWIS2	Two-wire Slave Interface - TWIS2

Table 5-3. Peripheral Address Mapping

Address	Peripheral	Description
0xFFFE0000	HFLASHC	Flash Controller - HFLASHC
0xFFFE1000	USBC	USB 2.0 OTG Interface - USBC
0xFFFE2000	HMATRIX	HSB Matrix - HMATRIX
0xFFFE2400	SAU	Secure Access Unit - SAU
0xFFFE2800	SMC	Static Memory Controller - SMC
0xFFFE2C00	SDRAMC	SDRAM Controller - SDRAMC
0xFFFE3000	MACB	Ethernet MAC - MACB
0xFFFF0000	INTC	Interrupt controller - INTC
0xFFFF0400	PM	Power Manager - PM
0xFFFF0800	SCIF	System Control Interface - SCIF
0xFFFF0C00	AST	Asynchronous Timer - AST
0xFFFF1000	WDT	Watchdog Timer - WDT
0xFFFF1400	EIC	External Interrupt Controller - EIC
0xFFFF1800	FREQM	Frequency Meter - FREQM
0xFFFF2000	GPIO	General Purpose Input/Output Controller - GPIO
0xFFFF2800	USART0	Universal Synchronous/Asynchronous Receiver/Transmitter - USART0
0xFFFF2C00	USART2	Universal Synchronous/Asynchronous Receiver/Transmitter - USART2
0xFFFF3000	USART3	Universal Synchronous/Asynchronous Receiver/Transmitter - USART3
0xFFFF3400	SPI1	Serial Peripheral Interface - SPI1

Table 5-3. Peripheral Address Mapping

Address	Module	Description
0xFFFF3800	TWIM0	Two-wire Master Interface - TWIM0
0xFFFF3C00	TWIM1	Two-wire Master Interface - TWIM1
0xFFFF4000	TWIS0	Two-wire Slave Interface - TWIS0
0xFFFF4400	TWIS1	Two-wire Slave Interface - TWIS1
0xFFFF4800	IISC	Inter-IC Sound (I2S) Controller - IISC
0xFFFF4C00	PWM	Pulse Width Modulation Controller - PWM
0xFFFF5000	QDEC0	Quadrature Decoder - QDEC0
0xFFFF5400	QDEC1	Quadrature Decoder - QDEC1
0xFFFF5800	TC1	Timer/Counter - TC1
0xFFFF5C00	PEVC	Peripheral Event Controller - PEVC
0xFFFF6000	ACIFA0	Analog Comparators Interface - ACIFA0
0xFFFF6400	ACIFA1	Analog Comparators Interface - ACIFA1
0xFFFF6800	DACIFB0	DAC interface - DACIFB0
0xFFFF6C00	DACIFB1	DAC interface - DACIFB1
0xFFFF7000	AW	aWire - AW

5.4 CPU Local Bus Mapping

Some of the registers in the GPIO module are mapped onto the CPU local bus, in addition to being mapped on the Peripheral Bus. These registers can therefore be reached both by accesses on the Peripheral Bus, and by accesses on the local bus.

Mapping these registers on the local bus allows cycle-deterministic toggling of GPIO pins since the CPU and GPIO are the only modules connected to this bus. Also, since the local bus runs at CPU speed, one write or read operation can be performed per clock cycle to the local bus-mapped GPIO registers.

The following GPIO registers are mapped on the local bus:

Table 5-4. Local bus mapped GPIO registers

Port	Register	Mode	Local Bus Address	Access
0	Output Driver Enable Register (ODER)	WRITE	0x4000_0040	Write-only
		SET	0x4000_0044	Write-only
		CLEAR	0x4000_0048	Write-only
		TOGGLE	0x4000_004C	Write-only
	Output Value Register (OVR)	WRITE	0x4000_0050	Write-only
		SET	0x4000_0054	Write-only
		CLEAR	0x4000_0058	Write-only
		TOGGLE	0x4000_005C	Write-only
	Pin Value Register (PVR)	-	0x4000_0060	Read-only
1	Output Driver Enable Register (ODER)	WRITE	0x4000_0240	Write-only
		SET	0x4000_0244	Write-only
		CLEAR	0x4000_0248	Write-only
		TOGGLE	0x4000_024C	Write-only
	Output Value Register (OVR)	WRITE	0x4000_0250	Write-only
		SET	0x4000_0254	Write-only
		CLEAR	0x4000_0258	Write-only
		TOGGLE	0x4000_025C	Write-only
	Pin Value Register (PVR)	-	0x4000_0460	Read-only
3	Output Driver Enable Register (ODER)	WRITE	0x4000_0440	Write-only
		SET	0x4000_0444	Write-only
		CLEAR	0x4000_0448	Write-only
		TOGGLE	0x4000_044C	Write-only
	Output Value Register (OVR)	WRITE	0x4000_0450	Write-only
		SET	0x4000_0454	Write-only
		CLEAR	0x4000_0458	Write-only
		TOGGLE	0x4000_045C	Write-only
	Pin Value Register (PVR)	-	0x4000_0460	Read-only

Table 5-4. Local bus mapped GPIO registers

Port	Register	Mode	Local Bus Address	Access
4	Output Driver Enable Register (ODER)	WRITE	0x4000_0640	Write-only
		SET	0x4000_0644	Write-only
		CLEAR	0x4000_0648	Write-only
		TOGGLE	0x4000_064C	Write-only
	Output Value Register (OVR)	WRITE	0x4000_0650	Write-only
		SET	0x4000_0654	Write-only
		CLEAR	0x4000_0658	Write-only
		TOGGLE	0x4000_065C	Write-only
	Pin Value Register (PVR)	-	0x4000_0660	Read-only

6. Supply and Startup Considerations

6.1 Supply Considerations

6.1.1 Power Supplies

The AT32UC3C has several types of power supply pins:

- **VDDIO: Powers I/O lines and the flash. 2 Voltage ranges available: 5V or 3.3V nominal.**
- **VDDANA: Powers the Analog part of the device (Analog I/Os, ADC, ACs, DACs). 2 voltage ranges available: 5V or 3.3V nominal.**
- **VDDIN_5: Input voltage for the 1.8V and 3.3V regulators. 2 Voltage ranges available: 5V or 3.3V nominal.**
- **VDDIN_33:**
    - **USB I/O power supply**
    - **if the device is 3.3V powered: Input voltage, voltage is 3.3V nominal.**
    - **if the device is 5V powered: stabilization for the 3.3V voltage regulator, requires external capacitors**
- **VDDCORE: Stabilization for the 1.8V voltage regulator, requires external capacitors.**
- **GNDCORE: Ground pins for the voltage regulators and the core.**
- **GNDANA: Ground pin for Analog part of the design**
- **GNDPLL: Ground pin for the PLLs**
- **GNDIO: Ground pins for the I/O**

See ”Electrical Characteristics” on page 50 for power consumption on the various supply pins.

For decoupling recommendations for the different power supplies, please refer to the schematic checklist.

6.1.2 Voltage Regulators

The AT32UC3C embeds two voltage regulators:

- One 1.8V internal regulator that converts from VDDIN_5 to 1.8V. The regulator supplies the output voltage on VDDCORE.
- One 3.3V internal regulator that converts from VDDIN_5 to 3.3V. The regulator supplies the USB pads. If the USB is not used, the 3.3V regulator can be disabled through the VREG33CTL field of the VREGCTRL SCIF register.

6.1.3 Regulators Connection

The AT32UC3C supports two power supply configurations.

- 5V single supply mode
- 3.3V single supply mode

6.1.3.1 5V Single Supply Mode

In 5V single supply mode, the 1.8V internal regulator is connected to the 5V source (VDDIN_5 pin) and its output feeds VDDCORE.

The 3.3V regulator is connected to the 5V source (VDDIN_5 pin) and its output feeds the USB pads. If the USB is not used, the 3.3V regulator can be disabled through the VREG33CTL field of the VREGCTRL SCIF register.

Figure 6-1 on page 47 shows the power schematics to be used for 5V single supply mode. All I/O lines and analog blocks will be powered by the same power (VDDIN_5 = VDDIO = VDDANA).

Figure 6-1. 5V Single Power Supply mode
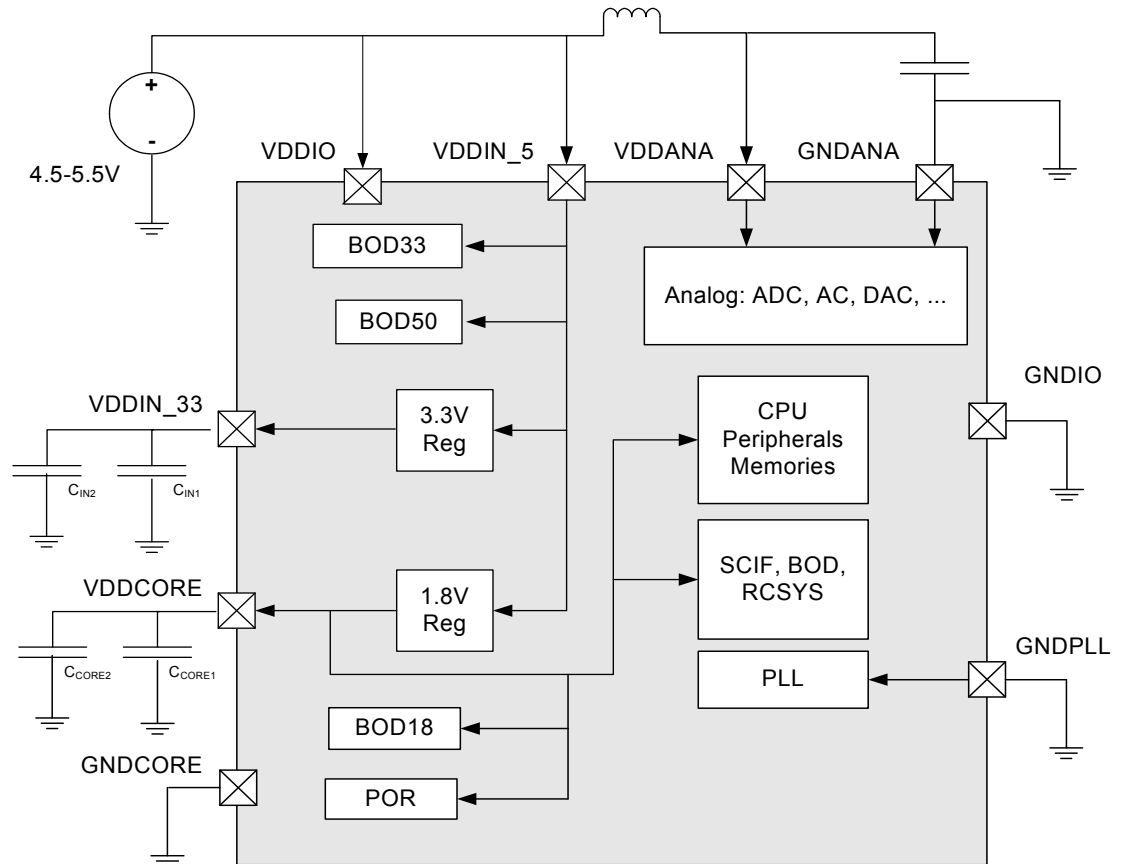
6.1.3.2 3.3V Single Supply Mode

In 3.3V single supply mode, the VDDIN_5 and VDDIN_33 pins should be connected together externally. The 1.8V internal regulator is connected to the 3.3V source (VDDIN_5 pin) and its output feeds VDDCORE.

The 3.3V regulator should be disabled once the circuit is running through the VREG33CTL field of the VREGCTRL SCIF register.

Figure 6-2 on page 48 shows the power schematics to be used for 3.3V single supply mode. All I/O lines and analog blocks will be powered by the same power (VDDIN_5 = VDDIN_33 = VDDIO = VDDANA).

Figure 6-2. 3 Single Power Supply Mode
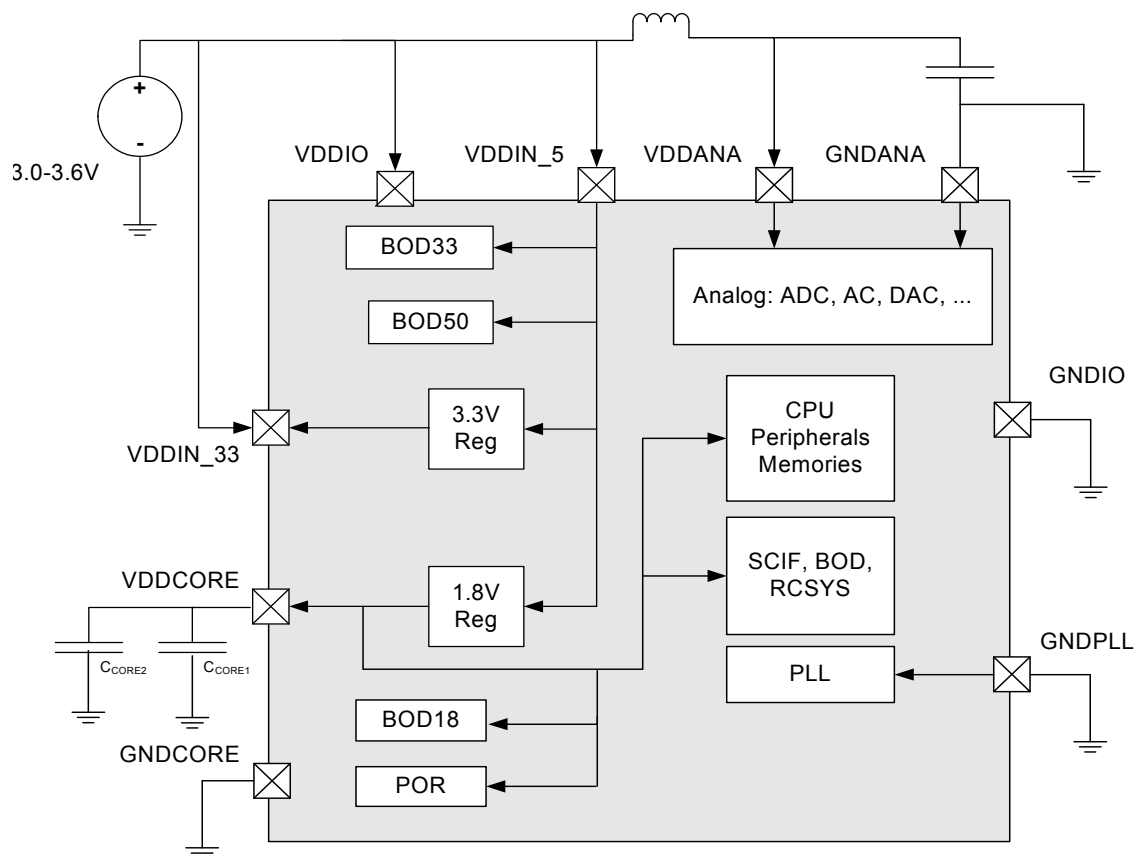
6.1.4 Power-up Sequence

6.1.4.1 Maximum Rise Rate

To avoid risk of latch-up, the rise rate of the power supplies must not exceed the values described in Table 7-2 on page 51 .

Recommended order for power supplies is also described in this table.

6.1.4.2 Minimum Rise Rate

The integrated Power-Reset circuitry monitoring the powering supply requires a minimum rise rate for the VDDIN_5 power supply.

See Table 7-2 on page 51 for the minimum rise rate value.

If the application can not ensure that the minimum rise rate condition for the VDDIN power supply is met, the following configuration can be used:

- A logic "0" value is applied during power-up on pin RESET_N until:
  - VDDIN_5 rises above 4.5V in 5V single supply mode.
  - VDDIN_33 rises above 3V in 3.3V single supply mode.

6.2 Startup Considerations

This chapter summarizes the boot sequence of the AT32UC3C. The behavior after power-up is controlled by the Power Manager. For specific details, refer to the Power Manager chapter.

6.2.1 Starting of clocks

At power-up, the BOD33 and the BOD18 are enabled. The device will be held in a reset state by the power-up circuitry, until the VDDIN_33 (resp. VDDCORE) has reached the reset threshold of the BOD33 (resp BOD18). Refer to the Electrical Characteristics for the BOD thresholds. Once the power has stabilized, the device will use the System RC Oscillator (RCSYS, 115KHz typical frequency) as clock source. The BOD18 and BOD33 are kept enabled or are disabled according to the fuse settings (See the Fuse Setting section in the Flash Controller chapter).

On system start-up, the PLLs are disabled. All clocks to all modules are running. No clocks have a divided frequency, all parts of the system receive a clock with the same frequency as the internal RC Oscillator.

6.2.2 Fetching of initial instructions

After reset has been released, the AVR32UC CPU starts fetching instructions from the reset address, which is 0x8000_0000. This address points to the first address in the internal Flash.

The internal Flash uses VDDIO voltage during read and write operations. It is recommended to use the BOD33 to monitor this voltage and make sure the VDDIO is above the minimum level (3.0V).

The code read from the internal Flash is free to configure the system to use for example the PLLs, to divide the frequency of the clock routed to some of the peripherals, and to gate the clocks to unused peripherals.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings*

Operating temperature...................................... -40°C to +85°C

Storage temperature....................................... -60°C to +150°C

Voltage on any pin except DM/DP/VBUS
with respect to ground .... -0.3V to V_{CC}+VDDIO+0.3V

Voltage on DM/DP with respect to ground.........-0.3V to +3.6V

Voltage on VBUS with respect to ground...........-0.3V to +5.5V

Maximum operating voltage (VDDIN_5) 5.5V

Maximum operating voltage (VDDIO, VDDANA) 5.5V

Maximum operating voltage (VDDIN_33) 3.6V

DC current per I/O pin... TBD mA

DC current V_{CC} and GND pins .... TBD mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Supply Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C, unless otherwise specified and are valid for a junction temperature up to T_J = 100°C. Please refer to Section 6. "Supply and Startup Considerations" on page 46.

Table 7-1. Supply Characteristics

| Symbol | Parameter | Condition | Voltage | | |
			Min	Max	Unit
V_{VDDIN_5}	DC supply internal regulators	5V range	4.5	5.5	V
		3V range	3.0	3.6	V
V_{VDDIN_33}	DC supply USB I/O	only in 3V range	3.0	3.6	V
V_{VDDANA}	DC supply analog part	5V range	4.5	5.5	V
		3V range	3.0	3.6	V
V_{VDDIO}	DC supply peripheral I/O	5V range	4.5	5.5	V
		3V range	3.0	3.6	V

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Table 7-2. Supply Rise Rates and Order

Symbol	Parameter	Rise Rate		
		Min	Max	Comment
V$_{VDDIN\_5}$	DC supply internal 3.3V regulator	0.01 V/ms	1.25 V/us	
V$_{VDDIN\_33}$	DC supply internal 1.8V regulator	0.01 V/ms	1.25 V/us	
V$_{VDDIO}$	DC supply peripheral I/O	0.01 V/ms	1.25 V/us	Rise after or at the same time as VDDIN_5, VDDIN_33
V$_{VDDANA}$	DC supply analog part	0.01 V/ms	1.25 V/us	Rise after or at the same time as VDDIN_5, VDDIN_33

7.3 Maximum Clock Frequencies

These parameters are given in the following conditions:

• V$_{VDDCORE}$ = 1.85V
• Temperature = -40°C to 85°C

Table 7-3. Clock Frequencies

Symbol	Parameter	Conditions	Min	Max[1]	Units
f$_{CPU}$	CPU clock frequency			66	MHz
f$_{PBA}$	PBA clock frequency			66	MHz
f$_{PBB}$	PBB clock frequency			66	MHz
f$_{PBC}$	PBC clock frequency			66	MHz
f$_{GCLK0}$	GCLK0 clock frequency	Generic clock for USBC		50	MHz
f$_{GCLK1}$	GCLK1 clock frequency	Generic clock for CANIF		66	MHz
f$_{GCLK2}$	GCLK2 clock frequency	Generic clock for AST		80	MHz
f$_{GCLK4}$	GCLK4 clock frequency	Generic clock for PWM		133	MHz
f$_{GCLK11}$	GCLK11 clock frequency	Generic clock for IISC		50	MHz

Note: 1.   These values are guaranteed by design and will be updated after characterization of current silicon.

7.4 Power Consumption

The values in Table 7-4 are measured values of power consumption under the following conditions, except where noted:

• Operating conditions core supply (Figure 7-1)
  – V$_{DDIN\_5}$ = V$_{DDIN\_33}$ = 3.3V
  – V$_{VDDCORE}$ = 1.85V, supplied by the internal regulator
  – V$_{DDIO}$ = 3.3V
  – V$_{DDANA}$: 3.3V
  – Internal 3.3V regulator is off.
• T$_A$ = 25°C

- I/Os are configured as inputs, with internal pull-up enabled.
- Oscillators
  - OSC0/1 (crystal oscillator) stopped
  - OSC32K (32KHz crystal oscillator) stopped
  - PLL0 running
  - PLL1 stopped
- Clocks
  - External clock on XIN0 as main clock source **(**10MHz**)**
  - CPU, HSB, and PBB clocks undivided
  - PBA, PBC clock divided by 4
  - The following peripheral clocks running
    - PM, SCIF, AST, FLASHC, PBA bridge
  - All other peripheral clocks stopped

Table 7-4. Power Consumption for Different Operating Modes

Mode	Conditions	Measured on	Consumption Typ	Unit
Active	-CPU running a recursive Fibonacci algorithm	Amp	TBD	µA/MHz
	-CPU running a division algorithm		TBD	
Idle			TBD	
Frozen			TBD	
Standby			TBD	
Stop			73	µA
DeepStop			43	
Static	-OSC32K and AST running		31	
	-AST and OSC32K stopped		31	

Figure 7-1. Measurement Schematic
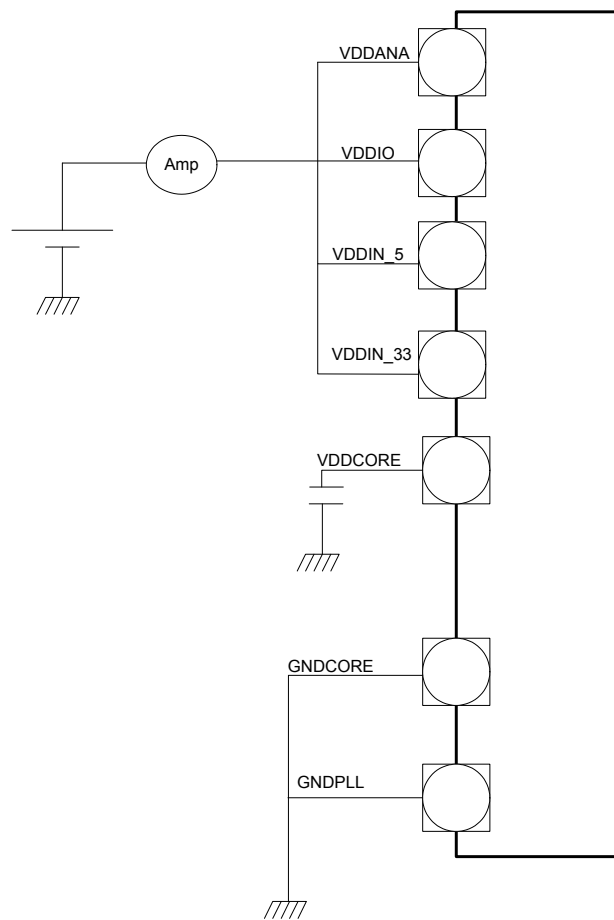
7.4.1 Peripheral Power Consumption

The values in Table 7-5 are measured values of power consumption under the following conditions.

- Operating conditions core supply (Figure 7-1)
  - $V_{DDIN\_5} = V_{DDIN\_33} = 3.3V$
  - $V_{VDDCORE} = 1.85V$, supplied by the internal regulator
  - $V_{DDIO} = 3.3V$
  - V_{DDANA}: 3.3V
  - Internal 3.3V regulator is off.
- $T_A = 25°C$
- I/Os are configured as inputs, with internal pull-up enabled.
- Oscillators
  - OSC0/1 (crystal oscillator) stopped
  - OSC32K (32KHz crystal oscillator) stopped
  - PLL0 running

Notes: 1. Includes the current consumption on VDDANA.

7.5 I/O Pin Characteristics

Table 7-6. Normal I/O Pin Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance			15		kOhm
$R_{PULLDOWN}$	Pull-down resistance			10		kOhm
V_{IL}	Input low-level voltage				0.8	V
V_{IH}	Input high-level voltage		2.0			V
V_{OL}	Output low-level voltage	I_{OL} = -3.5mA for pad drive x1[1]			0.4	V
		I_{OL} = -7mA for pad drive x2[1]				
		I_{OL} = -14mA for pad drive x4[1]				
V_{OH}	Output high-level voltage	I_{OL} = 3.5mA for pad drive x1[1]	V_{DDIO} - 0.7			V
		I_{OL} = 7mA for pad drive x2[1]				
		I_{OL} = 14mA for pad drive x4[1]				
f_{MAX}	Output frequency	V_{VDDIO} = 3.0V, load = 10pF			TBD	MHz
		V_{VDD} = 3.0V, load = 30pF			TBD	MHz
		V_{VDDIO} =4.5V, load = 10pF			TBD	MHz
		V_{VDD} = 4.5V, load = 30pF			TBD	MHz
t_{RISE}	Rise time	V_{VDD} = 3.0V, load = 10pF			TBD	ns
		V_{VDD} = 3.0V, load = 30pF			TBD	ns
		V_{VDDIO} =4.5V, load = 10pF			TBD	ns
		V_{VDD} = 4.5V, load = 30pF			TBD	ns
t_{FALL}	Fall time	V_{VDD} = 3.0V, load = 10pF			TBD	ns
		V_{VDD} = 3.0V, load = 30pF			TBD	ns
		V_{VDDIO} =4.5V, load = 10pF			TBD	ns
		V_{VDD} = 4.5V, load = 30pF			TBD	ns
I_{LEAK}	Input leakage current	Pull-up resistors disabled			TBD	µA
C_{IN}	Input capacitance				TBD	pF

Note: 1. All PA, PB, PC, PD pins have drive x1/x2 capabilities except PB00, PB01, PB02, PB03, PB30, PB31, PC02, PC03, PC04, PC05, PC06, PC07 which have drive x1 capability and PB06, PB21, PB26, PD02, PD06, PD13 which have drive x2/x4 capabilities. The drive strength is programmable through ODCR0, ODCR0S, ODCR0C, ODCR0T registers of GPIO.

7.6 Oscillator Characteristics

7.6.1 Oscillator (OSC0 and OSC1) Characteristics

7.6.1.1 Digital Clock Characteristics

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN0 or XIN1.

Table 7-7. Digital Clock Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CPXIN}	XIN clock frequency				50	MHz
t_{CPXIN}	XIN clock duty cycle		40		60	%
$t_{STARTUP}$	Startup time			0		cycles
C_{IN}	XIN input capacitance			TBD		pF

7.6.1.2 Crystal Oscillator Characteristics

The following table describes the characteristics for the oscillator when a crystal is connected between XIN and XOUT as shown in Figure 7-2. The user must choose a crystal oscillator where the crystal load capacitance C_L is within the range given in the table. The exact value of C_L can be found in the crystal datasheet. The capacitance of the external capacitors (C_{LEXT}) can then be computed as follows:

$$C_{LEXT} = 2(C_L - C_i) - C_{PCB}$$

where C_{PCB} is the capacitance of the PCB and C_i is the internal equivalent load capacitance.

Figure 7-2. Oscillator Connection
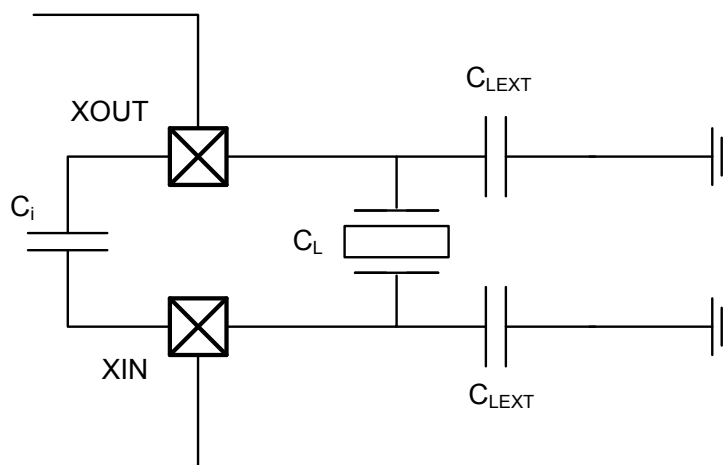
Table 7-8. Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Crystal oscillator frequency		0.4[1]		20[1]	MHz
C_L	Crystal load capacitance			12		pF
C_i	Internal equivalent load capacitance			2		pF
$t_{STARTUP}$	Startup time			TBD		cycles
I_{OSC}	Current consumption			TBD		µA

Notes: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

7.6.2 32KHz Crystal Oscillator (OSC32K) Characteristics

7.6.2.1 Digital Clock Characteristics

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN32.

Table 7-9. Digital 32KHz Clock Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CPXIN}	XIN32 clock frequency			32 768		Hz
t_{CPXIN}	XIN32 clock duty cycle		TBD		TBD	%
$t_{STARTUP}$	Startup time			TBD		cycles
C_{IN}	XIN32 input capacitance			TBD		pF

7.6.2.2 Crystal Oscillator Characteristics

Figure 7-2 and the equation above also applies to the 32KHz oscillator connection. The user must choose a crystal oscillator where the crystal load capacitance C_L is within the range given in the table. The exact value of C_L can then be found in the crystal datasheet..

Table 7-10. 32 KHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Crystal oscillator frequency			32 768		Hz
$t_{STARTUP}$	Startup time	R_S = TBDkOhm, C_L = TBDpF		TBD		cycles
C_L	Crystal load capacitance		TBD		TBD	pF
C_i	Internal equivalent load capacitance			TBD		pF
I_{OSC32}	Current consumption			TBD		µA
R_S	Equivalent series resistance	32 768Hz	TBD		TBD	kOhm

7.6.3 120 MHz RC Oscillator (RC120M) Characteristics

Table 7-11. Internal 120 MHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency		TBD	120[1]	TBD	MHz
I_{RC120M}	Current consumption			1.85[1]		mA
$t_{STARTUP}$	Startup time	$V_{VDDCORE}$ = 1.8 V		3[1]		µs

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

7.6.4 System RC Oscillator (RCSYS) Characteristics

Table 7-12. System RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency		TBD	115[1]	TBD	kHz

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

7.6.5 8MHz/1MHz RC Oscillator (RC8M) Characteristics

Table 7-13. 8MHz/1MHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency	SCIF.RCCR8.FREQMODE = 0[2]	TBD	8[1]	TBD	MHz
		SCIF.RCCR8.FREQMODE = 1[2]	TBD	1[1]	TBD	MHz

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.
2. Please refer to the SCIF chapter for details.

7.6.6 Phase Lock Loop (PLL0 and PLL1) Characteristics

Table 7-14. PLL Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{VCO}	Output frequency		80		240	MHz
f_{IN}	Input frequency		4		16	MHz
I_{PLL}	Current consumption			500		µA

7.7 Flash Characteristics

Table 7-15 gives the device maximum operating frequency depending on the number of flash wait states. The FSW bit in the FLASHC FSR register controls the number of wait states used when accessing the flash memory.

Table 7-15. Maximum Operating Frequency

Flash Wait States	Read Mode	Maximum Operating Frequency
0	1 cycle	33 MHz
1	2 cycles	66 MHz

Table 7-16. Flash Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{FPP}	Page programming time	$f_{CLK\_HSB} = 66\,MHz$		4		ms
t_{FPE}	Page erase time			4		
t_{FFP}	Fuse programming time			TBD		
t_{FEA}	Full chip erase time (EA)			8		
t_{FCE}	JTAG chip erase time (CHIP_ERASE)	$f_{CLK\_HSB} = 115\,kHz$		TBD		

Table 7-17. Flash Endurance and Data Retention

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{FARRAY}	Array endurance (write/page)		100k			cycles
N_{FFUSE}	General Purpose fuses endurance (write/bit)		10k			cycles
t_{RET}	Data retention		15			years

7.8 Analog Characteristics

7.8.1 1.8V Voltage Regulator Characteristics

Table 7-18. 1.8V Voltage Regulator Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{VDDIN_5}	Input voltage range	5V range		5		V
		3V range		3.3		V
$V_{VDDCORE}$	Output voltage, calibrated value			1.85		V
I_{OUT}	DC output current	Normal mode			TBD	mA
		Low power mode			TBD	mA
I_{VREG}	Static current of regulator	Normal mode		TBD		µA
		Low power mode		TBD		µA

Table 7-19. Decoupling Requirements

Symbol	Parameter	Condition	Typ	Techno.	Units
C_{IN1}	Input regulator capacitor 1		470	NPO	nF
C_{IN2}	Input regulator capacitor 2		2.2	X7R	nF
C_{OUT1}	Output regulator capacitor 1		470	NPO	µF
C_{OUT2}	Output regulator capacitor 2		2.2	X7R	nF

7.8.2 3.3V Voltage Regulator Characteristics

Table 7-20. 3.3V Voltage Regulator Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{VDDIN_5}	Input voltage range			5		V
V_{VDDIN_33}	Output voltage, calibrated value			3.3		V
I_{OUT}	DC output current	Normal mode			TBD	mA
		Low power mode			TBD	mA
I_{VREG}	Static current of regulator	Normal mode		TBD		µA
		Low power mode		TBD		µA

7.8.3   1.8V Brown Out Detector (BOD18) Characteristics

The values in Table 7-21 describe the values of the BODLEVEL in the flash General Purpose Fuse register.

Table 7-21.   BODLEVEL Values

BODLEVEL Value	Parameter	Min	Typ[1]	Max	Units
0			1.40		V
20			1.50		V
26	threshold at power-up sequence		1.57		V
28			1.60		V
32			1.65		V
36			1.70		V
40			1.75		V
44			1.80		V
52			1.90		V
58			1.95		V
64			2.00		V

Notes: 1.   These values are guaranteed by design and will be updated after characterization of current silicon.

7.8.4   3.3V Brown Out Detector (BOD33) Characteristics

The values in Table 7-23 describe the values of the BOD33.LEVEL field in the SCIF module.

Table 7-23.   BOD33.LEVEL Values

BOD33.LEVEL Value	Parameter	Min	Typ[1]	Max	Units
3			2.10		V
6			2.20		V
11			2.30		V
17			2.40		V
22			2.50		V
27			2.60		V
31	threshold at power-up sequence		2.63		V
33			2.70		V
39			2.80		V
44			2.90		V
49			3.00		V
53			3.10		V
60			3.20		V

Notes: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

7.8.5 5V Brown Out Detector (BOD50) Characteristics

The values in Table 7-25 describe the values of the BOD50.LEVEL field in the SCIF module.

Table 7-25. BOD50.LEVEL Values

BOD50.LEVEL Value	Parameter	Min	Typ[1]	Max	Units
7			3.25		V
16			3.50		V
25			3.75		V
35			4.00		V
44			4.25		V
53			4.50		V
61			4.75		V

Notes: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

7.8.6 Analog to Digital Converter (ADC) Characteristics

Table 7-27. Channel Conversion Time and ADC Clock

Parameter	Conditions	Min	Typ	Max	Units
ADC clock frequency	12-bit resolution mode - VDDANA = 5V			1.5[1]	MHz
	10-bit resolution mode - VDDANA = 5V			2[1]	MHz
	8-bit resolution mode - VDDANA = 5V			TBD	MHz
	12-bit resolution mode - VDDANA = 3.3V			1.2[1]	MHz
	10-bit resolution mode - VDDANA = 3.3V			1.6[1]	MHz
	8-bit resolution mode - VDDANA = 3.3V			TBD	MHz
Startup time	Return from idle mode			TBD	µs
Conversion time	12-bit resolution mode ADC clock = 1.5 MHz - VDDANA = 5V		8		ADC clock
	10-bit resolution mode ADC clock = 2MHz - VDDANA = 5V		7		ADC clock
	8-bit resolution mode ADC clock = TBD - VDDANA = 5V		6		ADC clock
	12-bit resolution mode ADC clock = 1.2 MHz - VDDANA = 3V		8		ADC clock
	10-bit resolution mode ADC clock = 1.6MHz - VDDANA = 3V		7		ADC clock
	8-bit resolution mode ADC clock = TBD - VDDANA = 3V		6		ADC clock
Throughput rate	12-bit resolution ADC clock = 1.5 MHz - VDDANA = 5V			1.5	MSPS
	10-bit resolution ADC clock = 2 MHz - VDDANA = 5V			2	MSPS
	12-bit resolution ADC clock = 1.2 MHz - VDDANA = 3V			1.2	MSPS
	10-bit resolution ADC clock = 1.6 MHz - VDDANA = 3V			1.6	MSPS

Notes: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

Table 7-28. Reference Voltage

Parameter	Conditions	Min	Typ	Max	Units
ADCREF0/ADCREF1 input voltage range	5V Range	1[1]		3.5[1]	V
	3V Range	1[1]		V_{VDDANA}-0.7[1]	V
ADCREF0/ADCREF1 average current	TBD			TBD	µA
Internal 1V reference			1.0[1]		V
Internal 0.6*VDDANA reference			0.6*V_{VDDANA}[1]		V

Notes: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

Table 7-29. Decoupling requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Units
$C_{ADCREFPN}$	ADCREFP-ADCREFN capacitance			100			nF

Table 7-30. ADC Inputs

Parameter	Conditions	Min	Typ	Max	Units
ADC input voltage range		0[1]		V_{VDDANA}[1]	
Input leakage current			1		μA
External source impedance	ADC used without S/H			1	kΩ
	ADC used with S/H			3	kΩ

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

Table 7-31. Transfer Characteristics 12-bit Resolution Mode

Parameter	Conditions	Min	Typ	Max	Units
Resolution	Differential mode			12[1]	Bit
	Single-ended mode			11[1]	Bit
Integral Non-Linearity (INL)				TBD	LSB
Differential Non-Linearity (DNL)				TBD	LSB
Offset error				TBD	LSB
Gain error				TBD	LSB

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

7.8.6.1 ADC S/H Characteristics

Table 7-32. Channel Conversion Time and ADC Clock

Parameter	Conditions	Min	Typ	Max	Units
Gain			1 to 64[1]		
Resolution	Gain = 1 with calibration		11[1]		bits
	Gain not equal to 1			9[1]	bits
clock frequency				1.5[1]	MHz

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

7.8.7 Digital to Analog Converter (DAC) Characteristics

Table 7-33. Channel Conversion Time and DAC Clock

Parameter	Conditions	Min	Typ	Max	Units
Startup time				TBD	µs
Throughput rate	12-bit resolution One S/H			1[1]	MSPS
	12-bit resolution Two S/H			0.750[1]	MSPS

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

Table 7-34. External Voltage Reference Input

Parameter	Conditions	Min	Typ	Max	Units
DACREF input voltage range		1[1]		TBD	V
DACREF input capacitance		1[1]		TBD	pF
DACREF input resistance		1[1]		TBD	kΩ
DACREF average current				TBD	µA
Current consumption on VDDANA				TBD	mA

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

Table 7-35. DAC Outputs

Parameter	Min	Typ	Max	Units
Output range	0[1]		V_{DACREF}[1][2]	
Output settling time			TBD	µs
Output capacitance			TBD	pF
Output resistance			TBD	kΩ

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

2. DACREF corresponds to the internal or external DAC reference voltage depending on the DACREF settings

Table 7-36. Transfer Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Resolution	Differential mode			12[1]	Bit
Integral Non-Linearity (INL)				TBD	LSB
Differential Non-linearity (DNL)				TBD	LSB
Offset error				TBD	LSB
Gain error				TBD	LSB
Calibrated Gain/Offset error				TBD	LSB

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

7.8.8 Analog Comparator Characteristics

Table 7-37. Analog Comparator Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Positive input voltage range		0		V$_{VDDANA}$	V
Negative input voltage range		0		V$_{VDDANA}$	V
Offset			+/-5[1]	TBD	mV
Hysteresis	No			TBD	mV
	Low		20[1]	TBD	mV
	High		50[1]	TBD	mV
Propagation delay	High Speed mode			TBD	ns
	Low Speed mode			TBD	ns
Current consumption on VDDANA	High Speed mode			170[1]	µA
	Low Speed mode			23[1]	µA
Start-up time				10[1]	µs

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

7.9 Timing Characteristics

7.9.1 Startup, Reset, and Wake-up Timing

The startup, reset, and wake-up timings are calculated using the following formula:

$$t = t_{CONST} + N_{CPU} \times t_{CPU}$$

Where t_{CONST} and N_{CPU} are found in Table 7-38. t_{CPU} is the period of the CPU clock. If another clock source than RCSYS is selected as CPU clock the startup time of the oscillator, $t_{OSCSTART}$, must added to the wake-up time in the stop, deepstop, and static sleep modes. Please refer to the source for the CPU clock in the for more details about oscillator startup times.

Table 7-38. Maximum Reset and Wake-up Timing[1]

Parameter		Measuring	Max t_{CONST} (in µs)	Max N_{CPU}
Startup time from power-up, using regulator		VDDIN_5 rising (TBD V/ms) Time from VDDIN_5=0 to the first instruction entering the decode stage of CPU. VDDCORE is supplied by the internal regulator.	TBD	0
Startup time from reset release		Time from releasing a reset source (except POR, BOD18, and BOD33) to the first instruction entering the decode stage of CPU.	1240[1]	0
Wake-up	Idle	From wake-up event to the first instruction of an interrupt routine entering the decode stage of the CPU.	0	TBD
	Frozen		0	TBD
	Standby		0	TBD
	Stop		TBD	TBD
	Deepstop		TBD	TBD
	Static		TBD	TBD

Note: 1. These values are guaranteed by design and will be updated after characterization of current silicon.

7.9.2 RESET_N characteristics

Table 7-39. RESET_N Clock Waveform Parameters

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{RESET}	RESET_N minimum pulse length		2 * T_{RCSYS}			clock cycles

8. Mechanical Characteristics

8.1 Thermal Considerations

8.1.1 Thermal Data

Table 8-1 summarizes the thermal resistance data depending on the package.

Table 8-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	No air flow	TQFP64	TBD	·C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP64	TBD	
θ_{JA}	Junction-to-ambient thermal resistance	No air flow	TQFP100	39.3	·C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP100	8.5	
θ_{JA}	Junction-to-ambient thermal resistance	No air flow	LQFP144	38.1	·C/W
θ_{JC}	Junction-to-case thermal resistance		LQFP144	8.4	

8.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 8-1 on page 68.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 8-1 on page 68.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in the section "Power Consumption" on page 51.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

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8.2 Package Drawings

Figure 8-1. QFN-64 package drawing
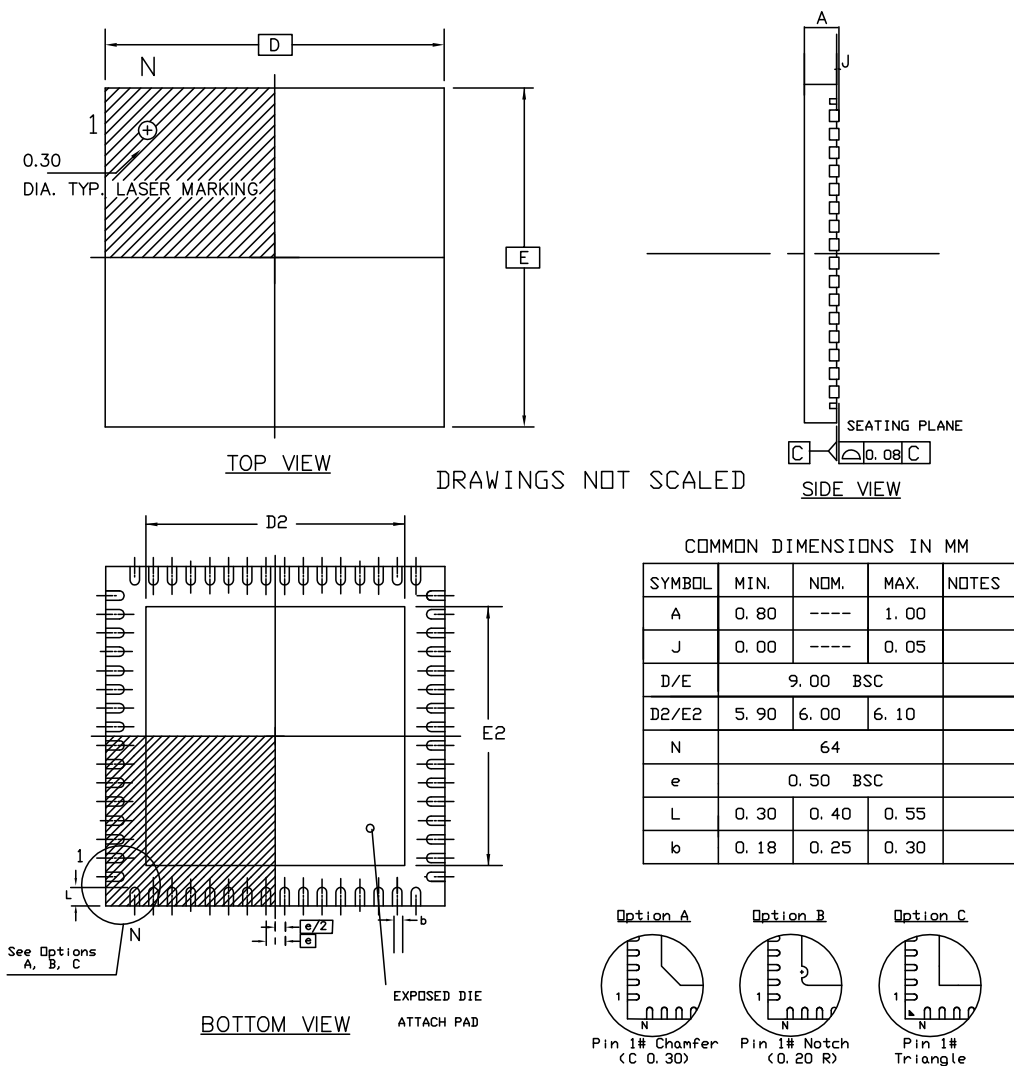
Note: The exposed pad is not connected to anything.

Table 8-2. Device and Package Maximum Weight

TBD	mg

Table 8-3. Package Characteristics

Moisture Sensitivity Level	Jdec J-STD0-20D - MSL 3

Table 8-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 8-2. TQFP-64 package drawing
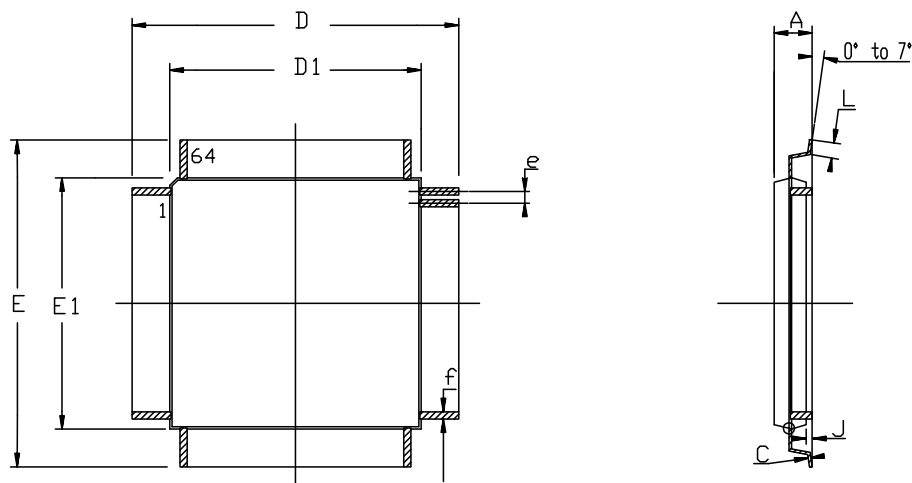
COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	
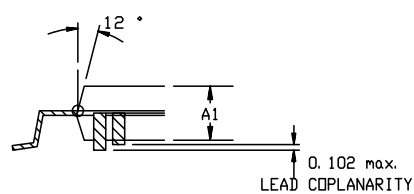
Table 8-5. Device and Package Maximum Weight

TBD	mg

Table 8-6. Package Characteristics

Moisture Sensitivity Level	Jdec J-STD0-20D - MSL 3

Table 8-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 8-3. TQFP-100 package drawing
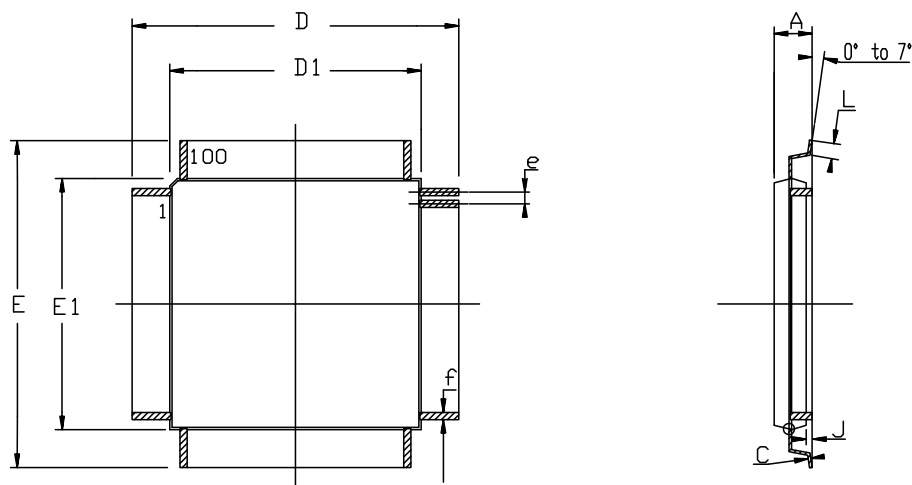
COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	
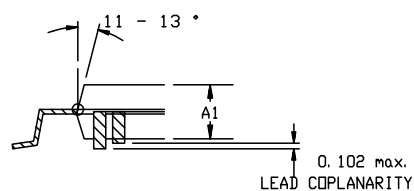
Table 8-8. Device and Package Maximum Weight

500	mg

Table 8-9. Package Characteristics

Moisture Sensitivity Level	Jdec J-STD0-20D - MSL 3

Table 8-10. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 8-4. LQFP-144 package drawing
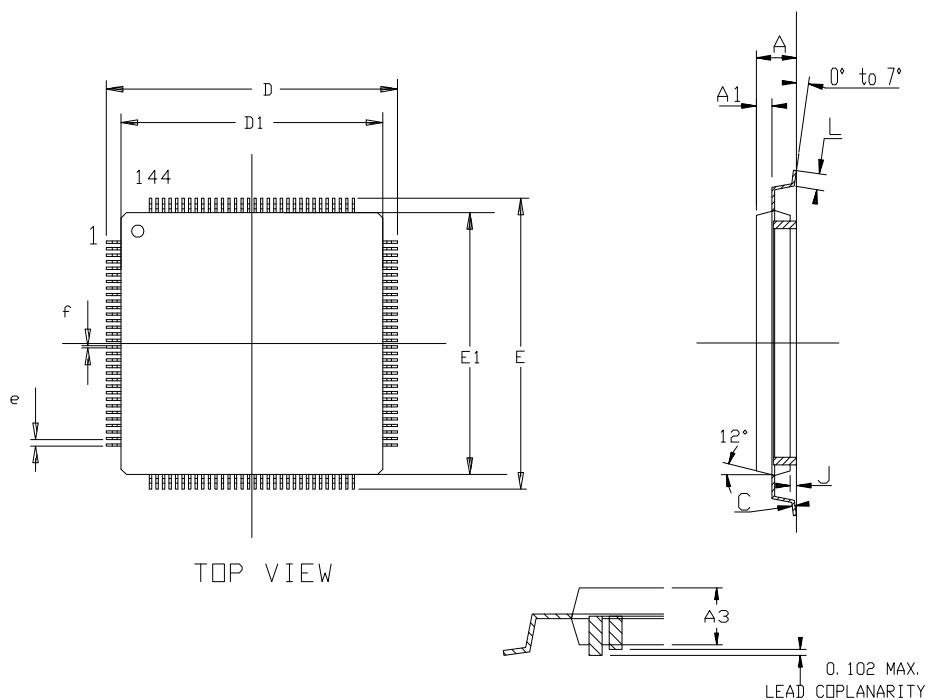
	Min	MM Nom	Max	Min	INCH Nom	Max
A	–	–	1.60	–	–	.063
C	0.09	–	0.20	.004	–	.008
A3	1.35	1.40	1.45	.053	.055	.057
D	21.90	22.00	22.10	.862	.866	.870
D1	19.90	20.00	20.10	.783	.787	.791
E	21.90	22.00	22.10	.862	.866	.870
E1	19.90	20.00	20.10	.783	.787	.791
J	0.05	–	0.15	.002	–	.006
L	0.45	0.60	0.75	.018	.024	.030
e	0.50 BSC			.0197 BSC		
f	0.22 BSC			.009 BSC		

Table 8-11. Device and Package Maximum Weight

1300	mg

Table 8-12. Package Characteristics

Moisture Sensitivity Level	Jdec J-STD0-20D - MSL 3

Table 8-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.3   Soldering Profile

Table 8-14 gives the recommended soldering profile from J-STD-20.

Table 8-14.   Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/sec
Preheat Temperature 175°C ±25°C	Min. 150 °C, Max. 200 °C
Temperature Maintained Above 217°C	60-150 sec
Time within 5·C of Actual Peak Temperature	30 sec
Peak Temperature Range	260 °C
Ramp-down Rate	6 °C/sec
Time 25·C to Peak Temperature	Max. 8 minutes

Note: It is recommended to apply a soldering temperature higher than 250°C.

A maximum of three reflow passes is allowed per component.

9. Ordering Information

Table 9-1. Ordering Information

Device	Ordering Code	Carrier Type	Package	Temperature Operating Range
AT32UC3C0512C	AT32UC3C0512C-ALUES	ES		
	AT32UC3C0512C-ALUT	Tray		
	AT32UC3C0512C-ALUR	Tape & Reel		
AT32UC3C0256C	AT32UC3C0256C-ALUT	Tray	LQFP 144	
	AT32UC3C0256C-ALUR	Tape & Reel		
AT32UC3C0128C	AT32UC3C0128C-ALUT	Tray		
	AT32UC3C0128C-ALUR	Tape & Reel		
AT32UC3C064C	AT32UC3C064C-ALUT	Tray		
	AT32UC3C064C-ALUR	Tape & Reel		
AT32UC3C1512C	AT32UC3C1512C-AUES	ES		
	AT32UC3C1512C-AUT	Tray		
	AT32UC3C1512C-AUR	Tape & Reel		
AT32UC3C1256C	AT32UC3C1256C-AUT	Tray	TQFP 100	
	AT32UC3C1256C-AUR	Tape & Reel		
AT32UC3C1128C	AT32UC3C1128C-AUT	Tray		
	AT32UC3C1128C-AUR	Tape & Reel		
AT32UC3C164C	AT32UC3C164C-AUT	Tray		Industrial (-40°C to 85°C)
	AT32UC3C164C-AUR	Tape & Reel		
AT32UC3C2512C	32UC3C2512C-A2UES	ES		
	32UC3C2512C-A2UT	Tray	TQFP 64	
	32UC3C2512C-A2UR	Tape & Reel		
	32UC3C2512C-Z2UES	ES		
	32UC3C2512C-Z2UT	Tray	QFN 64	
	32UC3C2512C-Z2UR	Tape & Reel		
AT32UC3C2256C	32UC3C2256C-A2UT	Tray	TQFP 64	
	32UC3C2256C-A2UR	Tape & Reel		
	32UC3C2256C-Z2UT	Tray	QFN 64	
	32UC3C2256C-Z2UR	Tape & Reel		
AT32UC3C2128C	32UC3C2128C-A2UT	Tray	TQFP 64	
	32UC3C2128C-A2UR	Tape & Reel		
	32UC3C2128C-Z2UT	Tray	QFN 64	
	32UC3C2128C-Z2UR	Tape & Reel		
AT32UC3C264C	32UC3C2128C-A2UT	Tray	TQFP 64	
	32UC3C2128C-A2UR	Tape & Reel		
	32UC3C2128C-Z2UT	Tray	QFN 64	
	32UC3C2128C-Z2UR	Tape & Reel		

When multiple chip selects are in use, if one of the baudrates is equal to 1 (CSRn.SCBR==1) and one of the others is not equal to 1, and CSRn.CPOL==1 and CSRn.NCPHA==0, an additional pulse will be generated on SCK.
Fix/Workaround
When multiple chip selects are in use, if one of the baudrates is equal to 1, the others must also be equal to 1 if CSRn.CPOL==1 and CSRn.NCPHA==0.

3. **SPI data transfer hangs with CSR0.CSAAT==1 and MR.MODFDIS==0**
When CSR0.CSAAT==1 and mode fault detection is enabled (MR.MODFDIS==0), the SPI module will not start a data transfer.
Fix/Workaround
Disable mode fault detection by writing a one to MR.MODFDIS.

4. **Disabling SPI has no effect on the SR.TDRE bit**
Disabling SPI has no effect on SR.TDRE whereas the write data command is filtered when SPI is disabled. This means that as soon as the SPI is disabled it becomes impossible to reset the SR.TDRE bit by writing to TDR. So if the SPI is disabled during a PDCA transfer, the PDCA will continue to write data to TDR (as SR.TDRE stays high) until its buffer is empty, and all data written after the disable command is lost.
Fix/Workaround
Disable the PDCA, add 2 NOP (minimum), and disable the SPI. To continue the transfer, enable the SPI and the PDCA.

10.1.5   TWI

1. **TWIM SMBAL polarity is wrong**
The SMBAL signal in the TWIM is active high instead of active low.
Fix/Workaround
Use an external inverter to invert the signal going into the TWIM. When using both TWIM and TWIS on the same pins, the SMBAL cannot be used.

10.1.6   USBC

1. **UPINRQx.INRQ field is limited to 8-bits**
In Host mode, when using the UPINRQx.INRQ feature together with the multi-packet mode to launch a finite number of packet among multi-packet, the multi-packet size (located in the descriptor table) is limited to the UPINRQx.INRQ value multiply by the pipe size.
Fix/Workaround
UPINRQx.INRQ value shall be less than the number of configured multi-packet.

10.1.7   WDT

1. **Clearing the Watchdog Timer (WDT) counter in second half of timeout period will issue a Watchdog reset**
If the WDT counter is cleared in the second half of the timeout period, the WDT will immediately issue a Watchdog reset.
Fix/Workaround
Use twice as long timeout period as needed and clear the WDT counter within the first half of the timeout period. If the WDT counter is cleared after the first half of the timeout period, you will get a Watchdog reset immediately. If the WDT counter is not cleared at all, the time before the reset will be twice as long as needed.

11. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

11.1 Rev. A – 10/10

1   Initial revision

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