BG96 Hardware Design

LTE Module Series

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Quectel Wireless Solutions Co., Ltd.
7th Floor, Hongye Building, No.1801 Hongmei Road, Xuhui District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local office. For more information, please visit:
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About the Document

History

Revision	Date	Author	Description
1.0	2017-08-04	Lyndon LIU/ Daryl DU	Initial
1.1	2017-08-31	Daryl DU	1. Modified GSM features in Table 2. 2. Added a note for e-I-DRX in Chapter 3.3. 3. Elaborated the description of e-I-DRX in Chapter 3.4.3. 4. Updated RF receiving sensitivity in Chapter 6.6.
1.2	2017-12-22	Lyndon LIU/ Daryl DU	1. Added the storage temperature of the module in Table 2 and Chapter 6.3. 2. Updated transmitting power values in Table 2. 3. Added the description of sleep mode in Table 5 and Chapter 3.4.4. 4. Added the description of ADC interfaces in Chapter 3.16. 5. Updated the GNSS performance in Table 21. 6. Updated the peak supply current values in Table 28. 7. Updated the current consumption values in Chapter 6.4. 8. Updated RF output power values in Table 34. 9. Updated LTE Cat NB1 RF receiving sensitivity values (without repetitions) in Table 35. 10. Updated the recommended footprint in Chapter 7.2.

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1 Introduction

This document defines BG96 module and describes its air interface and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand the interface specifications, electrical and mechanical details, as well as other related information of BG96. To facilitate its application in different fields, reference design is also provided for customers' reference. Associated with application note and user guide, customers can use the module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating BG96. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden, so as to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers an Airplane Mode which must be enabled prior to boarding an aircraft.
	Switch off your wireless device when in hospitals, clinics or other health care facilities. These requests are designed to prevent possible interference with sensitive medical equipment.
	Cellular terminals or mobiles operating over radio frequency signal and cellular network cannot be guaranteed to connect in all conditions, for example no mobile fee or with an invalid (U)SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.
	Your cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

BG96 is an embedded IoT (LTE Cat M1, LTE Cat NB1 and EGPRS) wireless communication module. It provides data connectivity on LTE-TDD/LTE-FDD/GPRS/EDGE networks, and supports half-duplex operation in LTE networks. It also provides GNSS[1)] and voice functionality[2)] to meet customers' specific application demands. The following table shows the frequency bands of BG96 module.

Table 1: Frequency Bands of BG96 Module

Module	LTE Bands	GSM [3)]	Rx-diversity	GNSS [1)]
BG96	**Cat M1 & NB1:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/ B13/B18/B19/B20/B26/B28 LTE-TDD: B39 (for Cat M1 only)	GSM850/GSM900/ DCS1800/PCS1900	Not Supported	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS

NOTES

1. [1)] GNSS function is optional.
2. [2)] BG96 supports VoLTE (Voice over LTE) under LTE Cat M1 network.
3. [3)] BG96 GSM only supports Packet Switch.

With a compact profile of 22.5mm × 26.5mm × 2.3mm, BG96 can meet almost all requirements for M2M applications such as smart metering, tracking system, security, wireless POS, etc.

BG96 is an SMD type module which can be embedded into applications through its 102 LGA pads. BG96 supports internet service protocols like TCP, UDP and PPP. Extended AT commands have been developed for customers to use these internet service protocols easily.

2.2. Key Features

The following table describes the detailed features of BG96 module.

Table 2: Key Features of BG96 Module

Features	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for GSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for GSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK
LTE Features	Support LTE Cat M1 and LTE Cat NB1 Support 1.4MHz RF bandwidth for LTE Cat M1 Support 200KHz RF bandwidth for LTE Cat NB1 Support SISO in DL direction Cat M1: Max. 300Kbps (DL)/375Kbps (UL) Cat NB1: Max. 32Kbps (DL)/70Kbps (UL)
GSM Features	**GPRS:** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max. 107Kbps (DL), Max. 85.6Kbps (UL) **EDGE:** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max. 296Kbps (DL), Max. 236.8Kbps (UL)
Internet Protocol Features	Support PPP/TCP/UDP/SSL/TLS/FTP(S)/HTTP(S) protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connections
SMS	Text and PDU mode

	Point to point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interface	Support USIM/SIM card: 1.8V, 3.0V
Audio Feature*	Support one digital audio interface: PCM interface
USB Interface	Compliant with USB 2.0 specification (slave only) and the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NEMA output, software debugging and firmware upgrade Support USB drivers for Windows XP, Windows Vista, Windows 7, Windows 8/8.1, Windows 10, Windows CE 5.0/6.0/7.0, Linux 2.6/3.x/4.1, Android 4.x/5.x/6.x/7.x
UART Interfaces	**UART1:** Used for data transmission and AT command communication 115200bps by default The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) Support RTS and CTS hardware flow control **UART2:** Used for module debugging and log output 115200bps baud rate **UART3:** Used for outputting GNSS data or NEMA sentences 115200bps baud rate
AT Commands	3GPP TS 27.007 and 3GPP TS 27.005 AT commands, as well as Quectel enhanced AT commands
Network Indication	One NETLIGHT pin for network connectivity status indication
Antenna Interfaces	Including main antenna (ANT_MAIN) and GNSS antenna (ANT_GNSS) interfaces
Physical Characteristics	Size: (22.5±0.15)mm × (26.5±0.15)mm × (2.3±0.2)mm Weight: approx. 3.1g
Temperature Range	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	USB interface, DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. "*" means under development.
2. [1)] Within operation temperature range, the module is 3GPP compliant.

3. [2] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of BG96 and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

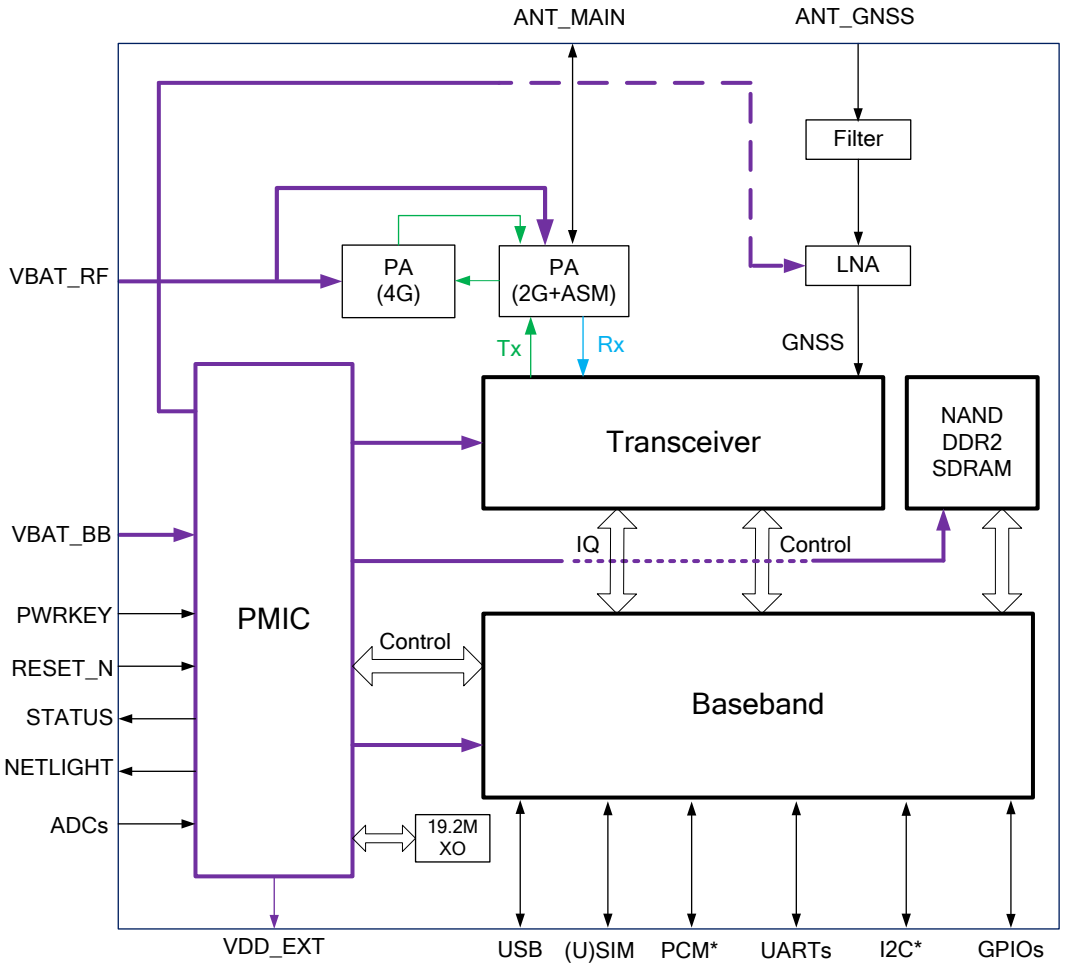


Figure 1: Functional Diagram

NOTE

"*" means under development.

2.4. Evaluation Board

In order to help customers develop applications conveniently with BG96, Quectel supplies the evaluation board (EVB), USB to RS-232 converter cable, USB data cable, earphone, antenna and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

3 Application Interfaces

BG96 is equipped with 102 LGA pads that can be connected to customers' cellular application platforms. The following sub-chapters will provide detailed description of interfaces listed below:

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM* and I2C* interfaces
- Status indication
- USB_BOOT interface
- ADC interfaces*

NOTE

"*" means under development.

3.1. Pin Assignment

The following figure shows the pin assignment of BG96.

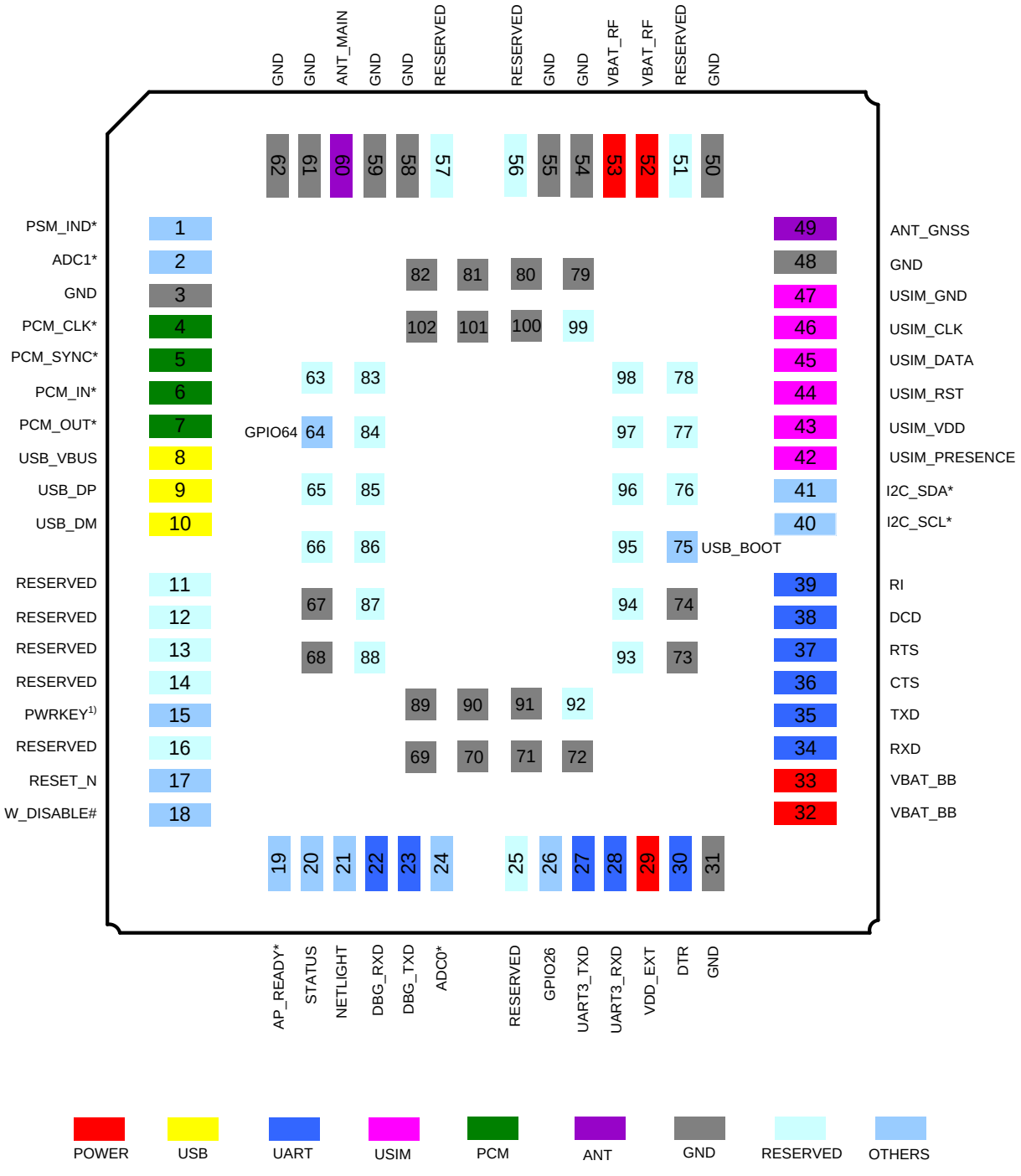


Figure 2: Pin Assignment (Top View)

NOTES

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pads should be connected to ground in the design.
3. [1)] PWRKEY output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
4. "*" means under development.

3.2. Pin Description

The following tables show the pin definition and description of BG96.

Table 3: Definition of I/O Parameters

Type	Description
IO	Bidirectional
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for module's baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	
VBAT_RF	52, 53	PI	Power supply for module's RF part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	

VDD_EXT	29	PO	Provide 1.8V for external circuit	Vnorm=1.8V $I_O$max=50mA	Power supply for external GPIO's pull up circuits.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67~74, 79~82, 89~91, 100~102		Ground		
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	17	DI	Reset signal of the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	If unused, keep this pin open.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicate the module's operation status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep this pin open.
NETLIGHT	21	DO	Indicate the module's network activity status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep this pin open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	PI	USB detection	Vmax=5.25V Vmin=3.0V Vnorm=5.0V	
USB_DP	9	IO	USB differential data bus (+)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.
USB_DM	10	IO	USB differential data bus (-)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.

(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_ PRESENCE	42	DI	(U)SIM card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
USIM_VDD	43	PO	Power supply for (U)SIM card	**For 1.8V (U)SIM:** Vmax=1.9V Vmin=1.7V **For 3.0V (U)SIM:** Vmax=3.05V Vmin=2.7V $I_O$max=50mA	Either 1.8V or 3.0V is supported by the module automatically.
USIM_RST	44	DO	Reset signal of (U)SIM card	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_DATA	45	IO	Data signal of (U)SIM card	**For 1.8V (U)SIM:** V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_CLK	46	DO	Clock signal of (U)SIM card	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_GND	47		Specified ground for (U)SIM card		

UART1 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DTR	30	DI	Data terminal ready(sleep mode control)	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
RXD	34	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
TXD	35	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
CTS	36	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
RTS	37	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
DCD	38	DO	Data carrier detection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
RI	39	DO	Ring indicator	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
UART2 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
DBG_TXD	23	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
UART3 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

UART3_TXD	27	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
UART3_RXD	28	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
PCM* Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK*	4	DO	PCM clock output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
PCM_SYNC*	5	DO	PCM frame synchronization output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
PCM_IN*	6	DI	PCM data input	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
PCM_OUT*	7	DO	PCM data output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
I2C* Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL*	40	OD	I2C serial clock. Used for external codec.		External pull-up resistor is required. 1.8V only. If unused, keep this pin open.
I2C_SDA*	41	OD	I2C serial data. Used for external codec.		External pull-up resistor is required. 1.8V only. If unused, keep this pin open.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	IO	Main antenna interface	50Ω impedance	
ANT_GNSS	49	AI	GNSS antenna interface	50Ω impedance	If unused, keep this pin open.

Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PSM_IND [1)]	1	DO	Power saving mode indicator	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
W_DISABLE#*	18	DI	Airplane mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pull-up by default. In low voltage level, the module can enter into airplane mode. If unused, keep this pin open.
AP_READY*	19	DI	Application processor sleep state detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
USB_BOOT	75	DI	Force the module to enter into emergency download mode	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO26	26	IO	General-purpose input/ output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO64	64	IO	General-purpose input/ output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
ADC Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC1*	2	AI	General purpose analog to digital converter interface	Voltage range: 0.3V to 1.8V	If unused, keep this pin open.

ADC0*	24	AI	General purpose analog to digital converter interface	Voltage range: 0.3V to 1.8V	If unused, keep this pin open.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	11~14, 16, 25, 51, 56, 57, 63, 65, 66, 76~78, 83~88, 92~99		Reserved		Keep these pins unconnected.

NOTES

1. "*" means under development.
2. [1)] When PSM is enabled and then reboot the module, the function of PSM_IND pin will be activated. This pin outputs a high level voltage when the module is in normal operation state, and outputs a low level voltage when the module enters into PSM.
3. Keep all RESERVED pins and unused pins unconnected.

3.3. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Extended Idle Mode DRX (e-I-DRX)	BG96 module and the network may negotiate over non-access stratum signaling the use of e-I-DRX for reducing power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	

Airplane Mode	**AT+CFUN** command or W_DISABLE#* pin can set the module into airplane mode. In this case, RF function will be invalid.
Minimum Functionality Mode	**AT+CFUN** command can set the module into a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.
Sleep Mode	In this mode, the current consumption of the module will be reduced to a lower level. During this mode, the module can still receive paging message, SMS and TCP/UDP data from the network normally.
Power Saving Mode (PSM)	BG96 module may enter into Power Saving Mode for reducing its power consumption. PSM is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections.
Power OFF Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible. But operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

NOTES

1. During e-I-DRX, it is recommended to use UART interface for data communication, as the use of USB interface will increase power consumption.
2. "*" means under development.

3.4. Power Saving

3.4.1. Airplane Mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Hardware:

W_DISABLE#* is pulled up by default. Driving it to low level will let the module enter into airplane mode.

Software:

AT+CFUN=<fun> command provides choice of the functionality level, through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTES

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"** command. The command is still under development.
2. The execution of **AT+CFUN** command will not affect GNSS function.
3. "*" means under development.

3.4.2. Power Saving Mode (PSM)

BG96 module can enter into PSM for reducing its power consumption. The mode is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. So BG96 in PSM cannot immediately respond users' requests.

When the module wants to use the PSM it shall request an Active Time value during every Attach and TAU procedures. If the network supports PSM and accepts that the module uses PSM, the network confirms usage of PSM by allocating an Active Time value to the module. If the module wants to change the Active Time value, e.g. when the conditions are changed in the module, the module consequently requests the value it wants in the TAU procedure.

If PSM is supported by the network, then it can be enabled via **AT+CPSMS** command.

Either of the following methods will wake up the module from PSM:

- Drive PWRKEY pin to low level will wake up the module.
- When the T3412 timer expires, the module will be automatically woken up.

NOTE

Please refer to ***document [2]*** for details about **AT+CPSMS** command.

3.4.3. Extended Idle Mode DRX (e-I-DRX)

The module (UE) and the network may negotiate over non-access stratum signalling the use of e-I-DRX for reducing its power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.

Applications that want to use e-I-DRX need to consider specific handling of mobile terminating services or data transfers, and in particular they need to consider the delay tolerance of mobile terminated data.

In order to negotiate the use of e-I-DRX, the UE requests e-I-DRX parameters during attach procedure and RAU/TAU procedure. The EPC may reject or accept the UE request for enabling e-I-DRX. In case the EPC accepts e-I-DRX, the EPC based on operator policies and, if available, the e-I-DRX cycle length

value in the subscription data from the HSS, may also provide different values of the e-I-DRX parameters than what was requested by the UE. If the EPC accepts the use of e-I-DRX, the UE applies e-I-DRX based on the received e-I-DRX parameters. If the UE does not receive e-I-DRX parameters in the relevant accept message because the EPC rejected its request or because the request was received by EPC not supporting e-I-DRX, the UE shall apply its regular discontinuous reception.

If e-I-DRX is supported by the network, then it can be enabled by **AT+CEDRXS=1** command.

NOTE

Please refer to ***document [2]*** for details about **AT+CEDRXS** command.

3.4.4. Sleep Mode

BG96 is able to reduce its current consumption to a lower value during the sleep mode. The following sub-chapters describe the power saving procedure of BG96 module.

3.4.4.1. UART Application

If the host communicates with module via UART interface, the following preconditions can let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the host.

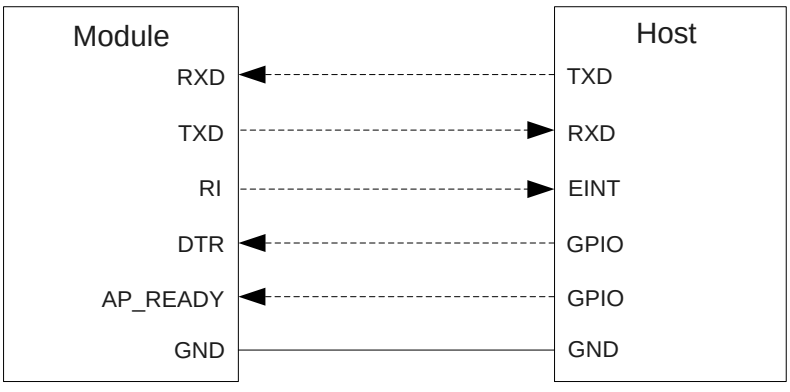


Figure 3: Sleep Mode Application via UART

- Driving the host DTR to low level will wake up the module.
- When BG96 has URC to report, RI signal will wake up the host. Please refer to ***Chapter 3.14*** for details about RI behavior.
- AP_READY will detect the sleep state of the host (can be configured to high level or low level detection). Please refer to **AT+QCFG="apready"** command for details.

NOTE

AT+QCFG="apready" command is under development.

3.5. Power Supply

3.5.1. Power Supply Pins

BG96 provides the following four VBAT pins for connection with an external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's baseband part.

The following table shows the details of VBAT pins and ground pins.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	32, 33	Power supply for module's baseband part	3.3	3.8	4.3	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67~74, 79~82, 89~91, 100~102	Ground	-	-	-	-

3.5.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure that the input voltage will never drop below 3.3V.

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm, and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use a zener diode with reverse zener voltage of 5.1V and dissipation power more than 0.5W, and place it as close to the VBAT pins as possible. The following figure shows the star structure of the power supply.

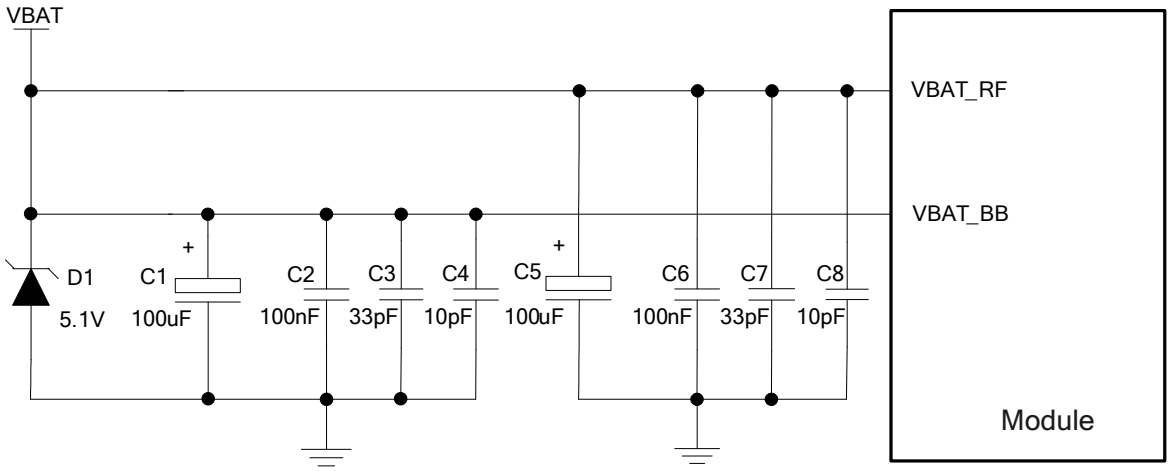


Figure 4: Star Structure of the Power Supply

3.5.3. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. For more details, please refer to ***document [2]***.

3.6. Turn on and off Scenarios

3.6.1. Turn on Module Using the PWRKEY Pin

The following table shows the pin definition of PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	15	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When BG96 is in power off mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 100ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin outputting a high level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

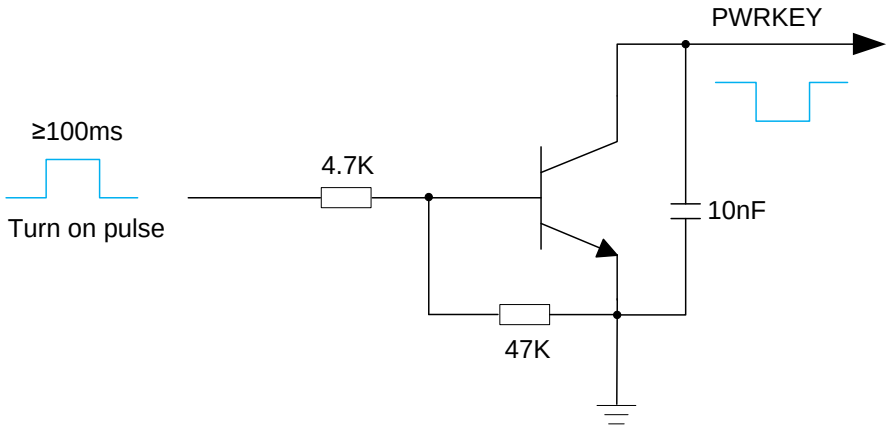


Figure 5: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

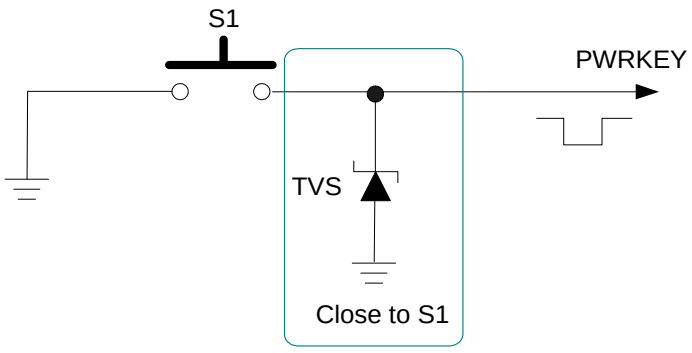


Figure 6: Turn on the Module Using Keystroke

The turn on scenario is illustrated in the following figure.

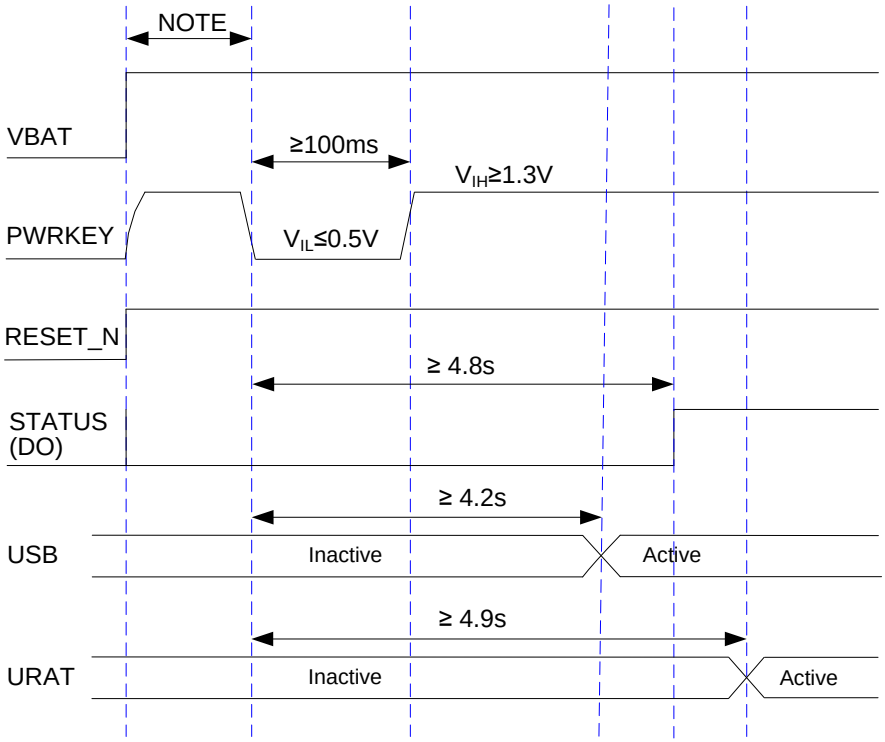


Figure 7: Timing of Turning on Module

NOTE

Make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.

3.6.2. Turn off Module

Either of the following methods can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using **AT+QPOWD** command.

3.6.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after the PWRKEY is released.

The power-down scenario is illustrated in the following figure.

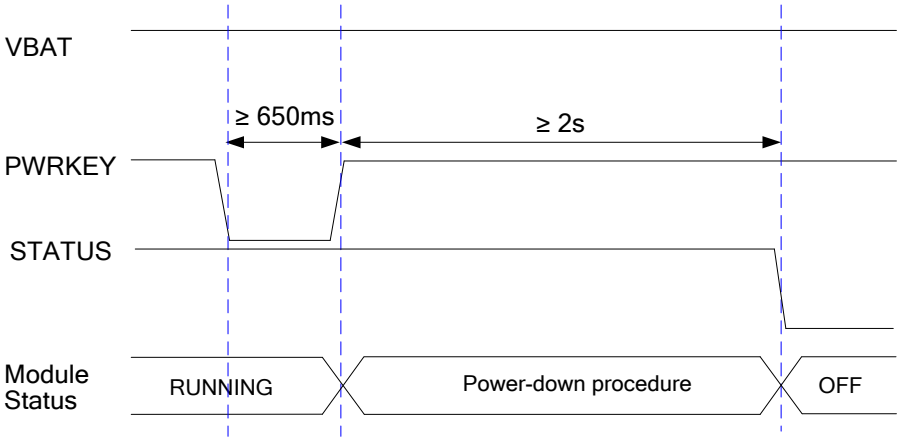


Figure 8: Timing of Turning off Module

3.6.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via PWRKEY pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

3.7. Reset the Module

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N to a low level voltage for time between 150ms and 460ms.

Table 8: RESET_N Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	17	Reset signal of the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

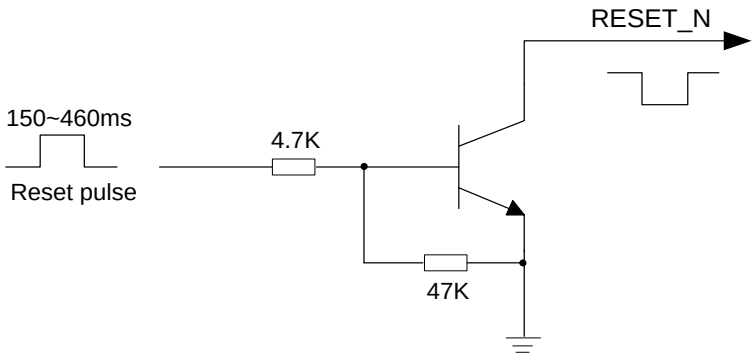


Figure 9: Reference Circuit of RESET_N by Using Driving Circuit

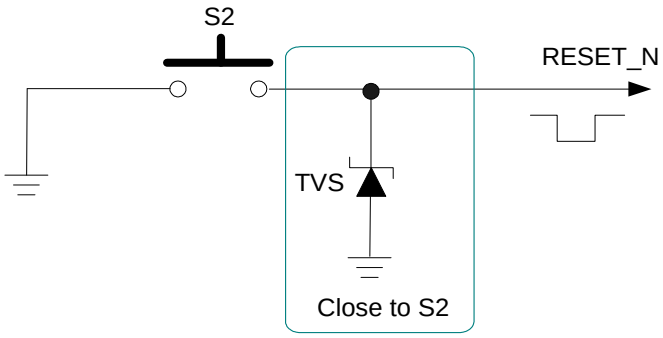


Figure 10: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

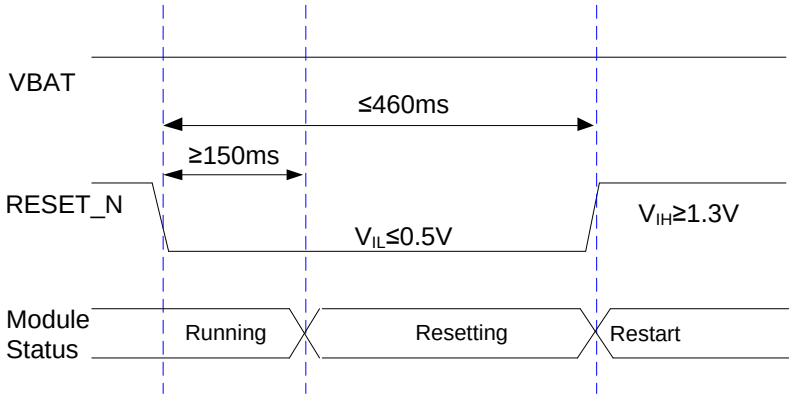


Figure 11: Timing of Resetting Module

NOTES

1. Use RESET_N only when turning off the module by **AT+QPOWD** command and PWRKEY pin both failed.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.8. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 9: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	43	PO	Power supply for (U)SIM card	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	45	IO	Data signal of (U)SIM card	
USIM_CLK	46	DO	Clock signal of (U)SIM card	
USIM_RST	44	DO	Reset signal of (U)SIM card	
USIM_ PRESENCE	42	DI	(U)SIM card insertion detection	
USIM_GND	47		Specified ground for (U)SIM card	

BG96 supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections, and is disabled by default. Please refer to ***document [2]*** about **AT+QSIMDET** command for details.

The following figure shows a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.

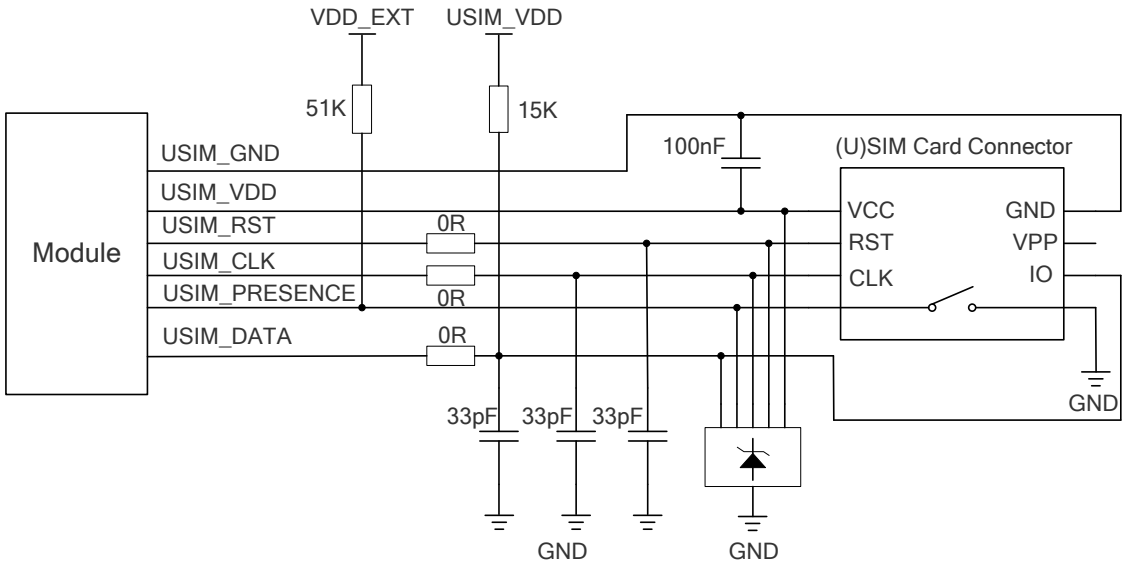


Figure 12: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

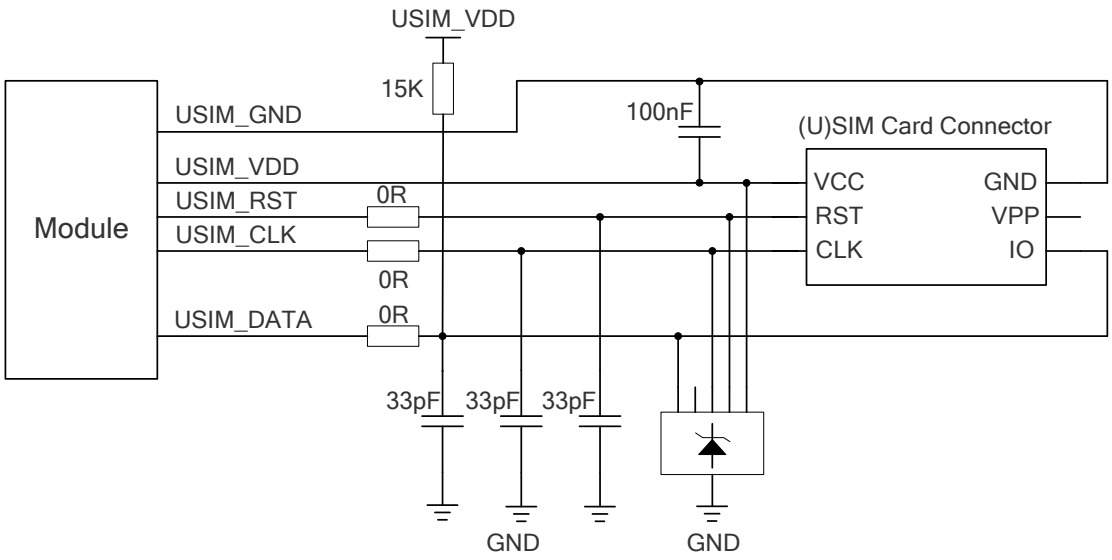


Figure 13: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1uF, and place it as close to (U)SIM card connector as possible. If the system ground plane is complete, USIM_GND can be connected to the system ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground. USIM_RST should also be ground shielded.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 15pF. In order to facilitate debugging, it is recommended to reserve series resistors for the (U)SIM signals of the module. The 33pF capacitors are used for filtering interference of GSM 900MHz. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.9. USB Interface

BG96 contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	PI	USB connection detection	Typically 5.0V
USB_DP	9	IO	USB differential data bus (+)	Require differential impedance of 90Ω
USB_DM	10	IO	USB differential data bus (-)	Require differential impedance of 90Ω
GND	3		Ground	

For more details about USB 2.0 specification, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in customers' designs. The following figure shows a reference circuit of USB interface.

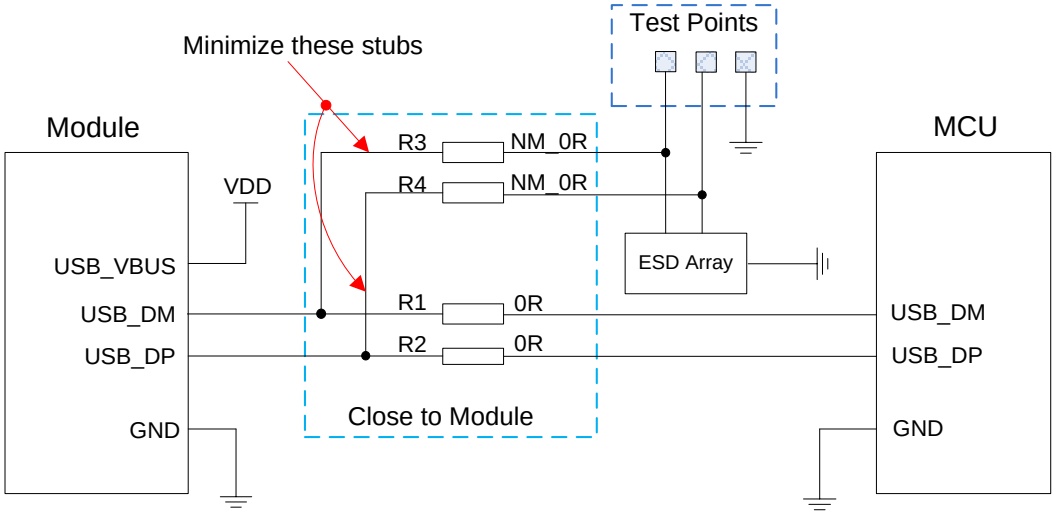


Figure 14: Reference Circuit of USB Application

In order to ensure signal integrity of USB data lines, components R1, R2, R3 and R4 must be placed close to the module, and also should be placed close to each other. The extra stubs of traces must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components as close to the USB connector as possible.

NOTE

BG96 module can only be used as a slave device.

3.10. UART Interfaces

The module provides three UART interfaces: UART1, UART2 and UART3 interfaces. The following are their features.

- UART1 interface supports 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600 baud rates, and the default is 115200bps. It is used for data transmission and AT command communication.
- UART2 interface supports 115200bps baud rate. It is used for module debugging and log output.
- UART3 interface supports 115200bps baud rate. It is used for outputting GNSS data and NEMA sentences.

The following tables show the pin definition of the three UART interfaces.

Table 11: Pin Definition of UART1 Interface

Pin Name	Pin No.	I/O	Description	Comment
DTR	30	DI	Data terminal ready	1.8V power domain
RXD	34	DI	Receive data	1.8V power domain
TXD	35	DO	Transmit data	1.8V power domain
CTS	36	DO	Clear to send	1.8V power domain
RTS	37	DI	Request to send	1.8V power domain
DCD	38	DO	Data carrier detection	1.8V power domain
RI	39	DO	Ring indicator	1.8V power domain

Table 12: Pin Definition of UART2 Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	23	DO	Transmit data	1.8V power domain
DBG_RXD	22	DI	Receive data	1.8V power domain

Table 13: Pin Definition of UART3 Interface

Pin Name	Pin No.	I/O	Description	Comment
UART3_TXD	27	DO	Transmit data	1.8V power domain
UART3_RXD	28	DI	Receive data	1.8V power domain

The logic levels are described in the following table.

Table 14: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interface. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

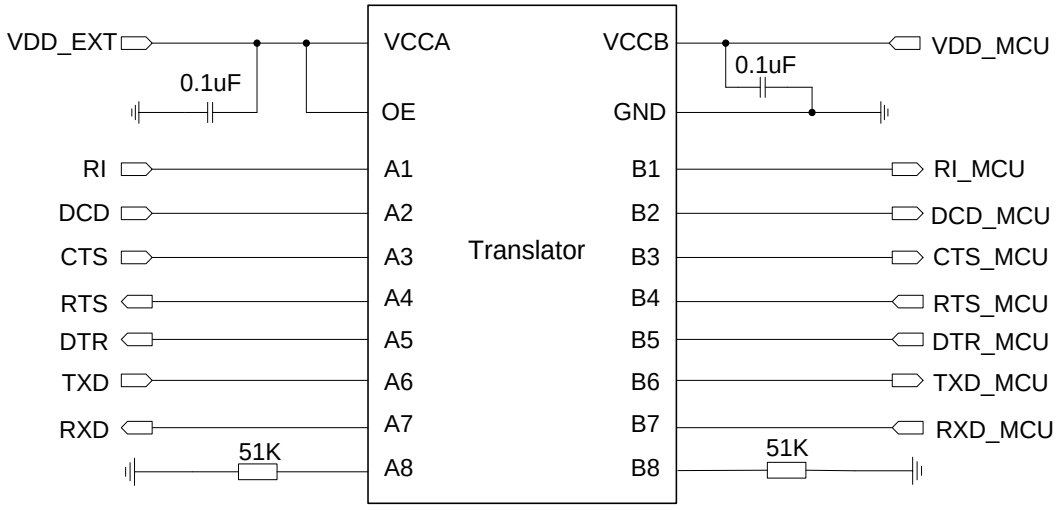


Figure 15: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to that of solid line section, in terms of both module input and output circuit designs, but please pay attention to the direction of connection.

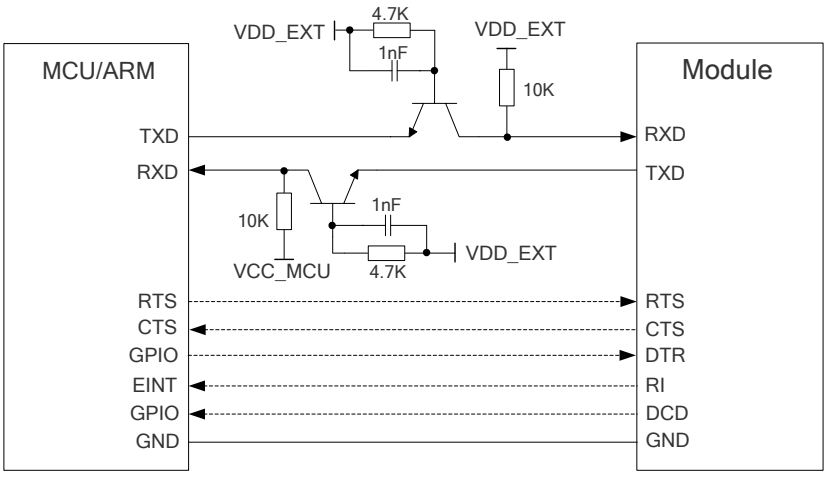


Figure 16: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.11. PCM* and I2C* Interfaces

BG96 provides one Pulse Code Modulation (PCM*) digital interface and one I2C* interface. The following table shows the pin definition of the two interfaces which can be applied on audio codec design.

Table 15: Pin Definition of PCM* and I2C* Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK*	4	DO	PCM clock output	1.8V power domain
PCM_SYNC*	5	DO	PCM frame synchronization output	1.8V power domain
PCM_IN*	6	DI	PCM data input	1.8V power domain
PCM_OUT*	7	DO	PCM data output	1.8V power domain
I2C_SCL*	40	OD	I2C serial clock	Require external pull-up to 1.8V
I2C_SDA*	41	OD	I2C serial data	Require external pull-up to 1.8V

The following figure shows a reference design of PCM* and I2C* interfaces with an external codec IC.

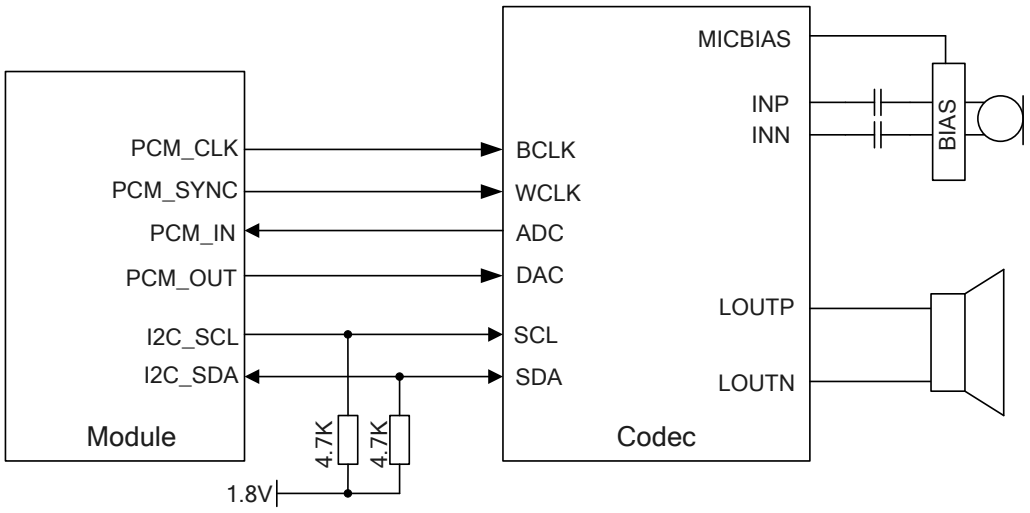


Figure 17: Reference Circuit of PCM Application with Audio Codec

NOTE

"*" means under development.

3.12. Network Status Indication

BG96 provides one network status indication pin: NETLIGHT. The pin is used to drive a network status indication LED. The following tables describe the pin definition and logic level changes of NETLIGHT in different network activity status.

Table 16: Pin Definition of NETLIGHT

Pin Name	Pin No.	I/O	Description	Comment
NETLIGHT	21	DO	Indicate the module's network activity status	1.8V power domain

Table 17: Working State of NETLIGHT

Pin Name	Logic Level Changes	Network Status
NETLIGHT	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always high	Voice calling

A reference circuit is shown in the following figure.

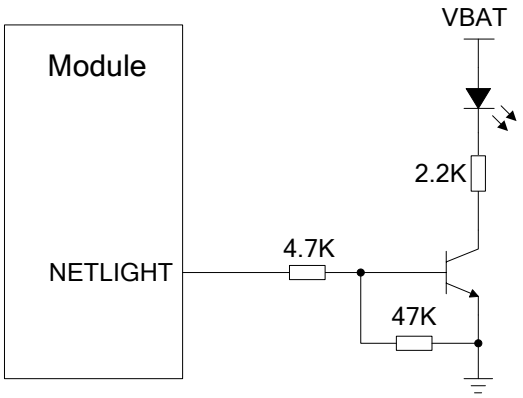


Figure 18: Reference Circuit of the Network Status Indicator

3.13. STATUS

The STATUS pin is used to indicate the operation status of BG96 module. It will output high level when the module is powered on.

The following table describes the pin definition of STATUS.

Table 18: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8V power domain

The following figure shows a reference circuit of STATUS.

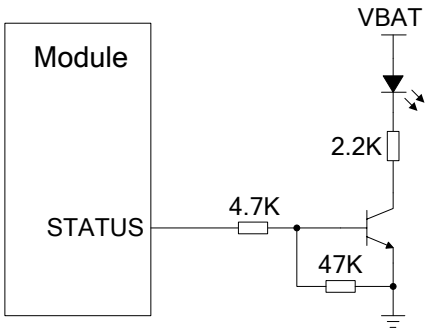


Figure 19: Reference Circuit of STATUS

3.14. Behaviors of RI

AT+QCFG="risignaltype","physical" command can be used to configure RI behavior.

No matter on which port URC is presented, URC will trigger the behavior of RI pin.

NOTE

URC can be outputted from UART port, USB AT port and USB modem port, through configuration via **AT+QURCCFG** command. The default port is USB AT port.

The default behaviors of RI are shown as below.

Table 19: Default Behaviors of RI

State	Response
Idle	RI keeps in high level.
URC	RI outputs 120ms low pulse when new URC returns.

The default RI behaviors can be configured flexibly by **AT+QCFG="urc/ri/ring"** command. For more details, please refer to ***document [2]***.

3.15. USB_BOOT Interface

BG96 provides a USB_BOOT pin. During development or factory production, USB_BOOT can force the module to boot from USB port for firmware upgrade.

Table 20: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module to enter into emergency download mode	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

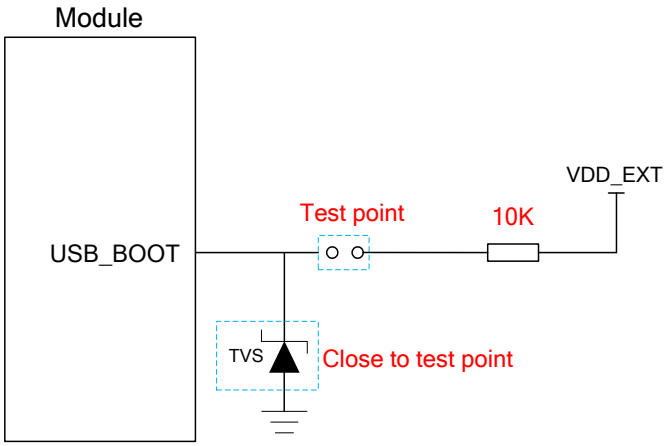


Figure 20: Reference Circuit of USB_BOOT Interface

NOTE

It is recommended to reserve the above circuit design during application design.

3.16. ADC Interfaces*

The module provides two analog-to-digital converter (ADC) interfaces. **AT+QADC=0** command can be used to read the voltage value on ADC0 pin. **AT+QADC=1** command can be used to read the voltage value on ADC1 pin. For more details about these AT commands, please refer to ***document [2]***.

In order to improve the accuracy of ADC voltage values, the trace of ADC should be surrounded by ground.

Table 21: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC0	24	General purpose analog to digital converter interface
ADC1	2	General purpose analog to digital converter interface

The following table describes the characteristics of ADC interfaces.

Table 22: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3		1.8	V
ADC1 Voltage Range	0.3		1.8	V
ADC Resolution			15	bits

NOTES

1. ADC input voltage must not exceed 1.8V.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.
4. "*" means under development.

4 GNSS Receiver

4.1. General Description

BG96 includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou/Compass, Galileo and QZSS).

BG96 supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, BG96 GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows the GNSS performance of BG96.

Table 23: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	31	s
		XTRA* enabled	TBD	s
	Warm start @open sky	Autonomous	21	s
		XTRA* enabled	TBD	s
	Hot start	Autonomous	2.7	s

	@open sky	XTRA* enabled	TBD	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	< 2.5	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.
4. "*" means under development.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in customers designs.

- Maximize the distance between GNSS antenna and main antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50Ω characteristic impedance for the ANT_GNSS trace.

Please refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

BG96 includes a main antenna interface and a GNSS antenna interface. The antenna ports have an impedance of 50Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

The pin definition of main antenna interface is shown below.

Table 24: Pin Definition of Main Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	IO	Main antenna interface	50Ω impedance

5.1.2. Operating Frequency

Table 25: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
B1	1920~1980	2110~2170	MHz
B2 (PCS1900)	1850~1910	1930~1990	MHz
B3 (DCS1800)	1710~1785	1805~1880	MHz
B4	1710~1755	2110~2155	MHz
B5 (GSM850)	824~849	869~894	MHz
B8 (GSM900)	880~915	925~960	MHz
B12	699~716	728~746	MHz

B13	777~787	746~757	MHz
B18	815~829.9	860~874.9	MHz
B19	830~844.9	875~889.9	MHz
B20	832~862	791~821	MHz
B26	814~848.9	859~893.9	MHz
B28	703~748	758~803	MHz
B39	1880~1920	1880~1920	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of main antenna pad is shown as below. A π-type matching circuit should be reserved for better RF performance, and the π-type matching components (R1/C1/C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

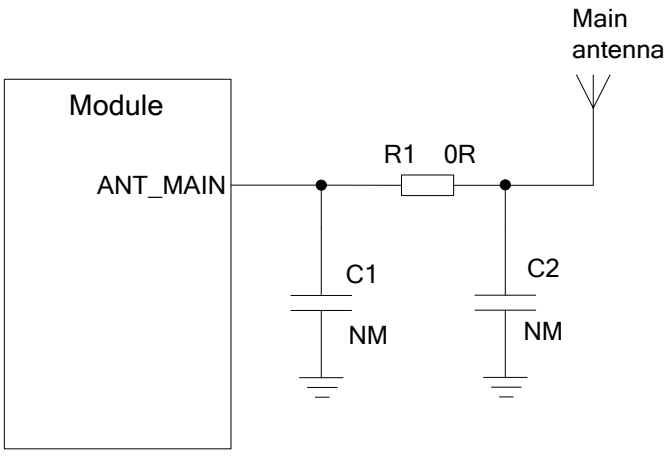


Figure 21: Reference Circuit of RF Antenna Interface

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures.

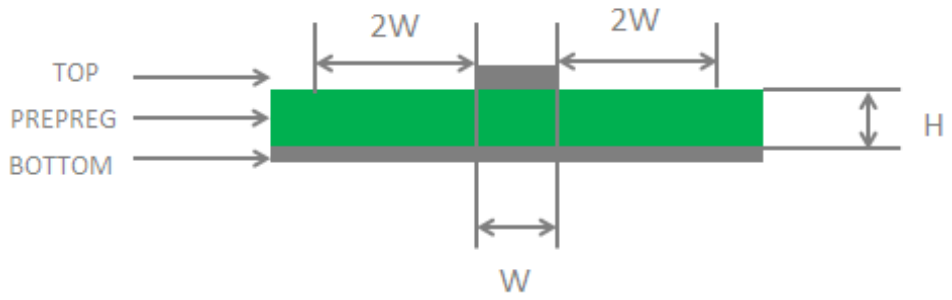


Figure 22: Microstrip Line Design on a 2-layer PCB

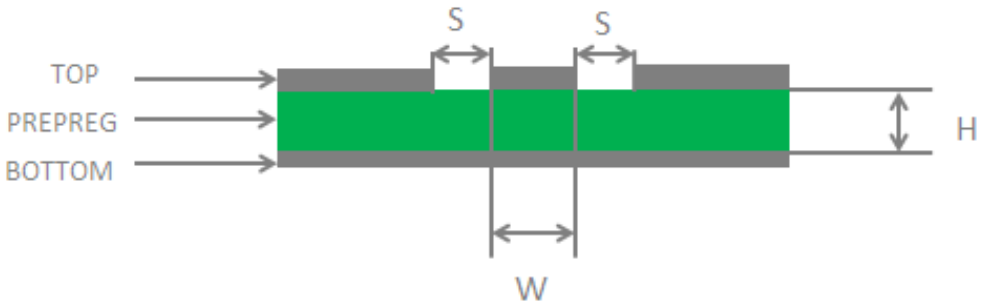


Figure 23: Coplanar Waveguide Line Design on a 2-layer PCB

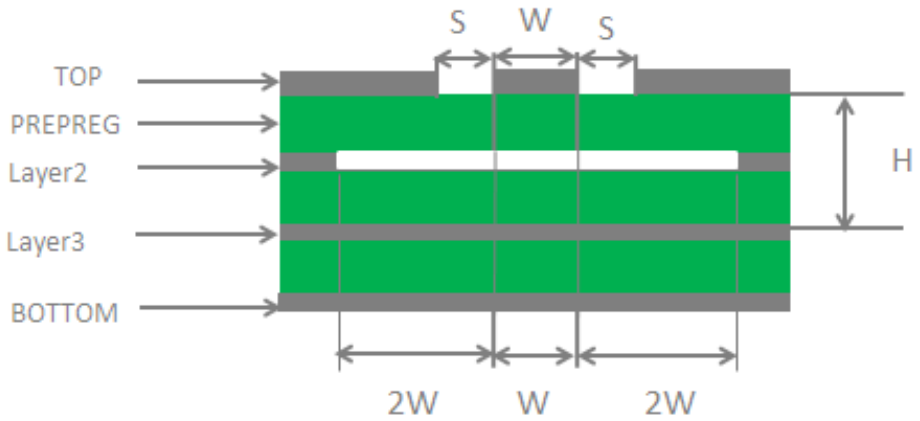


Figure 24: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

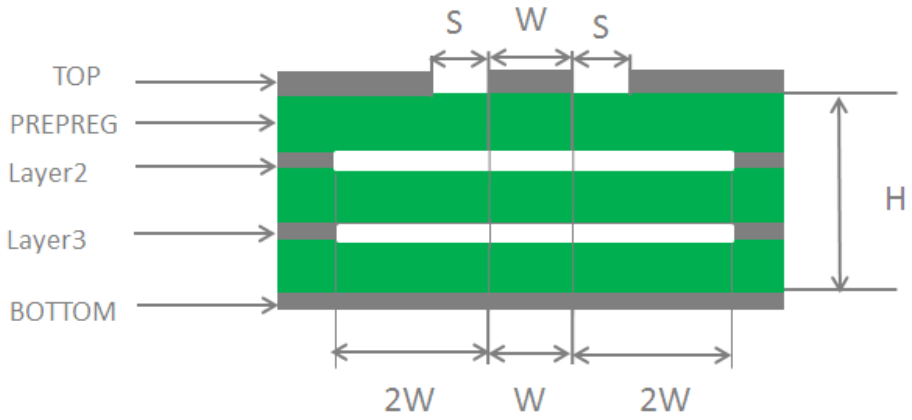


Figure 25: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [4].***

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 26: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50Ω impedance

Table 27: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo/QZSS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

A reference design of GNSS antenna interface is shown as below.

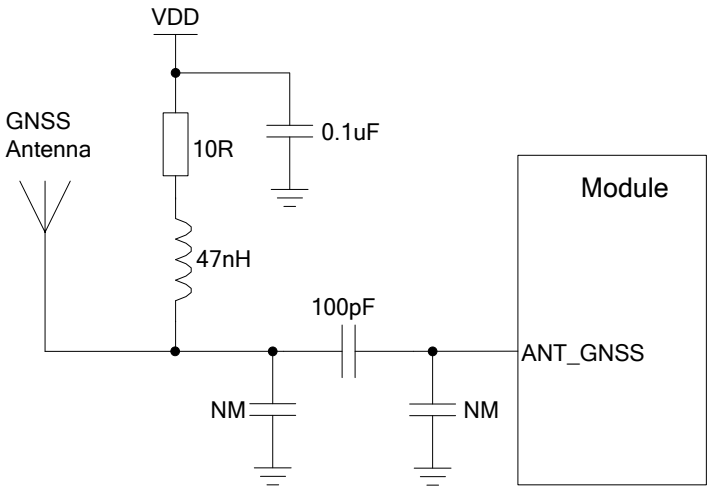


Figure 26: Reference Circuit of GNSS Antenna Interface

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirements

The following table shows the requirements on main antenna and GNSS antenna.

Table 28: Antenna Requirements

Antenna Type	Requirements
LTE/GSM Antenna	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1dB (LTE B5/B8/B12/B13/B18/B19/B20/B26/B28 GSM850/GSM900) Cable Insertion Loss: < 1.5dB (LTE B1/B2/B3/B4/B39, DCS1800/PCS1900)
GNSS Antenna	Frequency range: 1561~1615MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0dBi Active antenna noise figure: < 1.5dB Active antenna gain: > -2dBi Active antenna embedded LNA gain: 20dB (Typ.) Active antenna total gain: > 18dBi (Typ.)

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by *HIROSE*.

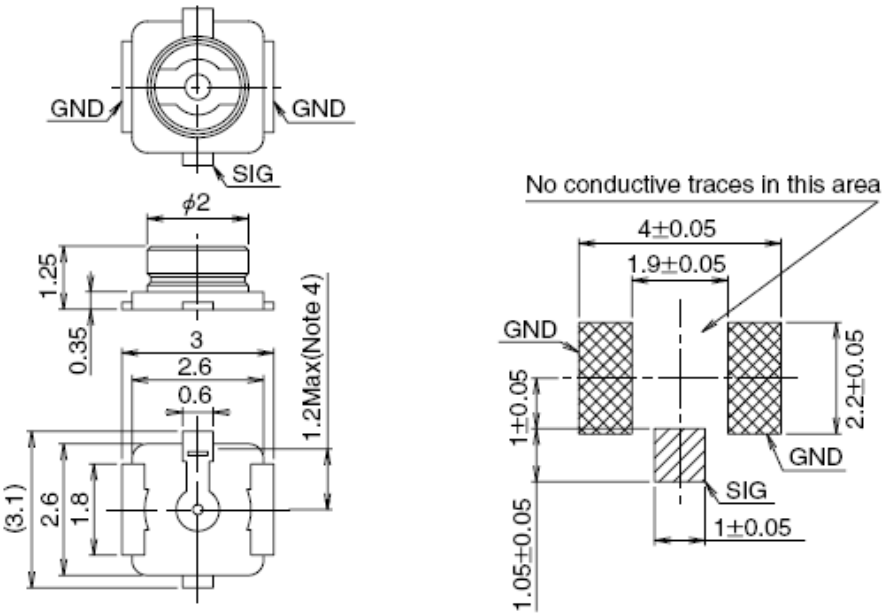


Figure 27: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

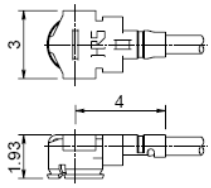
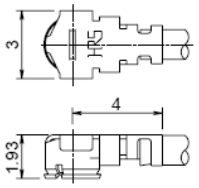
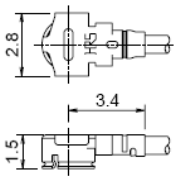
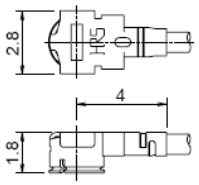
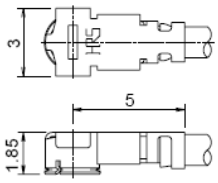
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 28: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

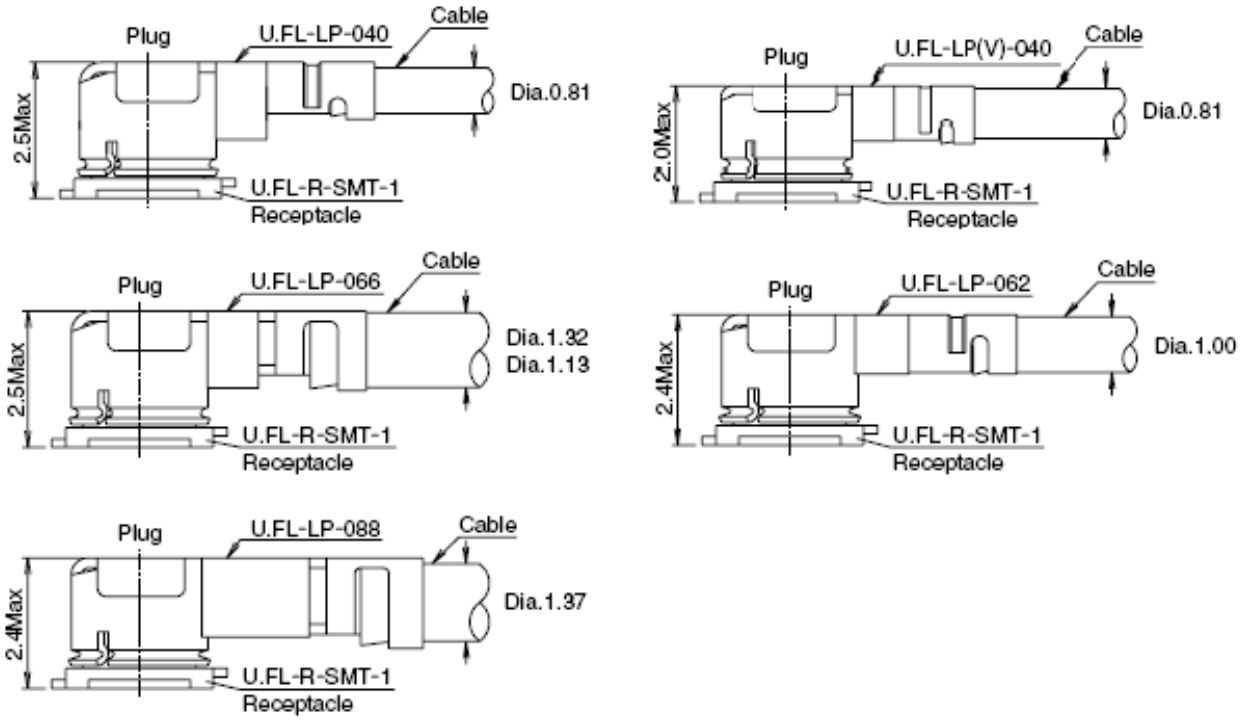


Figure 29: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 29: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB	-0.3	4.7	V
VBAT_RF	-1.2	6	V
USB_VBUS	-0.3	5.5	V
Voltage at Digital Pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 30: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on GSM900		1.8	2.0	A

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
USB_VBUS	USB detection		3.0	5.0	5.25	V

6.3. Operation and Storage Temperatures

The operation and storage temperatures of the module are listed in the following table.

Table 31: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

The following table shows current consumption of BG96 module.

Table 32: BG96 Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF State	Power down	8	uA
	PSM	Power Saving Mode @Real Network	10	uA
	Quiescent Current	**AT+CFUN=0**	0.8 [1]	mA
	Sleep State	DRX=1.28s @Real LTE Cat M1 Network	1.7 [2]	mA
		DRX=1.28s @Real LTE Cat NB1 Network	2.3 [2]	mA
		e-I-DRX=20.48s @Real LTE Cat M1 Network	1.1 [2]	mA
		e-I-DRX=20.48s @Real LTE Cat NB1 Network	1.7 [2]	mA
		@Real 2G Network	2.0 [2]	mA
	Standby State	DRX=1.28s @Real LTE Cat M1 Network	16 [3]	mA
		DRX=1.28s @Real LTE Cat NB1 Network	16 [3]	mA
		e-I-DRX=20.48s @Real LTE Cat M1 Network	15 [3]	mA
		e-I-DRX=20.48s @Real LTE Cat NB1 Network	15 [3]	mA
		@Real 2G Network	15 [3]	mA
	LTE Cat M1 data transfer (GNSS OFF)	LTE-FDD B1 @23.21dBm	217	mA
		LTE-FDD B2 @22.29dBm	211	mA
		LTE-FDD B3 @23.05dBm	223	mA
		LTE-FDD B4 @23.2dBm	227	mA
		LTE-FDD B5 @23.35dBm	211	mA
		LTE-FDD B8 @23.05dBm	213	mA
		LTE-FDD B12 @23.83dBm	217	mA
		LTE-FDD B13 @23.39dBm	225	mA
		LTE-FDD B18 @23.58dBm	217	mA
		LTE-FDD B19 @23.26dBm	212	mA

		LTE-FDD B20 @23.46dBm	215	mA
		LTE-FDD B26 @23.34dBm	226	mA
		LTE-FDD B28 @23.67dBm	236	mA
		LTE-TDD B39 @TBD	TBD	mA
	LTE Cat NB1 data transfer (GNSS OFF)	LTE-FDD B1 @23.5dBm	170	mA
		LTE-FDD B2 @23.3dBm	175	mA
		LTE-FDD B3 @23.5dBm	188	mA
		LTE-FDD B4 @23.6dBm	185	mA
		LTE-FDD B5 @23.5dBm	185	mA
		LTE-FDD B8 @23.1dBm	173	mA
		LTE-FDD B12 @23.6dBm	189	mA
		LTE-FDD B13 @23.3dBm	182	mA
		LTE-FDD B18 @23.6dBm	185	mA
		LTE-FDD B19 @23.4dBm	187	mA
		LTE-FDD B20 @23.4dBm	189	mA
		LTE-FDD B26 @23.4dBm	190	mA
		LTE-FDD B28 @23.2dBm	183	mA
	GPRS data transfer (GNSS OFF)	GSM850 4UL1DL @30.55dBm	603	mA
		GSM850 3UL2DL @31.87dBm	527	mA
		GSM850 2UL3DL @32.21dBm	380	mA
		GSM850 1UL4DL @32.41dBm	220	mA
		GSM900 4UL1DL @30.57dBm	564	mA
		GSM900 3UL2DL @31.79dBm	489	mA
		GSM900 2UL3DL @32.47dBm	372	mA
		GSM900 1UL4DL @32.61dBm	209	mA

		DCS1800 4UL1DL @29.95dBm	534	mA
		DCS1800 3UL2DL @30.15dBm	418	mA
		DCS1800 2UL3DL @30.34dBm	303	mA
		DCS1800 1UL4DL @30.54dBm	183	mA
		PCS1900 4UL1DL @29.58dBm	497	mA
		PCS1900 3UL2DL @29.72dBm	388	mA
		PCS1900 2UL3DL @29.91dBm	282	mA
		PCS1900 1UL4DL @30.11dBm	171	mA
		GSM850 4UL1DL @26.35dBm	415	mA
		GSM850 3UL2DL @26.47dBm	320	mA
		GSM850 2UL3DL @26.69dBm	230	mA
		GSM850 1UL4DL @26.88dBm	140	mA
		GSM900 4UL1DL @26.05dBm	390	mA
		GSM900 3UL2DL @26.46dBm	301	mA
		GSM900 2UL3DL @26.33dBm	217	mA
	EDGE data transfer (GNSS OFF)	GSM900 1UL4DL @26.69dBm	133	mA
		DCS1800 4UL1DL @24.95dBm	370	mA
		DCS1800 3UL2DL @25.12dBm	282	mA
		DCS1800 2UL3DL @25.25dBm	204	mA
		DCS1800 1UL4DL @25.43dBm	127	mA
		PCS1900 4UL1DL @25.24dBm	375	mA
		PCS1900 3UL2DL @25.37dBm	290	mA
		PCS1900 2UL3DL @25.49dBm	210	mA
		PCS1900 1UL4DL @25.72dBm	130	mA
	LTE Voice (GNSS OFF)	Voice @LTE Cat M1 network	108	mA

NOTES

1. [1] Typical value with USB and UART disconnected.
2. [2] Sleep state with UART connected and USB disconnected. The module can enter into sleep state through executing **AT+QSCLK=1** command via UART interface and then controlling the module's DTR pin. For details, please refer to ***Chapter 3.4.4***.
3. [3] Standby state with UART connected and USB disconnected.

Table 33: GNSS Current Consumption

Description	Conditions	Typ.	Unit
Searching (**AT+CFUN=0**)	Cold Start @Passive Antenna	41.7	mA
	Lost State @Passive Antenna	42	mA
Tracking (**AT+CFUN=0**)	Instrument Environment	21.7	mA
	Open Sky @Passive Antenna	TBD	mA
	Open Sky @Active Antenna	TBD	mA

6.5. RF Output Power

The following table shows the RF output power of BG96 module.

Table 34: RF Output Power

Frequency	Max.	Min.
LTE-FDD B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B26/B28	23dBm±2dB	<-39dBm
LTE-TDD B39	23dBm±2dB	<-39dBm
GSM850/GSM900	33dBm±2dB	5dBm±5dB
DCS1800/PCS1900	30dBm±2dB	0dBm±5dB
GSM850/GSM900 (8-PSK)	27dBm±3dB	5dBm±5dB
DCS1800/PCS1900 (8-PSK)	26dBm±3dB	0dBm±5dB

6.6. RF Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of BG96 module.

Table 35: BG96 Conducted RF Receiving Sensitivity

Network	Band	Primary	Diversity	Sensitivity (dBm)	
				Cat M1/3GPP	Cat NB1[1)]/3GPP
LTE	LTE-FDD B1	Supported	Not Supported	-107.0/-102.7	-112.5/-107.5
	LTE-FDD B2			-106.7/-100.3	-112.5/-107.5
	LTE-FDD B3			-106.8/-99.3	-113/-107.5
	LTE-FDD B4			-106.9/-102.3	-112.5/-107.5
	LTE-FDD B5			-107.0/-100.8	-114/-107.5
	LTE-FDD B8			-107.3/-99.8	-113/-107.5
	LTE-FDD B12			-107.7/-99.3	-113.5/-107.5
	LTE-FDD B13			-106.5/-99.3	-112/-107.5
	LTE-FDD B18			-107.5/-102.3	-113.5/-107.5
	LTE-FDD B19			-107.1/-102.3	-114/-107.5
	LTE-FDD B20			-107.2/-99.8	-114/-107.5
	LTE-FDD B26			-107.1/-100.3	-113/-107.5
	LTE-FDD B28			-107.2/-100.8	-113/-107.5
	LTE-TDD B39			TBD /-103	Not Supported
Network	**Band**	**Primary**	**Diversity**	**Sensitivity (dBm)**	
				GSM/3GPP	
GSM	GSM850/GSM900	Supported	Not Supported	-109/-102	
	DCS1800/PCS1900			-108.5/-102	

NOTE

[1] LTE Cat NB1 receiving sensitivity without repetitions.

6.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of BG96 module.

Table 36: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±10	±15	kV
Main/GNSS Antenna Interfaces	±10	±15	kV

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the tolerances for dimensions without tolerance values are ±0.05mm.

7.1. Mechanical Dimensions of the Module

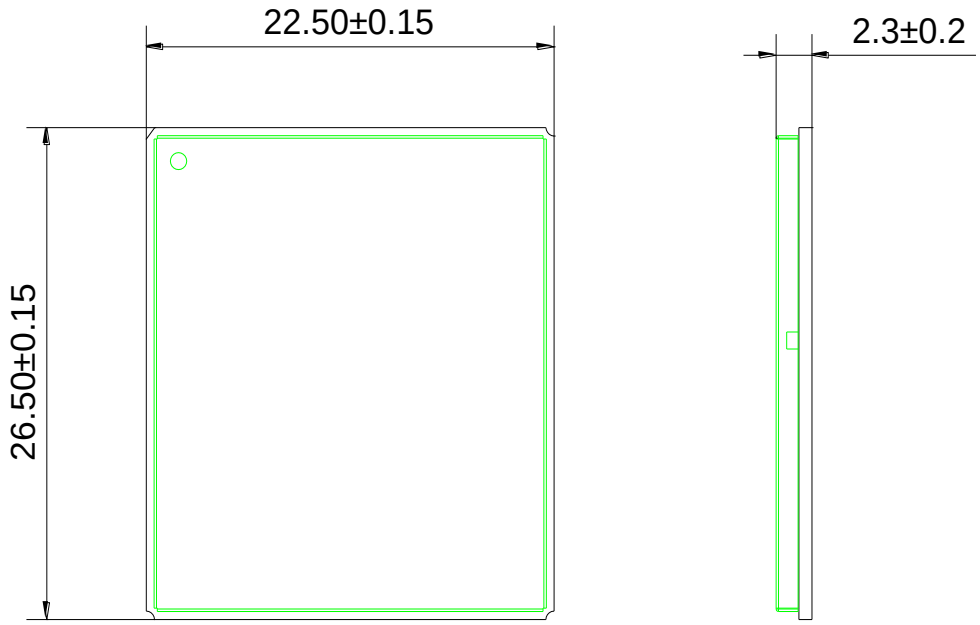


Figure 30: Module Top and Side Dimensions

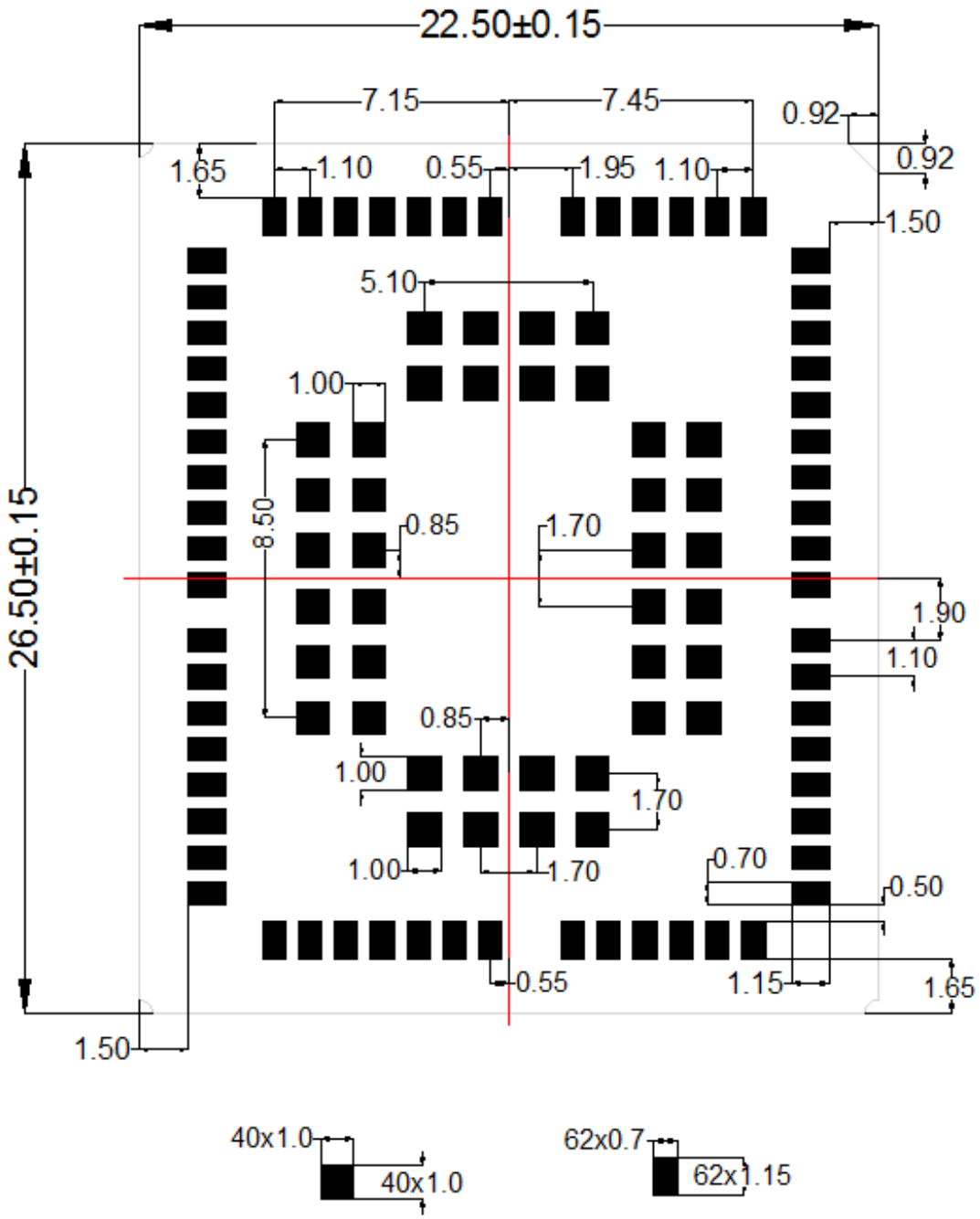


Figure 31: Module Bottom Dimensions (Bottom View)

7.2. Recommended Footprint and Stencil Design

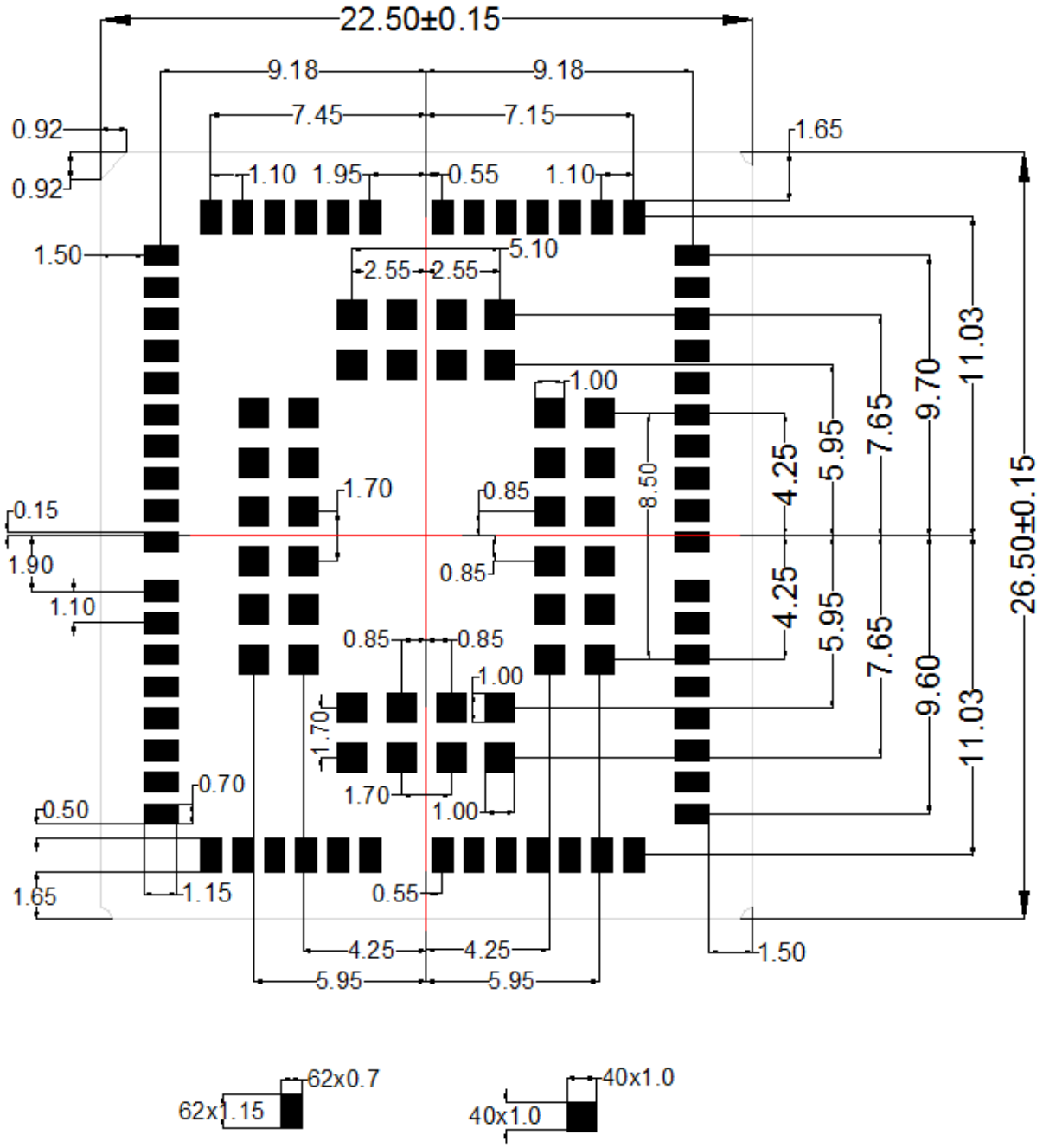


Figure 32: Recommended Footprint (Top View)

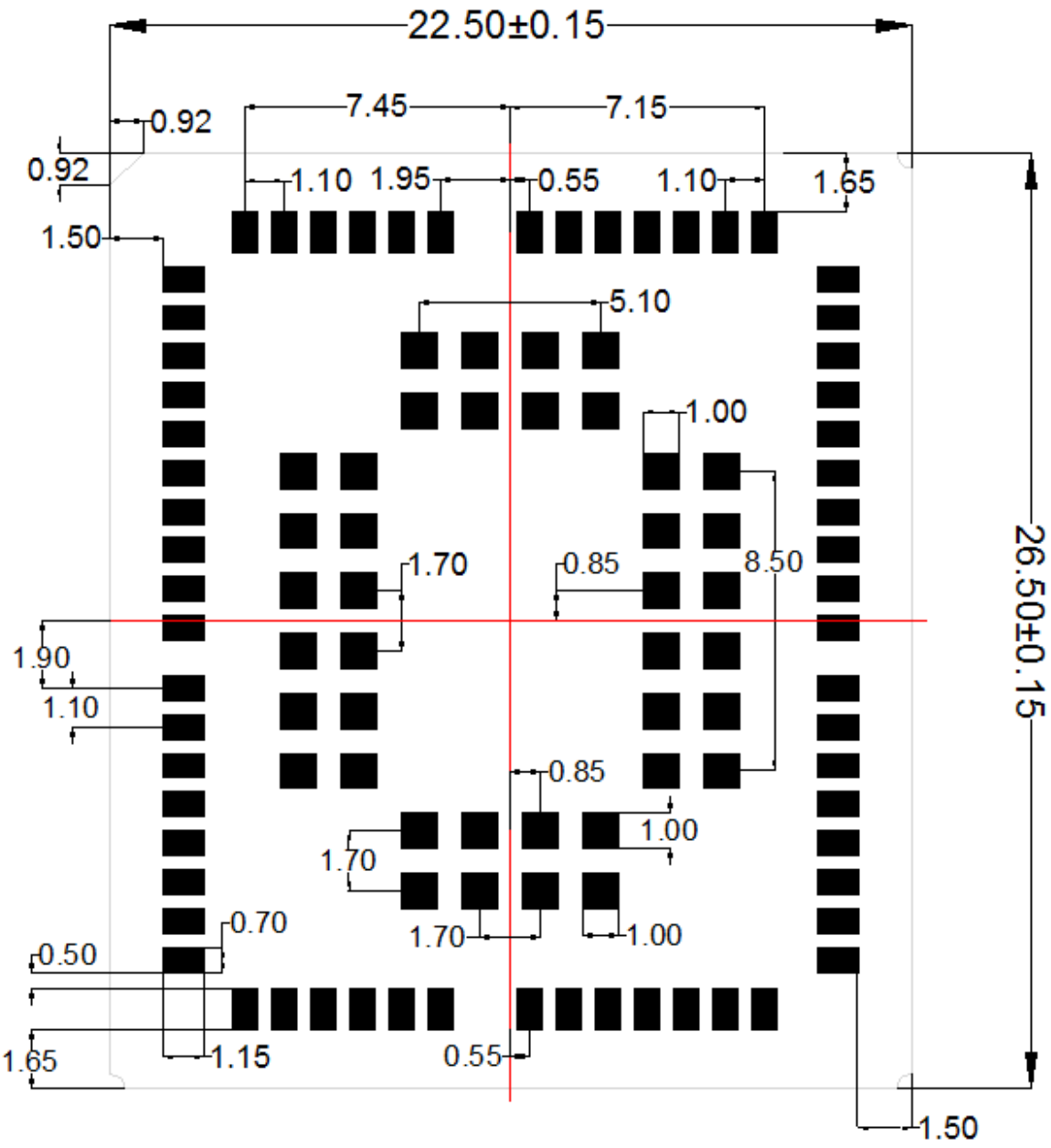


Figure 33: Recommended Stencil Design (Top View)

NOTES

1. For easy maintenance of the module, please keep about 3mm between the module and other components on the host PCB.
2. All reserved pins must be kept open.
3. The thickness of stencil should be stepped-up to 0.18mm. The stencil openings should be shrunken inward by 0.30mm and moved outward by 0.40mm. Cut four 1.00×1.00mm openings with 0.05mm square chamfer on the pads in the center.

7.3. Design Effect Drawings of the Module

Figure 34: Top View of the Module

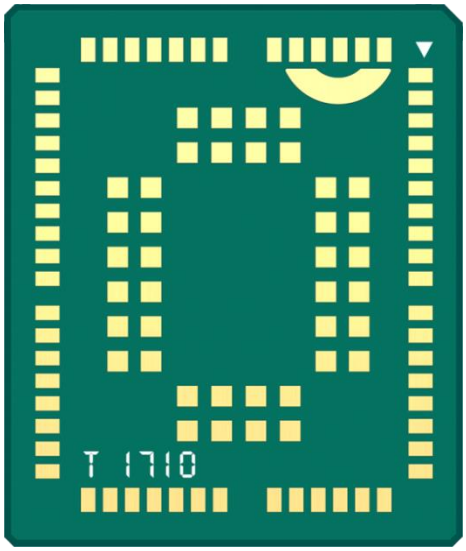


Figure 35: Bottom View of the Module

NOTE

These are design effect drawings of BG96 module. For more accurate pictures, please refer to the module that you get from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

BG96 is stored in a vacuum-sealed bag. The storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10%RH.

3. Devices require baking before mounting, if any circumstance below occurs.
   - When the ambient temperature is 23ºC±5ºC and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%

4. If baking is required, devices may be baked for 48 hours at 125ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (125ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm. For more details, please refer to ***document [5]***.

It is suggested that the peak reflow temperature is 235~245ºC (for SnAg3.0Cu0.5 alloy). The absolute max reflow temperature is 260ºC. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below.

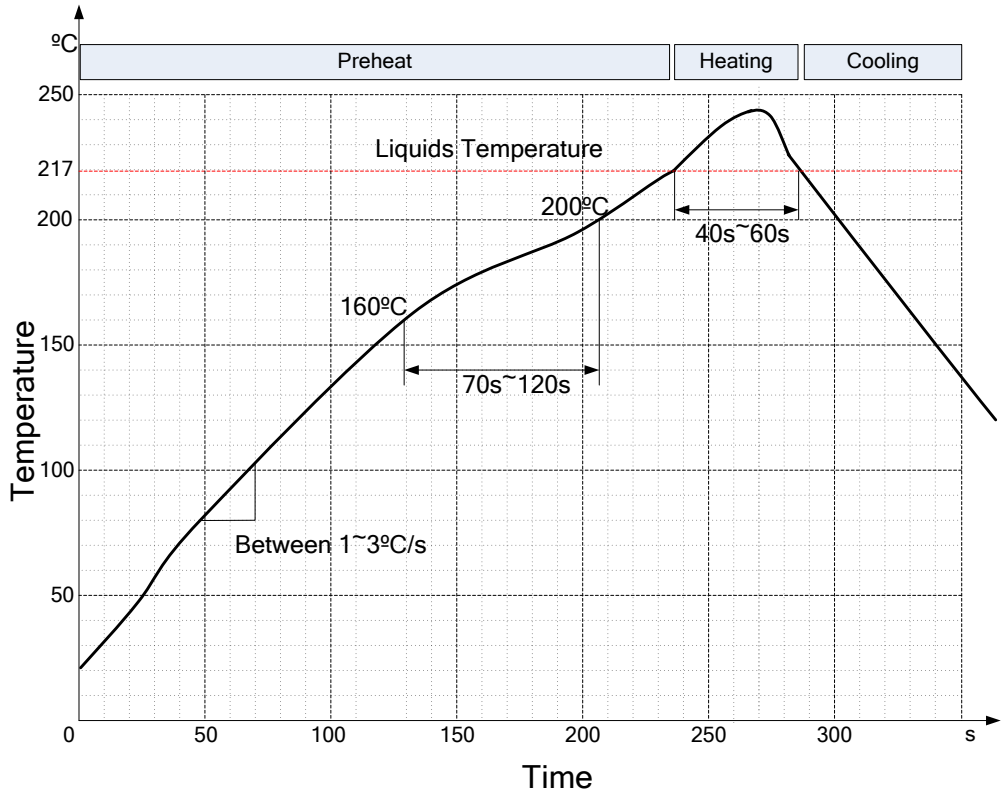


Figure 36: Reflow Soldering Thermal Profile

8.3. Packaging

BG96 is packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

The reel is 330mm in diameter and each reel contains 250 modules. The following figures show the packaging details, measured in mm.

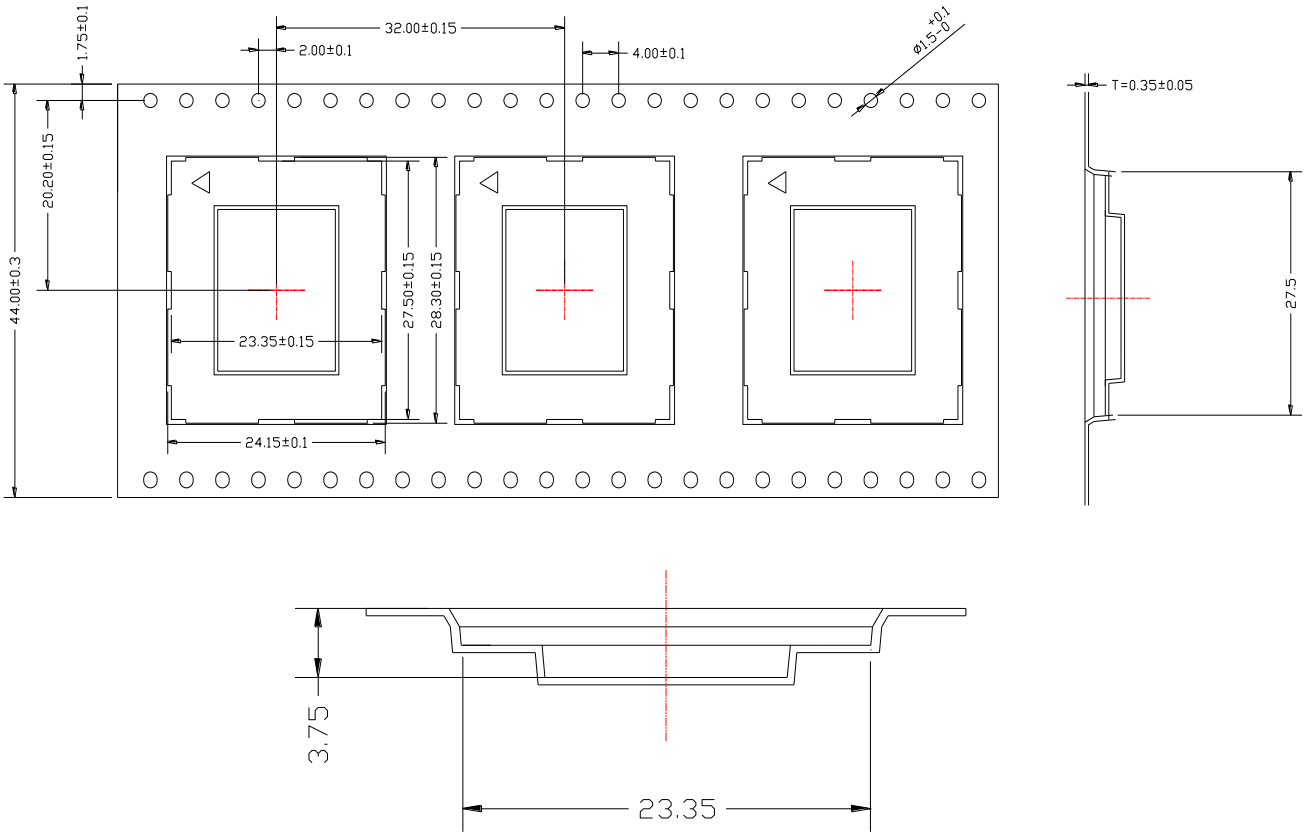


Figure 37: Tape Dimensions

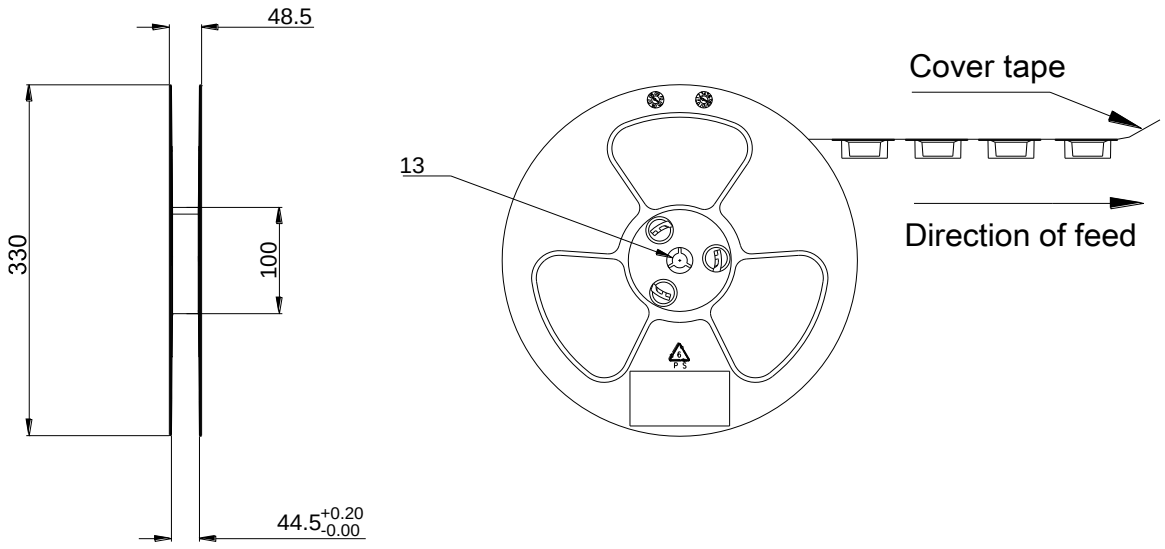


Figure 38: Reel Dimensions

Table 37: Reel Packaging

Model Name	MOQ for MP	Minimum Package: 250pcs	Minimum Package x 4=1000pcs
BG96	250pcs	Size: 370mm × 350mm × 56mm N.W: 0.78kg G.W: 1.46kg	Size: 380mm × 250mm × 365mm N.W: 3.1kg G.W: 6.45kg

9 Appendix A References

Table 38: Related Documents

SN	Document Name	Remark
[1]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB User Guide
[2]	Quectel_BG96_AT_Commands_Manual	BG96 AT Commands Manual
[3]	Quectel_BG96_GNSS_AT_Commands_Manual	BG96 GNSS AT Commands Manual
[4]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[5]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide

Table 39: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
e-I-DRX	Extended Idle Mode Discontinuous Reception
EPC	Evolved Packet Core
ESD	Electrostatic Discharge

FDD	Frequency Division Duplex
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HSS	Home Subscriber Server
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SISO	Single Input Single Output
SMS	Short Message Service
TDD	Time Division Duplexing
TX	Transmitting Direction
UL	Uplink
UE	User Equipment

URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio

10 Appendix B GPRS Coding Schemes

Table 40: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 41: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

12 Appendix D EDGE Modulation and Coding Schemes

Table 42: EDGE Modulation and Coding Schemes

Coding Schemes	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps