ESP8089

Datasheet

Version 3.4

About This Guide

This document provides the specifications of ESP8089.

Release Notes

Date	Version	Release Notes
2014.12	V1.0	First Release.
2016.08	V2.0	Updated formatting.
2017.05	V3.0	Updated the document structure; Changed the input impedance of 50Ω to output impedance of 39+j6Ω.
2017.05	V3.1	Updated Chapter 1 Introduction, Chapter 3 Functional Description, Chapter 4 Peripheral Interface; Added Chapter 2 Pin Definition; Updated Figure 3-1 Block Diagram.
2017.06	V3.2	Added Section 5.1; Added Documentation Change Notification.
2017.11	V3.3	Updated Chapter 3 regarding the range of clock amplitude to 0.8 ~ 1.5V.
2017.12	V3.4	Corrected typos in the descriptions of pin16 and pin24 in Table 2-1.

Table of Contents

1. Overview 1
    1.1. Features 1
    1.2. Applications 1
2. Pin Definition 3
3. Functional Description 5
    3.1. Block Diagram 5
    3.2. Ultra-Low-Power Technology 5
    3.3. HighLevel of Integration 5
    3.4. Clock 6
        3.4.1. High Frequency Clock 6
        3.4.2. External Reference Requirements 6
    3.5. Radio 7
        3.5.1. Channel Frequencies 7
        3.5.2. 2.4 GHz Receiver 7
        3.5.3. 2.4 GHz Transmitter 7
        3.5.4. Clock Generator 8
    3.6. Bluetooth Co-Existence 8
    3.7. Power Management 8
4. Peripheral Interface 10
    4.1. SDIO Host Interface 10
    4.2. General Purpose Input Output (GPIO) 11
    4.3. Real Time Clock IO (EXT_LFC) 11
    4.4. Digital IO Pads 11
5. Electrical Characteristics 12
    5.1. Absolute Maximum Ratings 12
    5.2. Power Consumption 12
    5.3. RF Specifications 13
6. QFN32 Package Information 15
7. Schematics 16

1. Overview

The ESP8089 offers a complete and self-contained Wi-Fi networking solution. When serving as a Wi-Fi adapter, ESP8089 can work with any microcontroller-based systems to achieve wireless connectivity through the SPI/SDIO interface.

ESP8089 allows direct connection to cellular baseband and application processors via SPI/SDIO or memory-mapped parallel interfaces. Its built-in processing and storage capabilities allow it to integrate with the host platform, with minimal development upfront and loading during runtime. ESP8089 is highly-integrated, including the antenna switch balun and power management converters, reducing the external circuitries. The entire solution, including the front-end module, requires minimal PCB area.

The ESP8089-based systems have the following advanced features:

- fast sleep/wake context switching for energy-efficient VoIP,
- adaptive radio biasing for low-power operation,
- advanced signal processing, and
- spur cancellation and radio co-existence features for cellular/Bluetooth/802.11 interference mitigation.

1.1. Features

ESP8089 has the following features:

- 802.11 b/g/n
- Wi-Fi Direct (P2P), Miracast, SoftAP
- Integrated TR switch, balun, LNA, power amplifier and matching network
- Integrated PLL, regulators, and power management units
- +19 dBm output power in 802.11 b mode
- Power down leakage current of < 10 μA
- SDIO 2.0, SPI, UART
- STBC, 1×1 MIMO, 2×1 MIMO
- A-MPDU & A-MSDU aggregation & 0.4 μs guard interval
- Wake up and transmit packets in < 22 ms
- Standby power consumption of < 1.0 mW (DTIM3)

1.2. Applications

ESP8089 is ideally designed for the following applications:

- Cellphone
- Portable Media Player (PMP) such as MP3 or MP4 players

- Mobile gaming devices
- Digital cameras
- Camcorder
- Tablets

2. Pin Definition

Figure 2-1 shows the pin layout for 32-pin QFN package.

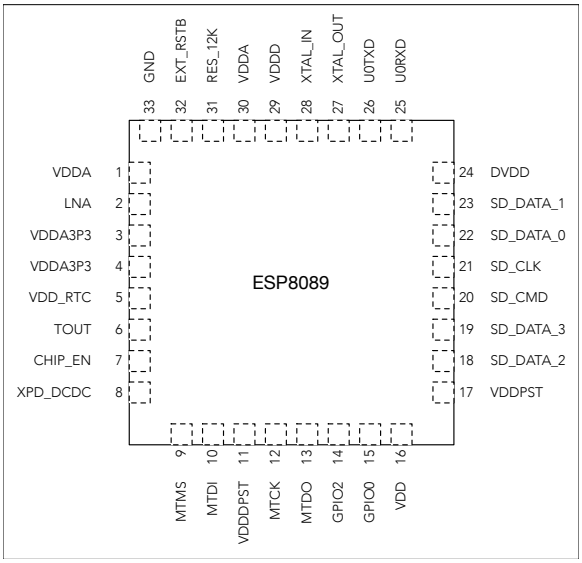


Figure 2-1. Pin Layout

Table 2-1 lists the definitions and functions of each pin.

Table 2-1. ESP8089 Pin Definition

Pin	Name	Type	Function
1	VDDA	P	Analog Power 2.5V ~ 3.6V
2	LNA	I/O	RF antenna interface Chip output impedance=39+j6 Ω. It is suggested to retain the π-type matching network to match the antenna.
3	VDD3P3	P	Amplifier Power 2.5V ~ 3.6V
4	VDD3P3	P	Amplifier Power 2.5V ~ 3.6V
5	VDD_RTC	P	NC (1.1V)
6	TOUT	I	ADC pin. It can be used to test the power-supply voltage of VDD3P3 (Pin3 and Pin4) and the input power voltage of TOUT (Pin 6). However, these two functions cannot be used simultaneously.
7	CHIP_EN	I	Chip Enable High: On, chip works properly Low: Off, small current consumed
8	XPD_DCDC	I/O	GPIO16
9	MTMS	I/O	GPIO14
10	MTDI	I/O	GPIO12
11	VDDPST	P	Digital/IO Power Supply (1.8V ~ 3.3V)

Pin	Name	Type	Function
12	MTCK	I/O	GPIO13
13	MTDO	I/O	GPIO15
14	GPIO2	I/O	GPIO2
15	GPIO0	I/O	GPIO0
16	VDD	P	2.5V digital power supply, NC
17	VDDPST	P	Digital/IO Power Supply (1.8V ~ 3.3V)
18	SDIO_DATA_2	I/O	SDIO
19	SDIO_DATA_3	I/O	SDIO
20	SDIO_CMD	I/O	SDIO
21	SDIO_CLK	I/O	SDIO
22	SDIO_DATA_0	I/O	SDIO
23	SDIO_DATA_1	I/O	SDIO
24	DVDD	P	1.1V digital power supply, NC
25	U0RXD	I/O	UART
26	U0TXD	I/O	UART
27	XTAL_OUT	I/O	Connect to crystal oscillator output, can be used to provide BT clock input
28	XTAL_IN	I/O	Connect to crystal oscillator input
29	VDDD	P	Analog Power 2.5V ~ 3.6V
30	VDDA	P	Analog Power 2.5V ~ 3.6V
31	RES12K	I	Serial connection with a 12 kΩ resistor and connect to the ground
32	EXT_RSTB	I	External reset signal (Low voltage level: Active)

3. Functional Description

3.1. Block Diagram

Figure 3-1 shows the block diagram of ESP8089.

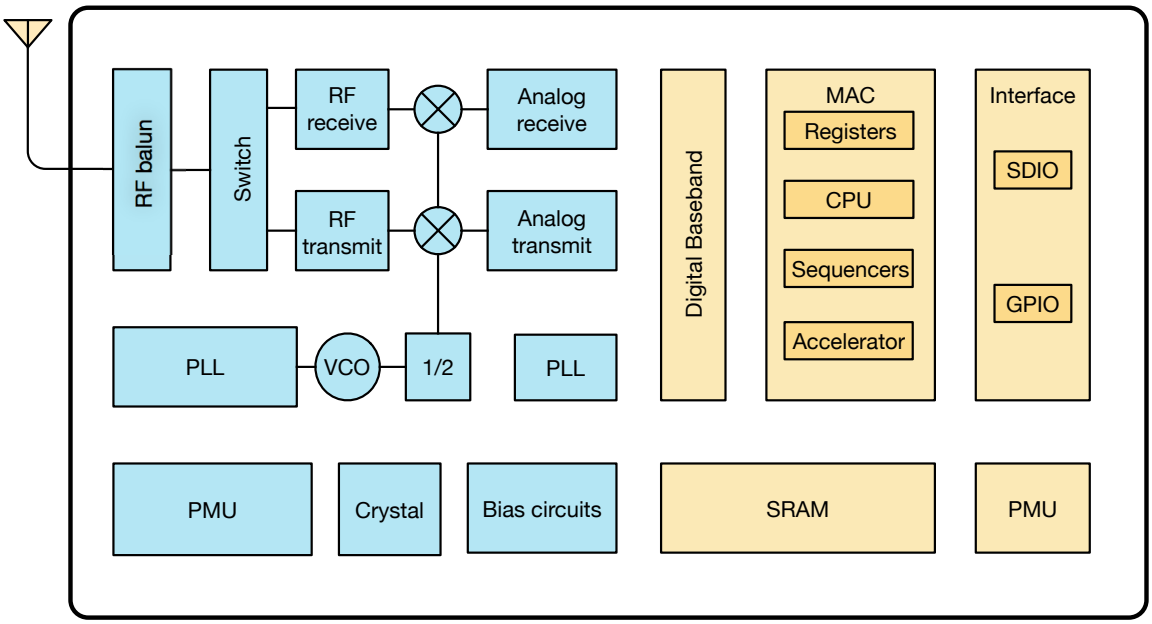


Figure 3-1. Block Diagram

3.2. Ultra-Low-Power Technology

ESP8089 is designed to achieve the lowest power consumption with a combination of several proprietary techniques. The power-saving architecture operates in two modes: active mode and sleep mode.

With the advanced power-management techniques, ESP8089 consumes less than 12 μA in sleep mode, and less than 1.0 mW (DTIM=3), or less than 0.5 mW (DTIM=10) to stay connected.

In sleep mode, only the calibrated real-time clock and watchdog timer remain active. The real-time clock can be programmed to wake up ESP8089 at any required interval.

ESP8089 can be programmed to wake up when a specified condition is detected. This feature can be used in mobile devices, which are able to remain in low-power standby mode until Wi-Fi functionality is needed.

3.3. HighLevel of Integration

By integrating the most important components such as power management unit, TR switch, RF balun, high power PA capable of delivering +23 dBm (peak), ESP8089 ensures the lowest BOM cost, and the ease of integration into any system. The only external

components needed are resistors, capacitors, and crystal. For cellphone compatibility's sake, an SAW filter may be required.

3.4. Clock

3.4.1. High Frequency Clock

The high frequency clock on ESP8089 is used to drive both the Tx and Rx mixers. This clock is generated from the internal crystal oscillator and an external crystal. The crystal frequency can range from 26 MHz to 52 MHz.

While internal calibration of the crystal oscillator ensures that a wide range of crystals can be used, in general, the quality of the crystal is still a factor to consider, in order to obtain reasonable phase noise and Wi-Fi sensitivity. When the crystal used is not optimal due to a frequency offset or quality problem, the maximum data processing ability and sensitivity will decrease.Please refer to the following table for measurement of frequency offset.

Table 3-1. High Frequency Clock

Parameter	Symbol	Min	Max	Unit
Frequency	F_{XO}	26	52	MHz
Loading capacitance	C_L	-	32	pF
Motional capacitance	C_M	2	5	pF
Series resistance	R_S	0	65	Ω
Frequency tolerance	ΔF_{XO}	-15	15	ppm
Frequency vs. temperature (-25°C ~ 75°C)	$\Delta F_{XO,\ Temp}$	-15	15	ppm

3.4.2. External Reference Requirements

For an externally-generated clock, the frequency can range from 26 MHz to 52 MHz. For good radio performance, the clock should possess the following characteristics:

Table 3-2. External Reference Requirements

Parameter	Symbol	Min	Max	Unit
Clock amplitude	V_{XO}	0.8	1.5	Vpp
External clock accuracy	$\Delta F_{XO,EXT}$	-15	15	ppm
Phase noise @1 kHz offset, 40 MHz clock	-	-	-120	dBc/Hz
Phase noise @10 kHz offset, 40 MHz clock	-	-	-130	dBc/Hz
Phase noise @100 kHz offset, 40 MHz clock	-	-	-138	dBc/Hz

3.5. Radio

The ESP8089 radio consists of the following main blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- High-speed clock generators and crystal oscillator
- Real-time clock
- Bias and regulators
- Power management

3.5.1. Channel Frequencies

The RF transceiver supports the following channels according to the IEEE 802.11 b/g/n standards.

Table 3-3. Channel Frequencies

Channel No.	Frequency (MHz)	Channel No.	Frequency (MHz)
1	2412	8	2447
2	2417	9	2452
3	2422	10	2457
4	2427	11	2462
5	2432	12	2467
6	2437	13	2472
7	2442	14	2484

3.5.2. 2.4 GHz Receiver

The 2.4 GHz receiver downconverts the RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution high-speed ADCs. To adapt to varying signal channel conditions, RF filters, automatically-gained control, DC offset cancelation circuits and baseband filters are integrated into the radio.

3.5.3. 2.4 GHz Transmitter

The 2.4 GHz transmitter upconverts the quadrature baseband signals to 2.4 GHz, and drives the antenna with a high-powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier, enabling a state of art performance of delivering +20.5 dBm average power for 802.11 b transmission and +16 dBm for 802.11 n transmission.

Additional calibrations are integrated, in order to cancel any imperfections of the radio. The calibrations include the following:

- carrier leakage
- I/Q phase matching
- baseband nonlinearities

This reduces the amount of time and test equipment required for production testing.

3.5.4. Clock Generator

The clock generator produces quadrature 2.4 GHz clock signals for the receiver and transmitter. All components of the clock generator are integrated on-chip, including:

- inductor
- varactor
- loop filter

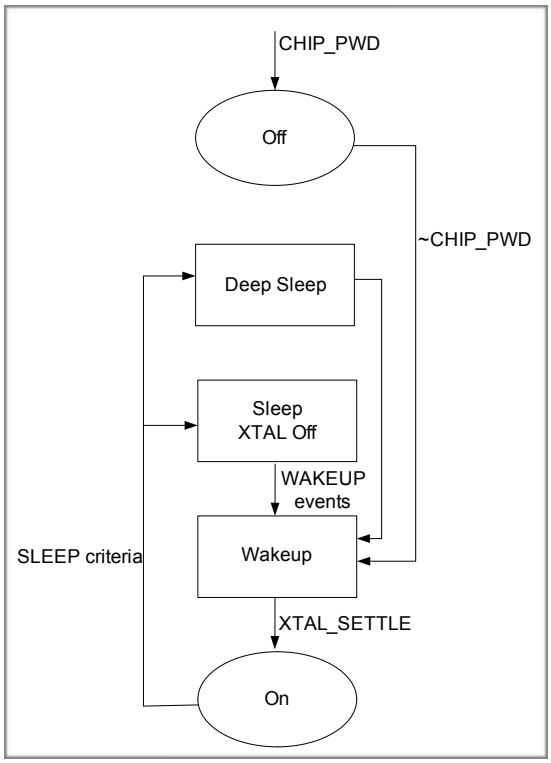
The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on-chip with patented calibration algorithms to ensure the best receiver and transmitter performance.

3.6. Bluetooth Co-Existence

ESP8089 features pre-assigned pins for BT/Wi-Fi co-existence and BT clock-request. These pins act as the interface to a BT system to facilitate traffic arbitration between the two systems. The control system is in firmware and supports various standards or proprietary co-existence protocols.

3.7. Power Management

The chip can be put into the following states:



- OFF: CHIP_PD pin is low. The RTC is disabled. All registers are cleared.
- DEEP_SLEEP: Only RTC is powered on – the rest of the chip is powered off. Recovery memory of RTC can keep basic Wi-Fi connecting information.
- SLEEP: Only the RTC is operating. The crystal oscillator is disabled. Any wake-up events (MAC, host, RTC timer, external interrupts) will put the chip into the WAKE-UP state.
- WAKE-UP: In this state, the system goes from the sleep states to the PWR state. The crystal oscillator and PLLs are enabled.
- ON state: the high speed clock is operational and sent to each block enabled by the clock control register. Lower-level clock gating is implemented at the block level, including the CPU, which can be gated off using the WAITI instruction, while the system is on.

4. Peripheral Interface

4.1. SDIO Host Interface

The IO pins can be set to the following modes:

- 4-bit 25 MHz SDIO v1.1
- 4-bit 50 MHz SDIO v2.0
- SPI mode

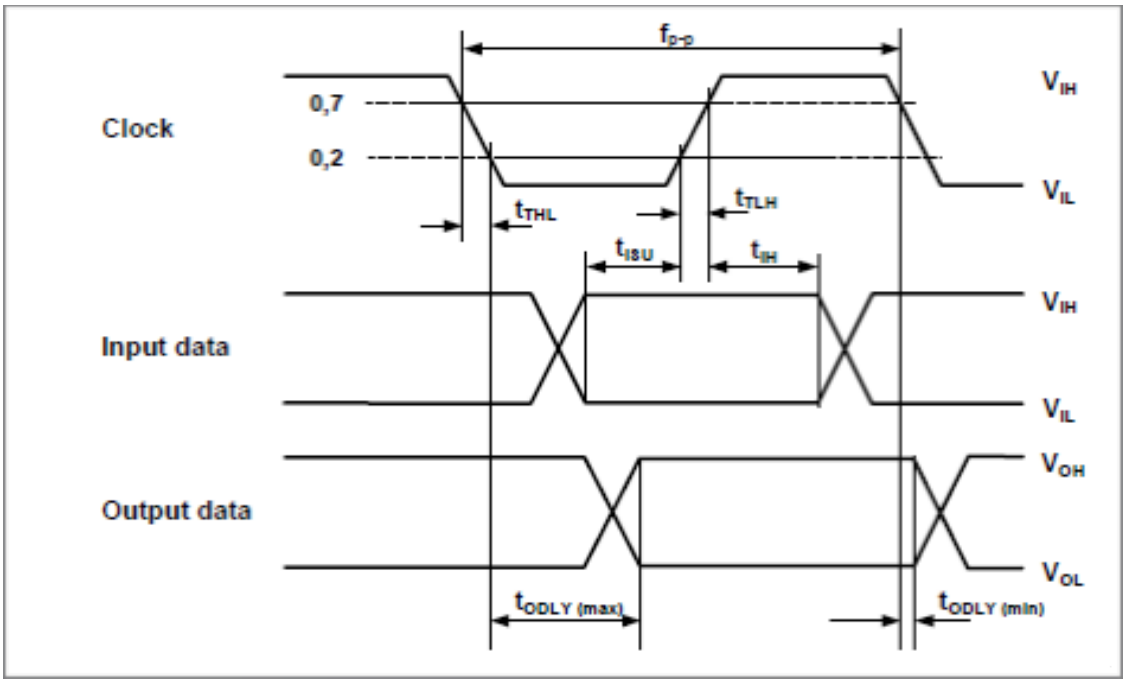


Figure 4-1. SDIO Timing Diagram

Table 4-1. SDIO Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Input setup time	t_{ISU}	6	-	ns
Input hold time	t_{IH}	2.5	-	ns
Clock fall time	t_{THL}	-	3	ns
Clock rise time	t_{TLH}	-	3	ns
Output delay time	t_{DLY}	2	12	ns
Clock frequency	f_{SDIO}	-	50	MHz

4.2. General Purpose Input Output (GPIO)

ESP8089 16 GPIO pins. They can be assigned to various functions by the firmware. Each GPIO can be configured with internal pull-up/down, input available for sampling by a software register, input triggering an edge or level CPU interrupt, input triggering a level wakeup interrupt, open-drain or push-pull output driver, or output source from a software register, or a sigma-delta PWM DAC.

These pins are multiplexed with other functions such as host interface, UART, SI, Bluetooth co-existence, etc.

4.3. Real Time Clock IO (EXT_LFC)

If a 32.768 kHz LFC clock is available, it can be connected to EXT_LFC. If no clock is available on this pin, the internal LFC will be used. If an EXT_LFC is available, the selection of LFC source, internal LFC or EXT_LFC can be done by a strapping pin.

4.4. Digital IO Pads

The digital IO pads are bidirectional, non-inverting and tri-state. It includes input and an output buffer with tri-state control inputs. Besides this, for low power operations, the IO can also be set to hold. For instance, when we power down the chip, all output enable signals can be set to hold low.

An optional hold functionality can be built into the IO if requested. When the IO is not driven by the internal or external circuitry, the hold functionality can be used to hold the state to the last used state.

The hold functionality introduces some positive feedback into the pad. Hence, the external driver that drives the pad must be stronger than the positive feedback. The required drive strength, however, is small – in the range of 5 µA.

All digital IO pins are protected from over-voltage with a snap-back circuit connected between the pad and the ground. The snap back voltage is typically about 6V, and the holding voltage is 5.8V. This provides protection from over-voltages and ESD. The output devices are also protected from reversed voltages with diodes.

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Table 5-1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Input low voltage	V_{IL}	-0.3	$0.25 \times V_{IO}$	V
Input high voltage	V_{IH}	$0.75 \times V_{IO}$	3.3	V
Input leakage current	I_{IL}	-	50	nA
Output low voltage	V_{OL}	-	$0.1 \times V_{IO}$	V
Output high voltage	V_{OH}	$0.8 \times V_{IO}$	-	V
Input pin capacitance	C_{pad}	-	2	pF
VDDIO	V_{IO}	1.8	3.3	V
Maximum drive capability	I_{MAX}	-	12	mA
Operating temperature	T_{amb}	-40	125	°C
Storage temperature	T_{STR}	-40	150	°C

5.2. Power Consumption

Unless otherwise specified, the power consumption measurements are taken with a 3.3V supply at 25°C of ambient temperature. All transmitters' measurements are based on a 50% duty cycle.

Table 5-2. Power Consumption

Mode	Min	Typical	Max	Unit
Transmit 802.11 b, DSSS 1 Mbps, POUT=+19.5 dBm	-	215	-	mA
Transmit 802.11 b, CCK 11 Mbps, POUT=+18.5 dBm	-	197	-	mA
Transmit 802.11 g, OFDM 54 Mbps, POUT =+16 dBm	-	145	-	mA
Transmit 802.11 n, MCS 7, POUT=+14 dBm	-	135	-	mA
Receive 802.11 b, packet length=1024 byte, -80 dBm	-	60	-	mA
Receive 802.11 g, packet length=1024 byte, -70 dBm	-	60	-	mA
Receive 802.11 n, packet length=1024 byte, -65 dBm	-	62	-	mA
Standby	-	0.9	-	mA

Mode	Min	Typical	Max	Unit
Deep sleep	-	10	-	µA
Power save mode DTIM 1	-	1.2	-	mA
Power save mode DTIM 3	-	0.86	-	mA
Total shutdown	-	0.5	-	µA

5.3. RF Specifications

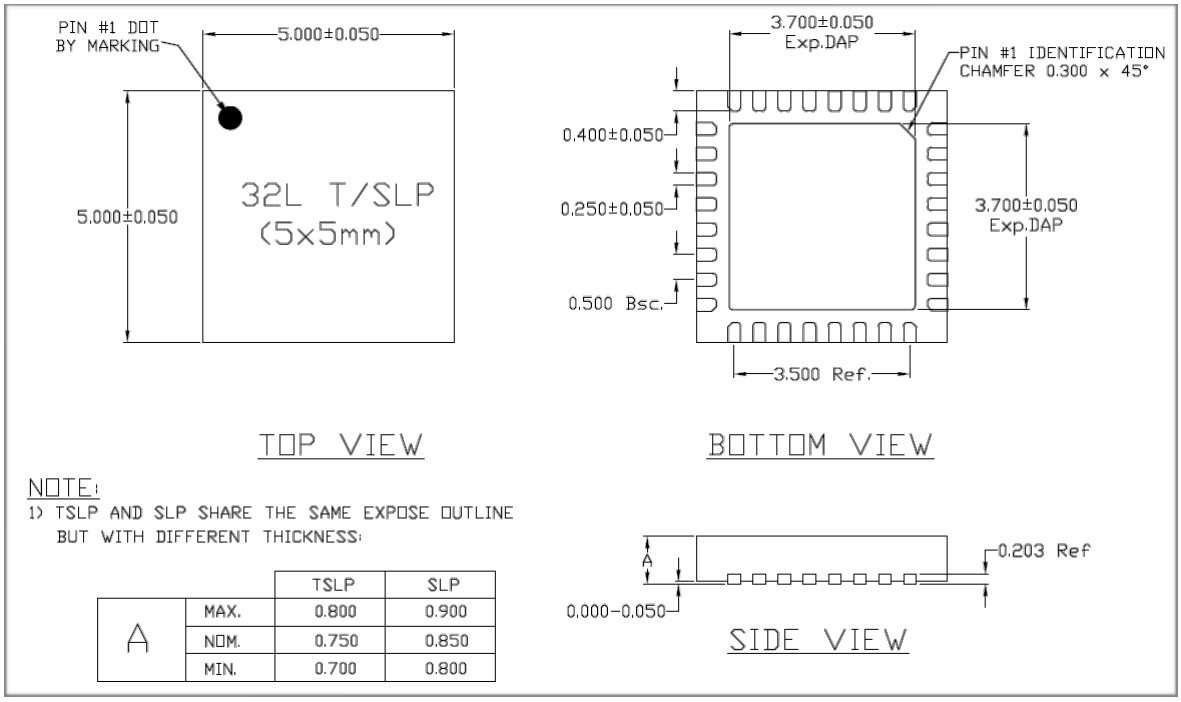
The following data are from tests conducted at room temperature, with a 3.3V power supply.

Table 5-3. RF Specifications

Description	Min	Typical	Max	Unit
Input frequency	2412	-	2484	MHz
Output impedance	-	39+j6	-	Ω
Input reflection	-	-	-10	dB
Output power of PA for 72.2 Mbps	14	15	16	dBm
Output power of PA for 11b mode	17.5	18.5	19.5	dBm
Sensitivity				
DSSS, 1 Mbps	-	-98	-	dBm
CCK, 11 Mbps	-	-91	-	dBm
6Mbps (1/2 BPSK)	-	-93	-	dBm
54Mbps (3/4 64-QAM)	-	-75	-	dBm
HT20, MCS 7 (65 Mbps, 72.2 Mbps)	-	-71	-	dBm
Adjacent channel rejection				
OFDM, 6 Mbps	-	37	-	dB
OFDM, 54 Mbps	-	21	-	dB
HT20, MCS 0	-	37	-	dB
HT20, MCS 7	-	20	-	dB
Time				
Crystal power up time	-	500	-	µs
Baseband PLL power up time	-	100	-	µs
RF PLL power up time	-	200	-	µs

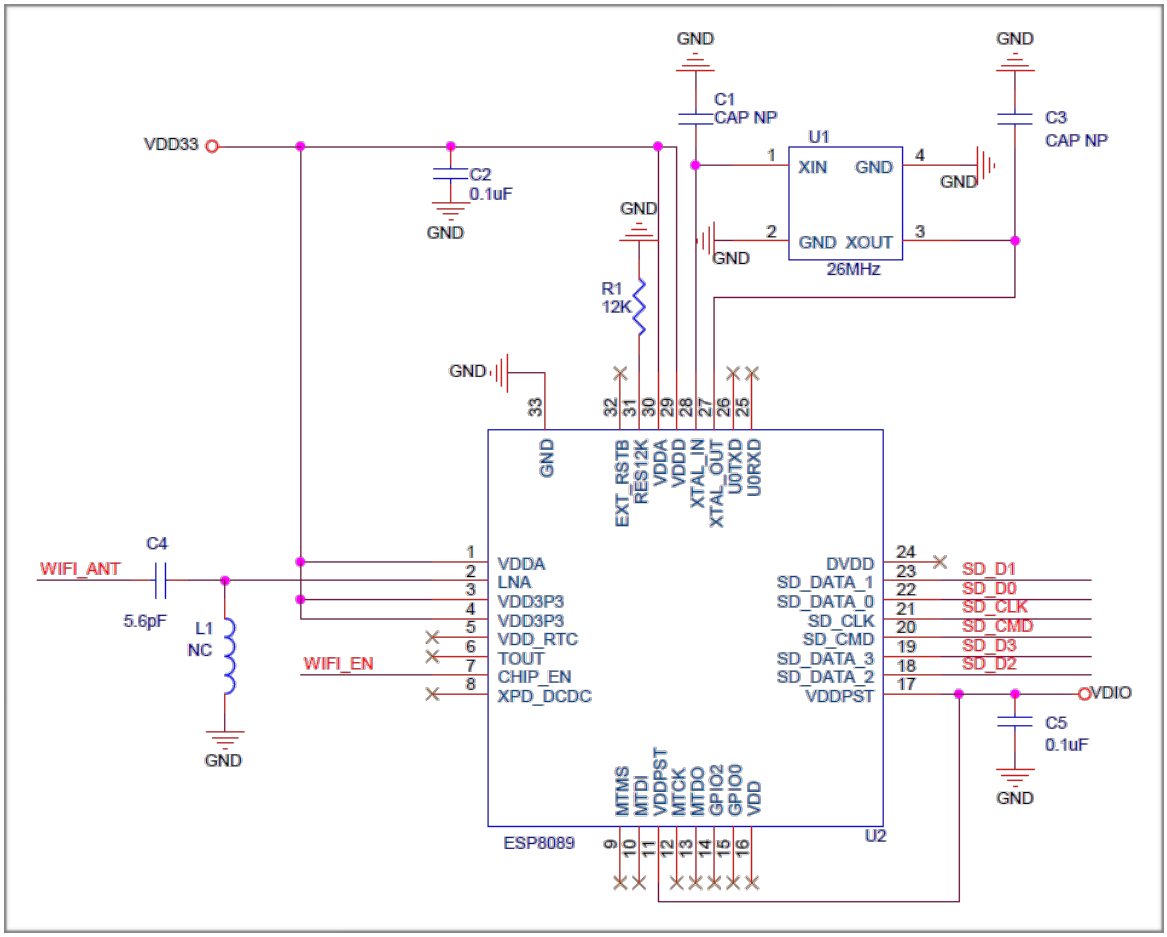
Description	Min	Typical	Max	Unit
Rx RF power up time	-	2	-	µs
Tx RF power up time	-	2	-	µs

6. QFN32 Package Information



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

7. Schematics



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