HV9120/HV9123

High-Voltage, Current-Mode PWM Controller

Features

- 10 to 450V Input Voltage Range
- <1.3 mA Supply Current
- ≤1 MHz Clock
- Maximum Duty Version
  - HV9120: 49%
  - HV9123: 99%

Applications

- Offline High-Frequency Power Supplies
- Universal Input Power Supplies
- High Density Power Supplies
- Very High Efficiency Power Supplies
- Extra Wide Load Range Power Supplies

General Description

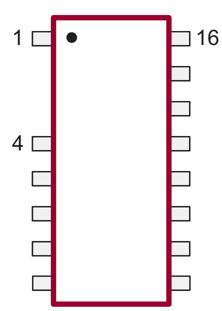
HV9120 and HV9123 are Switch-Mode Power Supply (SMPS) controllers suitable for the control of a variety of converter topologies, including flyback and forward converter.

Using an internal, high-voltage regulator, HV9120 and HV9123 can derive a bias supply for starting-up and powering a converter from a variety of power sources, such as a 12V battery or the rectified AC (230 V_{AC}) line.

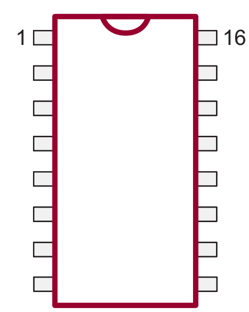
HV9120/HV9123 controllers include all essentials for a power-converter design, such as a bandgap reference, an error amplifier, a ramp generator, a high-speed PWM comparator, and a gate driver. A shutdown latch provides on/off control. Device power consumption is less than 6 mW when shutdown.

HV9120 offers 50% maximum duty, and HV9123 offers nearly 100% duty.

Package Types



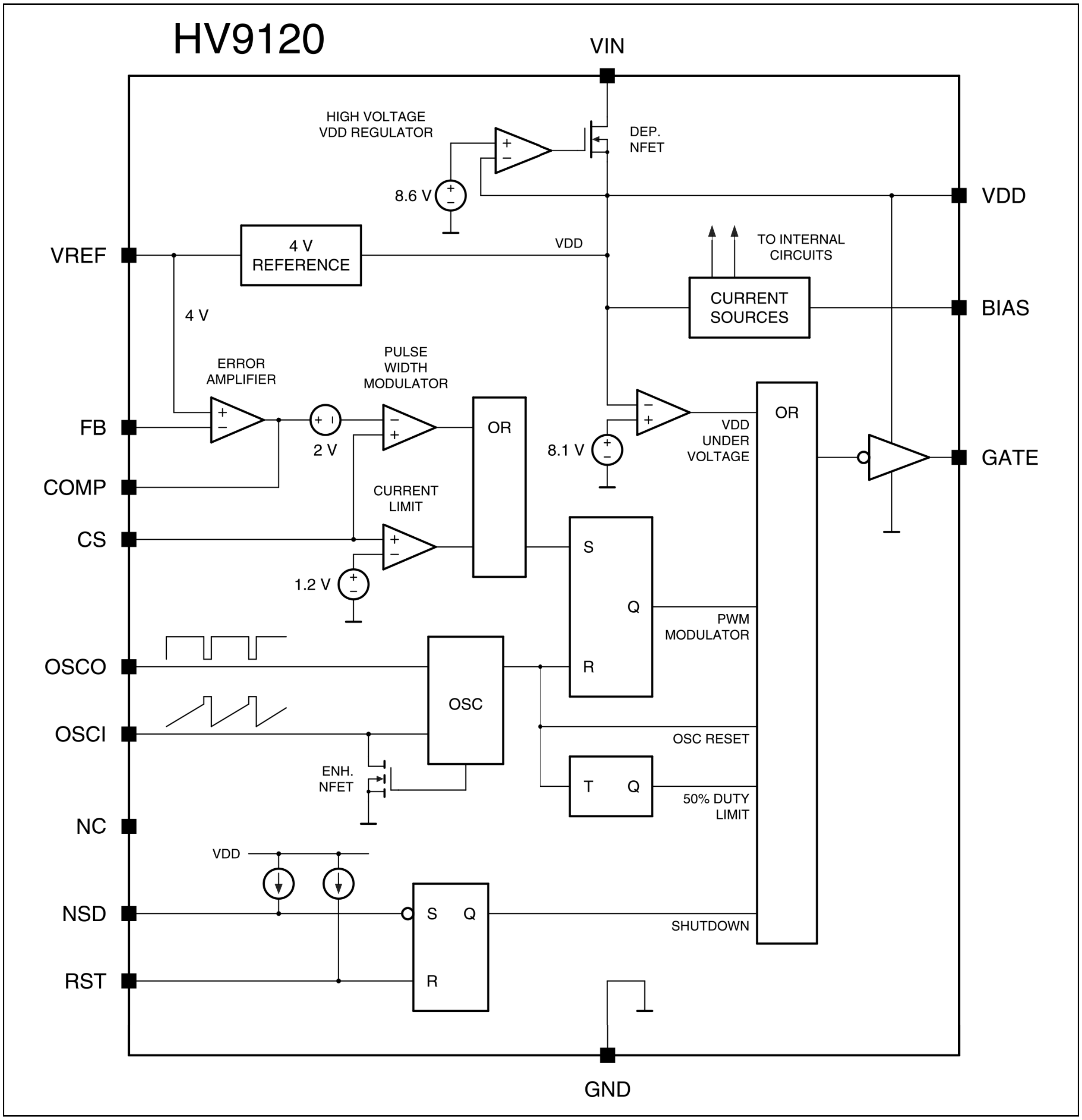
16-lead SOIC



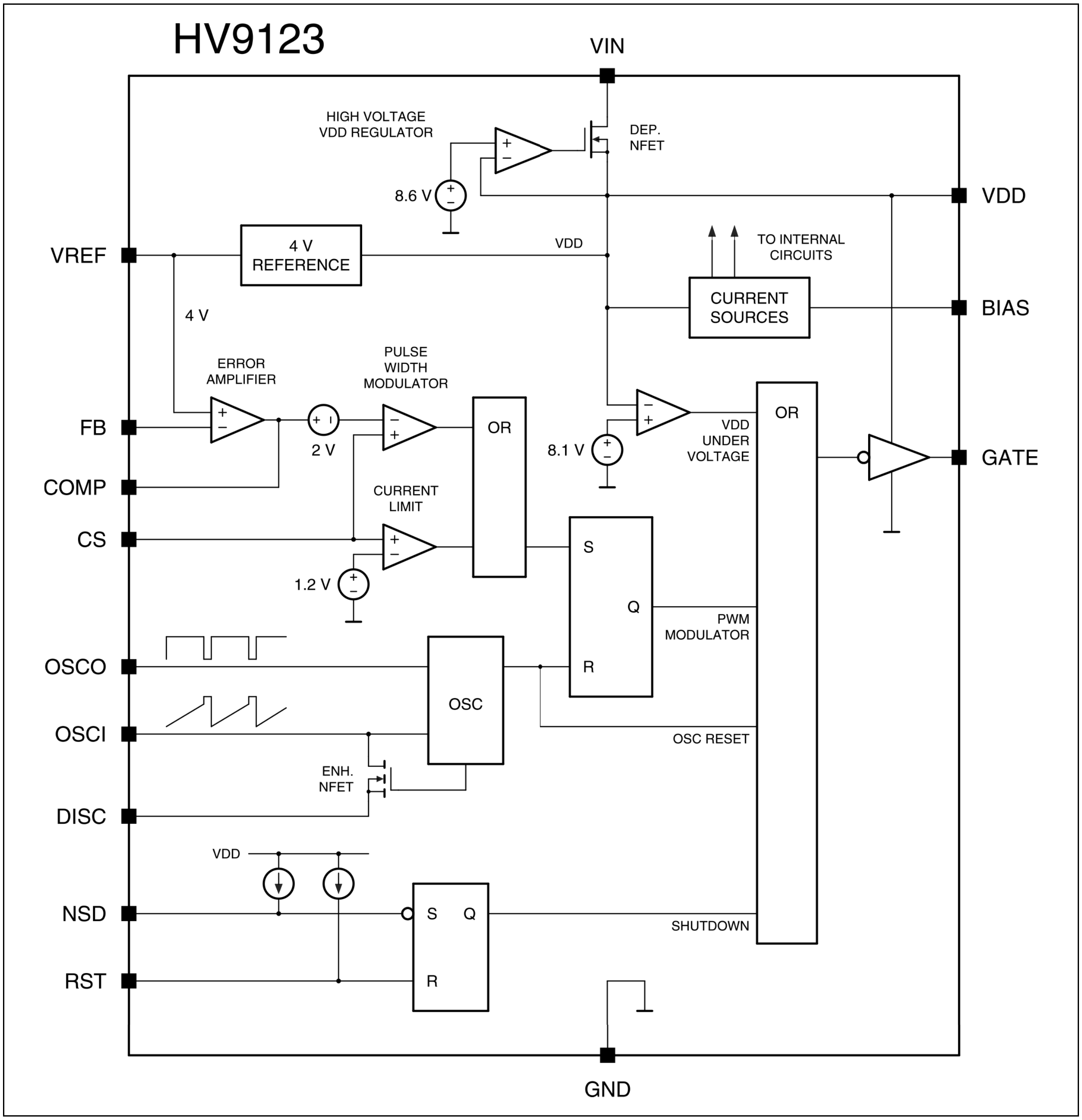
16-lead PDIP

See Table 3-1 for pin information

Block Diagram HV9120



Block Diagram HV9123



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Input voltage, V_{IN} 450V
Device supply voltage, V_{DD}.......... 15.5V
Logic input voltage .... -0.3V to V_{DD} + 0.3V
Linear input voltage.......... -0.3V to V_{DD} + 0.3V
High-voltage regulator input current (continuous), I_{IN} .... 2.5 mA
Power dissipation: 16-Lead SOIC .... 900 mW
16-Lead PDIP .... 1000 mW

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{DD} = 10V, V_{IN} = 48V, V_{DISC} = 0V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Reference						
Output Voltage	V_{REF}	3.92	4.00	4.08	V	R_L= 10 MΩ
		3.84	4.00	4.16		R_L= 10 MΩ, T_A= -40°C to +125°C
Output Impedance	Z_{OUT}	15	30	45	kΩ	(Note 1)
Short Circuit Current	I_{SHORT}	—	125	250	µA	V_{REF}= GND
Change in V_{REF} with Temperature	ΔV_{REF}	—	0.25	—	mV/°C	T_A= -40°C to +125°C (Note 1)
Oscillator						
Oscillator Frequency	f_{MAX}	1.0	3.0	—	MHz	R_{OSC}= 0Ω
Initial Accuracy	f_{OSC}	80	100	120	kHz	R_{OSC}= 330 kΩ (Note 2)
		160	200	240		R_{OSC}= 150 kΩ (Note 2)
V_{DD} Regulation	—	—	—	15	%	9.5V< V_{DD}<13.5V
Temperature Coefficient	—	—	170	—	ppm/°C	T_A= -40°C to +125°C (Note 1)
PWM						
Maximum Duty Cycle — HV9120	D_{MAX}	49.0	49.4	49.6	%	(Note 1)
Maximum Duty Cycle — HV9123		95	97	99		
Dead Time — HV9123	D_{MIN}	—	225	—	ns	HV9123 only (Note 1)
Minimum Duty Cycle		—	—	0	%	—
Pulse Width Where Pulse Drops Out		—	80	125	ns	(Note 1)
Current Limit						
Maximum Input Signal	V_{LIM}	1.0	1.2	1.4	V	V_{FB}= 0V
Delay to Output	t_D	—	80	120	ns	V_{CS}= 1.5V, V_{COMP}≤ 2.0V (Note 1)

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: V_{DD} = 10V, V_{IN} = 48V, V_{DISC} = 0V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ, T_A = 25°C, unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Error Amplifier							
Feedback Voltage		V_{FB}	3.92	4.00	4.08	V	FB shorted to COMP
Input Bias Current		I_{IN}	—	25	500	nA	V_{FB}= 4.0V
Input Offset Voltage		V_{OS}	nulled during trim			—	—
Open Loop Voltage Gain		A_{VOL}	60	80	—	dB	(Note 1)
Unity Gain Bandwidth		GB	1.0	1.3	—	MHz	(Note 1)
Output Source Current		I_{SOURCE}	-1.4	-2.0	—	mA	V_{FB}= 3.4V
Output Sink Current		I_{SINK}	0.12	0.15	—	mA	V_{FB}= 4.5V
High-Voltage Regulator and Start-up							
Input Voltage		V_{IN}	10	—	450	V	I_{IN}< 10 µA; V_{CC} > 9.4V
Input Leakage Current		I_{IN}	—	—	10	µA	V_{DD} > 9.4V
Regulator Turn-off Threshold Voltage		V_{TH}	8.0	8.7	9.4	V	I_{IN}= 10 µA
Undervoltage Lockout		V_{LOCK}	7.0	8.1	8.9	V	—
Supply							
Supply Current		I_{DD}	—	0.75	1.3	mA	C_L< 75 pF
Quiescent Supply Current		I_Q	—	0.55	—	mA	V_{NSD} = 0V
Nominal Bias Current		I_{BIAS}	—	20	—	µA	—
Operating Range		V_{DD}	9.0	—	13.5	V	—
Shutdown Logic							
Shutdown Delay		t_{SD}	—	50	100	ns	C_L= 500 pF, V_{CS} = 0V (Note 1)
NSD Pulse Width		t_{SW}	50	—	—	ns	(Note 1)
RST Pulse Width		t_{RW}	50	—	—	ns	(Note 1)
Latching Pulse Width		t_{LW}	25	—	—	ns	V_{NSD}, V_{RST} = 0V(Note 1)
Input Low Voltage		V_{IL}	—	—	2.0	V	—
Input High Voltage		V_{IH}	7.0	—	—	V	—
Input Current, Input High Voltage		I_{IH}	—	1.0	5.0	µA	V_{IN} = V_{DD}
Input Current, Input Low Voltage		I_{IL}	—	-25	-35	µA	V_{IN} = 0V
Output							
Output High Voltage		V_{OH}	V_{DD}-0.25	—	—	V	I_{OUT} = 10 mA
			V_{DD}-0.3	—	—		I_{OUT} = 10 mA, T_A = -40°C to 125°C
Output Low Voltage		V_{OL}	—	—	0.2	V	I_{OUT} = -10 mA
			—	—	0.3		I_{OUT} = -10 mA, T_A = -40°C to 125°C
Output Resistance	Pull up	R_{OUT}	—	15	25	Ω	I_{OUT} = ±10 mA
	Pull down		—	8.0	20		
	Pull up		—	20	30	Ω	I_{OUT}= ±10 mA, T_A= -40°C to 125°C
	Pull down		—	10	30		
Rise Time		t_R	—	30	75	ns	C_L= 500 pF (Note 1)
Fall Time		t_F	—	20	75	ns	C_L= 500 pF(Note 1)

Note 1: Design guidance only; Not 100% tested in production.

2: Stray capacitance on OSC in pin must be ≤ 5 pF.

TEMPERATURE SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature	T_J	-40	—	125	°C	—
Storage Temperature	T_A	-65	—	150	°C	—
Package Thermal Resistances						
Thermal Resistance, SOIC	θ_{JA}	—	83	v	°C/W	—
Thermal Resistance, PDIP	θ_{JA}	—	51	—	°C/W	—

1.1 Truth Table

TRUTH TABLE

SHUTDOWN	RESET	OUTPUT
H	H	Normal operation
H	H → L	Normal operation, no change
L	H	Off, not latched
L	L	Off, latched
L → H	L	Off, latched, no change

2.0 TYPICAL PERFORMANCE CURVES

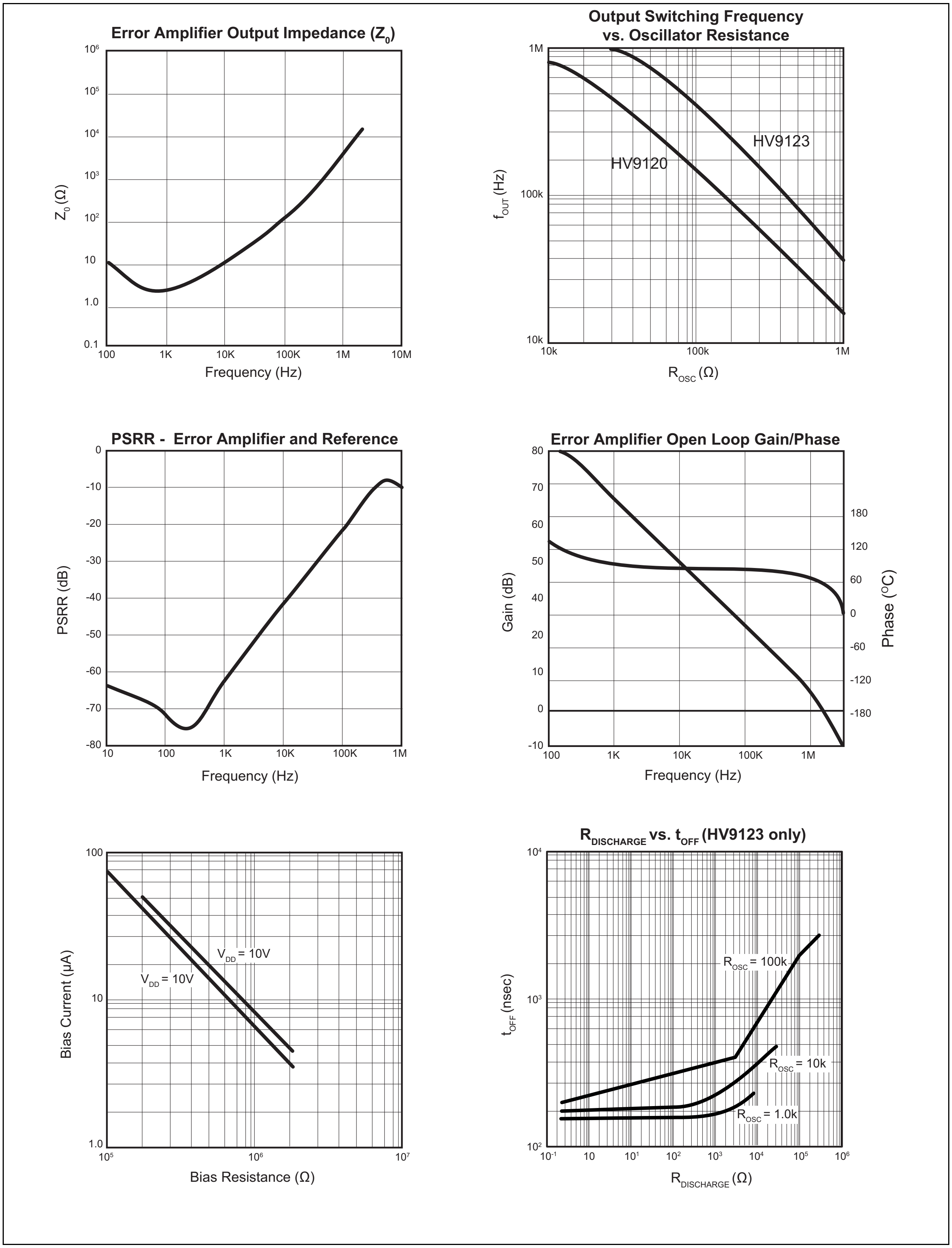


FIGURE 2-1: *Typical Performance Curves.*

3.0 PIN DESCRIPTION

The locations of the pins are listed in Features.

TABLE 3-1: PIN DESCRIPTION

Pin #	Symbol HV9120	Symbol HV9123	Description
1	V_{IN}	V_{IN}	High-voltage, V_{DD} regulator input
2	NC	NC	No connect
3	NC	NC	No connect
4	CS	CS	Current-sense input
5	GATE	GATE	Gate-drive output
6	GND	GND	Ground
7	V_{DD}	V_{DD}	High-voltage, V_{DD} regulator output
8	OSCO	OSCO	Oscillator output
9	OSCI	OSCI	Oscillator input
10	NC	DISC	Oscillator discharge, current set
11	V_{REF}	V_{REF}	4V Reference output Reference voltage level can be overridden by an externally-applied voltage source.
12	NSD	NSD	Active-low input to set shutdown latch
13	RST	RST	Active-high input to reset shutdown latch
14	COMP	COMP	Error-amplified output
15	FB	FB	Feedback-voltage input
16	BIAS	BIAS	Internal bias, current set

4.0 TEST CIRCUITS

The test circuits for characterizing error-amplifier output impedance, Z_{OUT}, and error-amplifier, power-supply rejection ratio (PSRR) are shown in Figure 4-1.

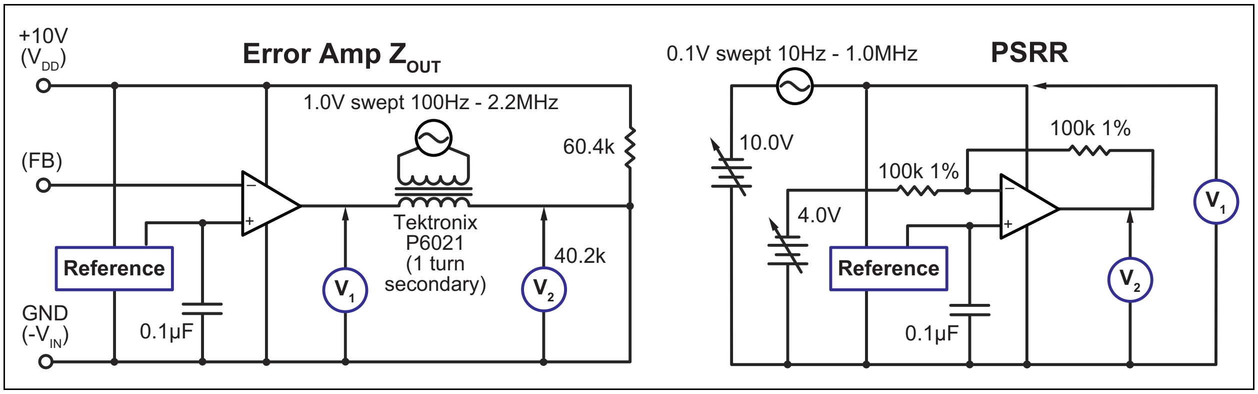


FIGURE 4-1: *Test Circuits.*

5.0 DETAILED DESCRIPTION

5.1 High-Voltage Regulator

The high-voltage regulator included in HV9120 and HV9123 consists of a high-voltage, n-channel, depletion-mode DMOS transistor, driven by an error amplifier, providing a current path between the V_{IN} terminal and the V_{DD} terminal. The maximum current, about 20 mA, occurs when V_{DD} = 0, with current reducing as V_{DD} rises. This path shuts off when V_{DD} rises to somewhere between 7.8 and 9.4V. So, if V_{DD} is held at 10 or 12V by an external source, no current other than leakage is drawn through the high-voltage transistor. This minimizes dissipation.

Use an external capacitor between V_{DD} and GND to store the energy used by the chip in the time between the shutoff of the high-voltage path and the V_{DD} supply's output rising enough to take over powering the chip. This capacitor should have a value of 100X or more the effective gate capacitance of the MOSFET being driven, as well as very good high-frequency characteristics (see the equation below). Ceramic caps work well. Electrolytic capacitors are generally not suitable.

EQUATION 5-1:

$$C_{VDD} \geq 100 \times (\text{gate charge of FETat 10V})$$

The device uses a resistor divider string to monitor V_{DD} for both the Undervoltage Lockout circuit and the shut-off circuit of the high-voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point ensures that the Undervoltage Lockout releases before the FET shuts off.

5.2 Bias Circuit

HV9120 and HV9123 require an external bias resistor connected between the BIAS pin and GND to set currents in a series of current mirrors used by the analog sections of the chip. The nominal external bias current requirement is 15 µA to 20 µA, which can be set by a 390 kΩ to 510 kΩ resistor if V_{DD} = 10V, or a 510 kΩ to 680 kΩ resistor if V_{DD} = 12V. A precision resistor is not required—just ±5% meets the device requirements.

5.3 Clock Oscillator

The clock oscillator of the HV9120 and HV9123 consists of a ring of CMOS inverters, timing capacitors, and a capacitor-discharge FET. A single external resistor between the OSCI and OSCO sets the oscillator frequency (see Figure 2-1, Output Switching Frequency vs Oscillator Resistance).

HV9120 includes a frequency-dividing flip-flop that allows the part to operate with a 50% duty limit. Accordingly, the effective switching frequency of the power converter is half the oscillator frequency (see Figure 2-1, Output Switching Frequency vs Oscillator Resistance).

An internal discharge FET resets the oscillator ramp at the end of the oscillator cycle. The FET is internally connected to GND in HV9120 (50% max duty version), whereas the FET is externally connected to GND, by way of a resistor, in the HV9123 (100% duty version). The resistor programs the oscillator dead time at the end of the oscillator period in HV9123 applications.

The oscillator turns off during shutdown to reduce supply current by about 150 µA.

5.4 Reference

The reference of the HV9120 and HV9123 consists of a band-gap reference, followed by a buffer amplifier, which scales the voltage up to 4.0V. The scaling resistors of the buffer amplifier are trimmed during manufacture so that the output of the error amplifier, when connected in a gain of -1 configuration, is as close to 4.0V as possible. This nulls out the input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4.0V, the feedback voltage required for proper regulation will be 4.0V.

An approximately 50 kΩ resistor is located internally between the output of the reference buffer amplifier and the circuitry it feeds—reference output pin and noninverting input to the error amplifier. This allows overriding the internal reference with a low-impedance voltage source ≤ 6.0V. Using an external reference reinstates the input offset voltage of the error amplifier. Overriding the reference should seldom be necessary.

The reference of the HV9120 and HV9123 is a high-impedance node, and usually there will be significant electrical noise nearby. Therefore, a bypass capacitor between the reference pin and GND is strongly recommended. The reference buffer amplifier is compensated to be stable with a capacitive load of 0.01 µF to 0.1 µF.

5.5 Error Amplifier

The error amplifier in HV9120 and HV9123 is a low-power, differential-input, operational amplifier. A PMOS input stage is used, so the Common-mode range includes ground and the input impedance is high.

5.6 Current Sense Comparators

HV9120 and HV9123 use a dual-comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps, except ESD protection, on the compensation pin.

5.7 Remote Shutdown

The NSD and RST pins control the shutdown latch. These pins have internal, current-source pull-ups so they can be driven from open-drain logic. When not used they should be left open, or connected to V_{DD}.

5.8 Output Buffer

The output buffer of HV9120 and HV9123 is of standard CMOS construction—P-channel pull-up and N-channel pull-down. Thus, the body-drain diodes of the output stage can be used for spike clipping. External Schottky diode clamping of the output is not required.

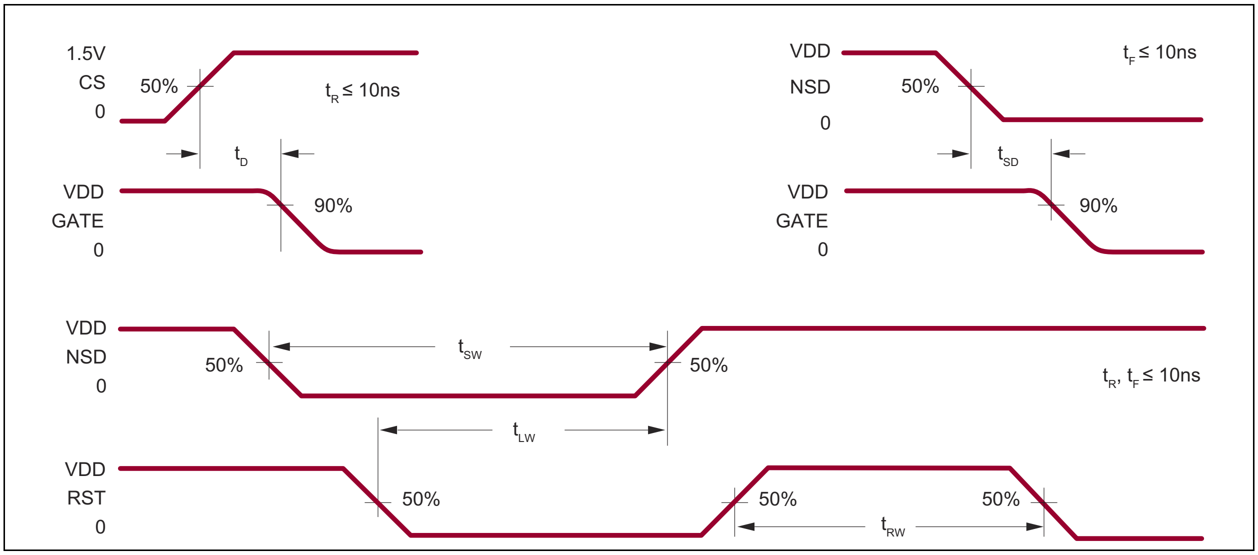
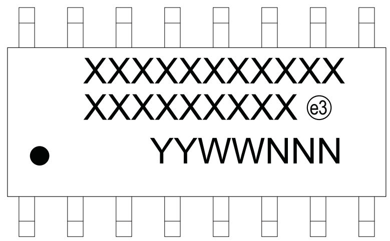


FIGURE 5-1: *Shutdown Timing Waveforms.*

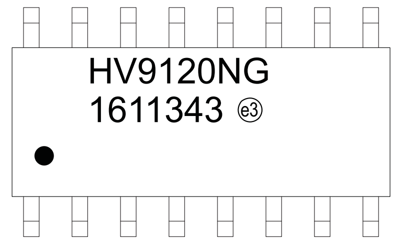
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

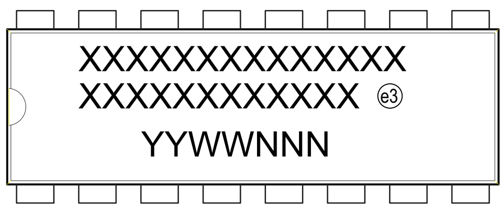
16-lead SOIC



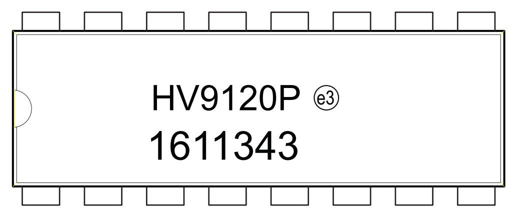
Example



16-lead PDIP



Example

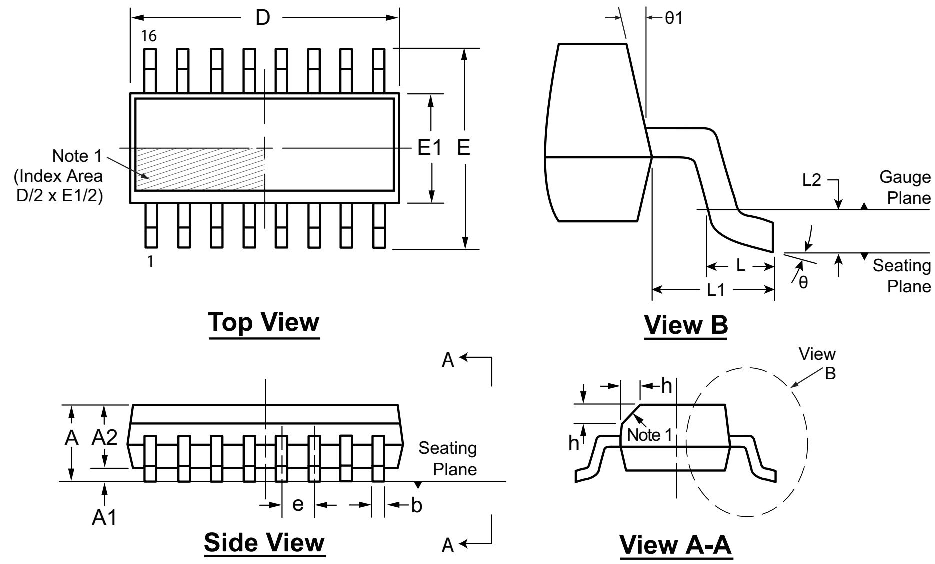


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

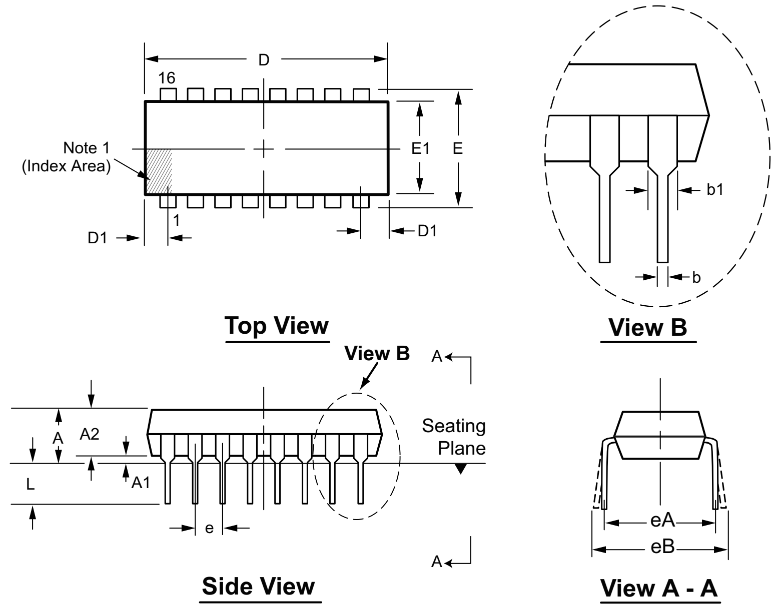
1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

16-Lead PDIP (.300in Row Spacing) Package Outline (P)

.790x.250in body, .210in height (max), .100in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	eA	eB	L
Dimension (inches)	MIN	.130*	.015	.115	.014	.045	.745†	.005	.290†	.240	.100 BSC	.300 BSC	.300*	.115
	NOM	-	-	.130	.018	.060	.790	-	.310	.250			-	.130
	MAX	.210	.035*	.195	.023†	.070	.810†	.050*	.325	.280			.430	.150

JEDEC Registration MS-001, Variation AB, Issue D, June, 1993.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision B (April 2024)

The following is the list of modifications:

- Updated **Product Identification System**.
- Corrected clock and maximum duty version details in the **Features** section.
- Added NC pin to the **Block Diagram HV9120**.
- Minor typographical changes.

Revision A (May 2016)

The following is the list of modifications:

- Updated file to Microchip format.
- Merged Supertex Doc #s DSFP-HV9120 and DSFP-HV9123 to Microchip DS20005519B.
- Revised **Electrical Characteristics** to accommodate the merged products.
- Updated Pin names to reflect new naming convention.
- Significant text changes to **Detailed Description**.
- Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. — **XX** - **X** - **X**

Device | **Package Options** | **Environmental** | **Media Type**

Device:	HV9120	= High-Voltage Current-mode PWM Controller, 10 to 450V input voltage range, 49% duty cycle
	HV9123	= High-Voltage Current-mode PWM Controller, 10 to 450V input voltage range, 99% duty cycle
Package:	NG	= 16-lead SOIC
	P	= 16-lead PDIP
Environmental	G	= Lead (Pb)-free/ROHS-compliant package
Media Type:	(blank)	= 45/Tube for NG package 24/Tube for P package
	M901	= 2600/Reel for NG package
	M934	= 2600/Reel for NG package

Examples:

a) HV9120NG-G — 16-Lead SOIC package, 53/Tube

b) HV9123NG-G — 16-Lead SOIC package, 53/Tube

c) HV9123NG-G-M901 — 16-Lead SOIC package, 2600/Reel

Note: For media types M901 and M934, the base quantity for tape and reel was standardized at 2600/reel. Both options will result in delivery of the same number of parts/reel.

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