ATSAMA5D27-WLSOM1-EK1

ATSAMA5D27-WLSOM1-EK1 User's Guide

Scope

This user's guide provides detailed information on the overall design of the ATSAMA5D27-WLSOM1-EK1 and describes how to use the kit.

The kit is the evaluation platform for the SAMA5D27 System-In-Package (SiP) and SAMA5D27 Wireless System-On-Module (WLSOM1), and comprises:

- a baseboard
- an ATSAMA5D27-WLSOM1 soldered on the baseboard
- an ATSAMA5D27C-LD2G-CU soldered on the SOM
- a USB cable

For the kit overview, see the figure below.

Figure 1. ATSAMA5D27-WLSOM1-EK1 Kit Overview

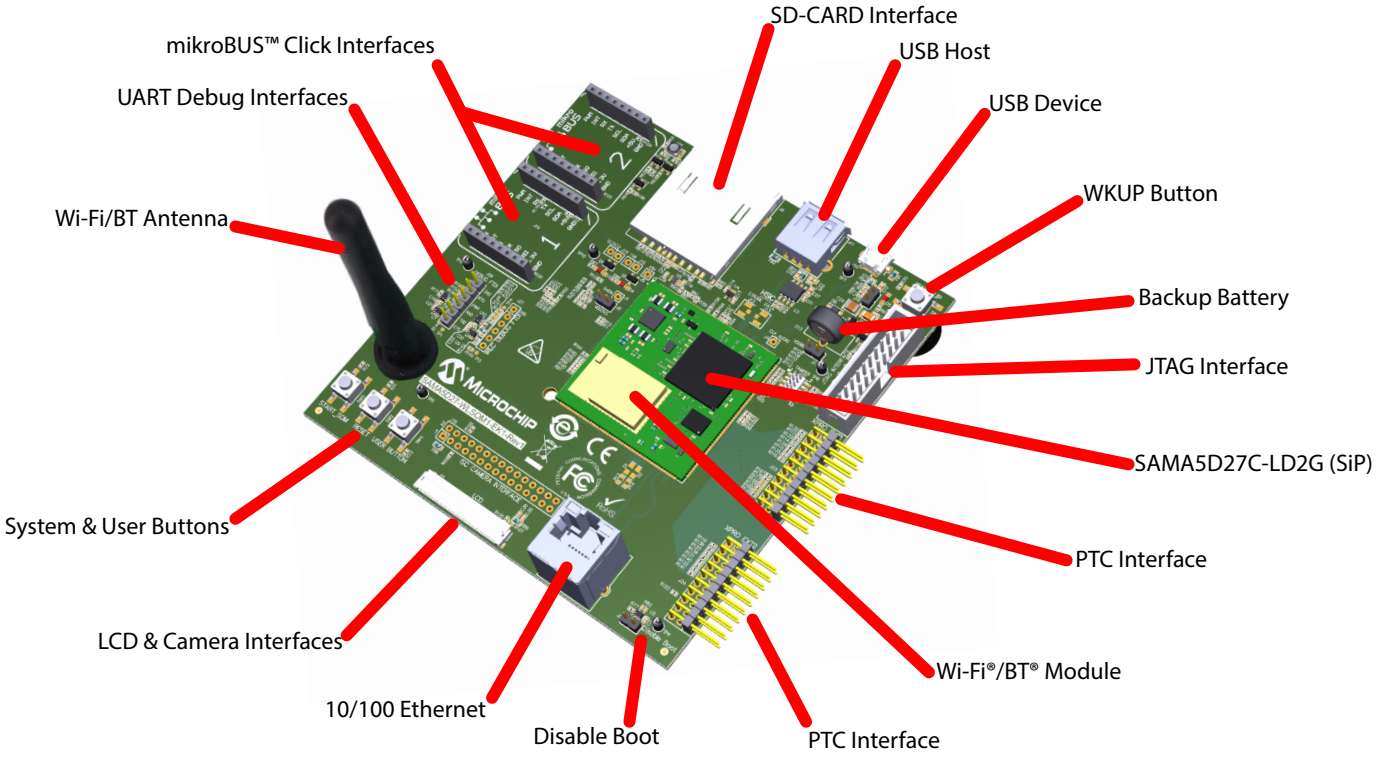


Table of Contents

1. Introduction

1.1 Document Layout

The document is organized as follows:

- Introduction
- Product Overview – Important information about the kit
- Board Components – Specifications of the kit and high-level description of the major components and interfaces
- Installation and Operation – Instructions on how to get started with the kit
- Appendix: Schematics and Layouts – Kit schematics and layout diagrams

1.2 Reference Documents

The following Microchip reference data sheets are available on https://www.microchip.com/ and recommended as supplemental reference resources.

Table 1-1. Reference Data Sheets

Document Title	Available	Document Ref.
SAMA5D2 Series	https://www.microchip.com/wwwproducts/en/ATSAMA5D27	DS60001476
ATSAMA5D27-WLSOM1	https://www.microchip.com/wwwproducts/en/ATSAMA5D27-WLSOM1	DS60001590
ATWILC3000-MR110UA	https://www.microchip.com/wwwproducts/en/ATWILC3000	DS70005327
SAMA5D2 System-In-Package (SiP) with LPDDR2	https://www.microchip.com/wwwproducts/en/ATSAMA5D27C-LD2G	DS60001484

2. Product Overview

2.1 Kit Contents

The kit includes the following:

- One baseboard with soldered ATSAMA5D27-WLSOM1
- One USB cable
- Wireless antenna set

2.2 Features

The kit comprises a baseboard with a soldered ATSAMA5D27-WLSOM1 module. The module features a SAMA5D27-LD2G-CU SiP embedding a 2-Gbit LPDDR2 SDRAM. The ATSAMA5D27-WLSOM1 module offers a reliable and cost-effective embedded platform for building end products, as well as a small form factor, complemented by many connectivity interfaces. The ATSAMA5D27-WLSOM1 module is a fully-featured industrially-certified single board computer designed for integration into customer applications.

The ATSAMA5D27-WLSOM1 module is a purpose-built small footprint hardware platform equipped with a wide array of high-speed connectivity engineered to support various applications such as IoT endpoints, wearables, appliances or industrial equipment.

The ATSAMA5D27-WLSOM1 module integrates a 2-Gbit LPDDR2 SDRAM, a Secure Element device, a Power Management IC, a Wi-Fi®/Bluetooth® module, a QSPI memory and a 10/100 Mbps Ethernet Phy.

94 GPIO pins are provided by the ATSAMA5D27-WLSOM1 module for general use in the system. All GPIO pins are independent and can be configured as inputs or outputs, with or without pull-up/pull-down resistors.

The baseboard features a wide range of peripherals, as well as a user interface and expansion options, including two mikroBUS™ click interface headers to support over 700 MikroElektronika Click boards™.

Table 2-1. Baseboard Features

Characteristics	Specifications	Components
USB Com Port	One USB Device	Micro-AB type USB connector
	One USB Host	Type A connector
	One USB HSIC	2 U.FL connectors (Not populated)
Ethernet	One Ethernet interface	RJ45 connector
Video	One LCD RGB 18-bit interface	50-pin FPC connector
	One ISC 12-bit camera interface	2x15 male connector (Not populated)
Storage	One standard SD card interface	With 3.3V/1.8V power switch
Debug Port	One JTAG interface	2x10 male connector
	One UART Interface	2x6 male connector
	One WILC UART Interface	2x6 male connector (Not populated)
Board Monitor	One RGB (Red, Green, Blue) LED	–
	Four push button switches	nSTART_SOM, Reset, Wakeup, User-free

.....continued		
Characteristics	**Specifications**	**Components**
Expansion	One tamper connector Two mikroBUS interfaces Two Xpro PTC Connectors	10-pin male connector 2x8-pin female connector Two 2x10 male connectors
Board Supply	From USB A	5 VDC
Power Saving	5.5V SuperCap	–

Refer to www.microchip.com for:

- Sample code and technical support
- Linux® software and demos

2.3 Kit Specification

Table 2-2. Kit Specification

Characteristics	Specifications
Board supply voltage	USB-powered
Temperature	Operating: 0°C to +70°C Storage: –40°C to +85°C
Relative humidity	0 to 90% (non-condensing)
Baseboard dimensions	120 × 120 × 20 mm
RoHS status	Compliant
Board marking	SAMA5D27-WLSOM1-EK1

2.4 Power Source

The kit can only be supplied by USB Port Device (J10) interface.

Table 2-3. Electrical Characteristics

Electrical Parameter	Value
Maximum Input Voltage	5.5V
Typical Input Voltage	5.0V
Maximum Input Current	2A
I/O Voltage (on-board signals)	3.3V

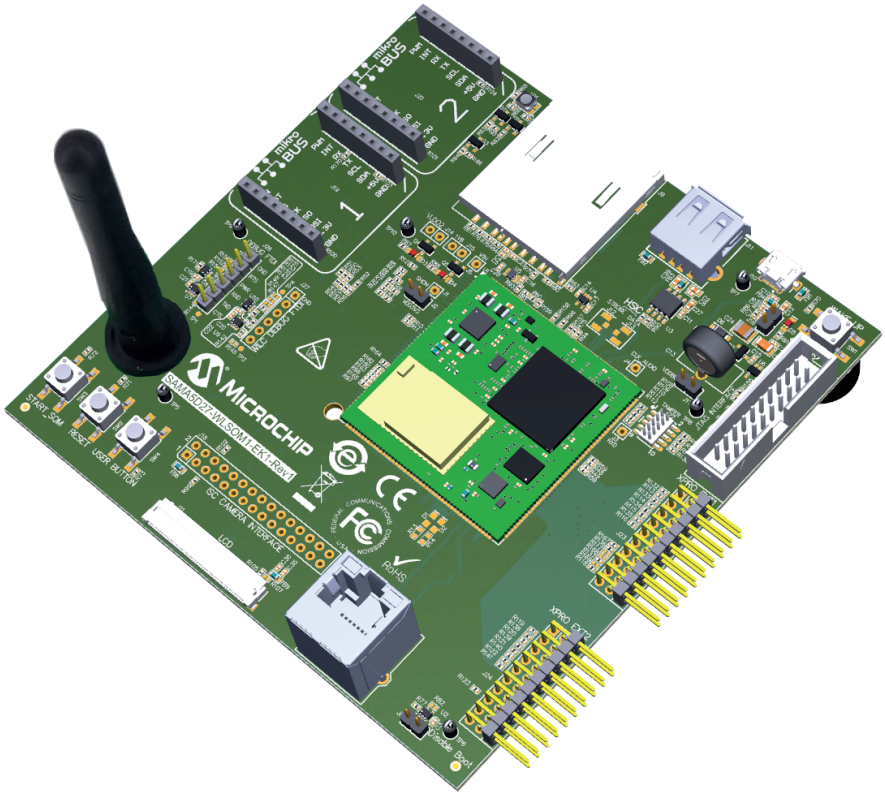
3. Baseboard Components

This section covers the specifications of the ATSAMA5D27-WLSOM1-EK1 and provides a high-level description of the baseboard's major components and interfaces. This document is not intended to provide a detailed documentation about the processor or about any other component used on the baseboard. It is expected that the user will refer to the appropriate documents of these devices to access detailed information.

3.1 Baseboard Overview

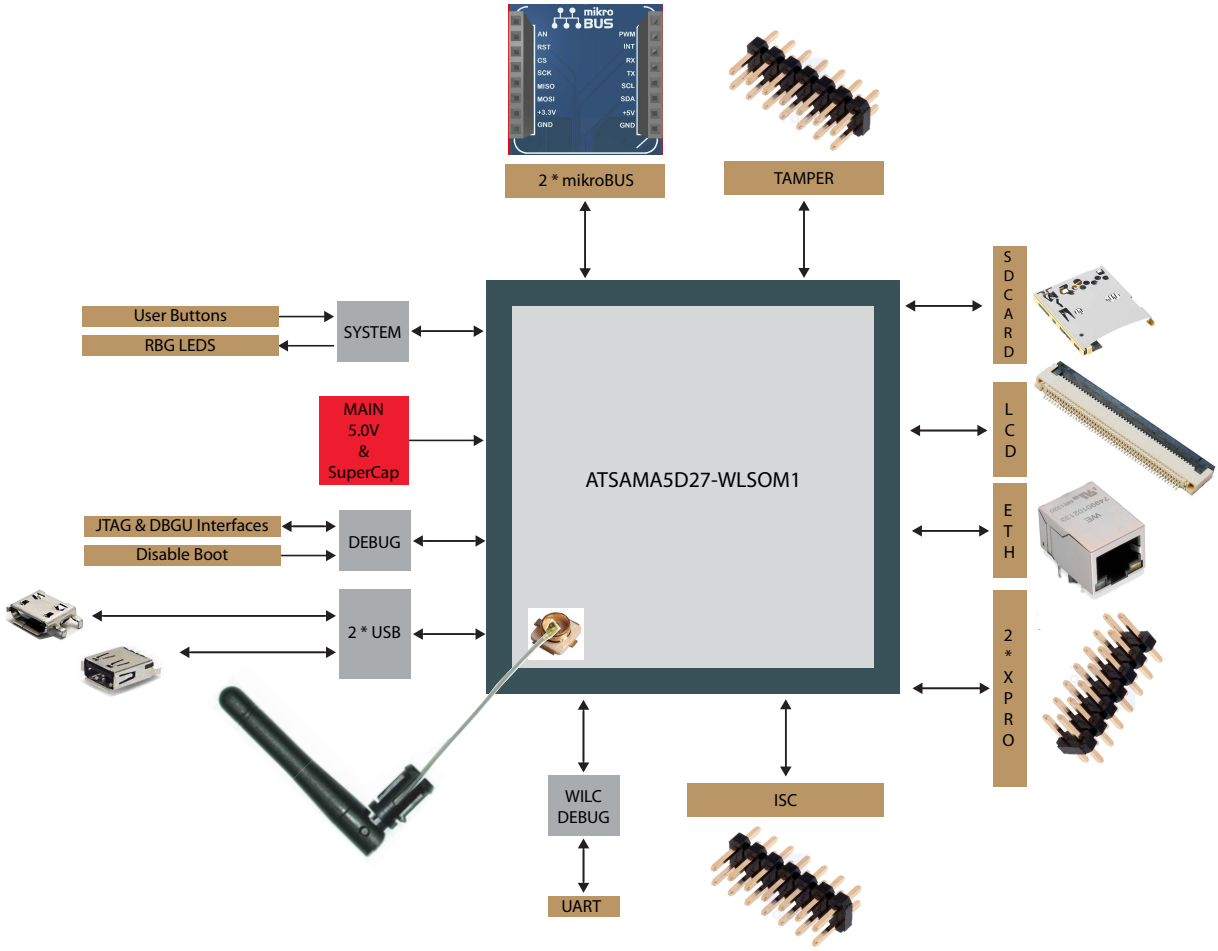
The fully-featured ATSAMA5D27-WLSOM1-EK1 integrates multiple peripherals and interface connectors, as shown in the figure below.

Figure 3-1. ATSAMA5D27-WLSOM1-EK1 Baseboard Overview



The following picture illustrates the kit block diagram.

Figure 3-2. ATSAMA5D27-WLSOM1-EK1 Block Diagram



3.2 Default Jumper Settings

The figure below shows the default jumper settings. Jumpers in red are configuration items and current measurement points. The following table describes the functionality of the jumpers.

Figure 3-3. Default Jumper Settings

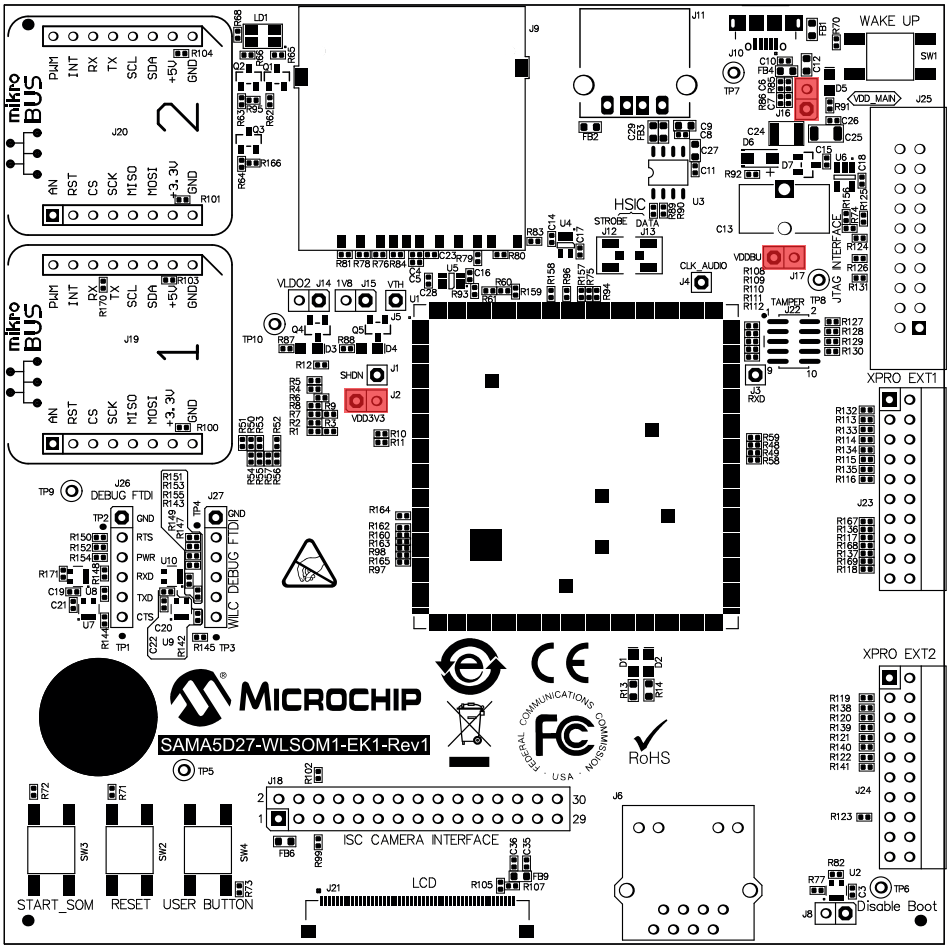


Table 3-1. Default Jumper Settings

Jumper	Default	Function
J2	Closed	VDD_3V3 WLSOM1 Current Measurement
J8	Open	Disable QSPI Boot Memory
J16	Closed	VDD_MAIN WLSOM1 Current Measurement
J17	Closed	VDDBU WLSOM1 Current Measurement

3.3 Baseboard Connectors

The following table describes the interface connectors on the ATSAMA5D27-WLSOM1-EK1.

Table 3-2. Baseboard Interface Connectors

Connector	Interfaces to
J1	SHDN Signal Supervising (Not populated)
J2	VDD_3V3 WLSOM1 Current Measurement
J3	RXD Signal Input (Not populated)
J4	CLK_AUDIO Signal Supervising (Not populated)

.....continued	
Connector	**Interfaces to**
J5	VTH Signal Supervising (Not populated)
J6	Ethernet RJ45 connector
J8	Disable QSPI Boot Memory (closed=disabled)
J9	Standard SDMMC0 connector
J10	USB-A MicroAB connector
J11	USB-B type A connector
J12	HSIC Strobe Line U.FL connector (Not populated)
J13	HSIC Data Line U.FL connector (Not populated)
J14	VLDO2 Voltage Measurement (Not populated)
J15	VDD_1V8 Voltage Measurement (Not populated)
J16	VDD_MAIN WLSOM1 Current Measurement
J17	VDDBU WLSOM1 Current Measurement
J18	ISC connector (Not populated)
J19	mikroBUS1 connectors
J20	mikroBUS2 connectors
J21	Expansion TFT LCD connector for display module
J22	Tamper and analog comparator connector
J23	Expansion XPRO 1 connector for PTC features
J24	Expansion XPRO 2 connector for PTC features
J25	JTAG Debug Connector
J26	UART FTDI Debug Connector
J27	WILC FTDI Debug Connector (Not populated)

3.4 Function Blocks

3.4.1 Wireless SOM (ATSAMAD27-WLSOM1)

The ATSAMA5D27-WLSOM1 main features are listed below.

Refer to the ATSAMA5D27-WLSOM1 data sheet for more information.

3.4.1.1 Features

- System-In-Package (ATSAMA5D27C-LD2G-CU) Including:
  - Arm® Cortex®-A5 processor-based SAMA5D27 MPU
  - 2 Gbit LPDDR2 SDRAM
- On-Board Power Management Unit (MCP16502AC-E/S8B)
- 64 Mb Serial Quad I/O Flash Memory (SST26VF064BEUIT-104I/MF) with Embedded EUI-48™ and EUI-64™ MAC Addresses
- IEEE® 802.11 b/g/n Wi-Fi plus Bluetooth (Wi-Fi/BT) Module (ATWILC3000-MR110UA)
- 10Base-T/100Base-TX Ethernet PHY (KSZ8081RNAIA)
- ATECC608A Secure Element

- MEMS Oscillators for Clock Generation
- 40.8 x 40.8 mm Module, Pitch 0.8mm, Solderable Manually for Prototyping
- 94 I/Os
- Up to 7 Tamper Pins
- One USB Device, one USB Host and one HSIC Interface
- Shutdown and Reset Control Pins
- Operational Specifications:
  - Main operating voltage: 3.0V to 5.5V ± 5%
  - Temperature range: 0°C to +70°C
  - Integrated oscillators, internal voltage regulators
  - Multiple interfaces and I/Os for easy application development

3.4.2 Power Supply Topology

3.4.2.1 Input Power

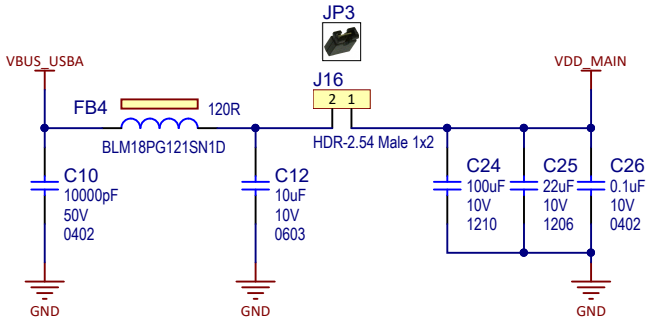
The ATSAMA5D27-WLSOM1-EK1 power source can come through a USB connector (J10) connected to a PC. This USB power source is sufficient to supply the board in most applications.

Important: In case of an external device connected through the USB-B port, it is recommended to use the 5V power supply input with an AC/DC wall adapter for the entire system rather than a PC or a USB hub, which are limited to 500 mA typical.

Jumper J16 is used to perform VDD_MAIN current measurements on the baseboard.

The following figure is a schematic of the power source.

Figure 3-4. VDD_MAIN Input Powering



3.4.2.2 Power Supply Requirements and Restrictions

Detailed information on the device power supplies is provided in tables “SAMA5D2 Power Supplies” and “Power Supply Connections” in the SAMA5D2 Series datasheet.

3.4.2.3 Power-up and Power-down Considerations

Power-up and power-down considerations are described in section “Power Considerations” of the SAMA5D2 Series datasheet.

Note: The power-up and power-down sequences provided in the SAMA5D2 Series datasheet must be respected for reliable operation of the device. These are respected by the on-board MCP16502.

3.4.2.3.1 LPDDR2 Power-Off Sequence

The LPDDR2 power-off sequence must be controlled by software to preserve the LPDDR2 device.

In this sequence, the CKE signal should be low during the full period the power rails are powering down.

The power failure can be controlled by the embedded Voltage Supervisor (MIC842) and handled at system level (IRQ on PD31). The LPDDR2 power-off sequence is applied using the bit LPDDR2_LPDDR3_PWOFF in the MPDDRC Low-Power register (MPDDRC_LPR).

For more information, refer to the following documents:

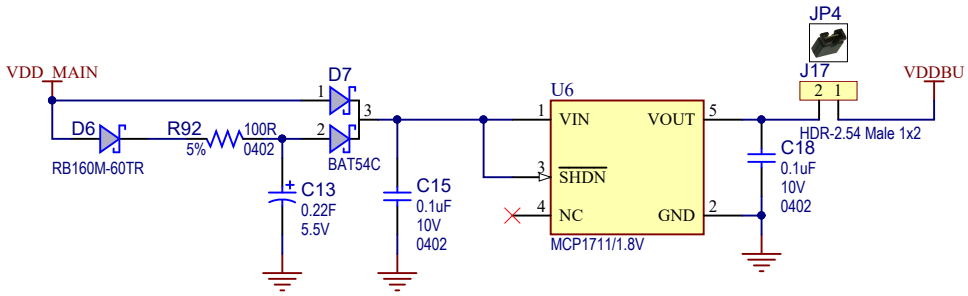
- SAMA5D2 Series Data sheet available on https://www.microchip.com/, sections *LPDDR2 Power Fail Management* and *MPDDRC Low-Power Register*
- Jedec Standard *Low Power Double Data Rate 2 (LPDDR2)*, JESD209-2B

Note: An uncontrolled power-off sequence can be applied only up to 400 times in the life of an LPDDR2 device.

3.4.2.4 Backup Power Supply

The ATSAMA5D27-WLSOM1-EK1 features a power source in order to permanently power the backup area of the SAMA5D2 device (refer to the SAMA5D2 Series datasheet). A super capacitor (C13) sustains such permanent power to VDDBU when all system power sources are off.

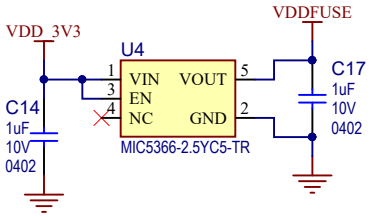
Figure 3-5. VDDBU Powering Options



3.4.2.5 VDDFUSE Regulator

The ATSAMA5D27-WLSOM1-EK1 board embeds an LDO that delivers 2.5V to VDDFUSE for Fuse box programming and for Secure Mode switching.

Figure 3-6. VDDFUSE Powering Options

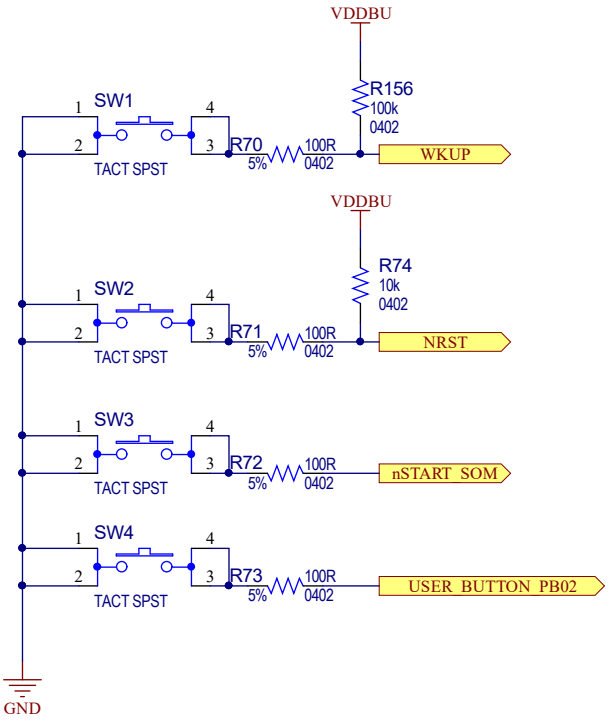


3.4.3 Push Button Switches

The ATSAMA5D27-WLSOM1-EK1 features four push buttons:

- SW1– Wake-up push button connected to the SAMA5D27 WKUP pin, used to exit the processor from Backup mode.
- SW2 – Reset push button. When pressed and released, the baseboard is reset.
- SW3 – Power-on/off button
- SW4 – User momentary push button connected to PIO PB2

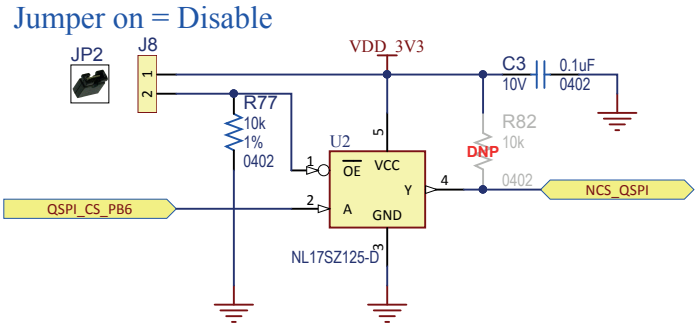
Figure 3-7. System and User Push Buttons



3.4.4 Disable Boot

One jumper (J8) controls the selection (CS#) of the bootable memory components (QSPI) using a noninverting 3-state buffer.

Figure 3-8. QSPI CS Disable Boot



The rule of operation is:

- SW2 (RESET) pressed and J8 open = booting from QSPI on WLSOM1
- SW2 (RESET) pressed and J8 closed = booting from external QSPI. The QSPI on WLSOM1 is disabled.

Refer to the SAMA5D2 Series data sheet for more information on standard boot strategies and sequencing.

3.4.5 Secure Digital Multimedia Card (SDMMC) Interface

The SD (Secure Digital) Card is a non-volatile memory card format used as a mass storage memory in mobile devices.

3.4.5.1 Secure Digital Multimedia Card (SDMMC) Controller

The ATSAMA5D27-WLSOM1-EK1 features two Secure Digital Multimedia Card (SDMMC) interfaces that support the MultiMedia Card (e.MMC) Specification V4.41, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 Specification.

- The SDMMC0 interface is connected to a standard SD card interface.
- The SDMMC1 interface is connected to a WILC3000.

3.4.5.2 SDMMC0 Card Connector (J9)

The board provides a standard MMC/SD card connector, connected to SDMMC0. The SDMMC0 communication is based on an 8-pin interface (clock, command, write protect, power switch and data (4)). A card detection switch is included.

The figure below illustrates the SDMMC0 interface implementation.

Figure 3-9. SDMMC0 Schematic

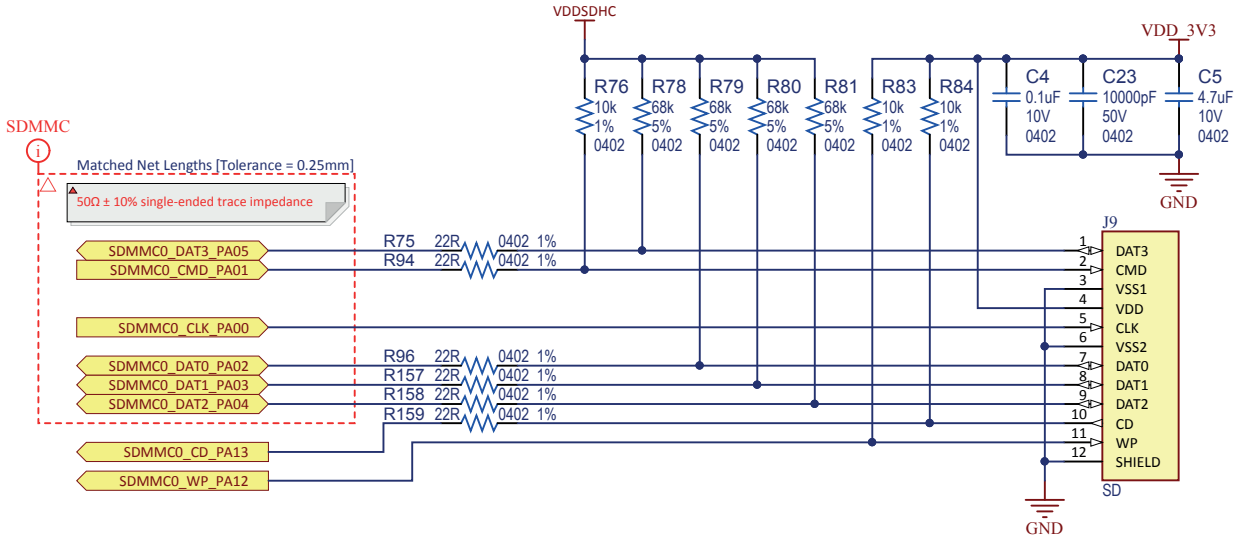


Figure 3-10. VDDSDHC Power Switch Schematic

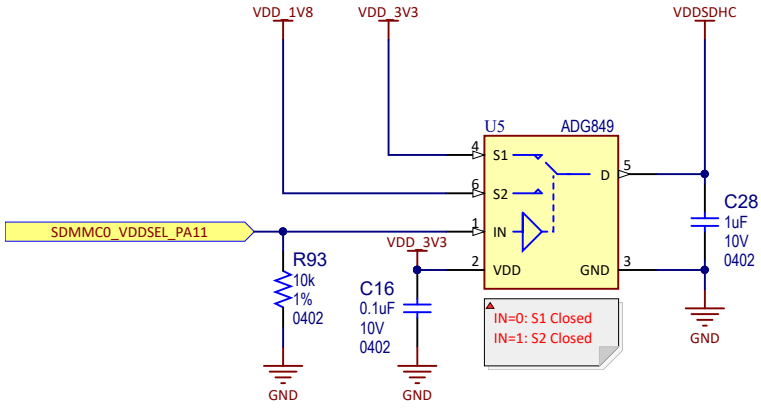
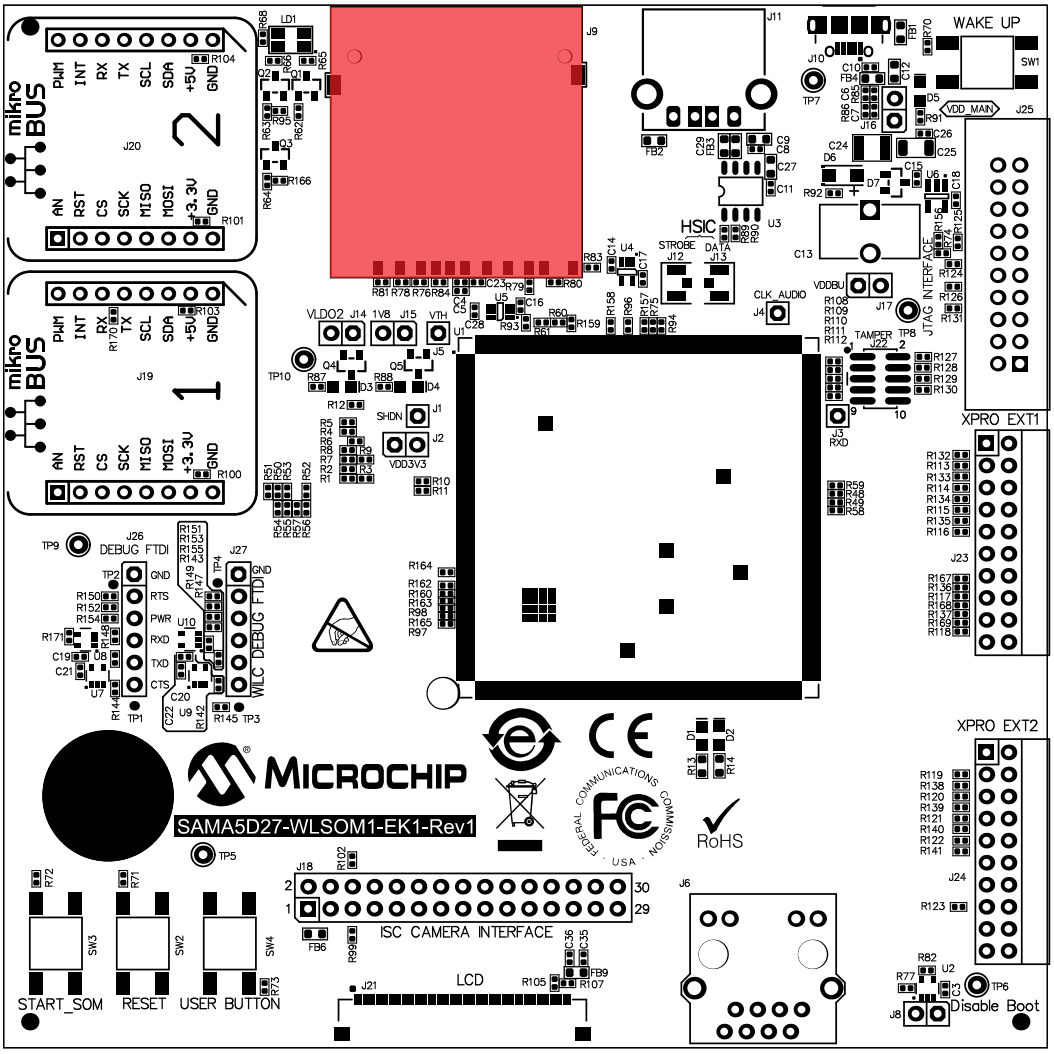


Figure 3-11. Standard SD Socket J9 Location



The table below describes the pin assignment of SD-CARD connector J9.

Table 3-3. SD-CARD Connector Pin Assignment

Pin No	Mnemonic	PIO	Signal Description
1	DAT3	PA5	Data Line
2	CMD	PA1	Command/Response Line
3	VSS1	–	GROUND
4	VDDSDHC	–	Power Line (3.3V/1.8V)
5	CLK	PA0	Clock Line
6	VSS2	–	GROUND
7	DAT0	PA2	Data Line
8	DAT1	PA3	Data Line
9	DAT2	PA4	Data Line
10	CD	PA13	Card Detect

.....continued			
Pin No	**Mnemonic**	**PIO**	**Signal Description**
11	WP	PA12	Write Protect
12	SHIELD	–	GROUND

3.4.6 Communication Interfaces

This section describes the signals and connectors related to the ETH and USB communication interfaces.

3.4.6.1 Ethernet 10/100 (GMAC) Port

The on-board ATSAMA5D27-WLSOM1 module integrates a 10/100 Mbps Ethernet Phy (KSZ8081RNA) allowing direct connection to any 10/100 Mbps Ethernet-based Local Area Network, for full interaction with local servers and wide area networks such as the Internet.

ETH signals from the WLSOM1 are connected to a RJ45 MagJack. Additionally, for monitoring and control purposes, a LED functionality is carried on the RJ45 connector to indicate link status.

Figure 3-12. Ethernet 10/100 Interface Schematic

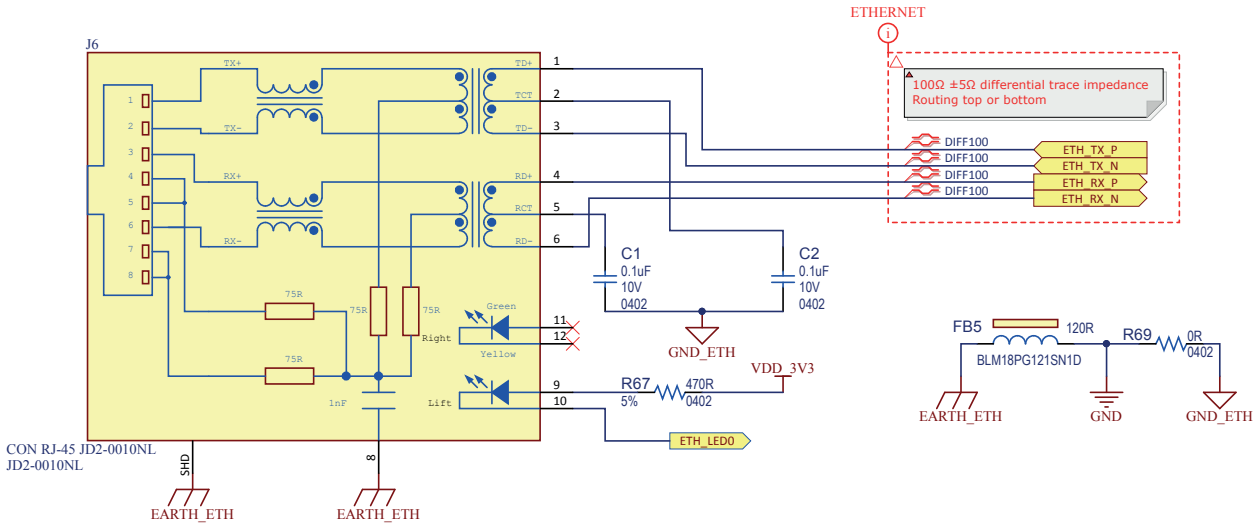
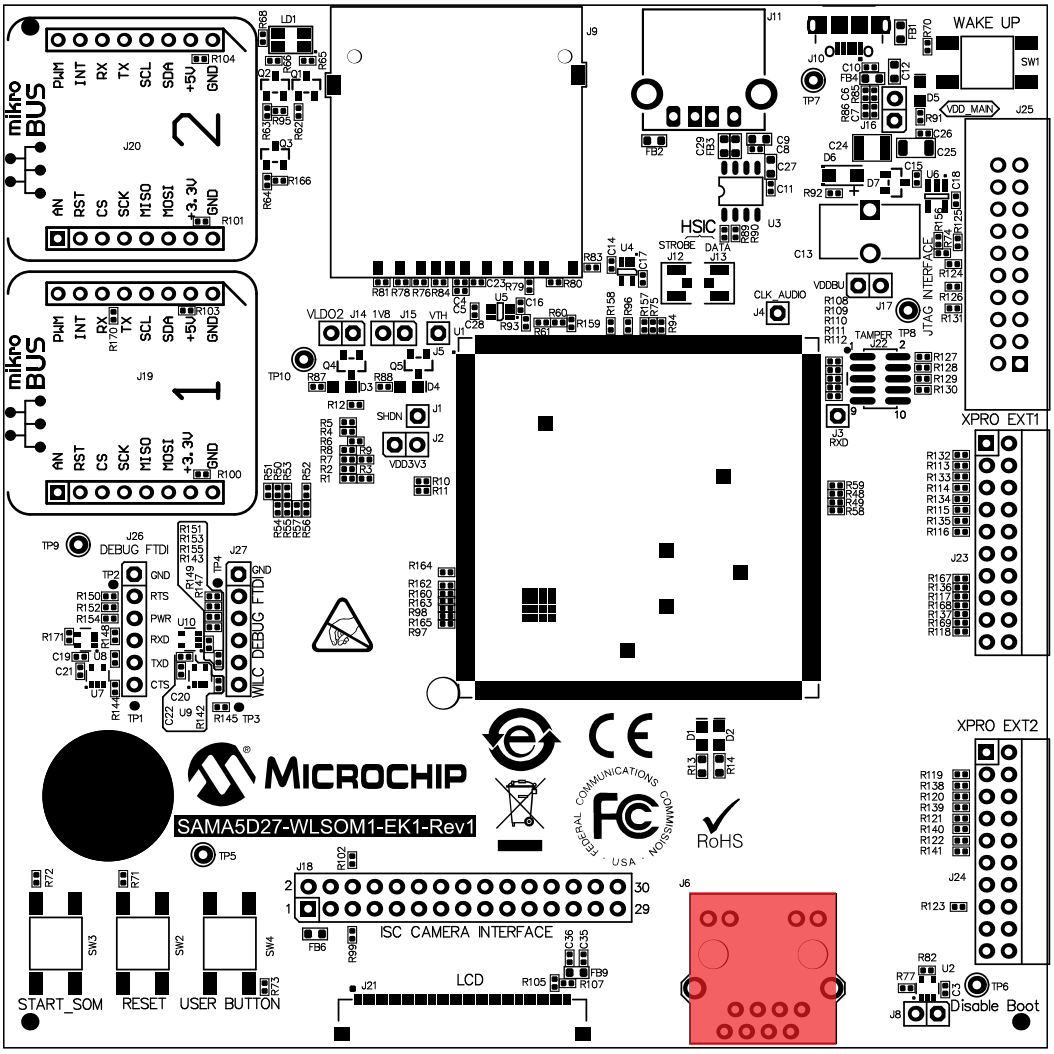


Figure 3-13. Ethernet 10/100 Connector J6 Location



The table below describes the pin assignment of Ethernet connector J6.

Table 3-4. Ethernet RJ45 Connector Pin Assignment

Pin No	Mnemonic	Signal Description
1	TD+	Transmit positive differential pair
2	TCT	Transmit differential pair decoupling capacitor
3	TD-	Transmit negative differential pair
4	RD+	Receive positive differential pair
5	RCT	Receive differential pair decoupling capacitor
6	RD-	Receive negative differential pair
8	EARTH	GROUND
9	YA	Yellow LED anode. Connected to ETH_LED0
10	YK	Yellow LED cathode. Connected to VDD_3V3 through 470R resistor.
11	GA	Green LED anode (Not connected)

.....continued		
Pin No	**Mnemonic**	**Signal Description**
12	GK	Green LED cathode (Not connected)
SHD	EARTH	GROUND

3.4.6.2 USB Interfaces

The USB (Universal Serial Bus) is a hot-pluggable general-purpose high-speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High-Speed USB). A USB host bus connector uses four pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin.

The ATSAMA5D27-WLSOM1-EK1 features three USB communication ports named USB-A to USB-C:

- USB-A device interface
  - One USB device standard Micro-AB connector
  - Offers a VBUS detection function through the R81-R83 resistor ladder
  - Used as a secondary power source and as a communication link for the ATSAMA5D27-WLSOM1-EK1, and derives power from the PC over the USB cable. In most cases, this port is limited to 500 mA.
- USB-B (host port B high- and full-speed interface)
  - One USB host type C connector
  - Equipped with a 500 mA high-side power switch
- USB-C (High-Speed Inter-Chip/HSIC port)
  - One USB high-speed host port with an HSIC interface
  - Connected to 2 U.FL connectors

3.4.6.3 USB-A Interface

The figure below shows the USB implementation on the USB-A port terminated on a Micro-AB type USB connector.

Figure 3-14. USB-A Device Interface Schematic

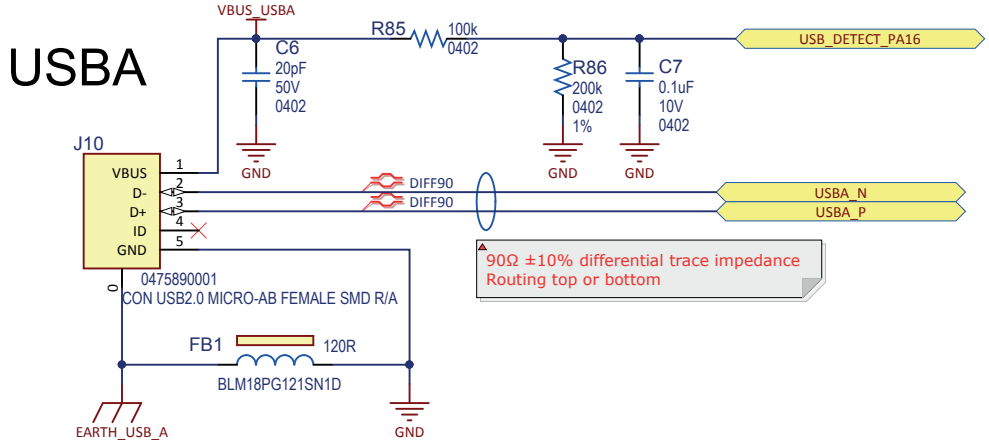
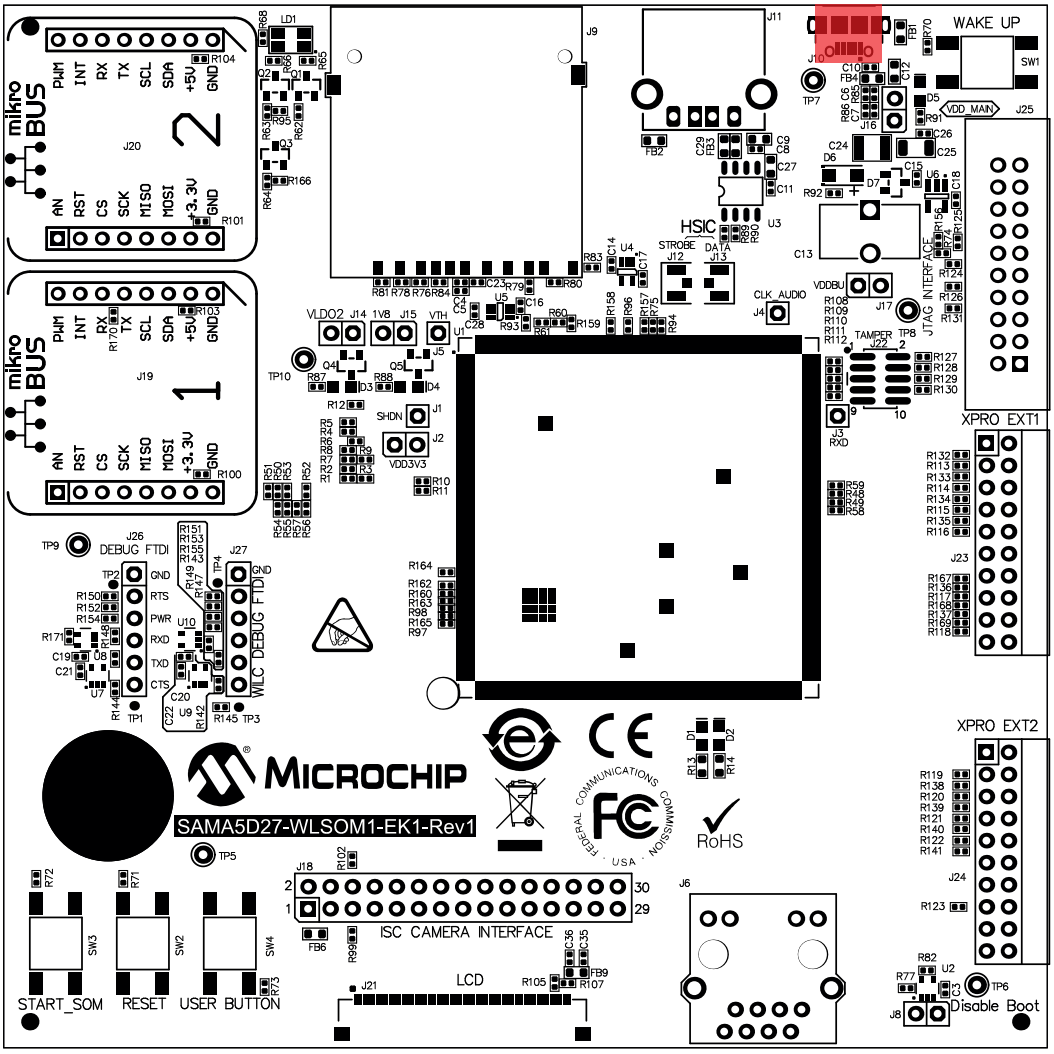


Figure 3-15. USB-A Device Connector J10 Location



The table below describes the pin assignment of USB-A connector J10.

Table 3-5. USB-A Pin Assignment

Pin No	Mnemonic	PIO	Signal Description
1	VBUS_USBA	–	Main 5V Input Supply
2	USBA_N	HHSDMA	USB Host Port A High Speed Data -
3	USBA_P	HHSDPA	USB Host Port A High Speed Data +
4	ID	–	Not connected
5	GND	–	GROUND
–	USB_DETECT	PA16	VBUS Insertion Detection

3.4.6.4 USB-B Interface and Power Switch

The figure below shows the USB implementation on the USB-B port terminated on USB Type A connector J11.

Figure 3-16. USB-B Host Interface Schematic

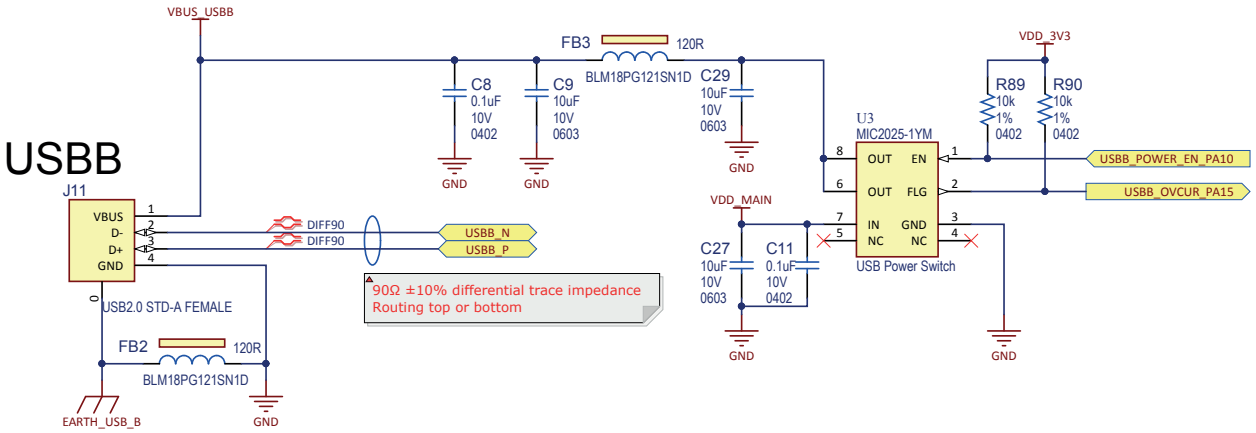
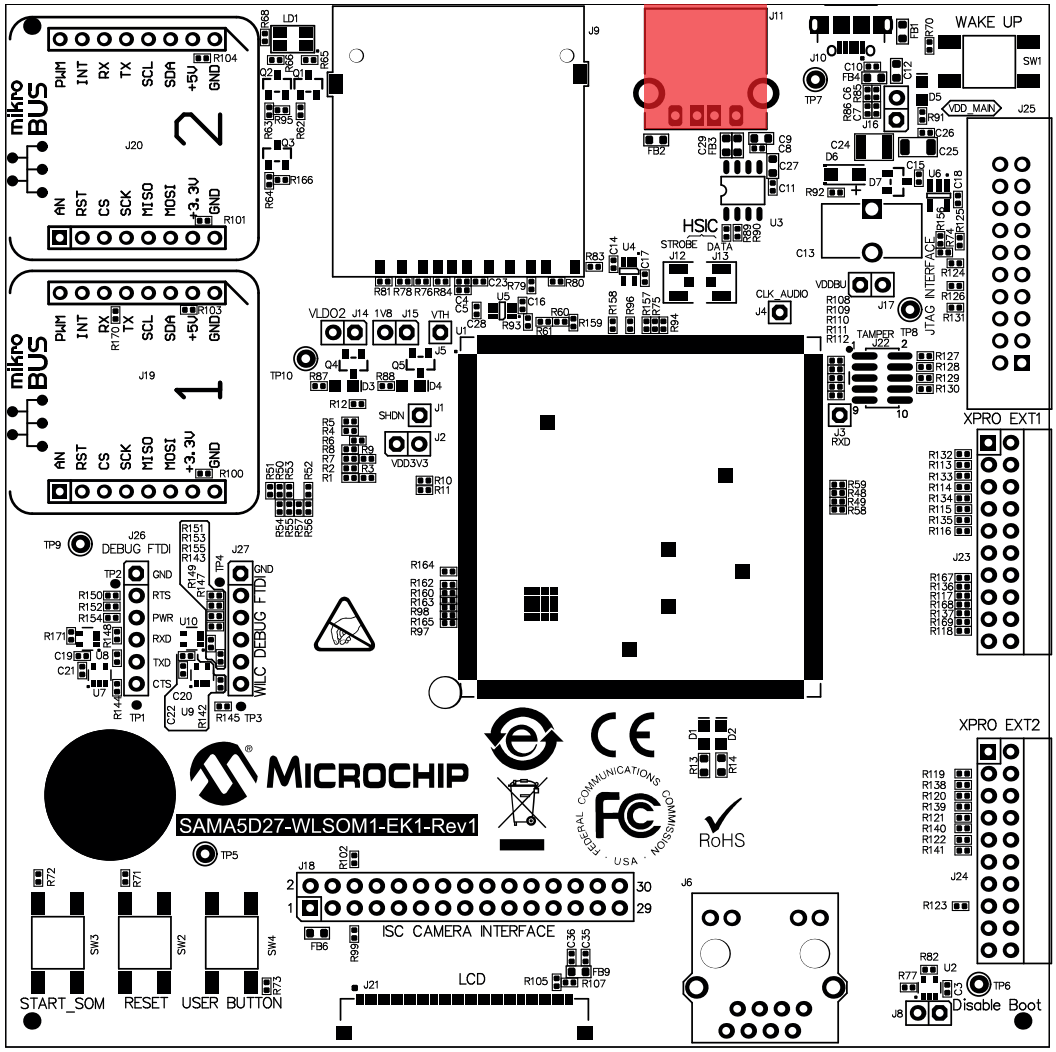


Figure 3-17. USB-B Host Connector J11 Location



The table below describes the pin assignment of USB-B connector J11.

Table 3-6. USB-B Pin Assignment

Pin No	Mnemonic	PIO	Signal Description
1	VBUS_USBB	–	Main 5V Input Supply
2	USBB_N	HHSDMB	USB Host Port B High Speed Data -
3	USBB_P	HHSDPB	USB Host Port B High Speed Data +
4	GND	–	GROUND
–	USBB_POWER_EN	PA14	USBB Power Switch Enable
–	USBB_OVCUR	PA15	VBUS Over Current Interrupt

3.4.6.5 HSIC Interface

High-Speed Inter-Chip (HSIC) is a standard for USB chip-to-chip interconnect with a 2-signal (strobe, data) source synchronous serial interface using 240 MHz DDR signaling to provide only high-speed 480 Mbps data rate.

The interface operates at high speed, 480 Mbps, and is fully compatible with existing USB software stacks. It meets all data transfer needs through a single unified USB software stack.

The HSIC port is connected to 2 U.FL connectors (not populated by default).

Figure 3-18. HSIC Interface Schematic

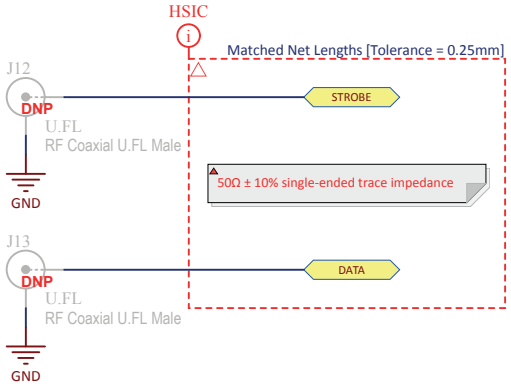
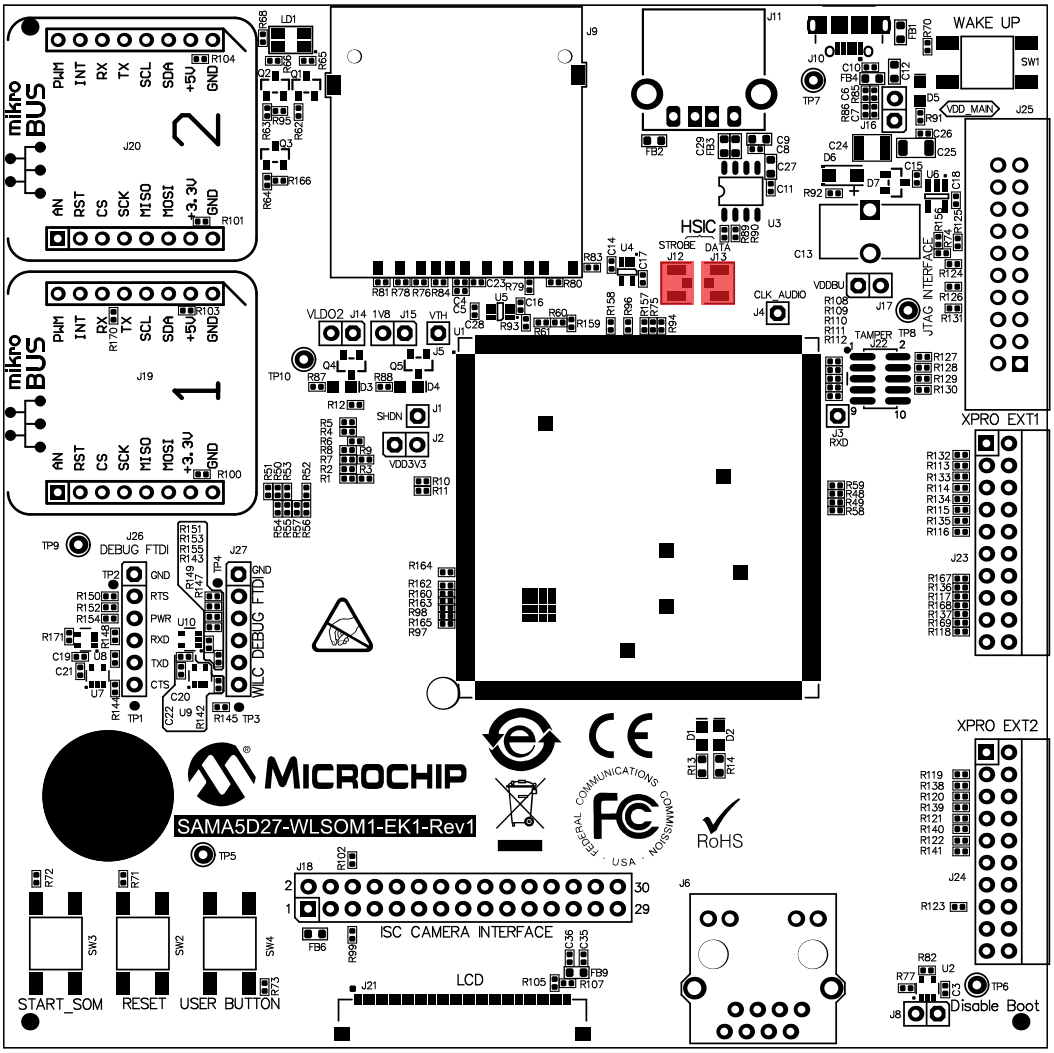


Figure 3-19. HSIC Connectors J12 and J13 Location



3.5 External Interfaces

3.5.1 LCD TFT Interface

The ATSAMA5D27-WLSOM1-EK1 provides an FPC connector with 18 bits of data and control signals to the LCD interface.

This connector is used to connect to an LCD display type AC320005-5.

A 50-pin FPC (J21) header is provided on the baseboard to interface the LCD module with the 18-bit parallel RGB mode and is used to connect to an LCD display type AC320005-5.

The connector provides two PIOs as interrupts, one SPI and a TWI port to interface the MaXTouch® touch controller or QTouch® button controller embedded on the LCD module.

In order to operate correctly from the processor with various LCD modules, two voltage lines are available: 3.3V and 5VCC (default). Both are selected by 0R resistors R107 and FB9.

Figure 3-20. LCD Interface Schematic

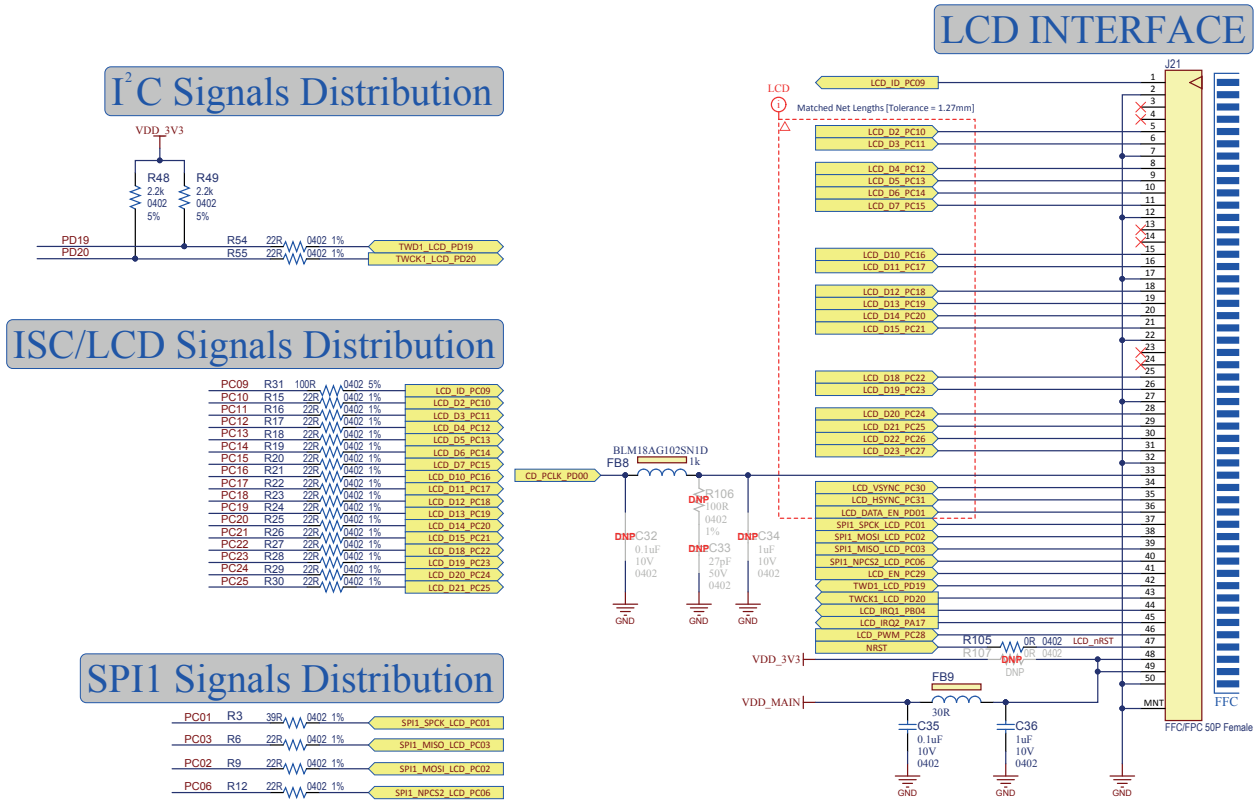
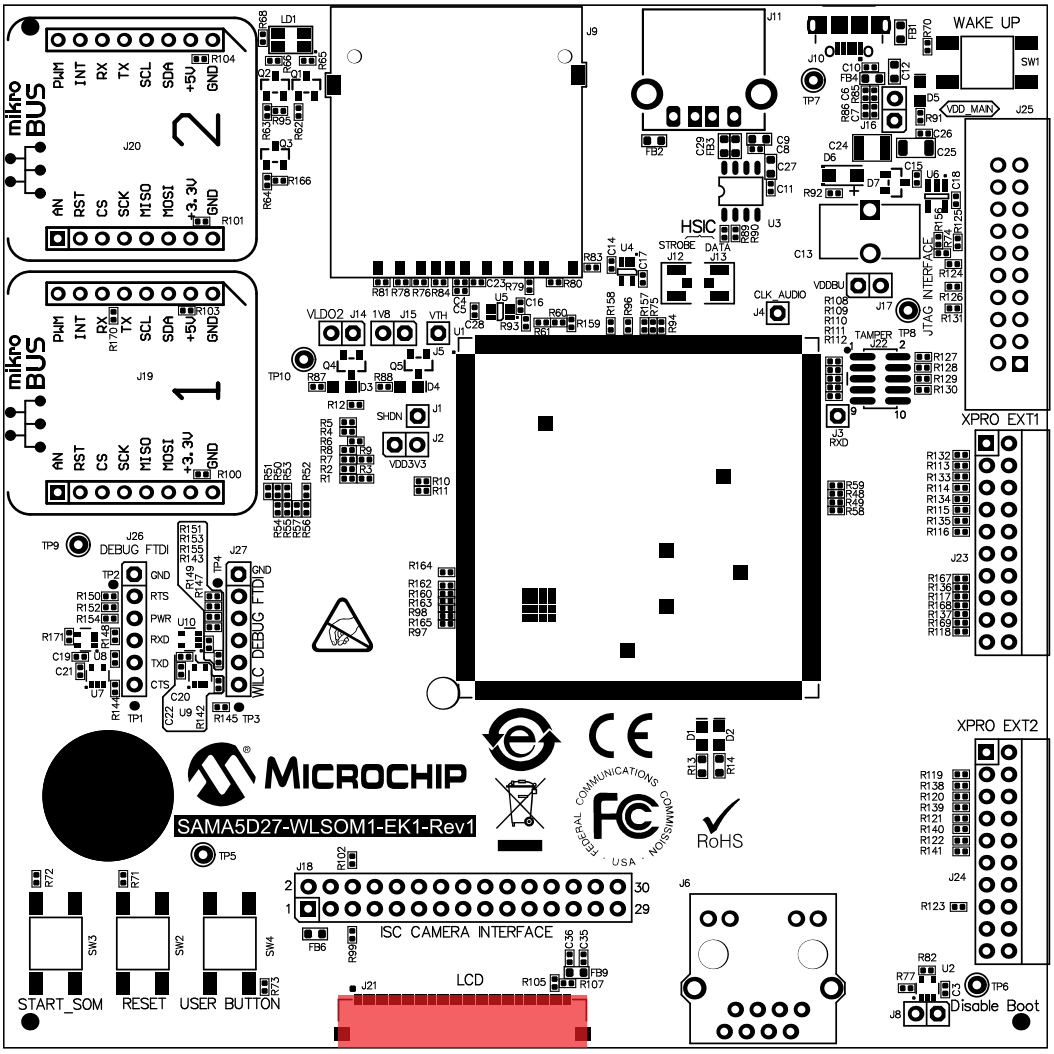


Figure 3-21. LCD Connector J21 Location



The table below describes the pin assignment of LCD connector J21.

Table 3-7. LCD Connector Pin Assignment

Pin No	Signal	PIO	Signal	RGB Interface Function
1	ID	PC9	ID	–
2	–	–	GND	Ground
3	NC	–	NC	Not connected
4	NC	–	NC	Not connected
5	LCDDAT2	PC10	D2	Data Line (BLUE 2)
6	LCDDAT3	PC11	D3	Data Line (BLUE 3)
7	–	–	GND	Ground
8	LCDDAT4	PC12	D4	Data Line (BLUE 4)
9	LCDDAT5	PC13	D5	Data Line (BLUE 5)
10	LCDDAT6	PC14	D6	Data Line (BLUE 6)

.....continued

Pin No	Signal	PIO	Signal	RGB Interface Function
11	LCDDAT7	PC15	D7	Data Line (BLUE 7)
12	–	–	GND	Ground
13	NC	–	NC	Not connected
14	NC	–	NC	Not connected
15	LCDDAT10	PC16	D10	Data Line (GREEN 2)
16	LCDDAT11	PC17	D11	Data Line (GREEN 2)
17	–	–	GND	Ground
18	LCDDAT12	PC18	D12	Data Line (GREEN 4)
19	LCDDAT13	PC19	D13	Data Line (GREEN 5)
20	LCDDAT14	PC20	D14	Data Line (GREEN 6)
21	LCDDAT15	PC21	D15	Data Line (GREEN 7)
22	–	–	GND	Ground
23	NC	–	NC	Not connected
24	NC	–	NC	Not connected
25	LCDDAT18	PC22	D18	Data Line (RED 2)
26	LCDDAT19	PC23	D19	Data Line (RED 3)
27	–	–	GND	Ground
28	LCDDAT20	PC24	D20	Data Line (RED 4)
29	LCDDAT21	PC25	D21	Data Line (RED 5)
30	LCDDAT22	PC26	D22	Data Line (RED 6)
31	LCDDAT23	PC27	D23	Data Line (RED 7)
32	–	–	GND	Ground
33	LCDPCK	PD0	PCLK	Pixel Clock
34	LCDVSYNC	PC30	VSYNC/CS	Vertical Synchro
35	LCDHSYNC	PC31	HSYNC/WE	Horizontal Synchro
36	LCDDEN	PD1	DATA_ENABLE	Data Enable
37	SPI_SPCK	PC1	SPI CLOCK	SPI Clock
38	SPI_MOSI	PC2	SPI MOSI	SPI Master OUT Slave IN
39	SPI_MISO	PC3	SPI MISO	SPI Master IN Slave OUT
40	SPI_NPCS0	PC6	SPI CS	SPI Chip Select
41	LCDDISP	PC29	ENABLE	Display Enable Signal
42	TWD	PD19	TWI_DATA	I²C Data Line (maXTouch)
43	TWCK	PD20	TWI_CLOCK	I²C clock Line (maXTouch)
44	GPIO	PB4	IRQ1	maXTouch Interrupt Line
45	GPIO	PA17	IRQ2	Interrupt Line for other I²C devices

.....continued

Pin No	Signal	PIO	Signal	RGB Interface Function
46	LCDPWM	PC28	PWM	Backlight Control
47	RESET	NRST	RESET	Reset for both display and maXTouch
48	Main_5V/3.3V	–	VCC	3.3V or 5V supply (5V by default)
49	Main_5V/3.3V	–	VCC	3.3V or 5V supply (5V by default)
50	–	–	GND	Ground

3.5.2 Image Sensor (ISC) Interface

This section describes the signals and connectors related to the ISC interface.

The Image Sensor Controller (ISC) system manages incoming data from a parallel or serial CSI-2 based CMOS/CCD sensor. The system supports a single active interface, as well as the ITU-R BT 656/1120 422 protocol with an 8-bit or 10-bit data width and raw Bayer format. The internal image processor includes adjustable white balance, color filter array interpolation, color correction, gamma correction, 12-bit to 10-bit compression, programmable color space conversion, as well as horizontal and vertical chrominance subsampling module.

Figure 3-22. Image Sensor Camera Interface Schematic

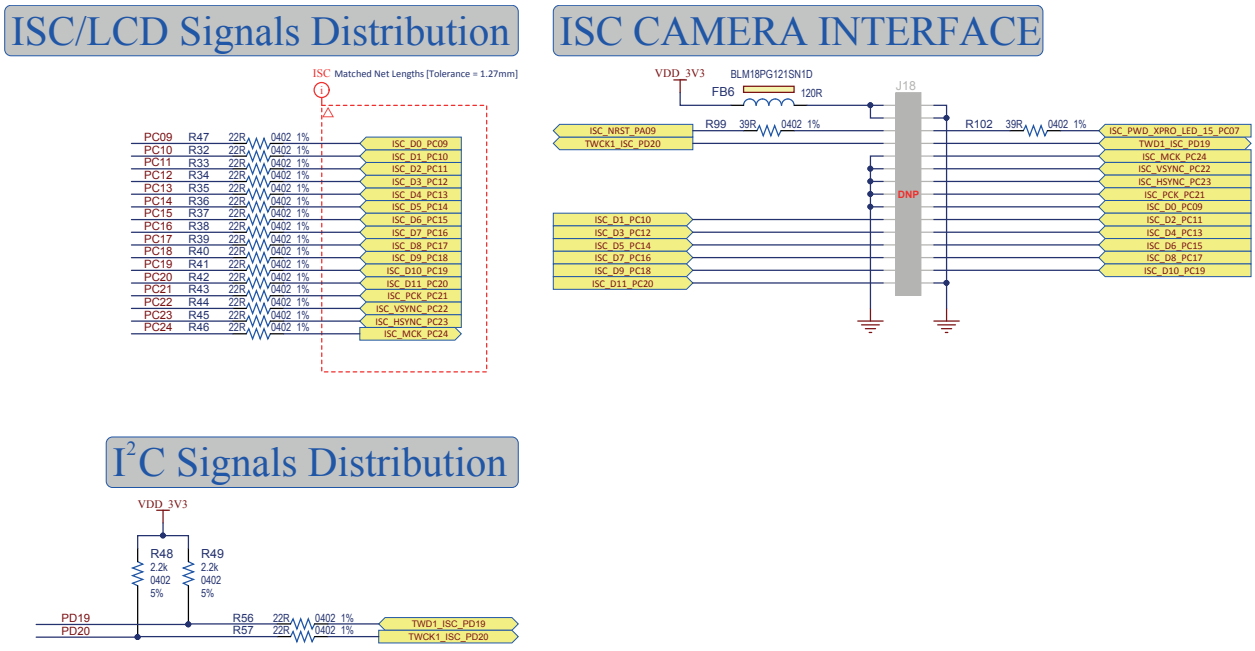
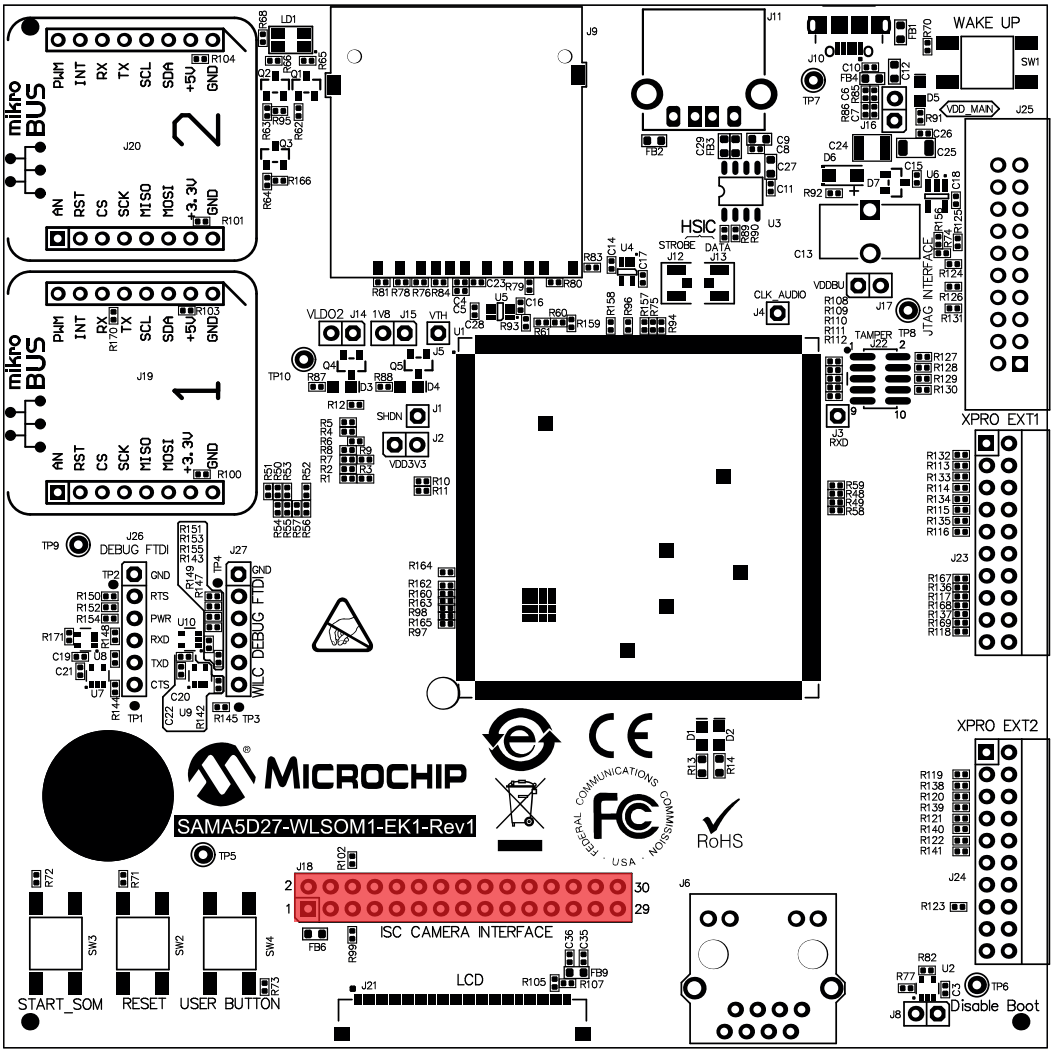


Figure 3-23. ISC Connector J18 Location



The table below describes the pin assignment of ISC connector J18.

Table 3-8. ISC Connector Pin Assignment

Function	PIO	Signal	Pin No		Signal	PIO	Function
3.3V	–	VDD_3V3	1	2	GND	–	GROUND
3.3V	–	VDD_3V3	3	4	GND	–	GROUND
Reset	PA9	ISC_nRST	5	6	ISC_PWD	PC7	Power Down
TWI Clock	PD20	TWCK	7	8	TWD	PD19	TWI Data
GROUND	–	GND	9	10	ISC_MCK	PC24	Master Clock
GROUND	–	GND	11	12	ISC_VSYNC	PC22	Vertical Synchro
GROUND	–	GND	13	14	ISC_HSYNC	PC23	Horizontal Synchro
GROUND	–	GND	15	16	ISC_PCK	PC21	Clock
GROUND	–	GND	17	18	ISC_D0	PC9	Data0
Data1	PC10	ISC_D1	19	20	ISC_D2	PC11	Data2

.....continued

Function	PIO	Signal	Pin No		Signal	PIO	Function
Data3	PC12	ISC_D3	21	22	ISC_D4	PC13	Data4
Data5	PC14	ISC_D5	23	24	ISC_D6	PC15	Data6
Data7	PC16	ISC_D7	25	26	ISC_D8	PC17	Data8
Data9	PC18	ISC_D9	27	28	ISC_D10	PC19	Data10
Data11	PC20	ISC_D11	29	30	GND	–	GROUND

3.5.3 RGB LED

The ATSAMA5D27-WLSOM1-EK1 features one RGB LED which can be controlled by the user. The three LED cathodes are controlled via GPIOs or Timer/Counter pins (only for red and green LEDs).

Figure 3-24. RGB LED Schematic

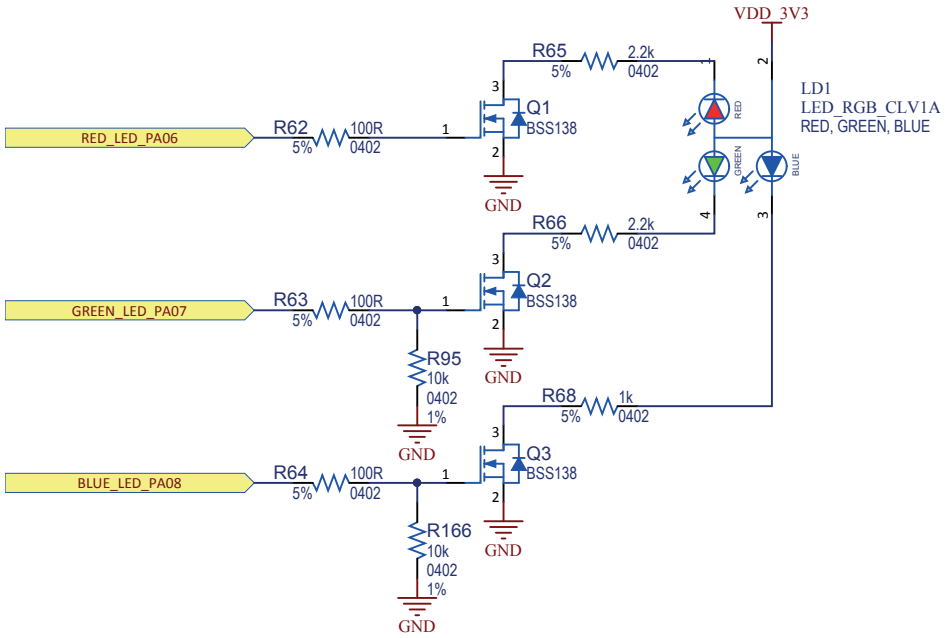
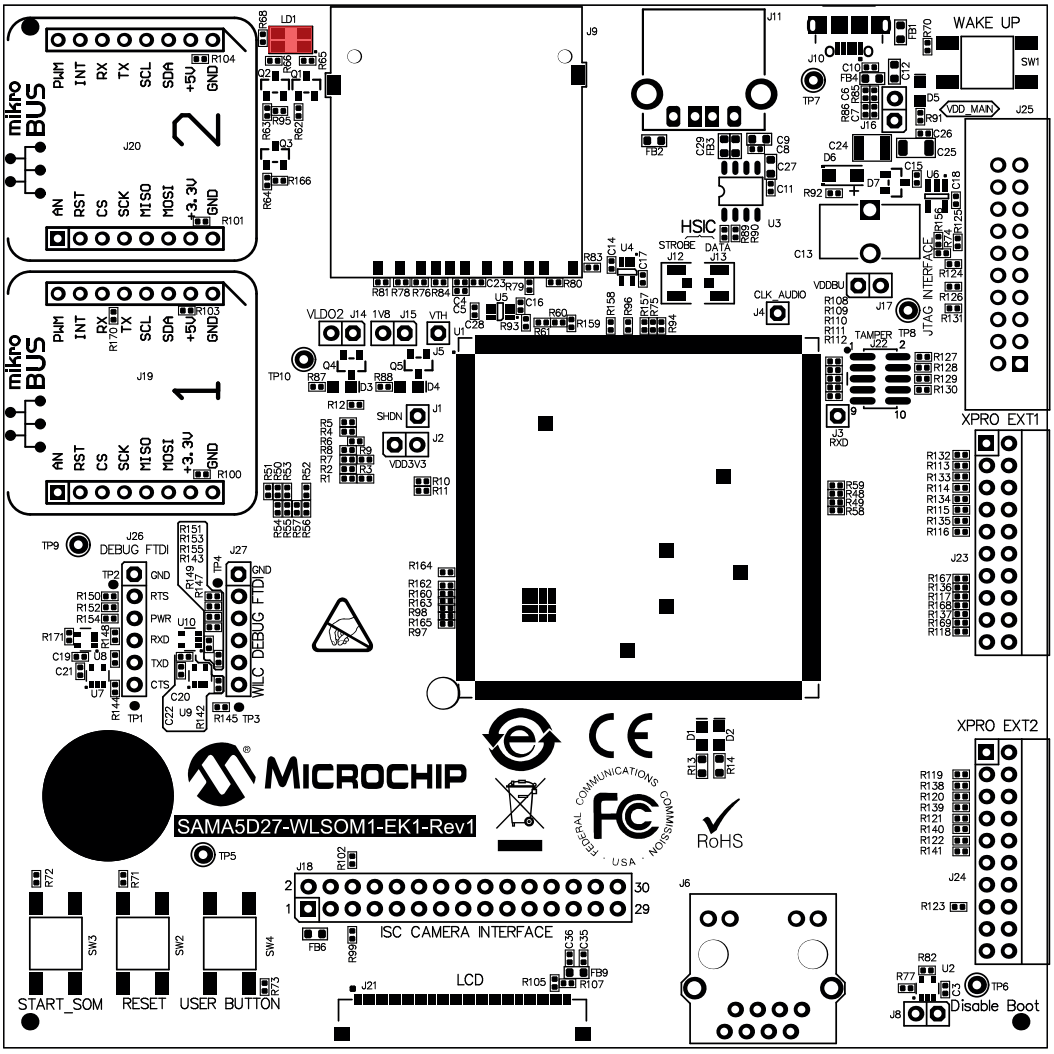


Figure 3-25. RGB LED Device Location



The table below describes the pin assignment of RGB LED.

Table 3-9. RGB LED Pin Assignment

Signal	PIO	Function
RED_LED	PA6	GPIO/TIOA5
GREEN_LED	PA7	GPIO/TIOB5
BLUE_LED	PA8	GPIO

3.6 Debugging Capabilities

The ATSAMA5D27-WLSOM1-EK1 includes two main debugging interfaces to provide debug-level access to the SAMA5D2:

- One JTAG interface connected from the MPU using connector J25.
- One UART interface connected from the MPU using connector J26.

3.6.1 Debug JTAG

This section describes the signals and connectors related to the JTAG interface.

A 20-pin JTAG header is provided on the baseboard to facilitate software development and debugging using various JTAG emulators. The interface signals have a voltage level of 3.3V.

Figure 3-26. JTAG Interface Schematic

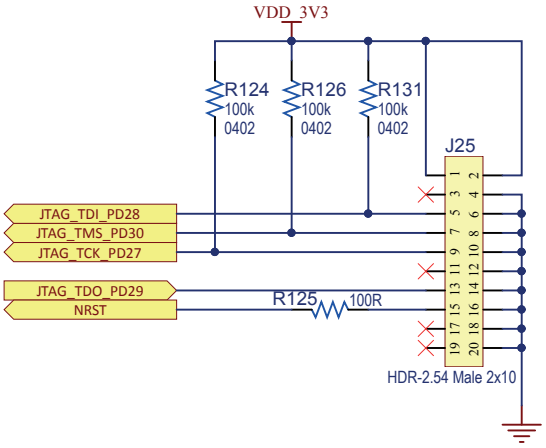
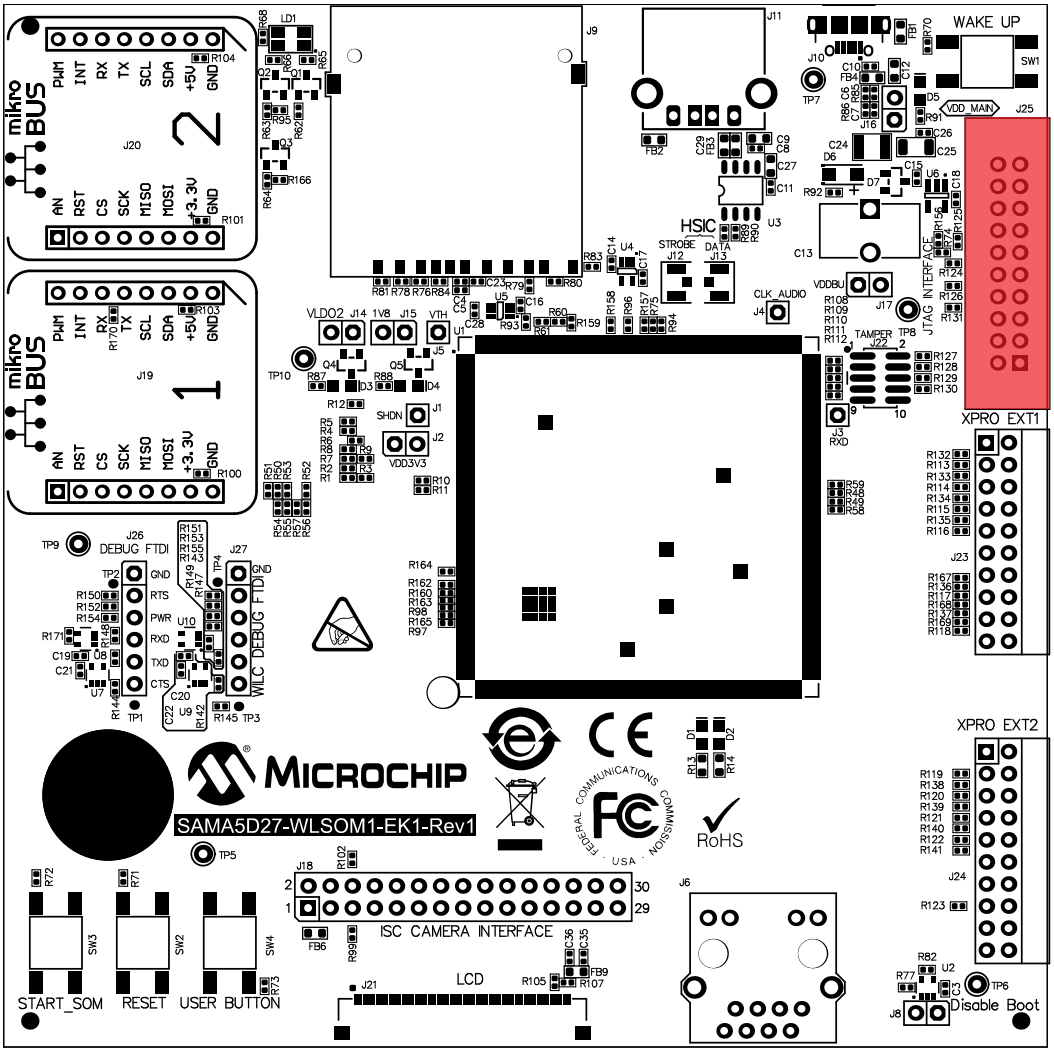


Figure 3-27. JTAG Connector J25 Location



The table below describes the pin assignment of JTAG connector J25.

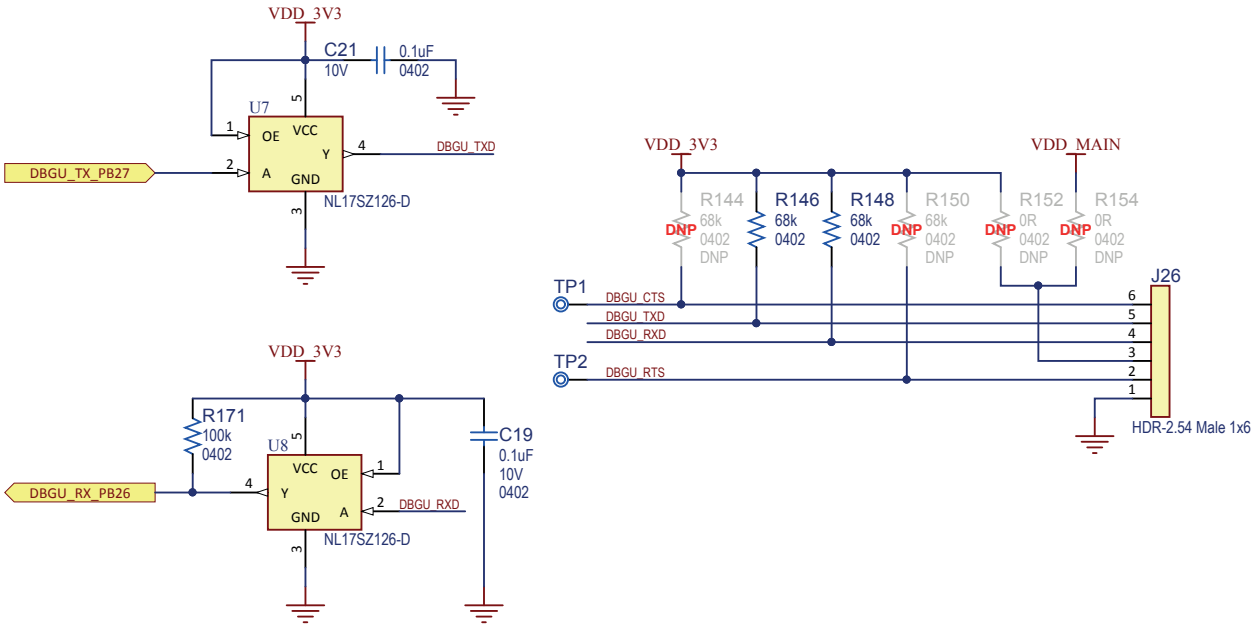
Table 3-10. JTAG Connector Pin Assignment

Pin No	Function	PIO	Signal
1	3.3V Supply Voltage	–	VDD_3V3
2	3.3V Supply Voltage	–	VDD_3V3
3	Not used	–	NC
4	GROUND	–	GND
5	JTAG data input into target processor	PD28	JTAG TDI
6	GROUND	–	GND
7	JTAG mode set input into target processor	PD30	JTAG TMS
8	GROUND	–	GND
9	JTAG clock signal into target processor	PD27	JTAG TCK
10	GROUND	–	GND
11	Not used	–	NC
12	GROUND	–	GND
13	JTAG data output from target processor	PD29	JTAG TDO
14	GROUND	–	GND
15	Active-low reset signal. Target processor reset signal.	NRST	NRST
16	GROUND	–	GND
17	Not used	–	NC
18	GROUND	–	GND
19	Not used	–	NC
20	GROUND	–	GND

3.6.2 Debug UART

The ATSAMA5D27-WLSOM1-EK1 board has a dedicated serial port for debugging, which is accessible through the 6-pin male header J26. Various interfaces can be used as a USB/Serial DBGU port bridge, such as FTDI TTL-232R USB to TTL serial cable or basic breakout board for the RS232/USB converter.

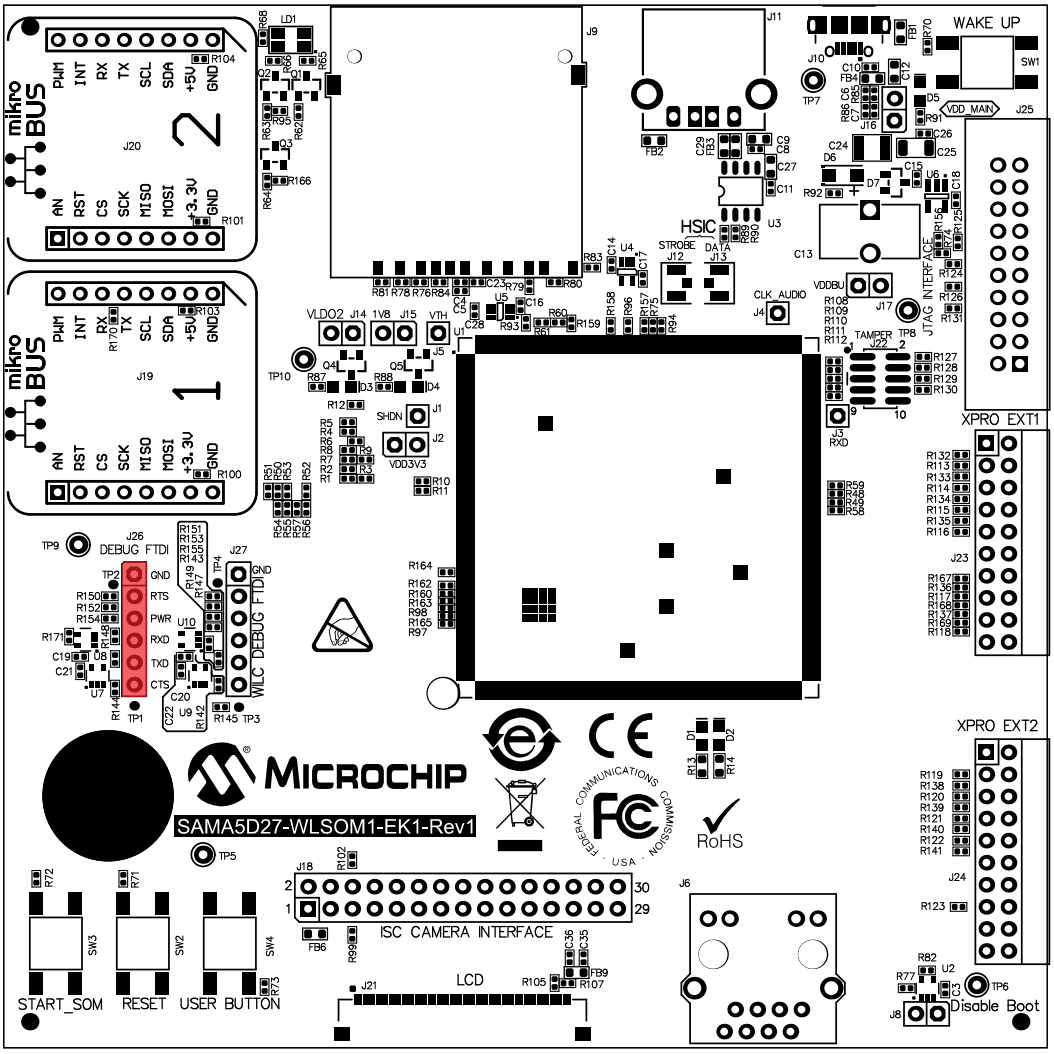
Figure 3-28. SAMA5D2 Debug FTDI Interface Schematic



Two Tri-State Buffers are available on TX and RX lines in order to protect the system against any leakage when an FTDI connector is present and when the system is not started yet.

R152 and R154 are optional (not implemented) resistors that can be used for power selection. Power can be delivered either by the ATSAMA5D27-WLSOM1-EK1 board or by the debug interface tool. To avoid malfunction between the debug interface (e.g., FTDI) and the on-board power system, ensure that the voltage level selected corresponds to the application requirements.

Figure 3-29. FTDI Debug Connector J26 Location



The table below describes the pin assignment of FTDI connector J26.

Table 3-11. FTDI Connector Pin Assignment

Pin No	Mnemonic	PIO	Signal Description
1	DBGU_CTS	RFU	Handshake Input
2	DBGU_TXD	PB27	RS232 serial data output signal
3	DBGU_RXD	PB26	RS232 serial data input signal
4	VDD	–	3.3V or 5V Supply
5	DBGU_RTS	RFU	Handshake Output
6	GND	–	GROUND

3.6.3 WILC3000 Debug UART

The ATSAMA5D27-WLSOM1-EK1 has a dedicated serial port for WILC3000 Module debugging, which is accessible through the 6-pin male header J27 (not populated by default).

Figure 3-30. WILC3000 Debug FTDI Interface Schematic

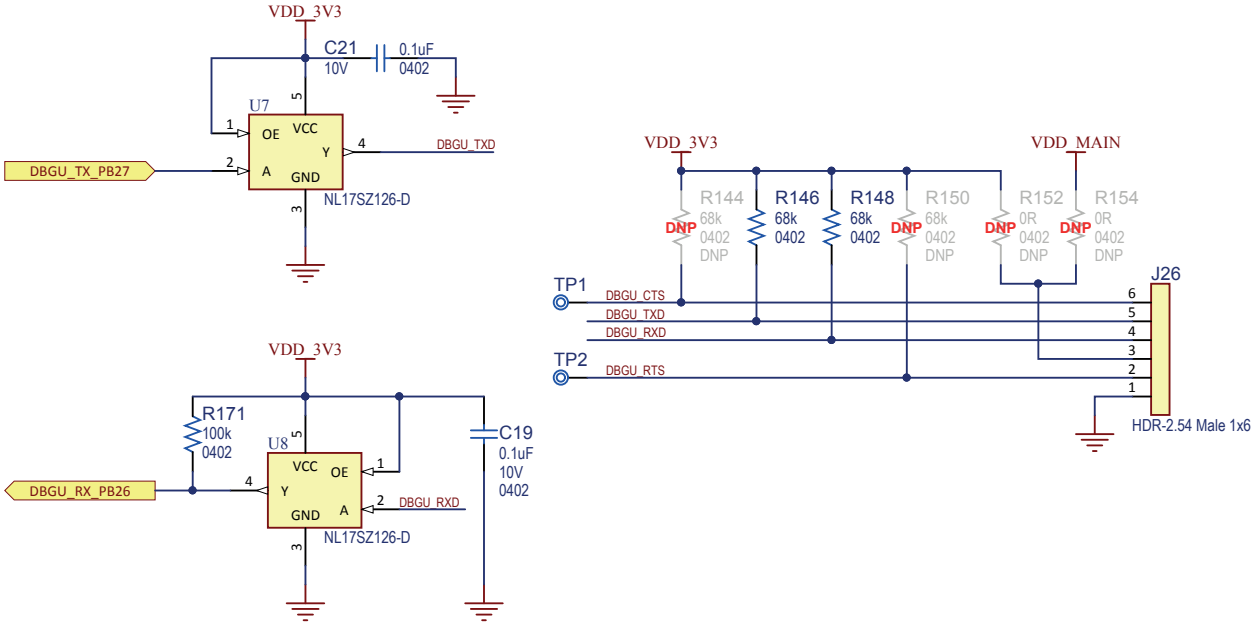
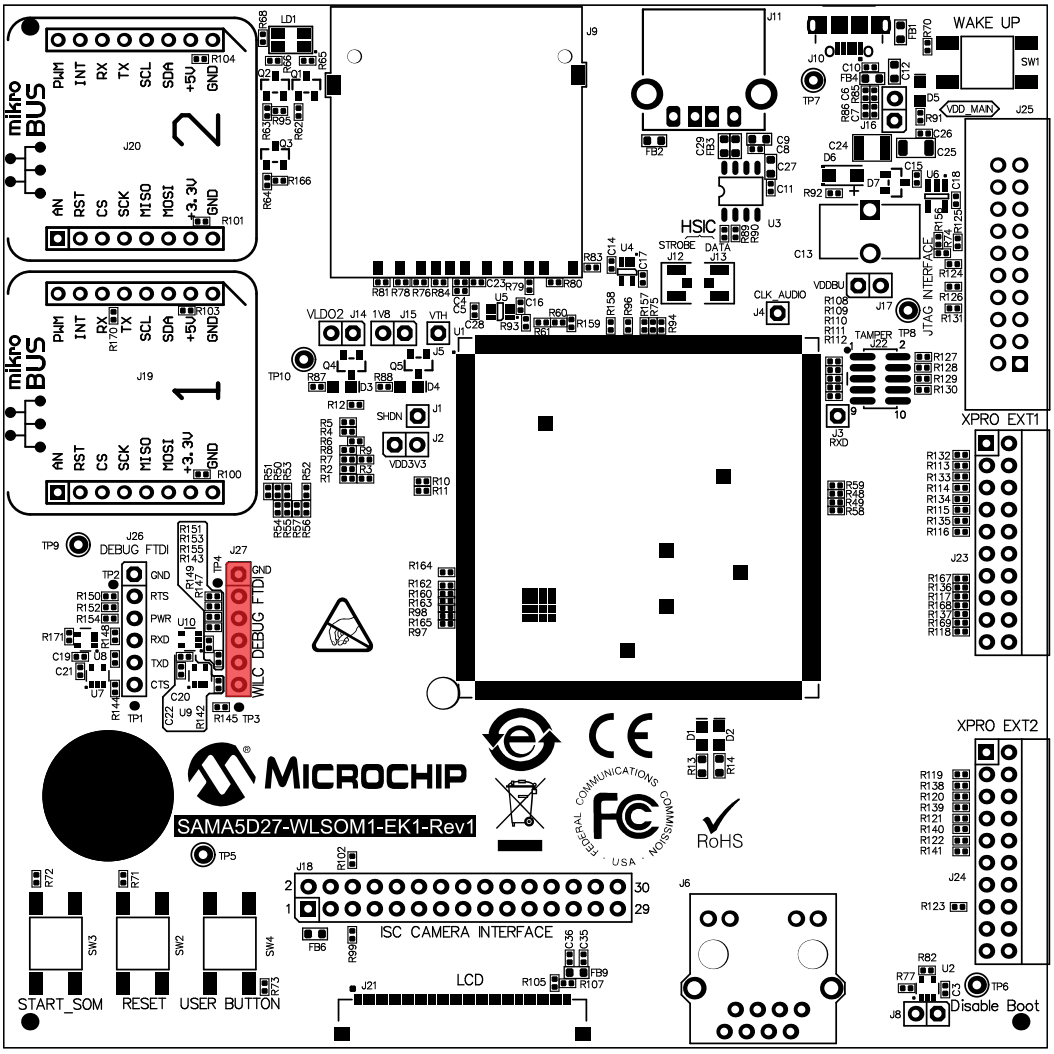


Figure 3-31. FTDI WILC Connector J27 Location



The table below describes the pin assignment of WILC3000 FTDI connector J27.

Table 3-12. WILC3000 FTDI Connector Pin Assignment

Pin No	Mnemonic	PIO	Signal Description
1	WILCFTDI_CTS	RFU	Handshake Input
2	WILCFTDI_TXD	TXD_WILC_DBGU	RS232 serial data output signal
3	WILCFTDI_RXD	RXD_WILC_DBGU	RS232 serial data input signal
4	VDD	–	3.3V or 5V Supply
5	WILCFTDI_RTS	RFU	Handshake Output
6	GND	–	GROUND

3.7 PIO Usage on Expansion Connectors

This section describes the signals and connectors related to the PIO usage on expansion connectors.

The baseboard includes numerous peripherals. Many of these are connected to the GPIO block so that the I/O pins can be configured to carry out many alternative functions. This provides great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Note that most pins are configured as GPIO inputs, with a 100 KOhm pull-up resistor, after reset.

3.7.1 Tamper Interface

The ATSAMA5D27-WLSOM1-EK1 features seven tamper pins for static or dynamic intrusion detection and two analog pins for comparison.

For a description of intrusion detection, refer to the SAMA5D2 data sheet, chapter “Security Module (SECUMOD)”.

Figure 3-32. Tamper Interface Schematic

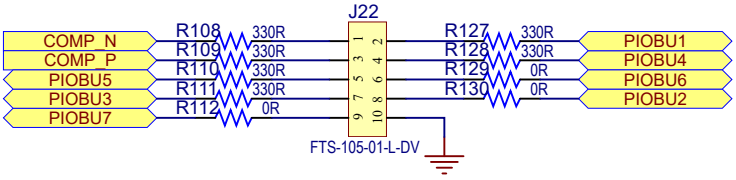
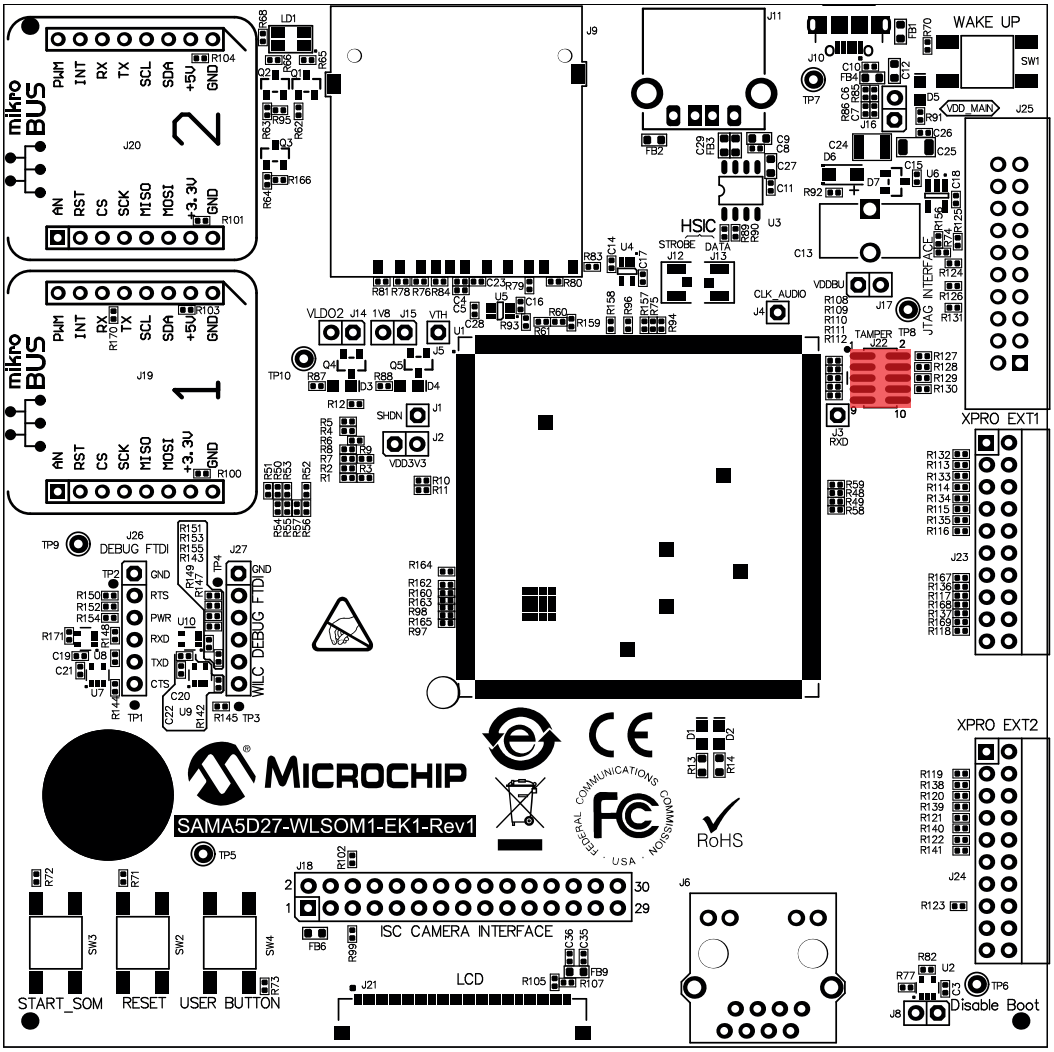


Figure 3-33. Tamper Connector J22 Location



The table below describes the pin assignment of Tamper connector J22.

Table 3-13. Tamper Connector Pin Assignment

Signal	Pin No		Signal
COMP_N	1	2	PIOBU1
COMP_P	3	4	PIOBU4
PIOBU5	5	6	PIOBU6
PIOBU3	7	8	PIOBU2
PIOBU7	9	10	GND

3.7.2 mikroBUS Interfaces

The ATSAMA5D27-WLSOM1-EK1 hosts two pairs of 8-pin female headers acting as mikroBUS interfaces. The mikroBUS standard defines the main board sockets and add-on boards, or Click boards, used for interfacing microprocessors with integrated modules having proprietary pin configuration and silkscreen markings. The pinout consists of three groups of communication pins (SPI, UART and TWI), four additional pins (PWM, interrupt, analog input and reset) and two power groups (+3.3V and GND on the left, and 5V and GND on the right 1x8 header).

Figure 3-34. mikroBUS1 Interface Schematic

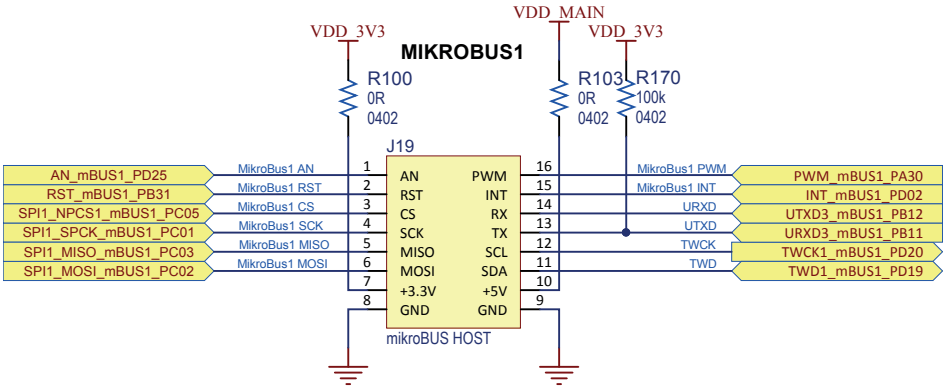
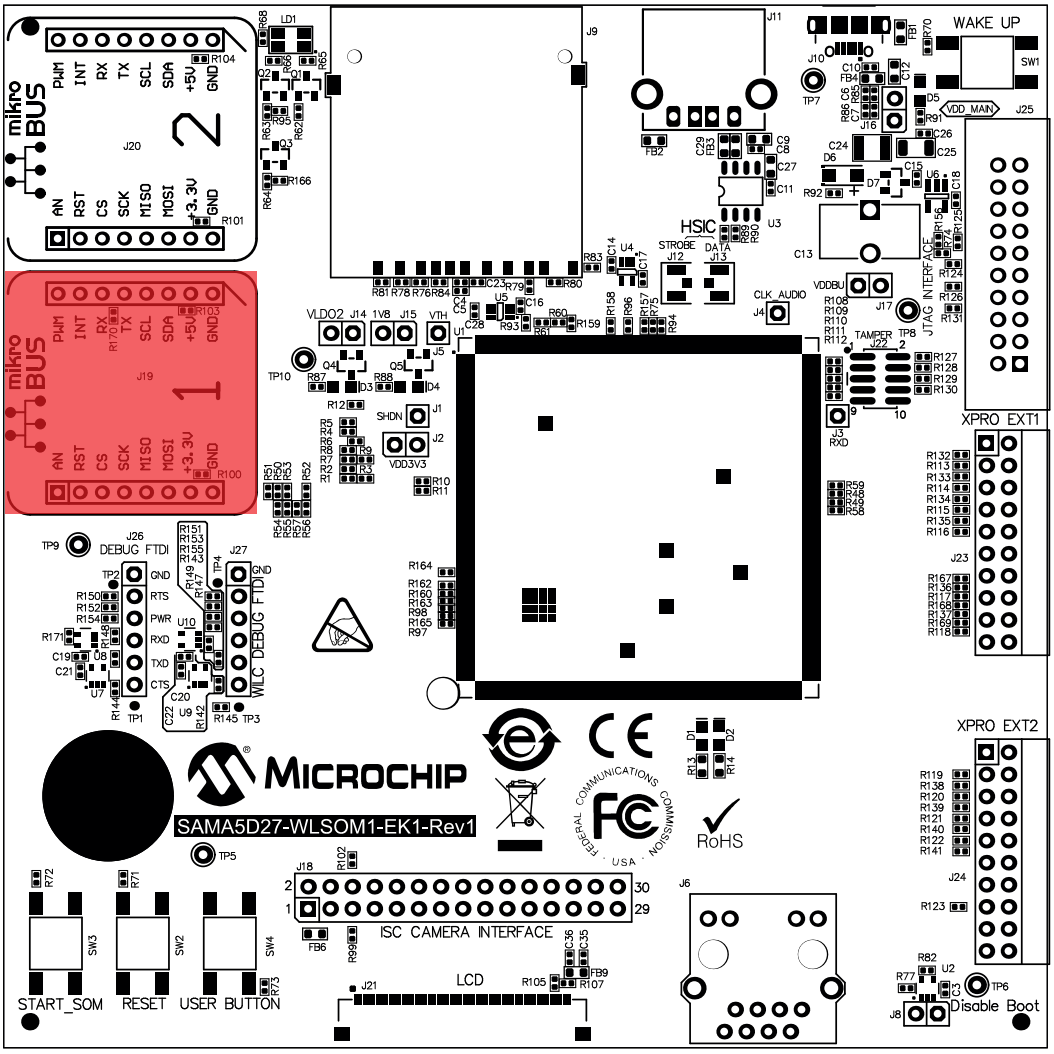


Figure 3-35. mikroBUS1 Connector J19 Location



The table below describes the pin assignment of mikroBUS1 connector J19.

Table 3-14. mikroBUS1 Connector Pin Assignment

Function	PIO	Signal	Pin No		Signal	PIO	Function
Analog Input	PD25	mikroBUS1_AN	1	16	mikroBUS1_PWM	PA30	PWM
Reset	PB31	mikroBUS1_RST	2	15	mikroBUS1_INT	PD2	Interrupt
SPI Chip Select	PC5	mikroBUS1_CS	3	14	URXD	PB12	UART Receive
SPI Clock	PC1	mikroBUS1_SCK	4	13	UTXD	PB11	UART Transmit
SPI MISO	PC3	mikroBUS1_MISO	5	12	TWCK	PD20	TWI Clock
SPI MOSI	PC2	mikroBUS1_MOSI	6	11	TWD	PD19	TWI Data
3.3V	–	VDD_3V3	7	10	VDD_MAIN	–	5V
GROUND	–	GND	8	9	GND	–	GROUND

Figure 3-36. mikroBUS2 Interface Schematic

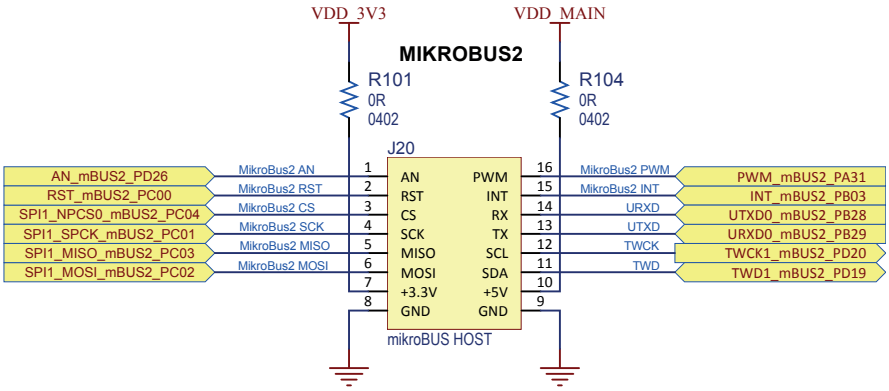
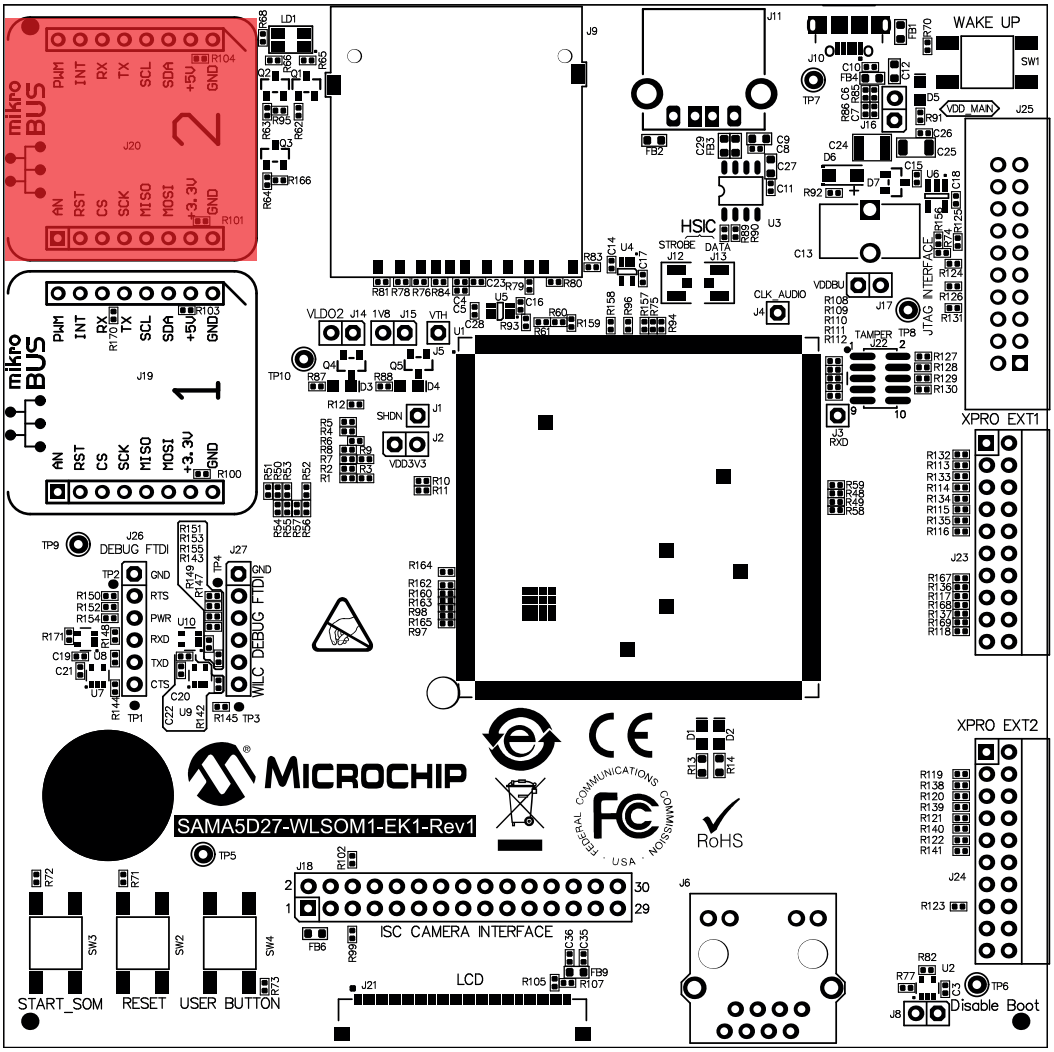


Figure 3-37. mikroBUS2 Connector J20 Location



The table below describes the pin assignment of mikroBUS2 connector J20.

Table 3-15. mikroBUS2 Connectors Pin Assignment

Function	PIO	Signal	Pin No		Signal	PIO	Function
Analog Input	PD26	mikroBUS2_AN	1	16	mikroBUS2_PWM	PA31	PWM

.....continued

Function	PIO	Signal	Pin No		Signal	PIO	Function
Reset	PC0	mikroBUS2_RST	2	15	mikroBUS2_INT	PB3	Interrupt
SPI Chip Select	PC4	mikroBUS2_CS	3	14	URXD	PB28	UART Receive
SPI Clock	PC1	mikroBUS2_SCK	4	13	UTXD	PB29	UART Transmit
SPI MISO	PC3	mikroBUS2_MISO	5	12	TWCK	PD20	TWI Clock
SPI MOSI	PC2	mikroBUS2_MOSI	6	11	TWD	PD19	TWI Data
3.3V	–	VDD_3V3	7	10	VDD_MAIN	–	5V
GROUND	–	GND	8	9	GND	–	GROUND

3.7.3 Expansion Header Interfaces

The ATSAMA5D27-WLSOM1-EK1 can host two connectors to interface with standard Xplained Pro extensions and, in particular, with QT Xplained Pro Extension boards.

The following QT Xplained Pro Extensions boards are compatible with the interfaces:

- QT1 Xplained Pro Extension Kit (ATQT1-XPRO)
- QT2 Xplained Pro Extension Kit (ATQT2-XPRO)
- QT6 Xplained Pro Extension Kit (ATQ6-XPRO)

Figure 3-38. Expansion Header Interface Schematic

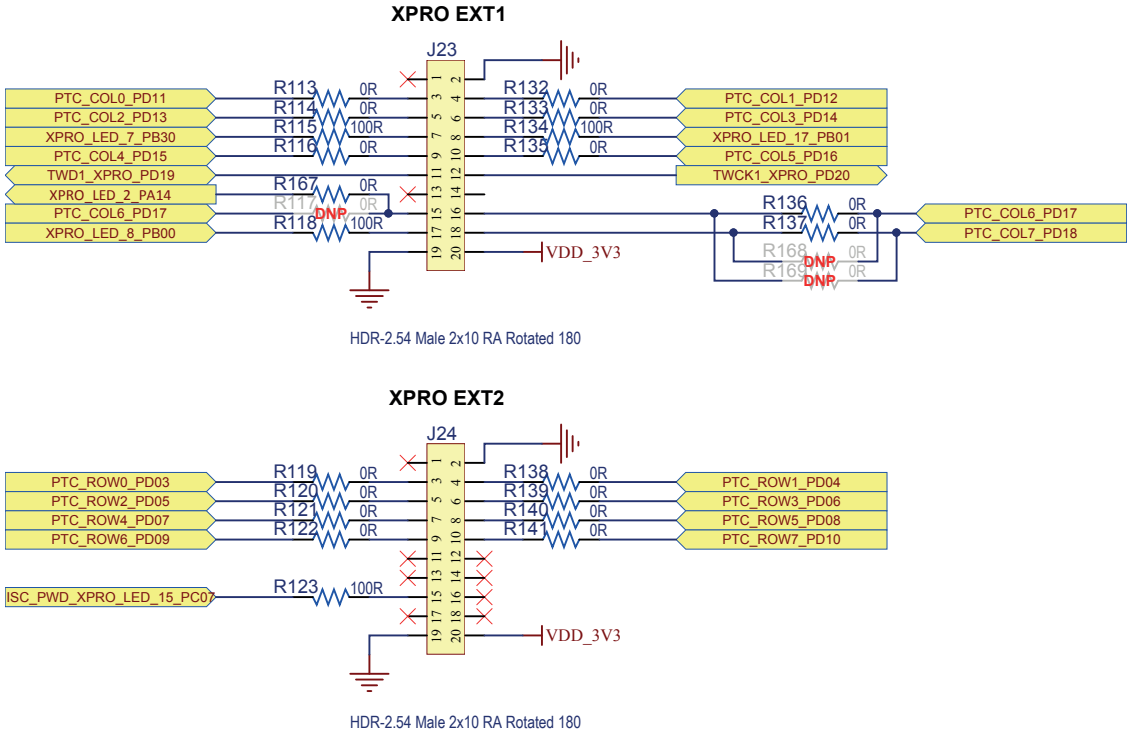
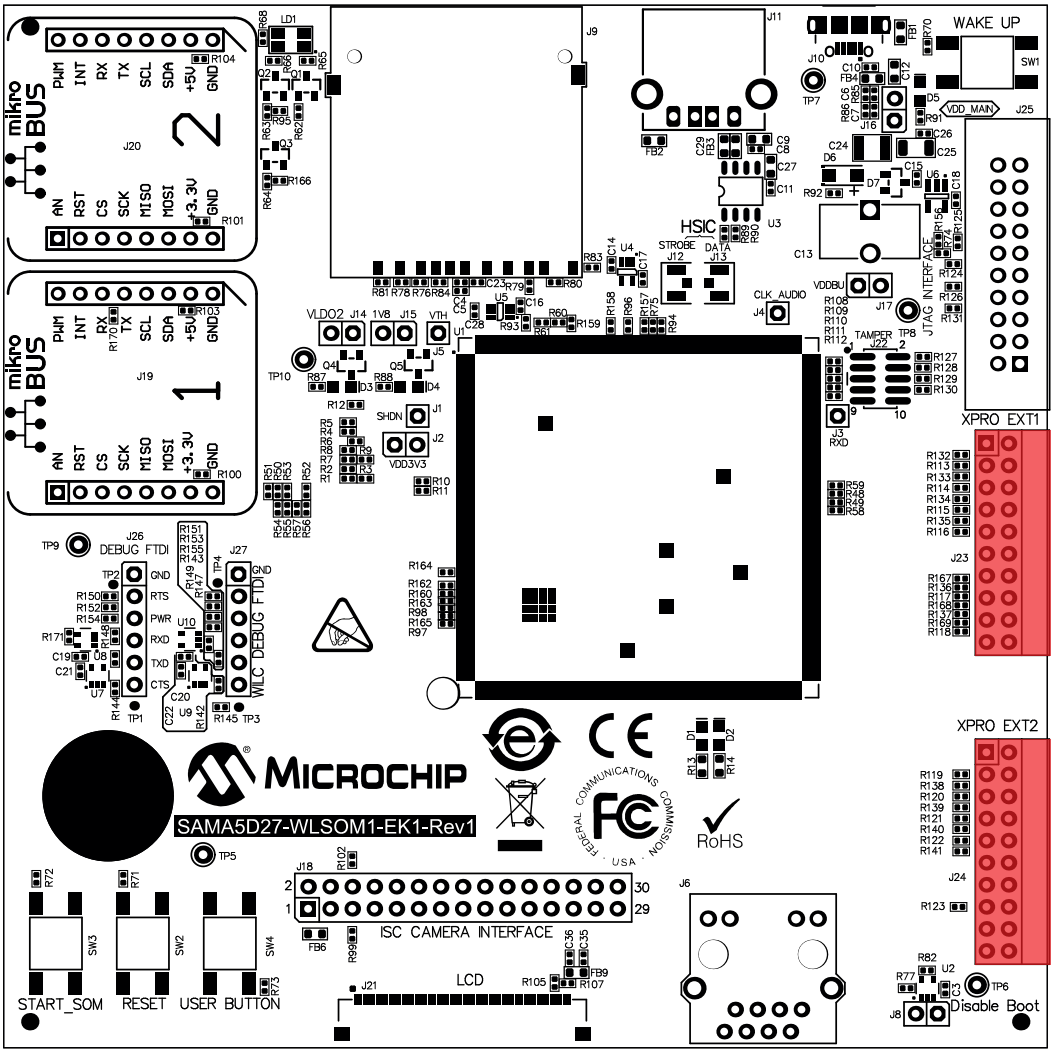


Figure 3-39. XPRO Connectors J23 and J24 Location



The table below describes the pin assignment of XPRO_EXT1 connector J23.

Table 3-16. EXT_XPRO_1 Connector Pin Assignment

Function	PIO	Signal	Pin No		Signal	PIO	Function
NC	–	NC	1	2	GND	–	GROUND
PTC COL	PD11	PTC_COL0_PD11	3	4	PTC_COL1_PD12	PD12	PTC COL
PTC COL	PD13	PTC_COL2_PD13	5	6	PTC_COL3_PD14	PD14	PTC COL
PTC LED	PB30	XPRO_LED_7_PB30	7	8	XPRO_LED_17_PB01	PB1	PTC LED
PTC COL	PD15	PTC_COL4_PD115	9	10	PTC_COL5_PD16	PD16	PTC COL
TWI Data	PD19	TWD1_XPRO_PD19	11	12	TWCK1_XPRO_PD20	PD20	TWI Clock
NC	–	NC	13	14	NC	–	NC
PTC LED	PA14	XPRO_LED_2_PA14	15	16	PTC_COL6_PD17	PD17	PTC COL
PTC COL(1)	*PD17*	*PTC_COL0_PD11*			*PTC_COL7_PD18*	*PD18*	*PTC COL*(1)

.....continued

Function	PIO	Signal	Pin No		Signal	PIO	Function
PTC LED	PB0	XPRO_LED_8_PB00	17	18	PTC_COL7_PD18	PD18	PTC COL
					PTC_COL6_PD17	*PD17*	*PTC COL*(1)
GROUND	–	GND	19	20	VDD_3V3	–	3.3V

Note:

1. Not the default setting.

The table below describes the pin assignment of XPRO_EXT2 connector J24.

Table 3-17. EXT_XPRO_2 Connector Pin Assignment

Function	PIO	Signal Name	Pin No		Signal Name	PIO	Function
NC	–	NC	1	2	GND	–	GROUND
PTC ROW	PD3	PTC_ROW0_PD03	3	4	PTC_ROW1_PD04	PD4	PTC ROW
PTC ROW	PD5	PTC_ROW2_PD05	5	6	PTC_ROW3_PD06	PD6	PTC ROW
PTC ROW	PD7	PTC_ROW4_PD07	7	8	PTC_ROW5_PD08	PD8	PTC ROW
PTC ROW	PD9	PTC_ROW6_PD09	9	10	PTC_ROW7_PD10	PD10	PTC ROW
NC	–	NC	11	12	NC	–	NC
NC	–	NC	13	14	NC	–	NC
PTC LED	PC7	ISC_PWD_XPRO_LED_15_PC07	15	16	NC	–	NC
NC	–	NC	17	18	NC	–	NC
GROUND	–	GND	19	20	VDD_3V3	–	3.3V

Important: These two connectors are compatible with QT1, QT2 and QT6 Xplained Pro Extension Kits. Other extension boards are not compatible.

3.8 Extra Features

3.8.1 VLDO2 Power Measurement Connector

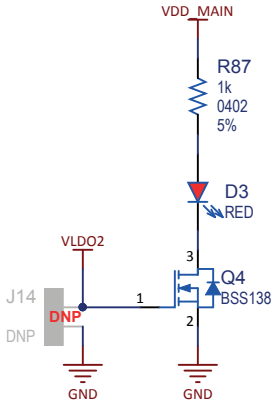
The ATSAMA5D27-WLSOM1 module embeds an LDO with capacities of:

- Output voltage from 1.2V to 3.3V by 50 mV steps
- Output current capability up to 300 mA

A 2-pin connector (J14), not populated by default, is available on the baseboard to measure output current capability of the VLDO2 regulator.

Note: The maximum current available on VLDO2 node is approximately 300 mA max @ 1.2V to 3.3V.

Figure 3-40. VLDO2 Load Connector



3.8.2 VDD_1V8 Power Measurement Connector

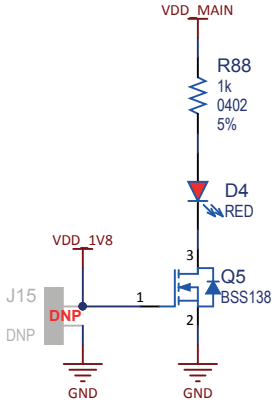
The ATSAMA5D27-WLSOM1 module embeds an LDO with capacities of:

- Output voltage @ 1.8V only
- Output current capability up to 900mA

A 2-pin connector (J15), not populated by default, is available on the baseboard to measure output current capability of the VDD_1V8 regulator.

Note: The maximum current available on VDD_1V8 node is approximately 900mA max @ 1.8V.

Figure 3-41. VDD_1V8 Load Connector



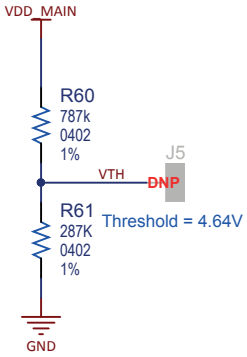
3.8.3 VTH Threshold

The ATSAMA5D27-WLSOM1 module mounted on the base board integrates a Voltage Supervisor MIC842.

A resistor ladder is mounted on the ATSAMA5D27-WLSOM1-EK1 board and detects a voltage drop when reduced to 4.64V.

It is possible to change this resistor ladder, values or reference if, for test purposes, another voltage reference is monitored (e.g. 12V). If the reference voltage is above 5.5V, then R60 should be removed (unsoldered).

Figure 3-42. VTH Threshold Schematic



4. Installation and Operation

4.1 System and Configuration Requirements

The ATSAMA5D27-WLSOM1-EK1 requires the following:

- Personal Computer
- USB cable (included in the kit box)
- Wireless antenna (included in the kit box)

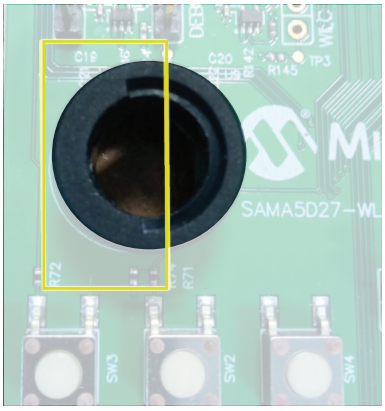
4.2 How to Mount the Wireless Antenna on the Kit

4.2.1 Place the Panel Sleeve

By default, two panel sleeves are included in the kit, one round and one hexagonal. Only the hexagonal one can be used with the kit.

Place the hexagonal sleeve as shown below. Ensure that the slot of the sleeve is correctly oriented.

Figure 4-1. Place the sleeve



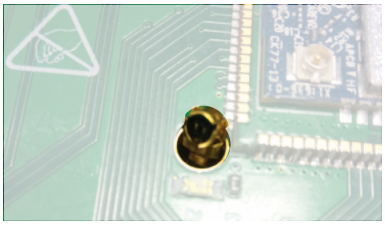
4.2.1.1 Place the Antenna Cable

Place the antenna cable into the sleeve as shown below.

Figure 4-2. Place the cable into the sleeve

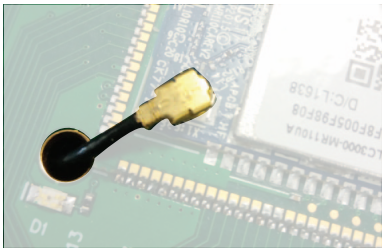
Near the module placed in the center of the board, pass the antenna cable through the small hole as shown below.

Figure 4-3. Place the cable in the small hole



Clip the cable onto the U-FL connector placed on the module. Extreme care must be taken to achieve proper processing during assembly. The U-FL connector is very fragile.

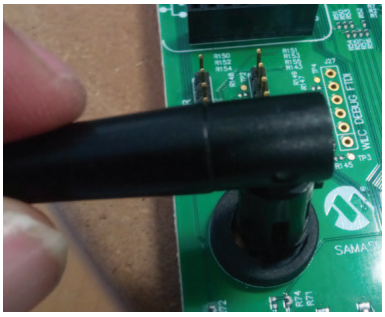
Figure 4-4. Clip the cable to the wireless module



4.2.2 Clip the Antenna

Clip the antenna on the sleeve as shown below. Be sure to respect the orientation

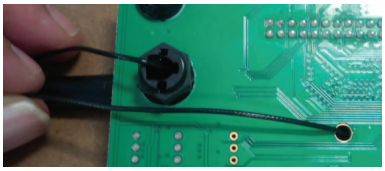
Figure 4-5. Clip the antenna



4.2.3 Reorganize the Antenna Cable

Reorganize the antenna cable as shown below.

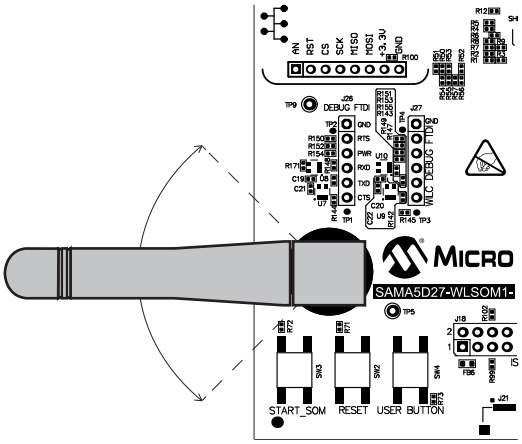
Figure 4-6. Reorganize the antenna cable



4.2.4 Antenna Orientation

The antenna has 180° free orientation for ease-of-use. Nonetheless, a 90° rotation is sufficient as shown below, when mikroBUS clicks and button are used.

Figure 4-7. Antenna orientation



4.3 Baseboard Setup

Follow these steps to ensure proper operation of the kit:

1. Unpack the baseboard, taking care to avoid electrostatic discharge.
2. Connect the radio antenna as described in the section How to Mount the Wireless Antenna on the Kit.
3. Check the default jumper settings.
4. Connect the USB Micro-AB cable to connector J10.
5. Connect FTDI UART cable to connector J26.
6. Connect the other end of the cable to a free port of your PC.
7. Open a terminal (console 115200, N, 8, 1) on your personal computer. Reset the baseboard. A start-up message appears on the console.

5. Appendix: Schematics and Layouts

Figure 5-1. ATSAMA5D27-WLSOM1-EK1 Schematic: Page 1

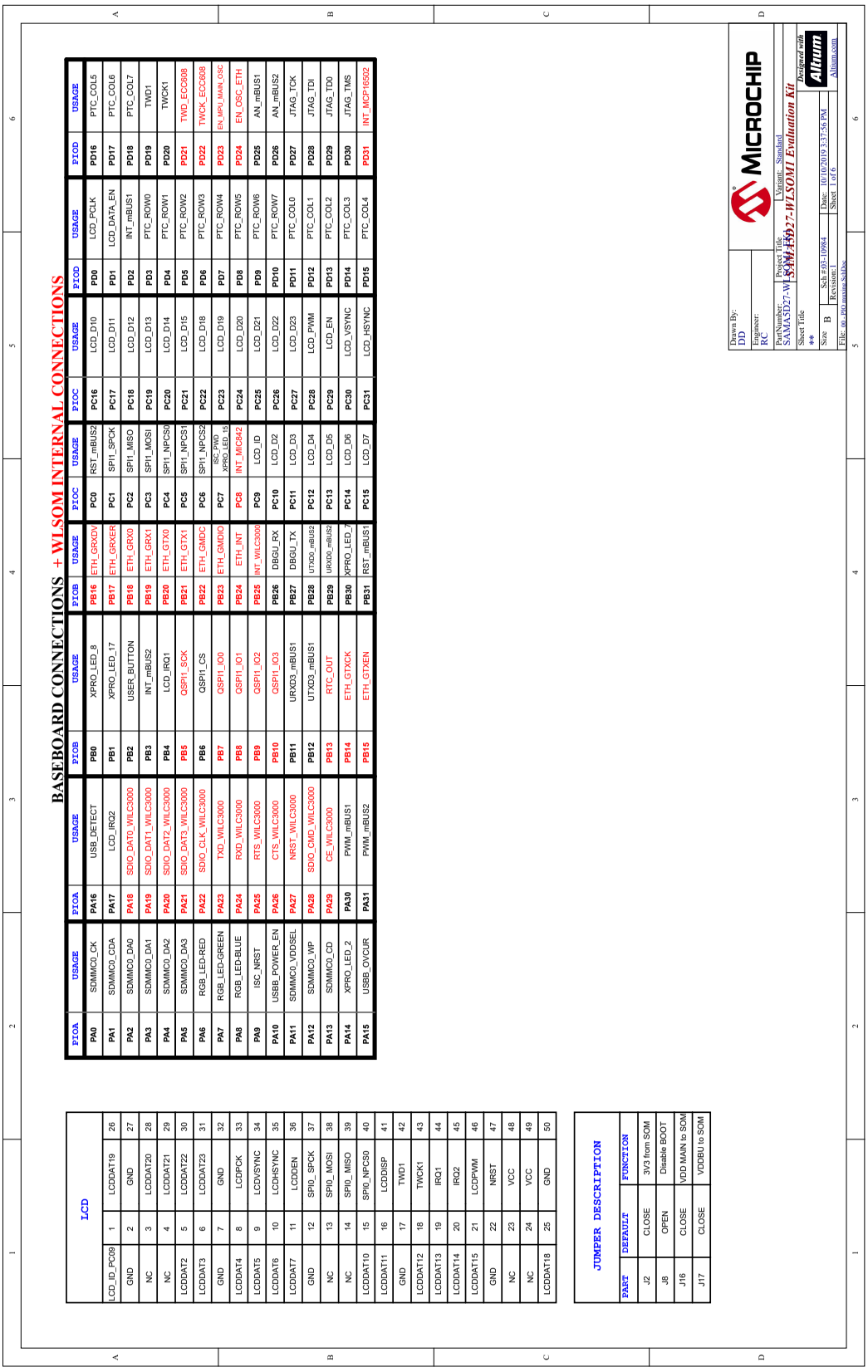


Figure 5-2. ATSAMA5D27-WLSOM1-EK1 Schematic: Page 2

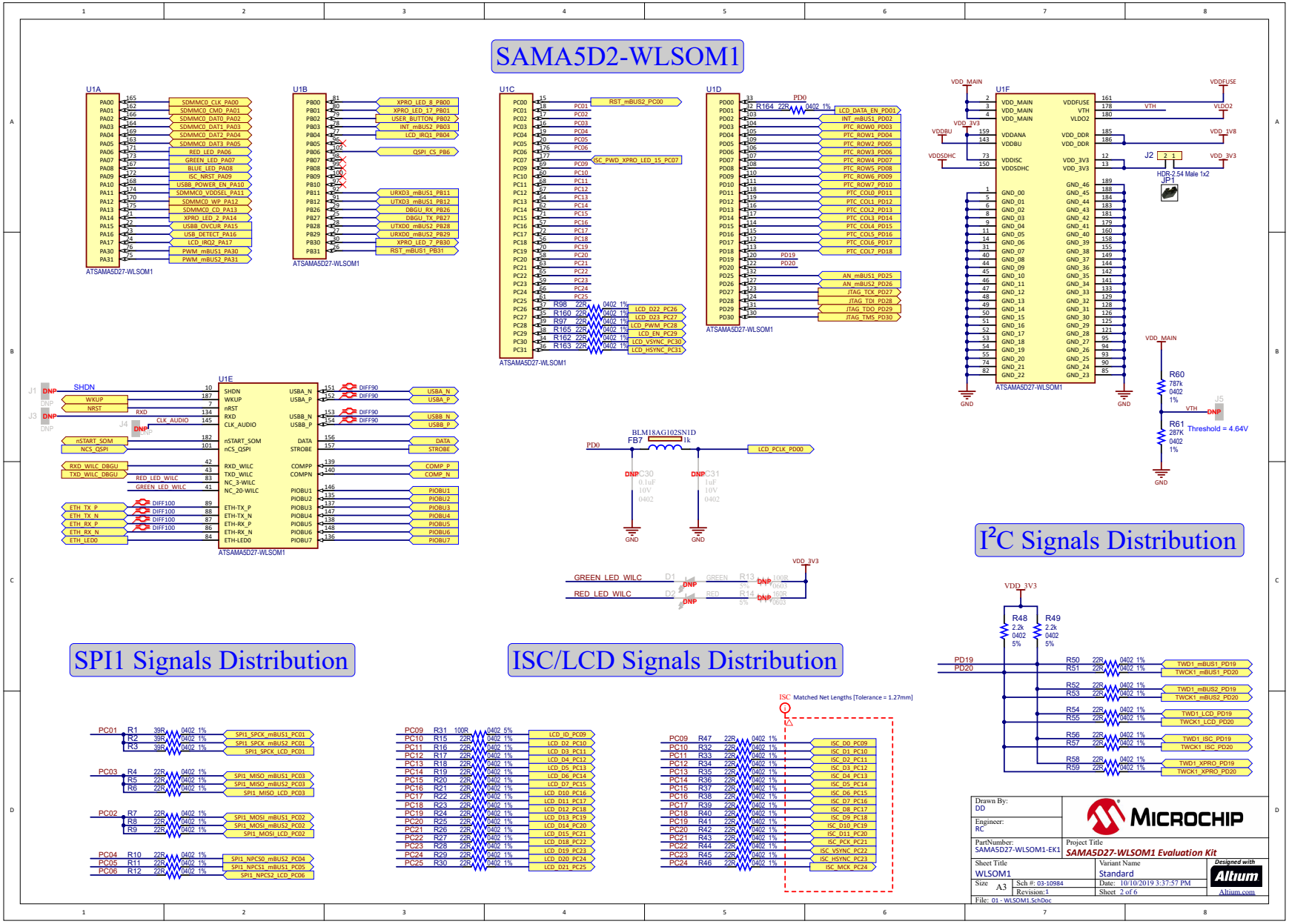


Figure 5-3. ATSAMA5D27-WLSOM1-EK1 Schematic: Page 3

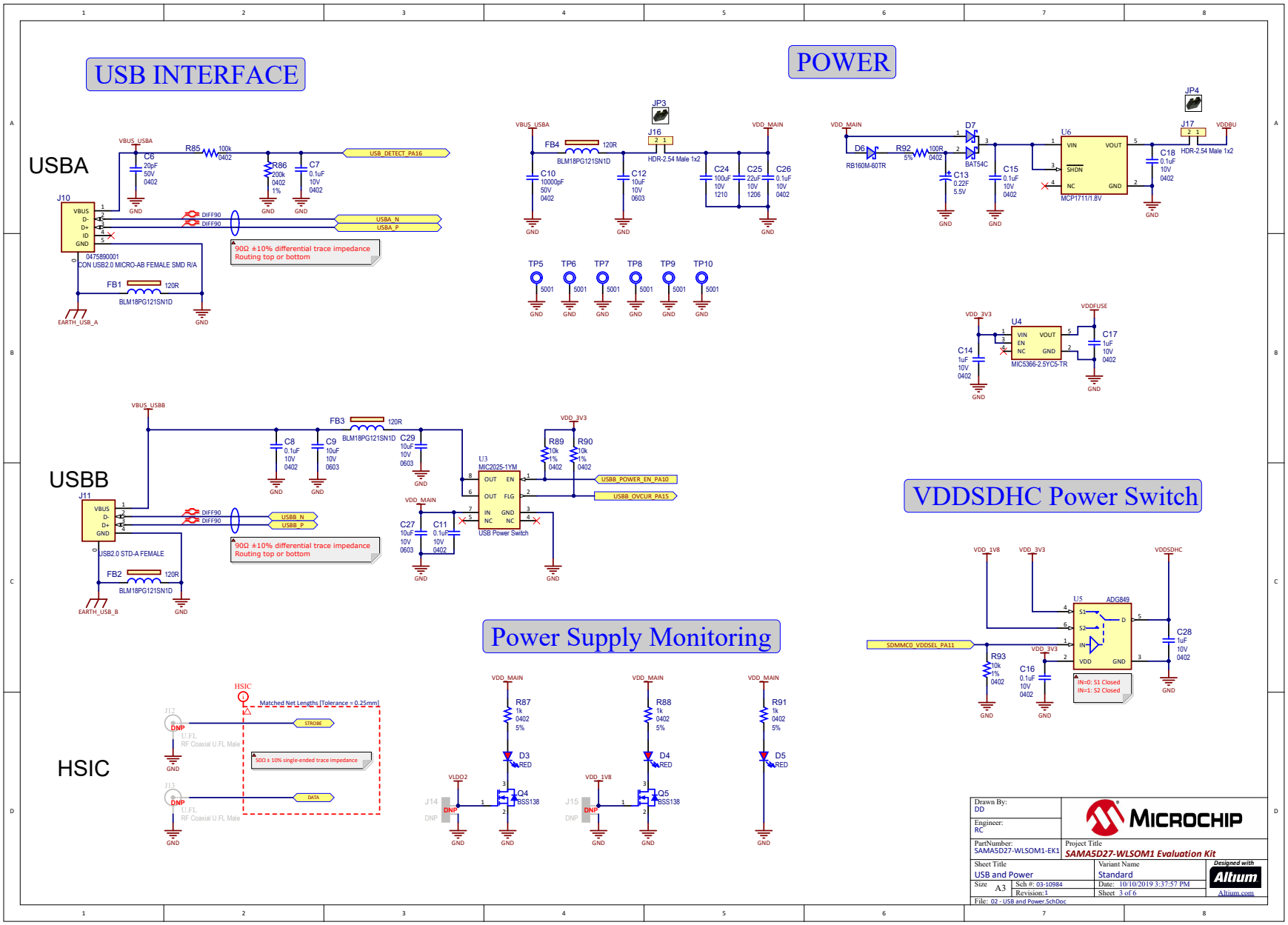


Figure 5-4. ATSAMA5D27-WLSOM1-EK1 Schematic: Page 4

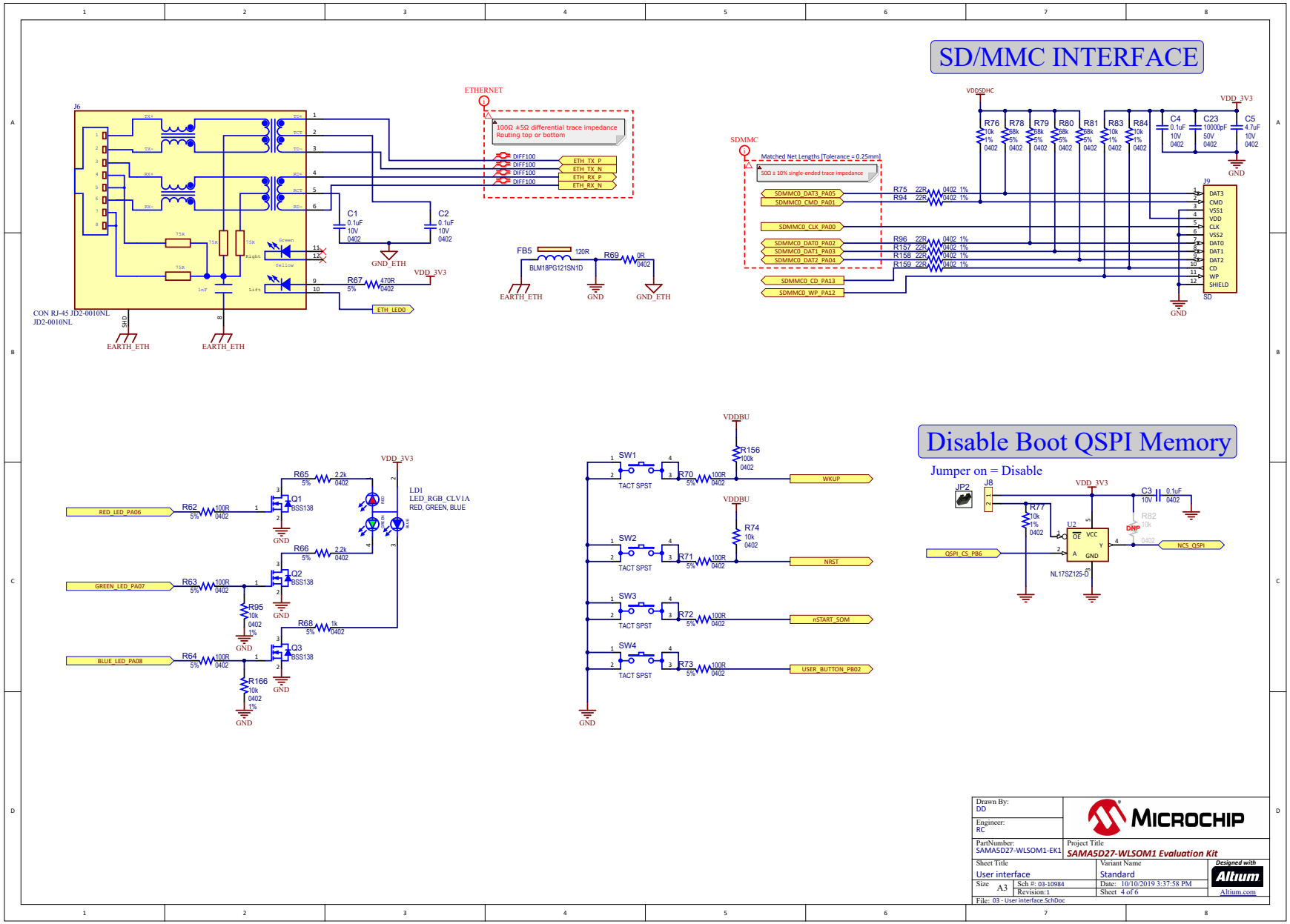


Figure 5-5. ATSAMA5D27-WLSOM1-EK1 Schematic: Page 5

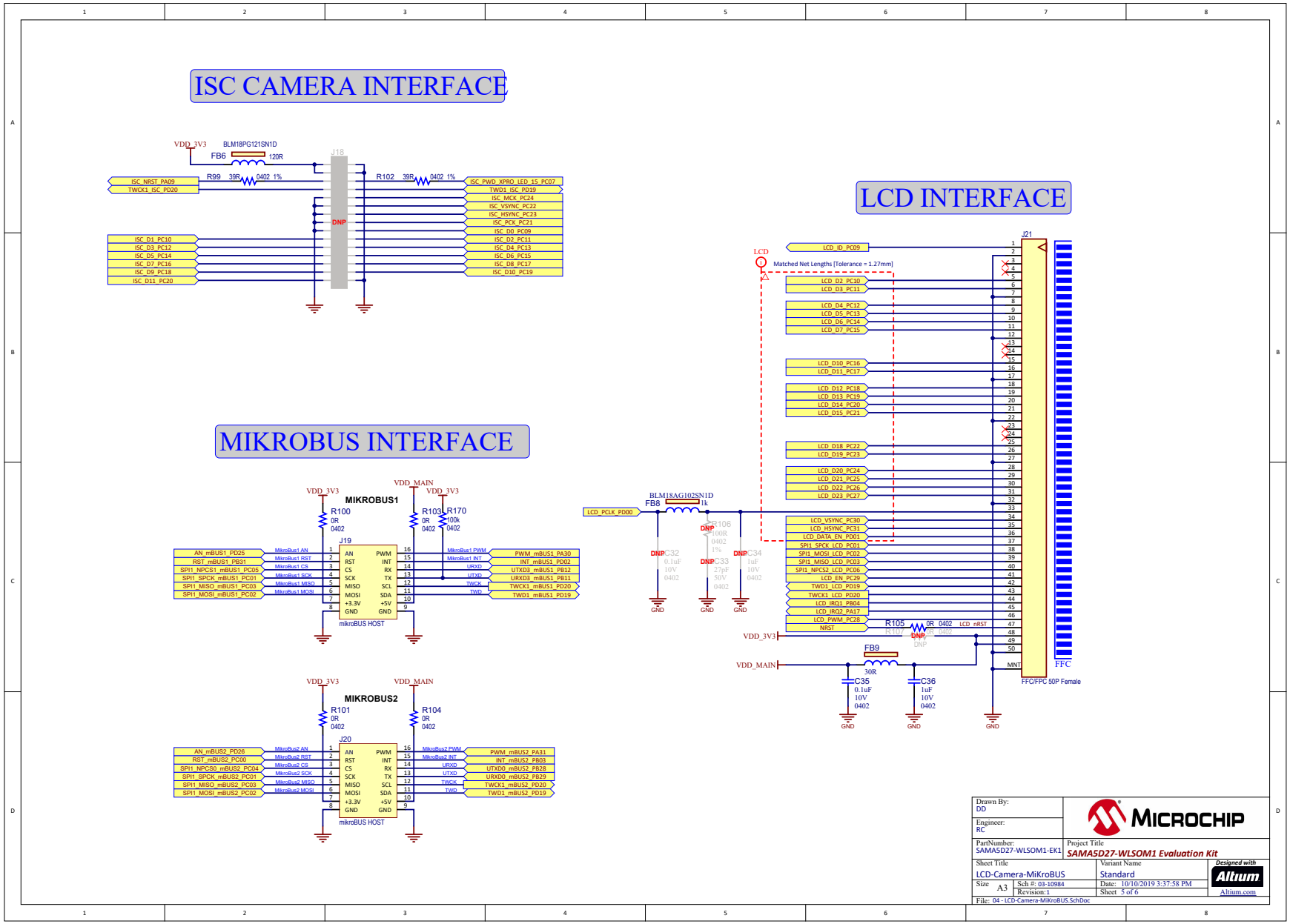


Figure 5-6. ATSAMA5D27-WLSOM1-EK1 Schematic: Page 6

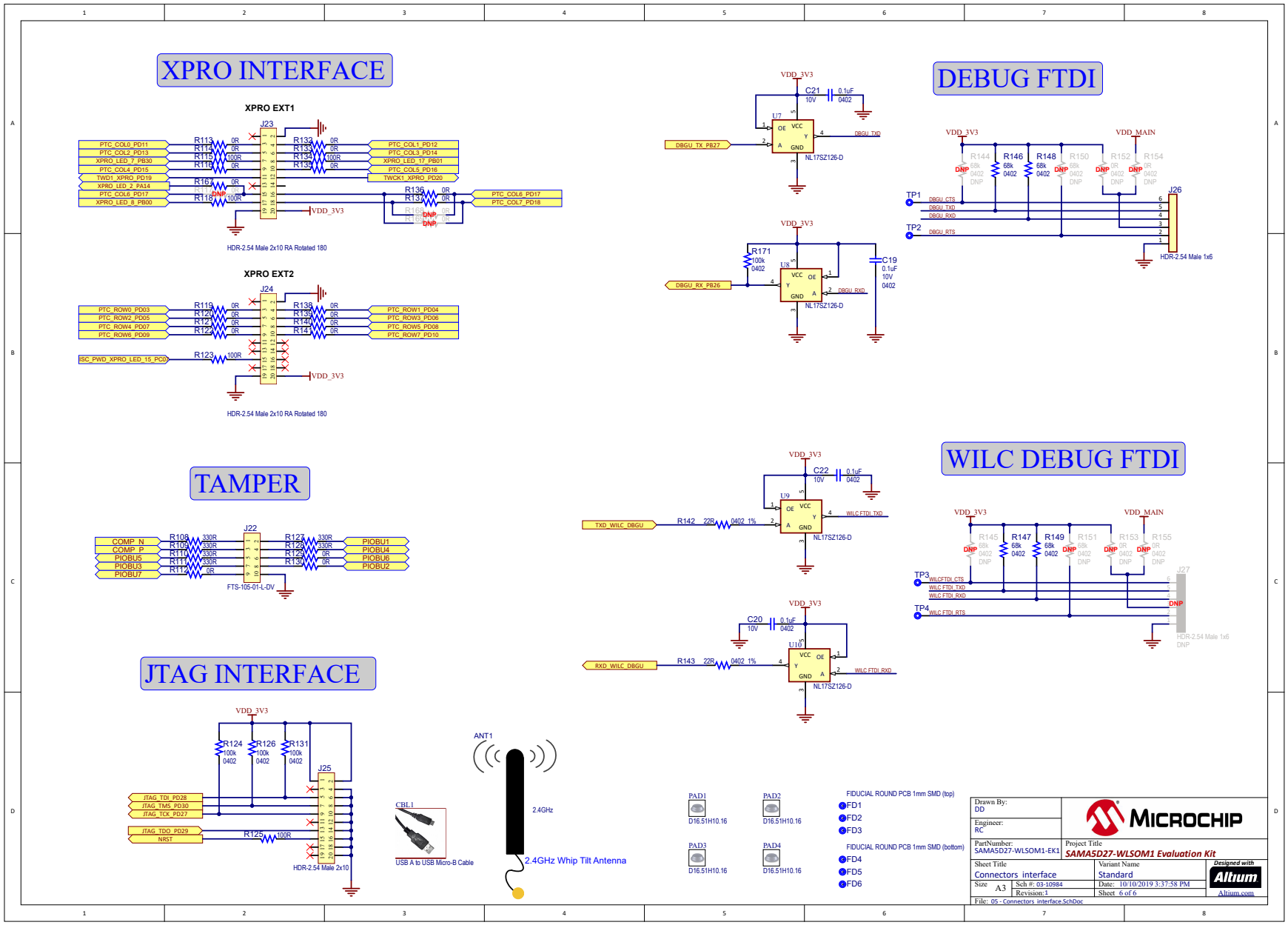


Figure 5-7. ATSAMA5D27-WLSOM1-EK1 Layout: Top Layer

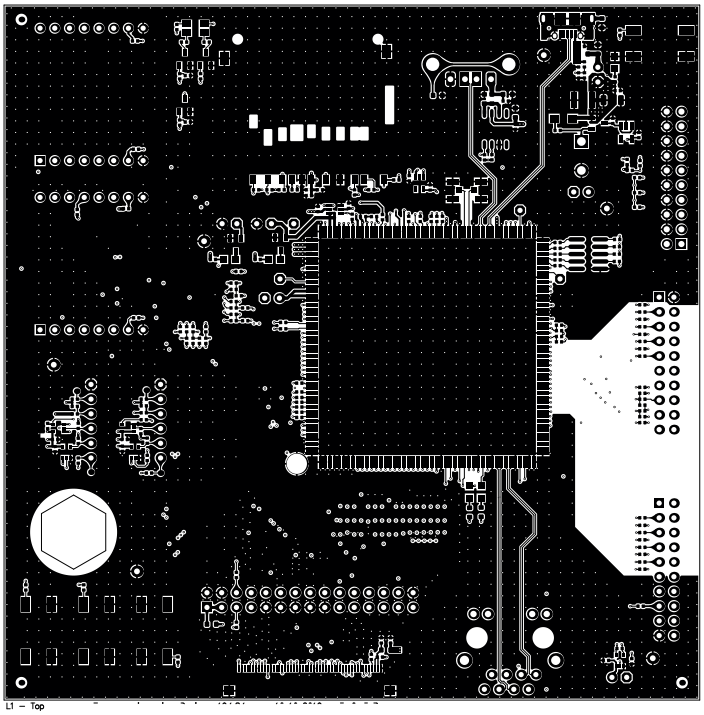


Figure 5-8. ATSAMA5D27-WLSOM1-EK1 Layout: Inner Layer 2 - Ground

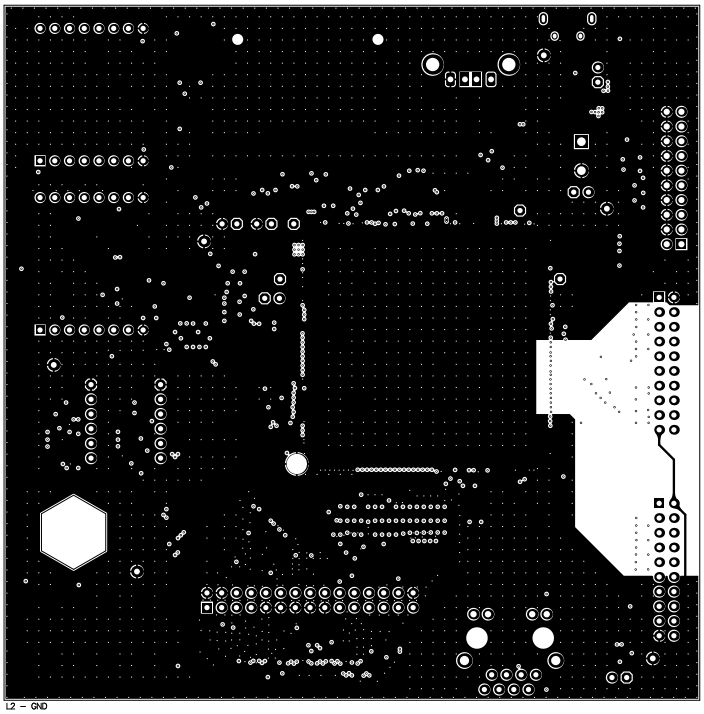


Figure 5-9. ATSAMA5D27-WLSOM1-EK1 Layout: Inner Layer 3 - Signals

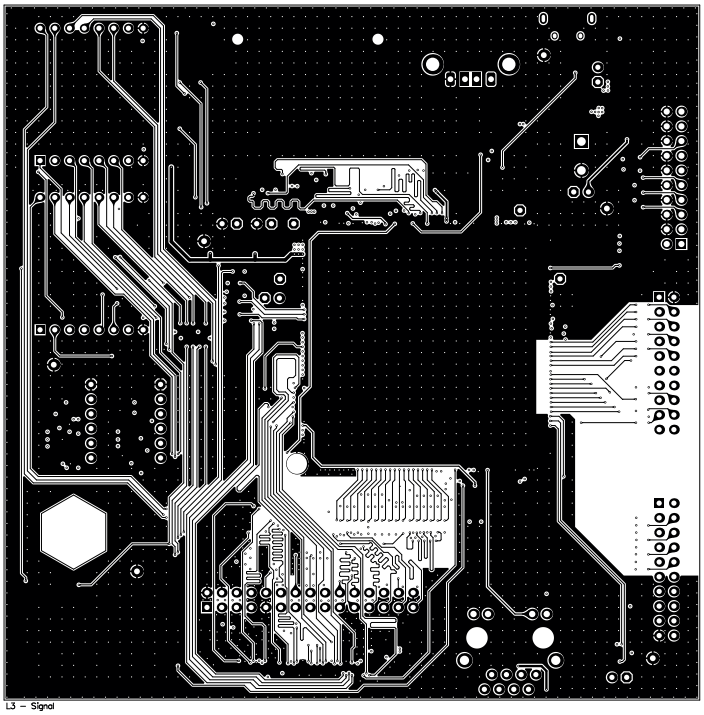


Figure 5-10. ATSAMA5D27-WLSOM1-EK1 Layout: Inner Layer 4: Signals

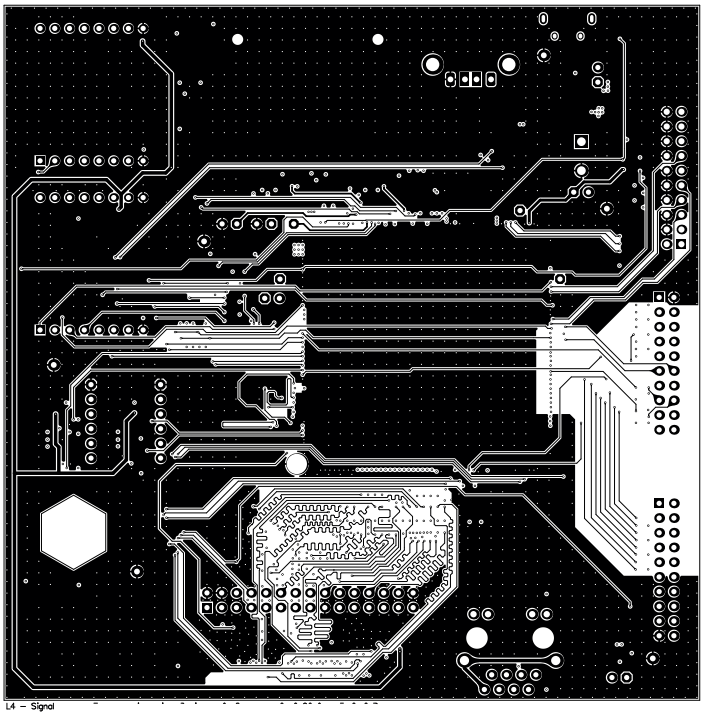


Figure 5-11. ATSAMA5D27-WLSOM1-EK1 Layout: Inner Layer 5: Power

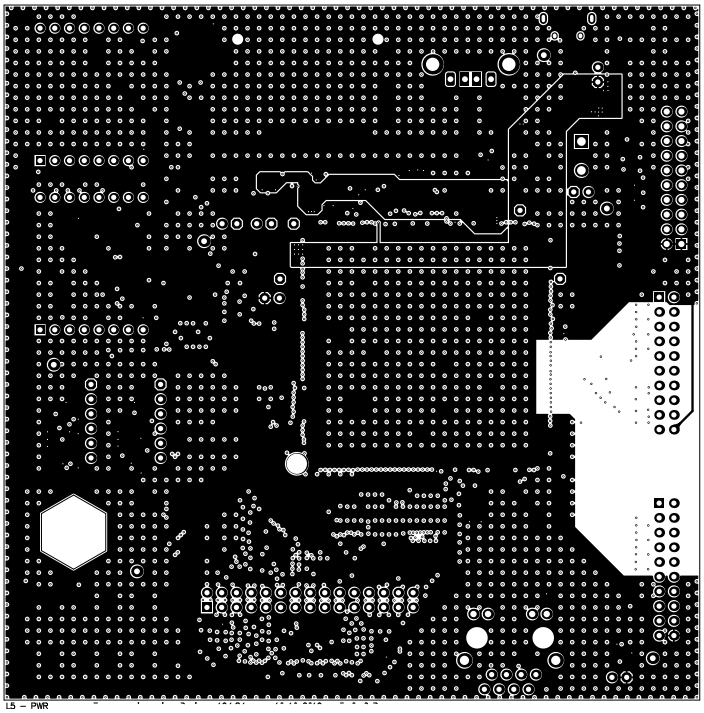
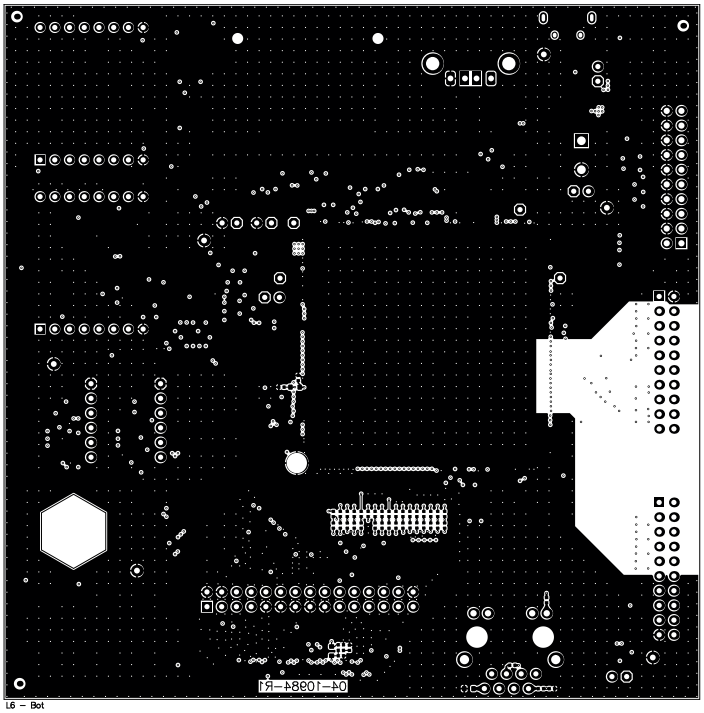


Figure 5-12. ATSAMA5D27-WLSOM1-EK1 Layout: Bottom Layer



6. Ordering Information

Table 6-1. Ordering Details

Ordering Code	Dimensions	Description	Regulatory Information
ATSAMA5D27-WLSOM1-EK1 (DM320117)	120 x 120 mm	Certified MPU Wireless Module with SAMA5D27, WILC3000 and U.FL connector	FCC, IC, CE, RED

7. Revision History

7.1 Rev. A - 10/2019

First issue.

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