

ON Semiconductor®

FDC6333C

30V N & P-Channel PowerTrench® MOSFETs

General Description

These N & P-Channel MOSFETs are produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

Applications

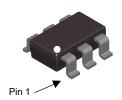
- DC/DC converter
- Load switch
- · LCD display inverter

Features

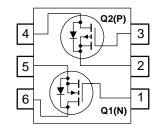
• Q1 2.5 A, 30V. $R_{DS(ON)} = 95 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$ $R_{DS(ON)} = 150 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$

• Q2 -2.0 A, 30V. $R_{DS(ON)} = 150 \text{ m}\Omega @ V_{GS} = -10 \text{ V}$ $R_{DS(ON)} = 220 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$

- Low gate charge
- High performance trench technology for extremely low R_{DS(ON)}.
- SuperSOT –6 package: small footprint (72% smaller than SO-8); low profile (1mm thick).



SuperSOT™-6



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units	
V _{DSS}	Drain-Source Voltage		30	-30	V
V _{GSS}	Gate-Source Voltage		±16	±25	V
I _D	Drain Current - Continuous	(Note 1a)	2.5	-2.0	Α
	– Pulsed		8	-8	
P _D	Power Dissipation for Single Operation	(Note 1a)	0.	96	
		(Note 1b)	0	.9	W
		(Note 1c)	0	.7	
T_J , T_{STG}	Operating and Storage Junction Temperat	–55 to	°C		

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case	(Note 1)	60	°C/W

Package Marking and Ordering Information

 Device Marking	Device	Reel Size	Tape width	Quantity	
.333	FDC6333C	7"	8mm	3000 units	

Symbol	Parameter		Test Conditions			Тур	Max	Units		
Off Char	acteristics				•					
BV _{DSS}	Drain-Source Breakdown Volta	age	$V_{GS} = 0 \text{ V}, \qquad I_D = 250 \mu\text{A} \ V_{GS} = 0 \text{ V}, \qquad I_D = -250 \mu\text{A}$	Q1 Q2	30 -30			V		
<u>ΔBVpss</u> ΔT _J	Breakdown Voltage Temperatu Coefficient	re	$I_D = 250 \mu A, Ref. to 25^{\circ}C$ $I_D = -250 \mu A, Ref. to 25^{\circ}C$	Q1 Q2		27 –22		mV/°C		
I _{DSS}	Zero Gate Voltage Drain Curre	nt	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$	Q1 Q2			1 –1	μА		
I _{GSSF}	Gate-Body Leakage, Forward		$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Q1 Q2			100 100	nA		
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -16 \text{ V}, V_{DS} = 0 \text{ V}$ $V_{GS} = -25 \text{ V}, V_{DS} = 0 \text{ V}$	Q1 Q2			-100 -100	nA			
On Char	acteristics (Note 2)									
$V_{GS(th)}$	Gate Threshold Voltage	Q1	$V_{DS} = V_{GS}, I_D = 250 \mu A$		1	1.8	3	V		
		Q2	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$		-1	-1.8	-3			
$\Delta V_{GS(th)}$	Gate Threshold Voltage	Q1	I _D = 250 μA,Ref. To 25°C			4		mV/°C		
ΔT_{J}	Temperature Coefficient	Q2	$I_D = -250 \mu\text{A,Ref. to } 25^{\circ}\text{C}$			-4				
R _{DS(on)}	Static Drain–Source	Q1	$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$			73	95	mΩ		
D3(0II)	On–Resistance		$V_{GS} = 4.5 \text{ V}, I_{D} = 2.0 \text{ A}$			90	150			
			$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}, T_J = 12$		106	148				
		Q2	$V_{GS} = -10 \text{ V}, I_D = -2.0 \text{ A}$			95	130			
			$V_{GS} = -4.5 \text{ V}, I_D = -1.7 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = -2.0 \text{ A}, T_J = 1$	25°€		142 149	220 216			
	On–State Drain Current		$V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	8	149	210	Α			
$I_{D(on)}$	On-State Diam Current	Q1 Q2	$V_{GS} = -10 \text{ V}, V_{DS} = 3 \text{ V}$ $V_{GS} = -10 \text{ V}, V_{DS} = -5 \text{ V}$		-8			^		
	Forward Transconductance	+	$V_{DS} = 5 \text{ V}$ $I_{D} = 2.5 \text{ A}$		-0	7		S		
g FS	Forward Transconductance	Q1 Q2	$V_{DS} = -5 \text{ V}$ $I_D = -2.0 \text{A}$			3		3		
Dynamic	Characteristics	, Q _	50 1 5 1		1					
C _{iss}	Input Capacitance	Q1	V _{DS} =15 V, V _{GS} = 0 V, f=1.0N	1Hz	1	282		pF		
Oiss	input Capacitance	Q2	V_{DS} =-15 V, V $_{GS}$ = 0 V, f=1.0			185		Pi		
C _{oss}	Output Capacitance	Q1	V_{DS} =15 V, V $_{GS}$ = 0 V, f=1.0N		49		pF			
Ooss	Output Capacitance	Q2	V_{DS} =-15 V, V $_{GS}$ = 0 V, f=1.0		56		Pi			
C _{rss}	Reverse Transfer Capacitance	+	V _{DS} =15 V, V _{GS} = 0 V, f=1.0N			20		pF		
O _{rss}	Reverse Transfer Capacitance	Q2	V_{DS} =-15 V, V $_{GS}$ = 0 V, f=1.00			26		рг		
Switchin	lg Characteristics (Note 2)	QZ	103 10 1, 1 63 0 1, 1 110			20				
		01	T			4.5	9	no		
t _{d(on)}	Turn-On Delay Time	Q1 Q2	For Q1 : V _{DS} =15 V, I _{DS} = 1 A			4.5	9	ns		
t _r	Turn-On Rise Time	Q1	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$			6	12	ns		
		Q2	For Q2 :			13	23			
t _{d(off)}	Turn-Off Delay Time	Q1	V _{DS} =-15 V, I _{DS} = -1 A			19	34	ns		
		Q2	V_{GS} = -10 V, R_{GEN} = 6 Ω			11	20			
t _f	Turn-Off Fall Time	Q1				1.5	3	ns		
		Q2				2	4			
Qg	Total Gate Charge	Q1	For Q1 :			4.7	6.6	nC		
	-	Q2	$V_{DS} = 15 \text{ V}, I_{DS} = 2.5 \text{ A}$			4.1	5.7			
Q _{gs}	Gate-Source Charge	Q1	V_{GS} = 10 V, R_{GEN} = 6 Ω			0.9		nC		
		Q2	For Q2 : V _{DS} =–15 V, I _{DS} = –2.0 A			0.8				
Q_{gd}	Gate-Drain Charge	Q1	$V_{DS} = -15 \text{ V}, T_{DS} = -2.0 \text{ A}$ - $V_{GS} = -10 \text{ V},$			0.6		nC		
		Q2	,			0.4				

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter Test Conditions		ons	Min	Тур	Max	Units		
Drain-Source Diode Characteristics and Maximum Ratings									
Is	Maximum Continuous Drain-Source Diode Forward Current Q1						0.8	Α	
	Q2					-0.8			
V _{SD}	Drain-Source Diode Forward	Q1	$V_{GS} = 0 \text{ V}, I_{S} = 0.8 \text{ A}$	(Note 2)		0.8	1.2	V	
	Voltage	Q2	$V_{GS} = 0 \text{ V}, I_{S} = 0.8 \text{ A}$	(Note 2)		0.8	-1.2		

Notes:

R_{8JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of
the drain pins. R_{8JC} is guaranteed by design while R_{8CA} is determined by the user's board design.



a) 130 °C/W when mounted on a 0.125 in² pad of 2 oz. copper.



b) 140°/W when mounted on a .004 in² pad of 2 oz copper



c) 180°/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics: N-Channel

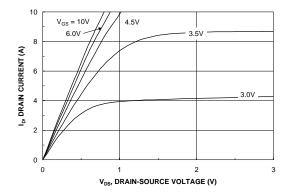


Figure 1. On-Region Characteristics.

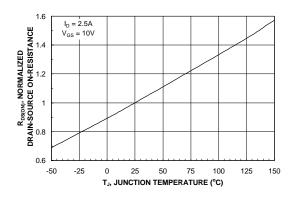


Figure 3. On-Resistance Variation withTemperature.

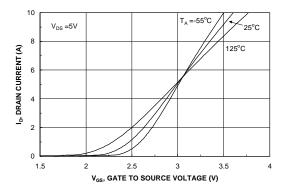


Figure 5. Transfer Characteristics.

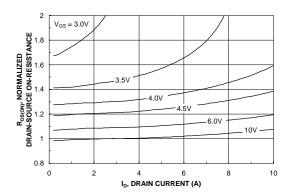


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

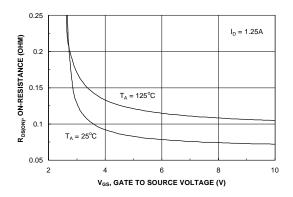


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

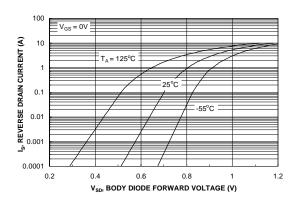
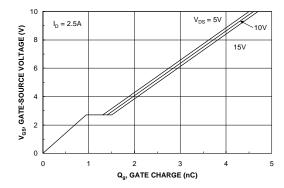


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-Channel (continued)



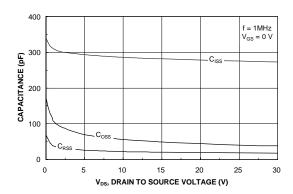
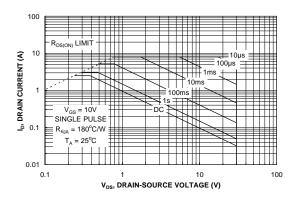


Figure 7. Gate Charge Characteristics.





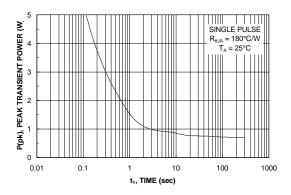


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: P-Channel

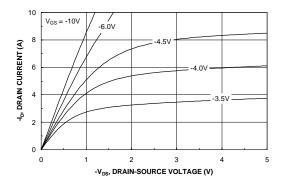


Figure 11. On-Region Characteristics.

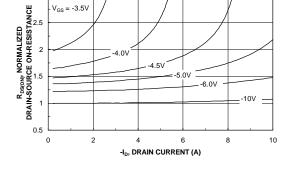


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

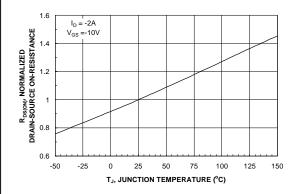


Figure 13. On-Resistance Variation withTemperature.

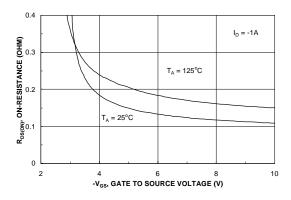


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

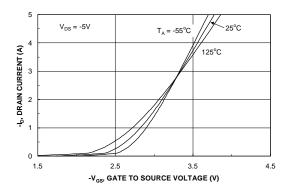


Figure 15. Transfer Characteristics.

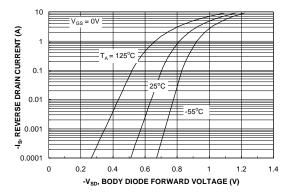
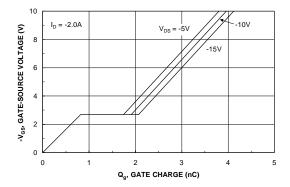


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: P-Channel (continued)



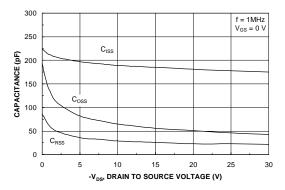


Figure 17. Gate Charge Characteristics.

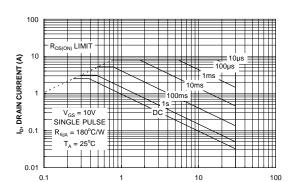


Figure 18. Capacitance Characteristics.

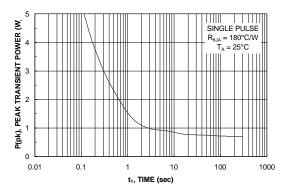


Figure 19. Maximum Safe Operating Area.

V_{DS}, DRAIN-SOURCE VOLTAGE (V)



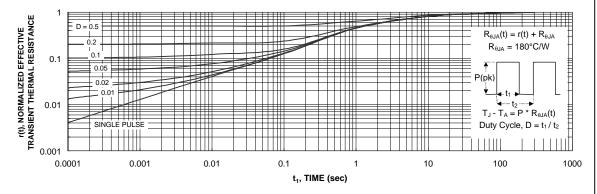


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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