IM283

Low-voltage RFID reader IC for 125kHz tags

DATA SHEET

Typical Applications

- Integrated RFID base-stations
- RFID reader-writers
- Car immobiliser
- Low voltage portable readers

Features

- Low voltage down to 2.5 volts
- Read and Write capabilities.
- Includes a full ID processing for EM4100 and EM4200* series
- Supported frequency range: 100 to 150 kHz
- Optimization of reading conditions by using RTA™: unique reader-transponder self-adapting technique.
- High-power dual antena drive.
- 100% and 50% modulation write capability.
- Multiple data rates: 2kbit/s, 4kbit/s, 8kbit/s.
- Operating temperture range: -40 to +85°C

Plastic SO18

Product Description

The IM283 is a fully-integrated 125 kHz RFID reader circuit. It is specially designed for being a space and cost efficient kernel IC of an RFID reading and writing base station. It covers the digital real time functions and the analogue signal processing necessary to access standard 64-bits transponders available on the market. IM283 is accessible by a standard micro – controller as an intelligent front - end peripheral device. A unique mutual tuning capability (RTA™) allows dynamic adaptation to every transponder read, particularly in poor reading conditions. IM283 is versatile enough to work in most low-power (short distance) and high power (longer distance) applications. IM283 is fully compatible with latest version of SW016 reader IC.

(*) using EM4100 / 4102 protocols

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1 Product Overview

1.1 *General Description*

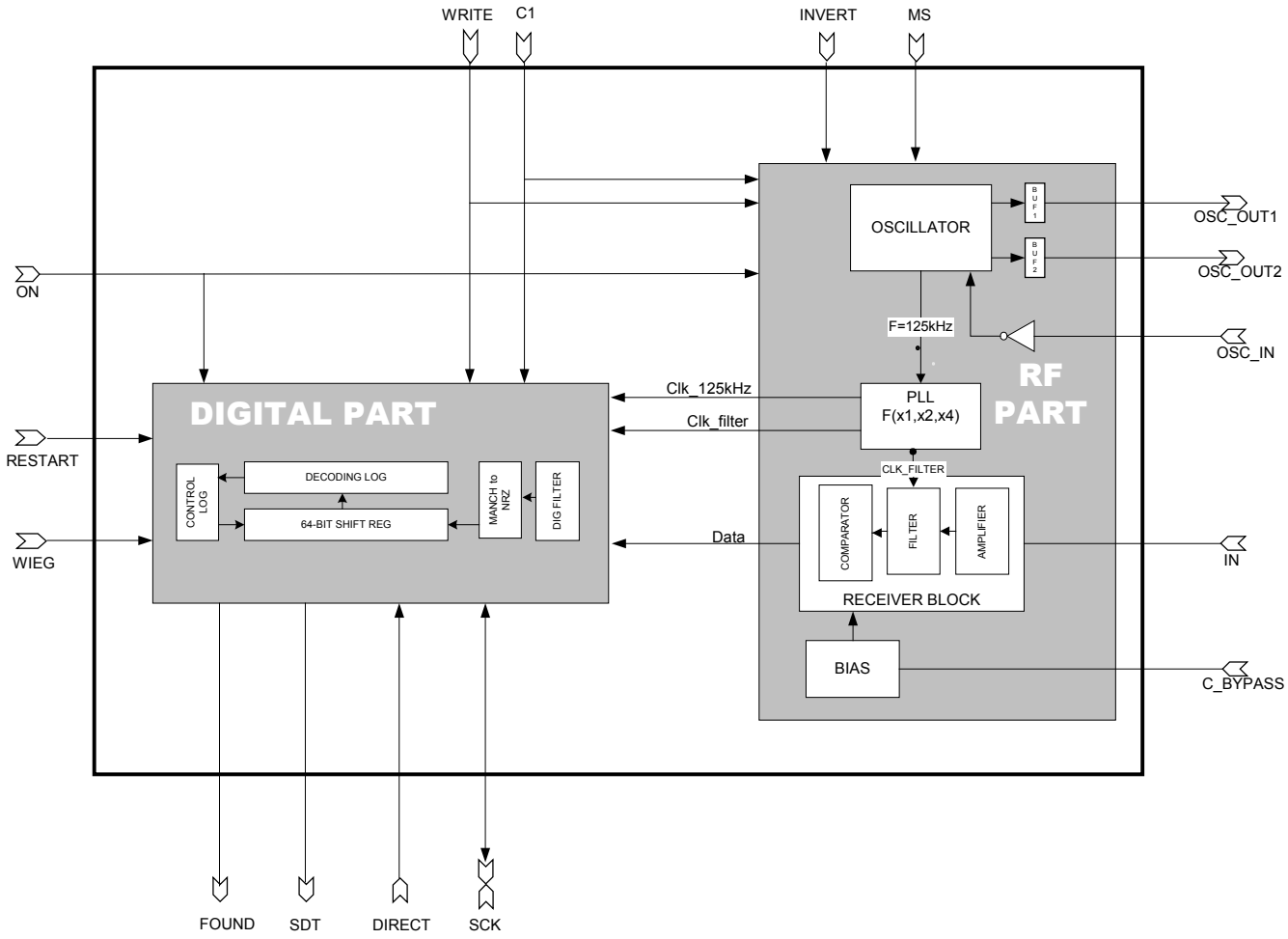
IM283 is a fully integrated RFID reader / writer that can be used as the dedicated RFID peripheral of your RFID base-station.

Adapted to EM410x transponders, IM283 enables a whole-in-one processing of 64-bits standard tags. it processes reading of the raw tag ID string, then performs dynamic parity and Manchester integrity checks and finally bufferizes the 40bits of usable ID code for the micro to stream out serially.

IM283 provides full a compatibility with old SW016 reader IC.

- Auto oscillation between OSC_OUT1 (and/or OSC_OUT2) and OSC_IN
- Possibility to drive OSC_IN with a 125kHz (100 – 150kHz) to fix the carrier frequency
- External envelope detection
- Internal filtering (sensitivity: 1mV rms)
- Digital-block functions identical to existing SW016 – decoding of Manchester coded input stream
- Writing capability

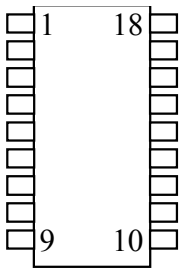
1.2 Block Diagram



1.3 I/O Description

Table.1 General pin description

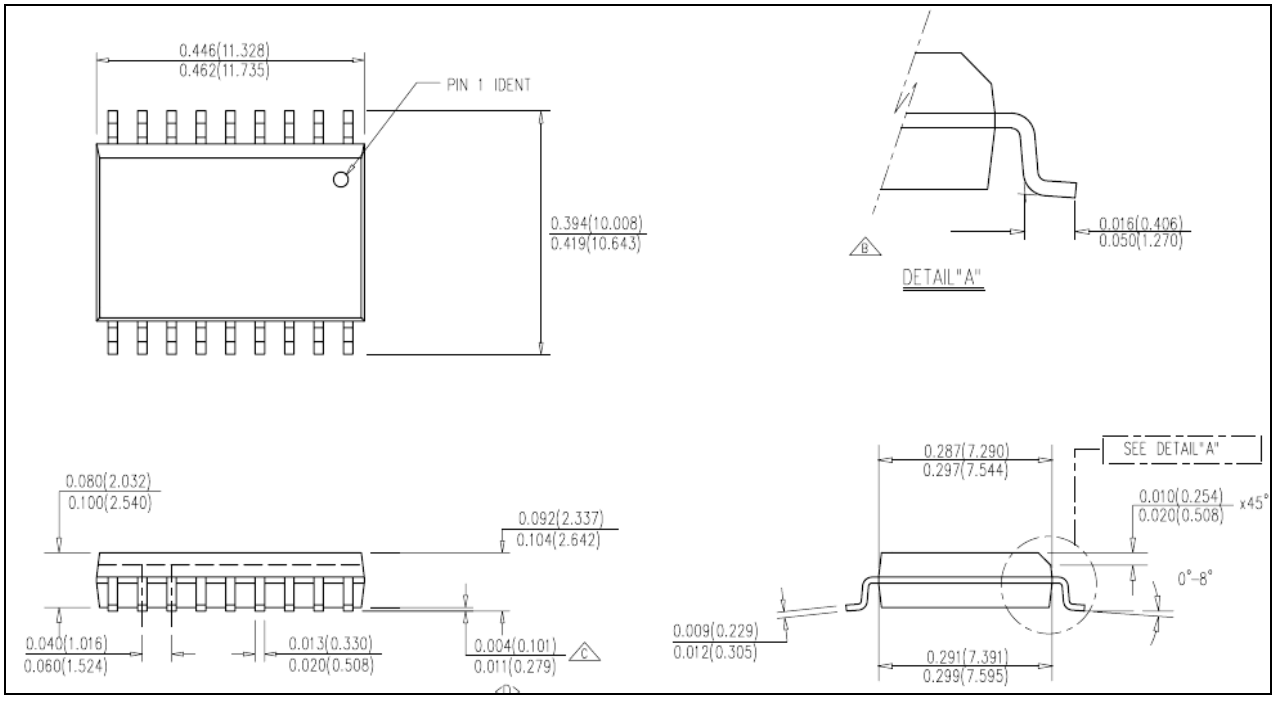
Package Pin #	Die-pad Name	I/O Type
1	INVERT	In
2	WRITE	In
3	RESTART	In
4	FOUND	Out
5	SCK	In/Out
6	SDT	Out
7	C1	In
8	MS	In
9	GND	
10	DIRECT	In
11	C_BYPASS	In
12	IN	In
13	OSC_IN	In
14	OSC_OUT2	Out
15	OSC_OUT1	Out
16	ON	In
17	VDDA	
18	VDD	



SOIC 18

1.4 Package outline

SOIC 18 PACKAGE



1.5 *Typical application schematics*

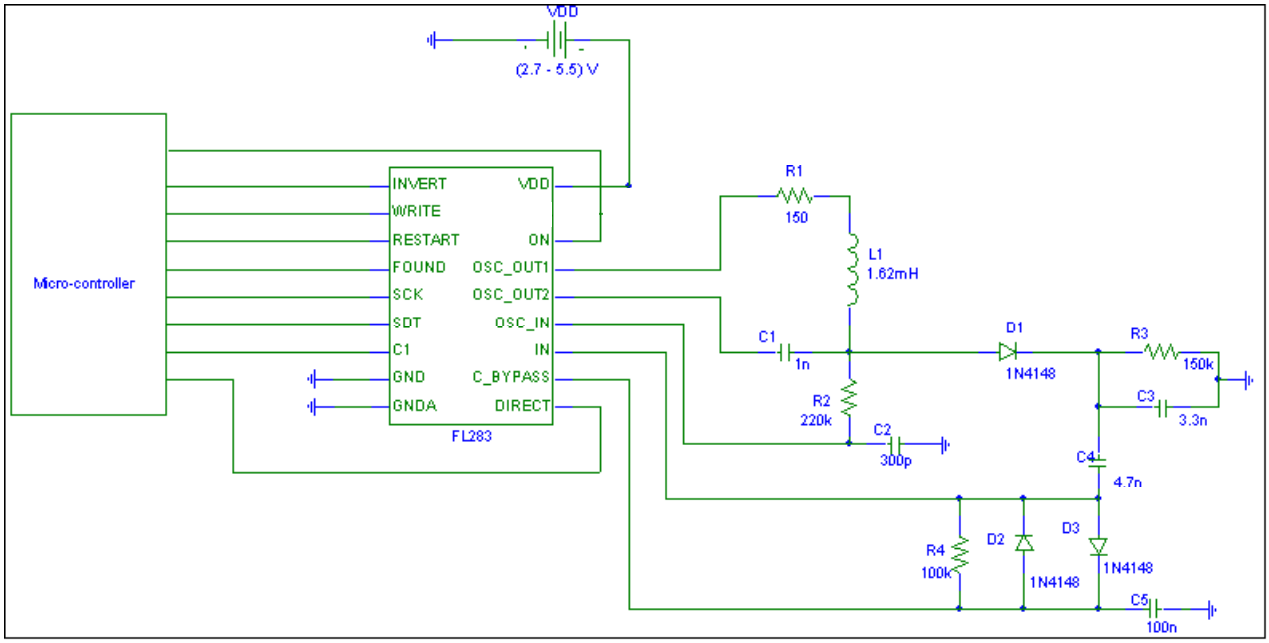


Fig. 1 : Application drawing (short distance reader)

1.6 *Packing & Ordering information*

- Standard packing: antistatic clear tubes
- Base quantity: 2000

Note: for smaller quantities, please check with your local distributor.

Table.2 Ordering codes

Product description	Package	Ordering code	Notice
IM283	SOIC18	IM283A-FT	-

2 Detailed description

2.1 *Overview*

Particularly dedicated to EM410x transponders, IM283 enables a whole-in-one processing of 64-bits standard tags. No stream decoding is necessary: IM283 reads the tags and stores the ID code for the host (micro-controller) to read whenever it can. IM283 then work as a pure slave peripheral and does not require any real-time resource from the host.

For customers who have been using the old SW016, IM283 will ensure full compatibility in their application.

- **IM283 is set by leaving pin DIRECT unconnected (or connected to ground)**

- IM283 is controlled by and external microcontroller, which provides the necessary control signals to:
  - Switch on and off (stand-by mode) IM283
  - Reset IM283 to restart ID searching (RESTARTcommand)
  - Send a SCK signal to clock the serial data bit stream store into IM283

  In return, it receives from IM283:
  - The indication that an ID has been successfully read (FOUND signal)
  - An error free ID number as a raw serial NRZ data

- The power output drives an antenna (coil) tuned to the right frequency and connected to the OSC_OUT1 pin provides a 125 Khz carrier.

The amplitude-modulated signal due to the response of the tag is superimposed to the main carrier. A simple diode and an RC network provide a first level of filtering to leave out the high amplitude carrier from the small feedback signal.
Additional on-chip filtering provides further rejection of mains disturbance and remaining carrier before full synchronization, demodulation and error checking.

2.2 *Data Frame Check*

A state machine is implemented for data integrity checking. The following states are sequenced:

STATE 1: Wait for header.
This state is valid after RESTART. Internal 64-bit shift register is reset and then data acquisition is performed.

STATE 2: Data format check.
This state is valid after STATE 1. In this state, the incoming data is checked for correct parity and for header + stop bit integrity.
If an error occurs, then the system goes back to STATE 1.
If no error - then STATE 3.

STATE 3: Ready for data transfer.
This state follows STATE 2 when there was no error in received data frame.
FOUND signal is asserted active high and remains active while STATE 3 is valid.
Digital part is ready to output serial data to the microcontroller.
STATE 3 is a stable state: it does not change unless a proper RESTART command is provided.
With a RESTART command the system goes back to STATE 1.

2.2.1 ID transfert protocol

IM283 is fully compatible with Marin EM4001, EM4002 EM4100 and EM4102 tags or 64-bits standard transponders of which the memory array is organized as:

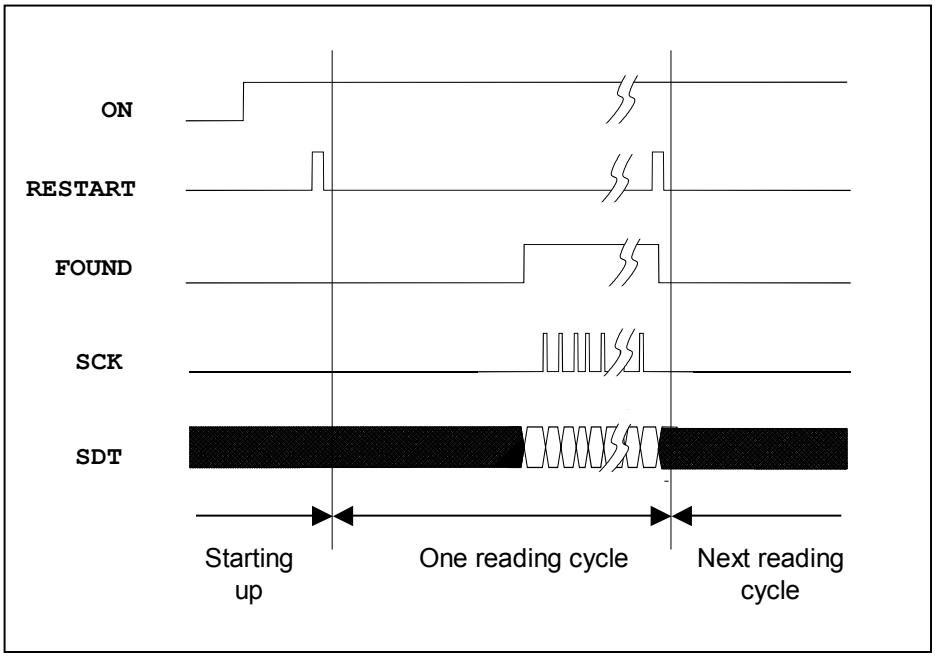
1	1	1	1	1	1	1	1	1	- 9bits header
8 version bits or customer ID				D00	D01	D02	D03	P0	- 4data bit &
				D10	D11	D12	D13	P1	- associated
				D20	D21	D22	D23	P2	even row
				D30	D31	D32	D33	P3	parity bit
				D40	D41	D42	D43	P4	
				D50	D51	D52	D53	P5	
				D60	D61	D62	D63	P6	
				D70	D71	D72	D73	P7	
				D80	D81	D82	D83	P8	
				D90	D91	D92	D93	P9	
				PC0	PC1	PC2	PC3	C	- 4 column even parity bits, no row parity bit
									- C = 0 as a stop bit

While STATE3 is valid (FOUND command is active), IM283 is ready to provide the 40 bits of the ID data (D00 to D93) to the microcontroller, MSB first.

2.2.2 ID transfer protocol

Transfer protocol is described below. For timing characteristics, refer to AC electrical characteristics.

When powered, activation of IM283 will occur only when the host applies high level to ON pin.
The host will turn FL283 in acquisition mode (reading) by applying a RESTART command of the type: low/high/low.
All readings should start only after such pulsed reset.
When a tag is read, IM283 returns a FOUND interrupt to the host that can then clock out the 40 ID bits.
When done so, next reading will occur only after than a RESTART command is sent.

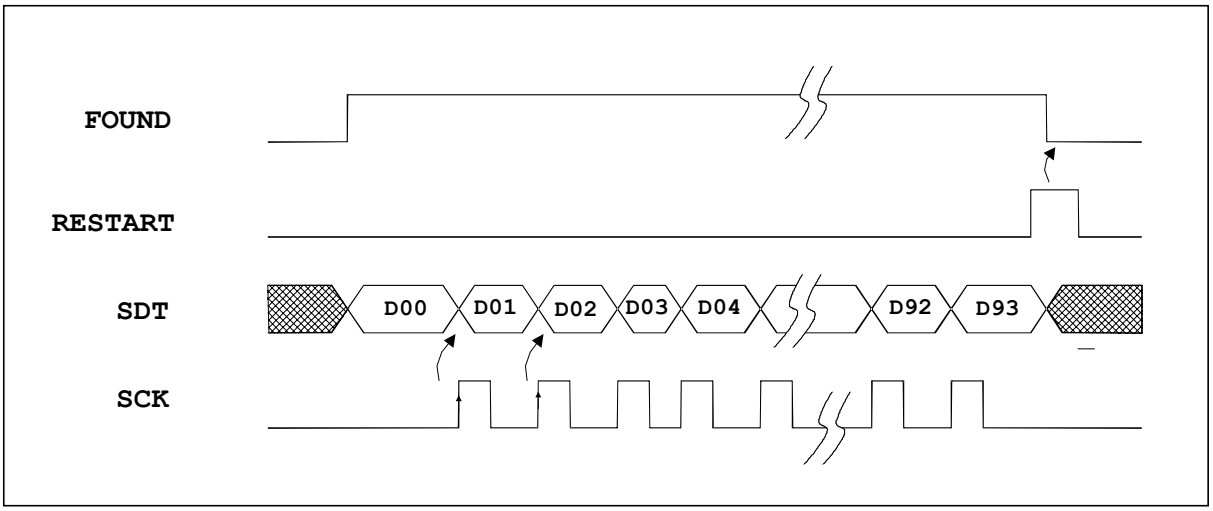


IMPORTANT NOTES:

➔ When FOUND turns active, the first bit of data is already present on the SDT output pin.

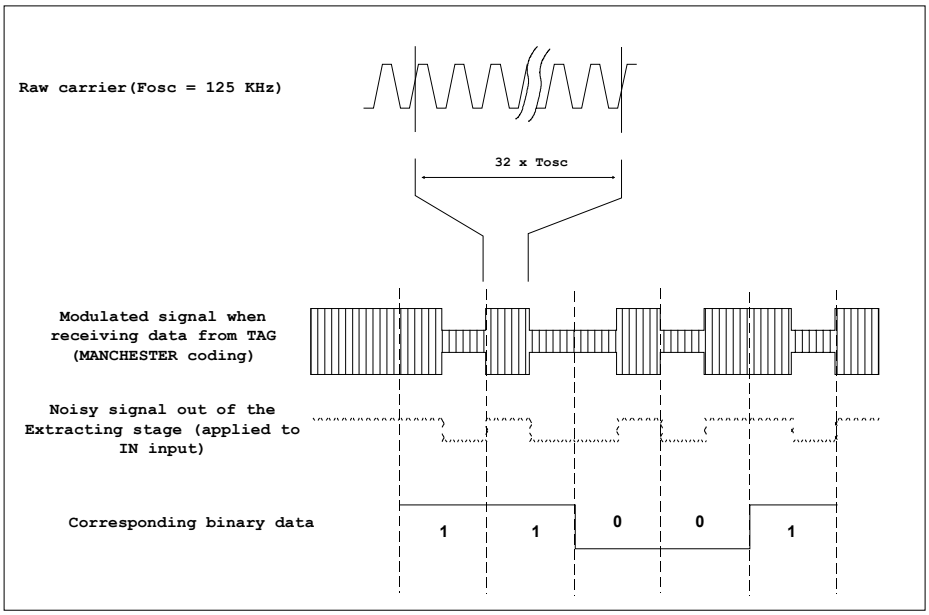
➔ Each changing low-to-high level of SCK provides the next bit on SDT.

Only 39 SCK pulses are necessary to clock the 40 ID bits.



2.2.3 Decoding of the input stream

According to Manchester coding the information read out from the tag is modulated as follows:



2.2.4 Detailed usage of the pins of IM283

Pin #	Pin Name	I/O Type	Description	NOTE
1	INVERT	CMOS input, pulled up	High level on the input induces 180° phase between OSC_OUT1 and OSC_OUT2,	See Table 4 for full description
2	WRITE	CMOS input, pulled down	WRITE and C1 pins control: - READ/WRITE mode - data-rate settings	See Table 3 for full description
3	RESTART	H-active CMOS input, internally pulled-down	A pulse on RESTART pin should occur before any reading cycle.	
4	FOUND	CMOS Output	High level on this output indicates that the received ID code is correct and can be read out from microcontroller.	
5	SCK	CMOS I/O (input is pulled-down)	Input pin In Read Mode. Each low-to-high transition on SCK (when FOUND is high) puts the next bit of the ID code on the SDT output. Output pin in Write mode. - Fc(125kHz) is output on SCK.	See Table 3 for full description
6	SDT	CMOS output	SDT acts as serial data output for the decoded ID code When FOUND is high, each low to high transition on SCK acts on the SDT pin to output the next bit of the ID code MSB (D00) is sent first (see “Data Transfer Protocol”).	See Table 3 for full description
7	C1	CMOS input, pulled down	WRITE and C1 pins control: - READ/WRITE mode - data-rate settings	See table 3 for full description.
8	MS	H-active CMOS input, pulled up	Three-state control of OSC_OUT1. When high – OSC_OUT1 is in high Z state	See Table 4 for full description.
9	GND		Power supply	
10	DIRECT	H-active CMOS input, internally pulled down	DIRECT should be left unconnected or tied to ZERO).	See table 3 for full description.
11	C_BYPASS	Analog pins connected to RF circuitry: Application schematics are given in Chapter 6. Applications Notes: 1. A square wave CMOS level signal can be applied on OSC_IN also. 2. External filtering capacitor on C_BYPASS. 3. OSC_OUT1 and OSC_OUT2 operating modes are described in table 4 and shown on Fig. 2, Fig. 3 and Fig. 4		
12	IN			
13	OSC_IN			
14	OSC_OUT2			
15	OSC_OUT1			
16	ON	H-active CMOS input, internally pulled down	When active high, the ON pin turns the circuit into full operation When ON is low, the circuit is turned into sleep, digital part is in reset state.	
17	VDDA		Analog power supply	

Pin #	Pin Name	I/O Type	Description	NOTE
18	VDD		Digital power supply	

Table.3: Read/Write operating modes control and digital signals behaviour

CONTROL PINS			BEHAVIOUR				
DIRECT	WRITE	C1	OPERATING MODES	RESTART	FOUND	SCK	SDT
0	0	0	WRITE	Not used	Not used	Out: Fc (125kHz)	Not used
0	0	1	READ (data rate=8Kbit/s)	Initiate new read cycle	Interrupt when ID code ready	Input clock to stream-out ID code on SDT	Serial ID code output; clocked by SCK
0	1	0	READ (data rate=2Kbit/s)	Initiate new read cycle	Interrupt when ID code ready	Input clock to stream-out ID code on SDT	Serial ID code output; clocked by SCK
0	1	1	READ (data rate=4Kbit/s)	Initiate new read cycle	Interrupt when ID code ready	Input clock to stream-out ID code on SDT	Serial ID code output; clocked by SCK

Application Note for Mode Control Pins:
Pins WRITE and C1 are static inputs in case of read-only tags. In case of read-write tags these two inputs (or only one of them) must be controlled dynamically by the host.

Table.4 : Specification of OSC_OUT1 and OSC_OUT2 behaviour according to different operating modes

OPERATING MODE	Pin INVERT	Pin MS (Modulation select)	OSC_OUT1 and OSC_OUT2 behaviour	Shown on Application figure :
READ	0	X	OSC_OUT1 = not OSC_IN OSC_OUT2 = not OSC_IN	Fig .3/ Fig.4
	1	0	OSC_OUT1 = not OSC_IN OSC_OUT2 = OSC_IN	Fig .2
		1	OSC_OUT1=”Z” OSC_OUT2 = not OSC_IN	Fig .5
WRITE	0	0	OSC_OUT1 = 0 OSC_OUT2 = 0	Fig .3
		1	OSC_OUT1=”Z” OSC_OUT2 = not OSC_IN	Fig .4
	1	0	OSC_OUT1 = 0 OSC_OUT2 = 0	Fig .2
		1	OSC_OUT1=”Z” OSC_OUT2 = 0	Fig .5

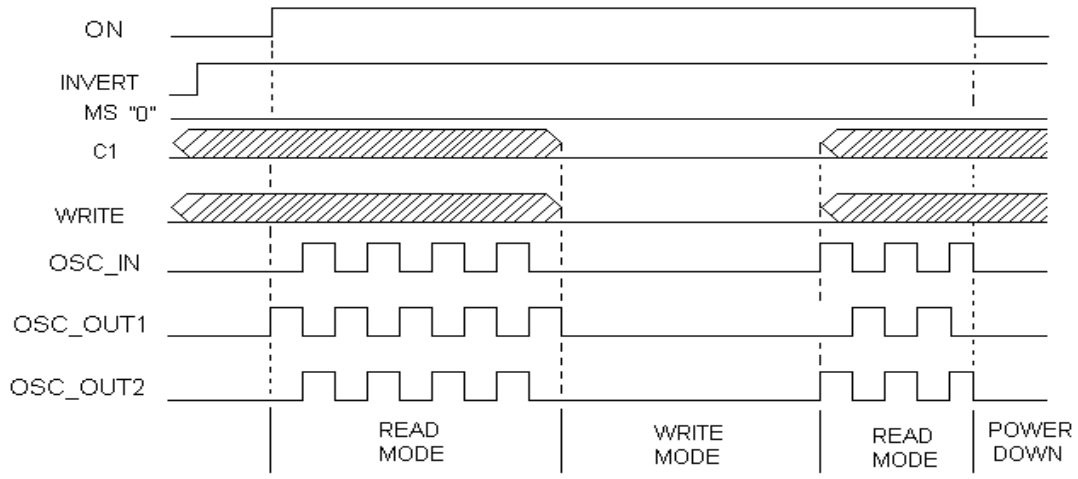


Fig.2 : OSC_OUT1 and OSC_OUT2 are inverted in Read mode, 100% modulation in Write mode

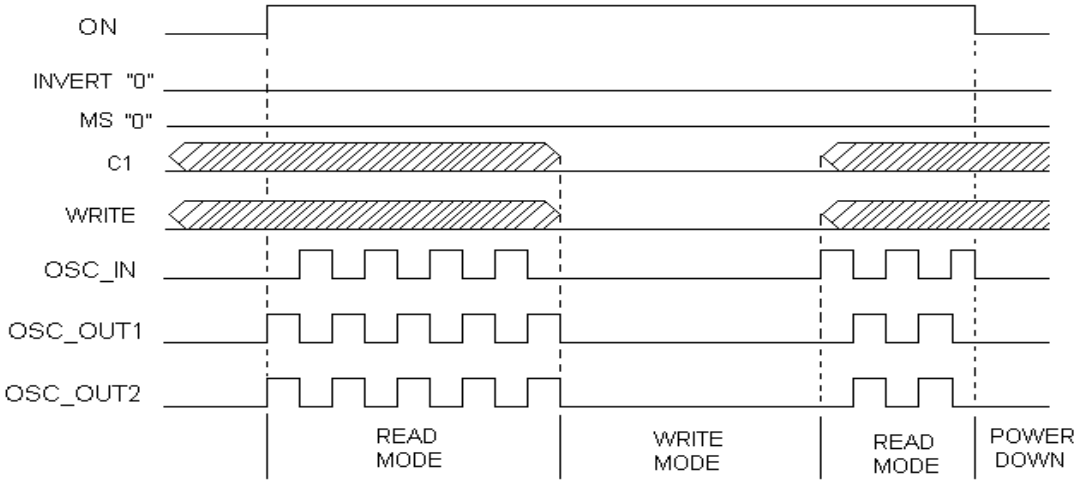


Fig.3 : OSC_OUT1 and OSC_OUT2 are in phase in Read mode, 100% modulation in Write mode

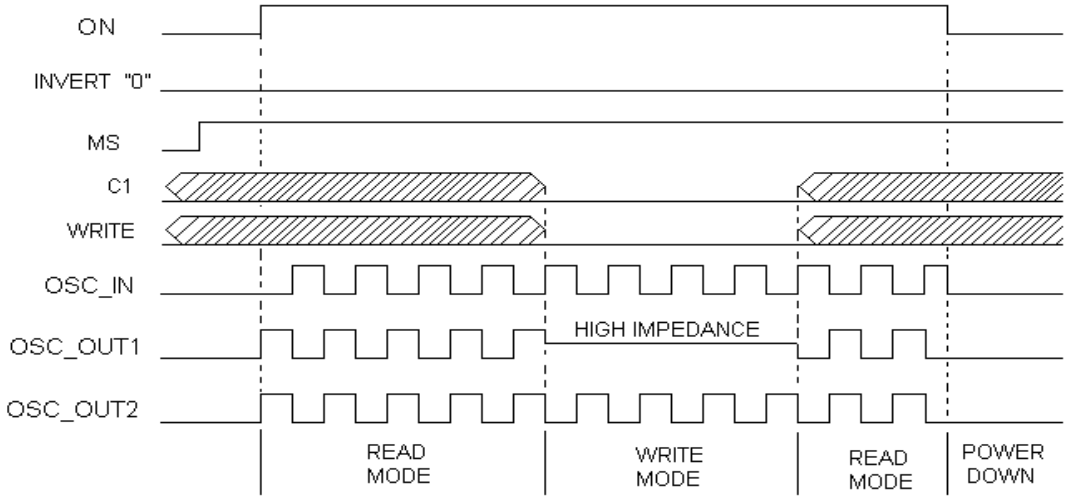


Fig.4 : OSC_OUT1 and OSC_OUT2 are in phase in Read mode, 50% modulation in Write mode

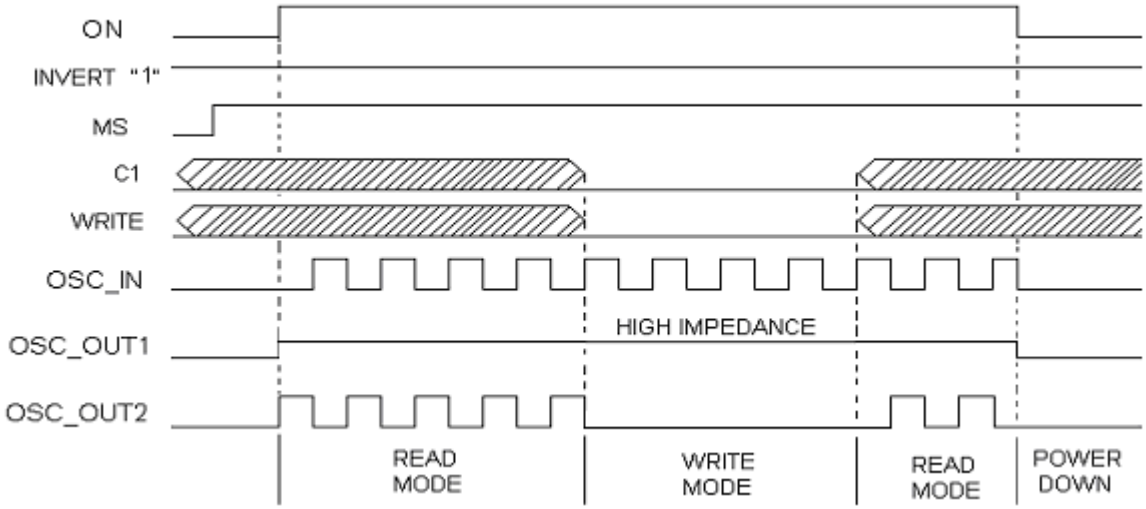


Fig.5 : OSC_OUT1 is in high impedance state, OSC_OUT2 is inverted in Read mode and zero in Write mode

3 Electrical characteristics

3.1 *Absolute Maximum Ratings*

Parameter	Symbol	Conditions
Max storage temperature	$T_{STOREmax}$	+150 °C
Min storage temperature	$T_{STOREmin}$	-65 °C
Power supply voltage	V_{DD} &V_{DDA}	-0.3 to 7V
Voltage on any inputs		GND -0.3V to V_{DD} +0.3V
Digital input current	I_{IL}	±10 mA for Vin<GND or Vin>V_{DD}
Analogue input current	I_{IA}	±10 mA for Vin<GND or Vin>V_{DD}
Electrostatic discharge according to MIL-STD 883C method 3015	V_{ESD}	750 V

Note: Stressed above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified conditions may affect device reliability or cause malfunction.

3.2 *Operating Conditions*

Parameter	Symbol	Min	Typ	Max	Units
Operating temperature	T_A	-40		+85	°C
Power supply voltage	V_{DD}	2.5		5.5	V

3.3 *Timing characteristics*

(V_{DD} = 5 V ± 5%, T_A = +27 °C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input pins capacitance	Cinp				10	pF
oscillator frequency	Fcarrier	2.5V≤V_{DD}≤5.5V	100	125	150	kHz
Frame duration (Data Rate = 2Kbit/s):	Tread_2K	FOSC=125kHz (Data Rate = 2Kbit/s)		32.76	-	mS
Frame duration (Data Rate = 4Kbit/s):	Tread_4K	FOSC=125kHz (Data Rate = 4Kbit/s)		16.38		mS
Frame duration (Data Rate = 8Kbit/s):	Tread_8K	FOSC=125kHz (Data Rate = 8Kbit/s)		8.19		mS
SCK frequency	F_{SCK}	Ton and Toff ≥100nS	0		5	MHz
RESTART pulse length	$T_{RESTART}$		100			ns

3.4 DC characteristics

(V_{DD} = 4 V ± 5%, T_A = +27 °C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
stand-by current	I_{SB}	ON = GND			100	µA
power consumption	ICC				4	mA
output leakage current	I_{LO}	Vout=V_{DD} or GND			10	µA
input low voltage	V_{IL}	digital inputs	- 0.3		0.4*V_{DD}	V
input high voltage	V_{IH}	digital inputs	0.8*V_{DD}		V_{DD}+ 0.3	V
digital output low voltage	V_{OL}	output current=3mA			0.4	V
digital output high voltage	V_{OH}	output current=3mA	2.6			V

3.5 I/O cells

Standard and custom CMOS I/O cells are used in the device.

Parameter	Conditions	Min	Max	Units
Output HIGH voltage **V_{OH}**	$I_{L=}$4mA	0.9*VDD		V
Output LOW voltage **V_{OL}**	$I_{L=}$4mA		0,5	V
HIGH level CMOS Input voltage		0.8*VDD		V
LOW level CMOS Input voltage			0.4	V
Standard Pull-up resistor		50	100	[kΩ]
Standard Pull-down resistor		50	100	[kΩ]
Custom Pull-up		370	3200	[kΩ]
Custom Pull-down		270	4000	[kΩ]

4 Application notes

4.1 *Low-power application*

Requirements :
Tuning the system: The self-oscillating property of the system requires stable value for coil and tuning capacitor. A ceramic capacitor NPO type or a polyethylene type is recommended

Detection diode: To sustain the voltage on coil a 100 V detection diode is needed. 2 diodes BAV99 in series are recommended.

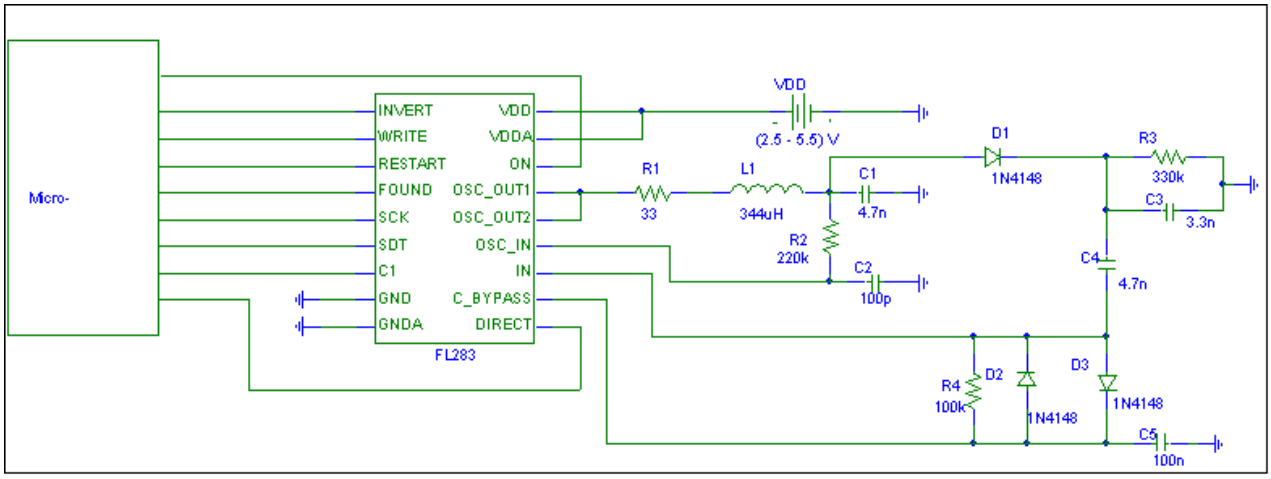
Other capacitors: Ceramic types are suitable

Decoupling supply: 100nF decoupling supply capacitor is recommended

Interface signals: limitation of clock speed to 5 MHz
100 ns min stable state for all signals

Supply voltage: Depending on application, 3 and 5 V supply is suitable

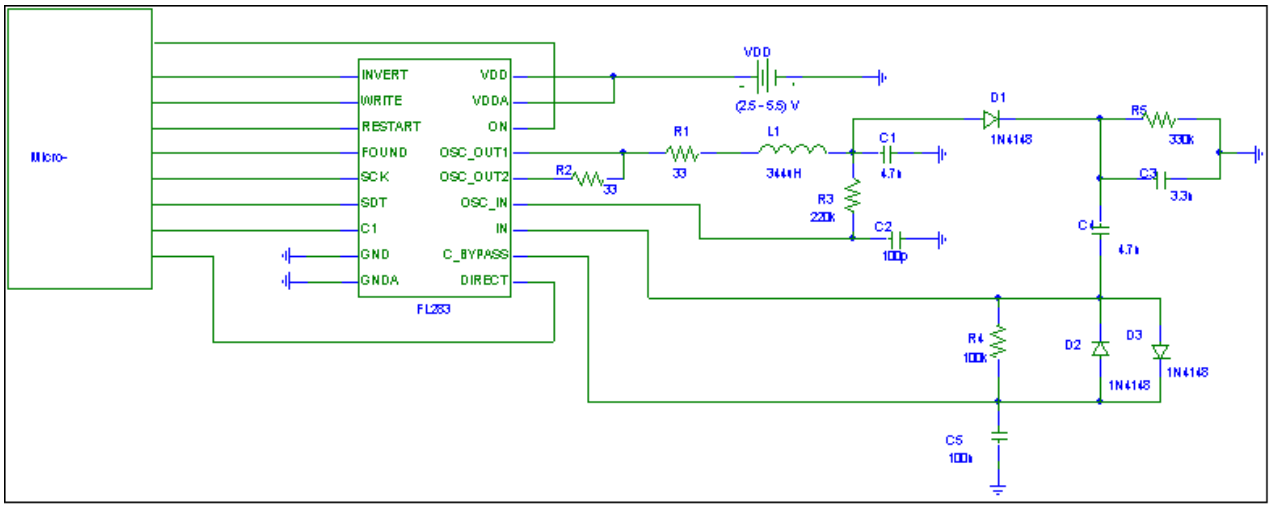
4.1.1 Application Schematics – for 100% Modulation if tag is in read/write mode



RECOMMENDED COMPONENTS

Item	Quantity	Reference	Part	Power	Tolerance	Voltage	Manufac turer
1	1	C1	4.7n		10%	1000V	
2	1	C2	100p		10%	63V	
3	1	C3	3.3n		10%	1000V	
4	1	C4,	4.7n		10%	1000V	
5	1	C5	100n		10%	63V	
6	1	R1	33		10%		
7	1	R2	220K		10%		
8	1	R3	330K		10%		
9	1	R4	100K		10%		
10	3	D1,D2,D3	1N4148				
11	1	L1	344uH		10%		

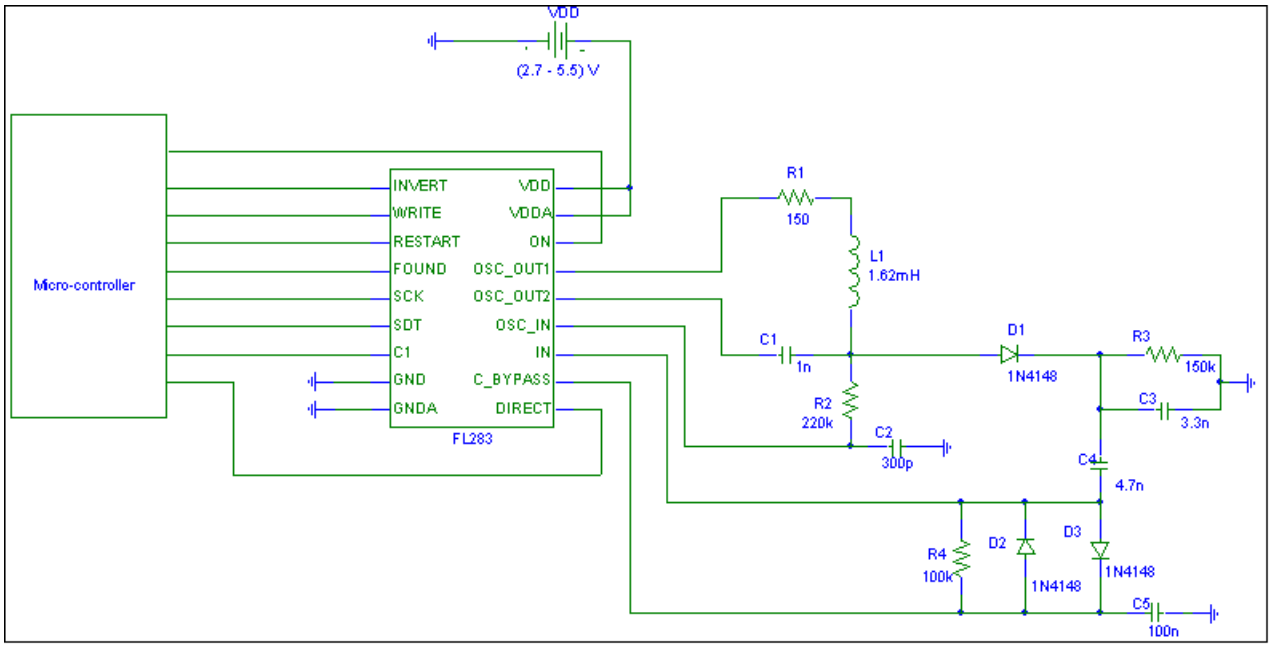
4.1.2 Application Schematics – for 50% Modulation if tag is in read/write mode



RECOMMENDED COMPONENTS

Item	Quantity	Reference	Part	Power	Tolerance	Voltage	Manufacturer
1	1	C1	4.7n		10%	1000V	
2	1	C2	100p		10%	63V	
3	1	C3	3.3n		10%	1000V	
4	1	C4,	4.7n		10%	1000V	
5	1	C5	100n		10%	63V	
6	2	R1, R2	33		10%		
7	1	R4	100K		10%		
8	1	R5	330K		10%		
9	3	D1,D2,D3	1N4148				
10	1	L1	344uH		10%		

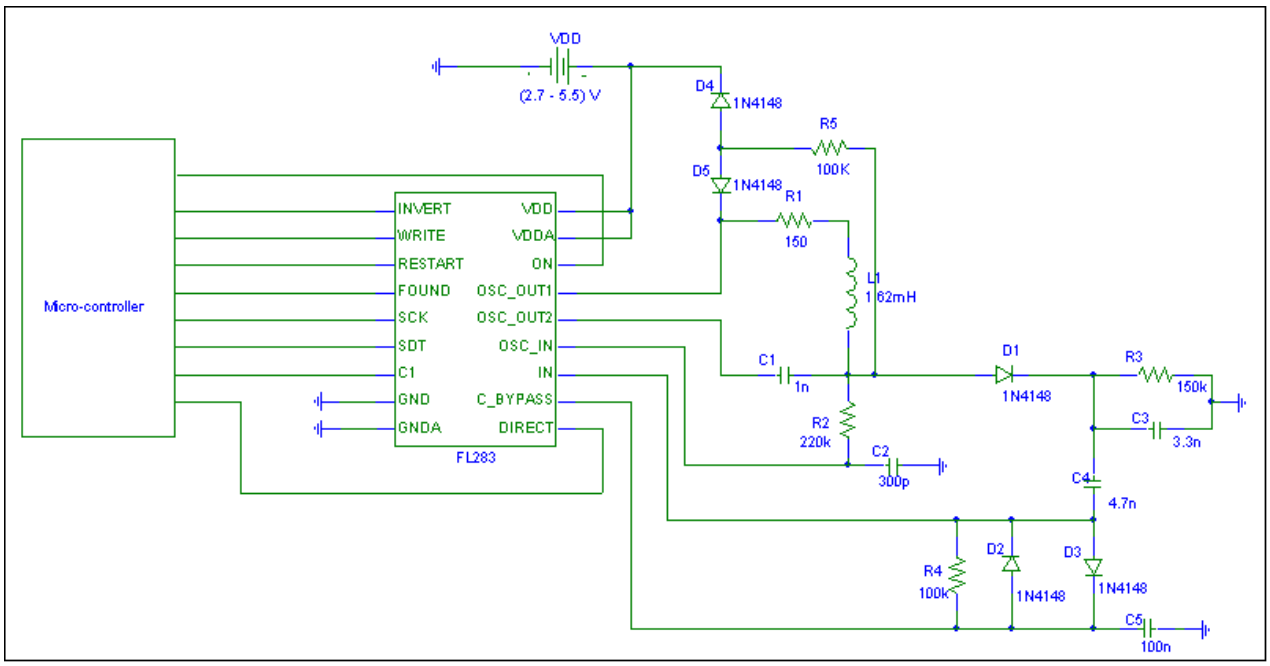
4.1.3 Application schematics for read only tags



RECOMMENDED COMPONENTS

Item	Quantity	Reference	Part	Power	Tolerance	Voltage	Manufacturer
1	1	C1	1n		10%	1000V	
2	1	C2	300p		10%	63V	
3	1	C3	3.3n		10%	1000V	
4	1	C4	4.7n		10%	1000V	
5	1	C5	100n		10%		
6	1	R1	150		10%		
7	1	R2	220k		10%		
8	1	R3	150K		10%		
9	1	R4	100K		10%		
10	3	D1,D2,D3	1N4148				
11	1	L1	1.62mH		10%		

4.1.4 Application schematics for 100% Modulation if tag is in read/write mode



RECOMMENDED COMPONENTS

Item	Quantity	Reference	Part	Power	Tolerance	Voltage	Manufacturer
1	1	C1	1n		10%	1000V	
2	1	C2	300p		10%	63V	
3	1	C3	3.3n		10%	1000V	
4	1	C4	4.7n		10%	1000V	
5	1	C5	100n		10%		
6	1	R1	150		10%		
7	1	R2	220k		10%		
8	1	R3	150K		10%		
9	2	R4,R5	100K		10%		
10	5	D1÷D5	1N4148				
11	1	L1	1.62mH		10%		

4.2 High Power application

- **Power devices:**

High current/low voltage (10A/30V) devices are needed. BUS11 or equivalent are suitable. Due the dissipation of these devices (approximately 1 W per device) a heat sink may be required if the reader is working in permanent mode.

- **Transformer**

Build in RM ferrite core; each winding is identical (8 turns for each of two primary windings and for the secondary winding.)

- **Tuning of the system:**

Stable values for coil and tuning capacitor are required, especially due to the high Q of such an application
A low losses polypropylene type capacitor (2000 V) is recommended for C1 to avoid drift generated by high currents in the capacitor

- **Detection diode:**

To sustain the voltage on coil, a 2000 V, high-speed detection diode is needed. 3 diodes BA159 in series are recommended.

- **Other capacitors:**

The 2 capacitors of the RC network (C3 and C4) are 1000V types (polyethylene)
Electrolytic types are suitable in other places

- **Decoupling supply:**

A 4.7uF decoupling capacitor is recommended

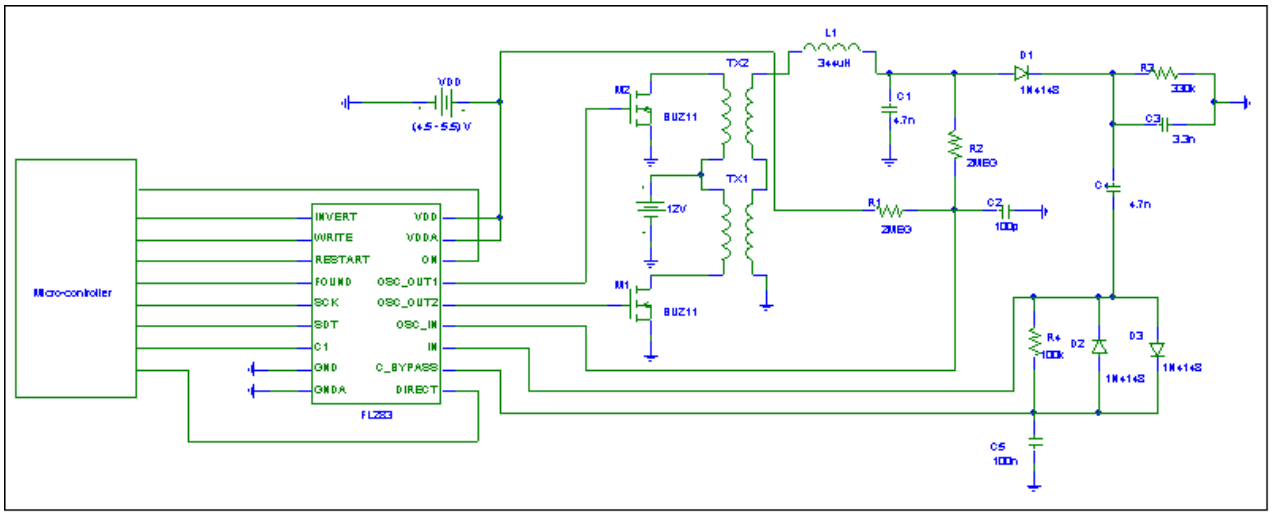
- **Interface signals:**

Limitation of clock speed to 5 MHz 100ns min. stable state for all signals

- **Supply voltage:**

5V supply is suitable for IM283A and 12V for the power devices

4.2.1 Application schematics for 100% Modulation if tag is in read/write mode



RECOMMENDED COMPONENTS

Item	Quantity	Reference	Part	Power	Tolerance	Voltage	Manufacturer
1	1	C1	4.7n		10%	1000V	
2	1	C2	100p		10%	63V	
3	1	C3	3.3n		10%		
4	1	C4	4.7n		10%		
5	1	C5	100n		10%		
6	2	R1,R2	2MEG	0.25W	10%		
7	1	R3	330K		10%		
8	1	R4	100K		10%		
9	3	D1, D2,D3	1N4148				
10	1	L1	344uH		10%		
11	2	M1, M2	BUZ11				
12	1	T1	RM5-N48/250, 3 x 8 turns ø 0.74 coated wire				Siemens, Matsushita Components

5 Notes

The information in this data sheet is believed to be accurate and reliable. ID MOS reserves the right to make changes without prior notice to any specifications of this product. This device is not intended to be used for systems that support or sustain life or for systems where failure may cause personal injury. The customers use this product at their own risk.