EVB-LAN7430 Evaluation Board User's Guide

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN7430 Evaluation Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the EVB-LAN7430 Evaluation Board as a high-performance and low-cost USB/Ethernet connectivity solution.

The manual layout is as follows:

- **Chapter 1. "Overview"** – Shows a brief description of the EVB-LAN7430 Evaluation Board.
- **Chapter 2. "Board Details and Configuration"** – Includes information about the EVB-LAN7430 Evaluation Board.
- **Chapter 3. "Using the EVB-LAN7430"** – Includes information on how to use the EVB-LAN7430 Evaluation Board.
- **Appendix A. "EVB-LAN7430 Evaluation Board"** – This appendix shows the EVB-LAN7430 Evaluation Board schematic.
- **Appendix B. "Schematics"** – This appendix shows the EVB-LAN7430 Evaluation Board schematic.
- **Appendix C. "Bill of Materials"** – This appendix includes the EVB-LAN7430 Evaluation Board Bill of Materials (BOM).

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50002841B (07-23-20)	Figure 2-1	Updated the figure.
	Table 2-1 and Table 2-2	Updated the tables.
	Section 2.1.4.3 "Available GPIO and LEDs While Using EEPROM and IEEE 1588 V2"	Added this section.
	Section 2.1.4.4 "DNP Parts"	Added this section.
	Figure A-1	Updated the figure.
	Figure B-1	Updated the schematics diagram.
	Table C-1	Updated the Bill of Materials table.
DS50002841A (01-18-19)	Initial release	

Chapter 1. Overview

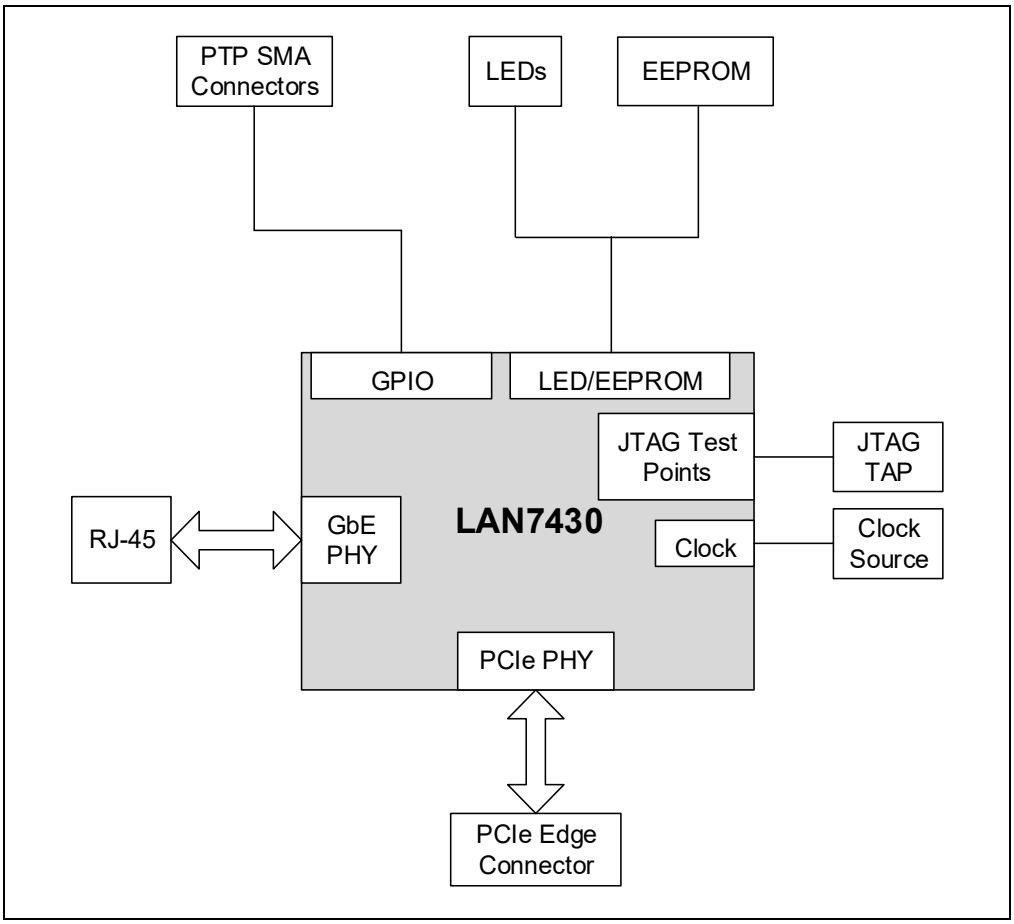
1.1 INTRODUCTION

The EVB-LAN7430 Evaluation Board features LAN7430, PCIe to Gigabit Ethernet bridge device. LAN7430 has an integrated 10/100/1000 Mbps Ethernet PHY, PCIe PHY, Gigabit Ethernet MAC, OTP memory, EEPROM controller, clock/reset/power management functions, PCIe endpoint controller, DMA controller and JTAG TAP. The device supports IEEE 802.3az Energy Efficient Ethernet (EEE), IEEE 1588-2008, and advanced power management features, which makes this device highly suitable across many application areas. This evaluation board requires a single lane PCIe slot.

The scope of this document is to describe the EVB-LAN7430 evaluation board setup and the corresponding jumper configuration.

A simplified block diagram of the board is shown in Figure 1-1.

FIGURE 1-1: EVB-LAN7430 BLOCK DIAGRAM



1.2 REFERENCES

Concepts and material available in the following documents will be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *LAN7430 Data Sheet*
- *EVB-LAN7430 Schematic*
- *Application Note: Implementing IEEE 1588-2008 with LAN7430*

1.3 TERMS AND ABBREVIATIONS

- EEE - Energy Efficient Ethernet
- EVB - Evaluation Board
- GND - Ground
- PHY - Physical Transceiver
- PTP - Point to Point
- SMA Connector - Sub-Miniature version A Connector

Chapter 2. Board Details and Configuration

2.1 BOARD DETAILS

This section includes the following EVB-LAN7430 board details:

- Power
- Resets
- Clock
- Configuration

2.1.1 Power

The board receives 3.3V supply through the PCIe interface. An internal 2.5V voltage regulator supplies power to the 2.5V tolerant supply pins such as the AVDDH_1/ AVDDH_2 and VPH pins, and the VDD12_SW_OUT pin supplies 1.2V to three VDD12CORE pins and VP and VPTX pins. An on-board power scheme can supply 3.3V to LAN7430 and other devices through the auxiliary pin of the PCIe interface.

2.1.2 Resets

Jumper J2 is required to be populated if the reset function is required for the board.

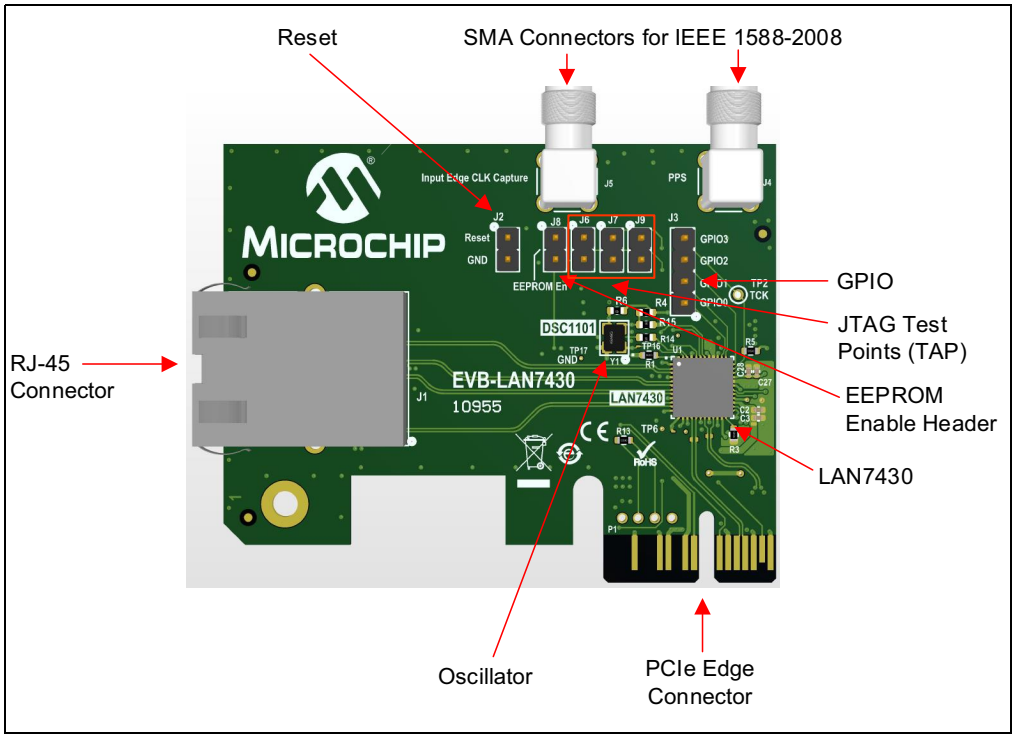
2.1.3 Clock

The evaluation board utilizes an external 25 MHz crystal oscillator.

2.1.4 Configuration

Figure 2-1 describes the board features and configuration settings.

FIGURE 2-1: EVB-LAN7430 TOP VIEW WITH CALLOUTS



2.1.4.1 JUMPER SETTINGS

Table 2-1 describes the jumper settings. The default configuration is shown in bold.

TABLE 2-1: JUMPERS

Jumper	Label	Description	Open	Close
J2	Reset	Provides the Hard-ware reset to the board	**(Default)** Board per-forms normal opera-tion.	Resets the board
J8	EEPROM EN	Enables optional EEPROM	EEPROM is dis-abled. Internal OTP is used to configure LAN7430.	**(Default)** EEPROM is enabled.
J6, J7, J9	EEPROM Connections	Enables EEPROM connections	Allows JTAG Testing	**(Default)** EEPROM is enabled.

2.1.4.2 HEADERS AND CONNECTORS

Table 2-2 describes the functions of the headers on the board.

TABLE 2-2: HEADERS AND CONNECTORS

Header	Label	Description
J1	8P8C (RJ-45) connector	Connects an Ethernet cable
J3	GPIO1, GPIO2, GPIO 3, GPIO4	General purpose input/output (I/O)
J4	PPS	IEEE 1588 Pulse Per Second (PPS) input
J5	Input Edge Clock Capture	IEEE 1588 Input Edge Clock Capture

2.1.4.3 AVAILABLE GPIO AND LEDS WHILE USING EEPROM AND IEEE 1588 V2

Table 2-3 shows the available GPIOs and LEDs while using the EEPROM and IEEE 1588 v2.

TABLE 2-3: AVAILABLE GPIO AND LED WHEN EEPROM AND IEEE 1588 ARE USED

Use Cases		Available GPIO/LED			
EEPROM	**PTP/IEEE 1588 V2**	**GPIO0/LED0**	**GPIO1/LED1**	**GPIO2/LED2**	**GPIO3/LED3**
Yes	No	Yes	Yes	No	Yes
Yes	Yes	No	Yes	Yes	Yes
No	Yes	Yes	Yes	Yes	Yes

Note 1: Since a GPIO will toggle either Chip Select (CS) or the clock signal on the EEPROM, one of the GPIOs will not be available while using the EEPROM.

2.1.4.4 DNP PARTS

Table 2-4 describes the components that are not populated on the board.

TABLE 2-4: DNP PARTS

Components	Description
J2	Reset
J4, J5	IEEE 1588 Testing - SMA Connectors
R18, R19, C1, C21	J4 Connector Supporting Components
R16, R17, C29, C39	J5 Connector Supporting Components

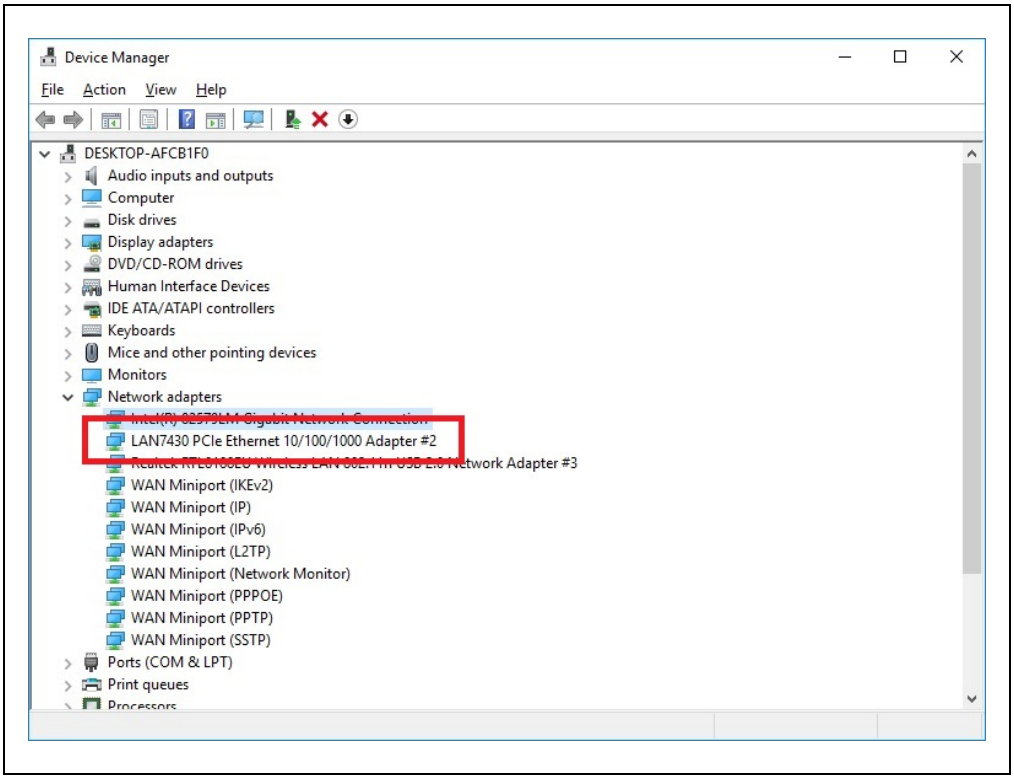
NOTES:

Chapter 3. Using the EVB-LAN7430

The EVB-LAN7430 board is connected to a PCIe slot of a PC. The LAN7430 device supports Windows 10 and Linux operating system. The drivers are provided on the LAN7430 device's product page for both operating systems. A 'readme' file is also provided with the drivers, which describes the driver installation process in detail.

Once the drivers are installed correctly for Windows 10, for example, the board can be detected in Device Manager as shown in Figure 3-1.

FIGURE 3-1: LAN7430 DETECTED IN DEVICE MANAGER



Once the PC detects the LAN7430 board correctly, the PC can then be connected to the Internet using an Ethernet cable to test the board.

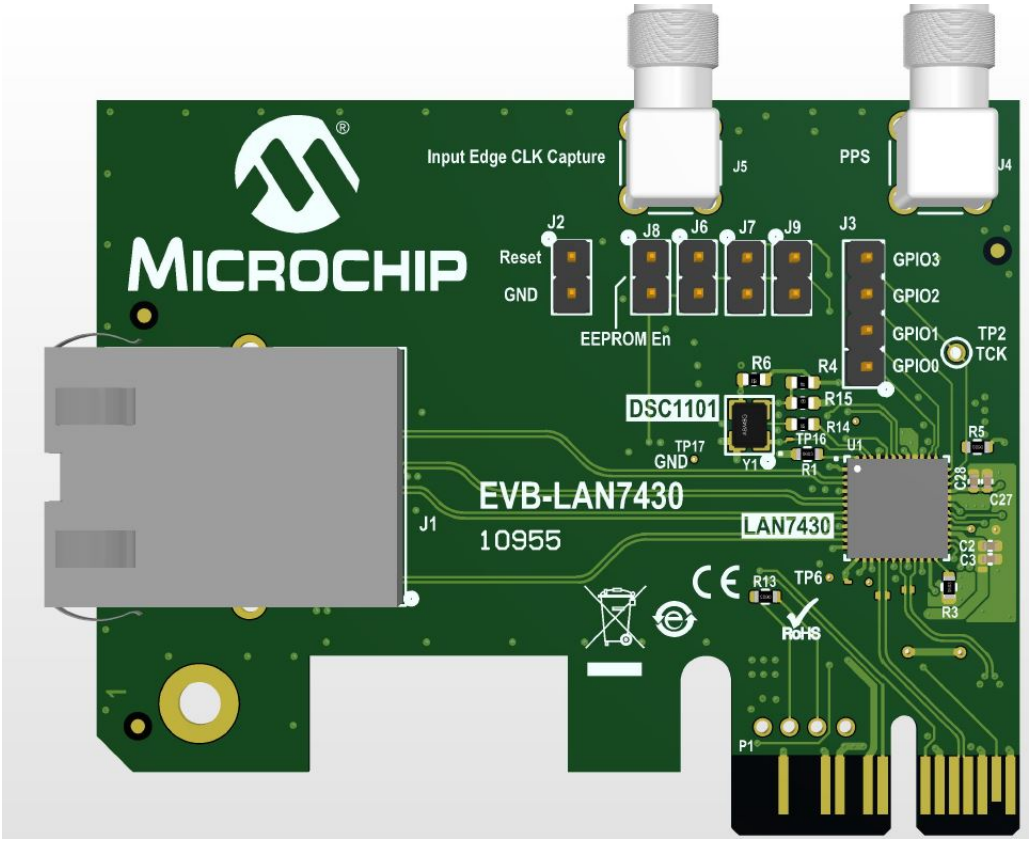
NOTES:

Appendix A. EVB-LAN7430 Evaluation Board

A.1 INTRODUCTION

This appendix shows the EVB-LAN7430 Evaluation Board.

FIGURE A-1: EVB-LAN7430 EVALUATION BOARD



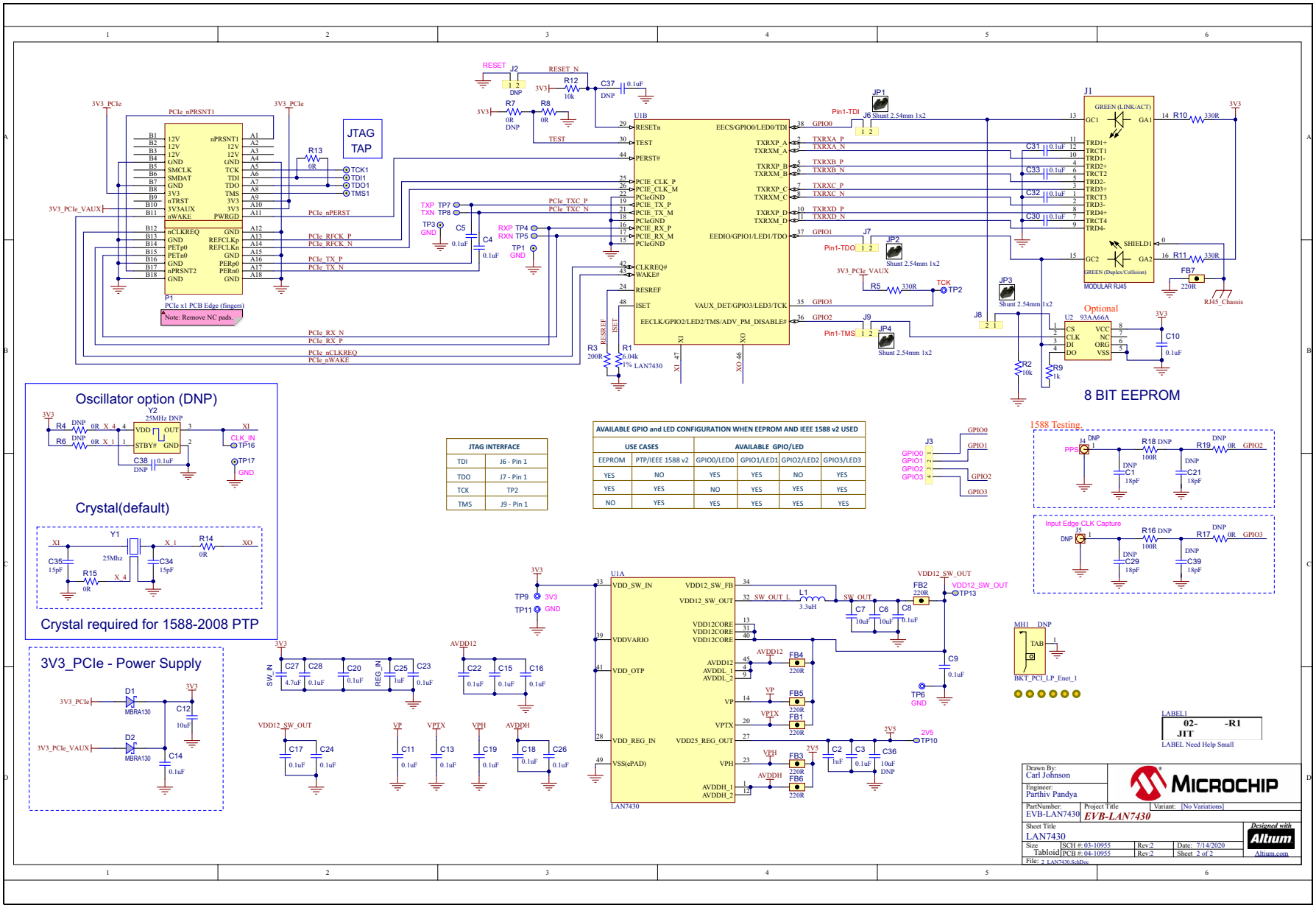
NOTES:

Appendix B. Schematics

B.1 INTRODUCTION

This appendix shows the EVB-LAN7430 Evaluation Board schematics.

FIGURE B-1: EVB-LAN7430 EVALUATION BOARD SCHEMATICS



Appendix C. Bill of Materials

C.1 INTRODUCTION

This appendix includes the EVB-LAN7430 Bill of Materials (BOM).

TABLE C-1: EVB-LAN7430 BILL OF MATERIALS

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
1	2	C2, C25	CAP CER 1uF 35V 10% X5R SMD 0402	Yes	Murata Electronics North America	GRM155R6YA105KE11D
2	24	C3, C4, C5, C8, C9, C10, C11, C13, C14, C15, C16, C17, C18, C19, C20, C22, C23, C24, C26, C28, C30, C31, C32, C33	CAP CER 0.1uF 50V 10% X7R SMD 0402	Yes	TDK Corporation	C1005X7R1H104K050BB
3	3	C6, C7, C12	CAP CER 10UF 25V 20% X5R SMD 0603	Yes	Murata Electronics North America	GRM188R61E106MA73D
4	1	C27	CAP CER 4.7uF 6.3V 20% X5R SMD 0402	Yes	Murata	GRM155R60J475ME47D
5	2	C34, C35	CAP CER 15pF 50V 5% NP0 SMD 0402	Yes	Murata	GRM1555C1H150JA01D
6	2	D1, D2	DIO SCTKY MBRA130LT3G 410mV 1A 30V SMD DO-214AC SMA	Yes	ON Semiconductor	MBRA130LT3G
7	7	FB1, FB2, FB3, FB4, FB5, FB6, FB7	FERRITE 500mA 220R SMD 0603	Yes	Murata	BLM18AG221SN1D
8	1	J1	CON MODULAR JACK RJ45 10/100/1000 MAGNETICS 2xLEDs SHIELD TH R/A	Yes	Amphenol Commercial Products	RJMG2012211A0FR
9	1	J3	CON HDR-2.54 Male 1x4 Gold 5.84MH TH VERT	Yes	Wurth Electronics Inc	61300411121
10	4	J6, J7, J8, J9	CON HDR-2.54 Male 1x2 Gold 5.84MH TH VERT	Yes	FCI	77311-118-02LF
11	1	L1	INDUCTOR 3.3uH 2.63A 20% SMD L3W3H1.2	Yes	TDK Corporation	VLS3012HBX-3R3M
12	1	MH1	Bracket, BKT_PCI_LP_Enet_1, GLOBE	Yes	Keystone	
13	1	R1	RES TKF 6.04k 1% 1/10W SMD 0603	Yes	Yageo	9T06031A6041FBHFT
14	2	R2, R12	RES TKF 10k 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF1002V
15	1	R3	RES TKF 200R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF2000V
16	3	R5, R10, R11	RES TKF 330R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF3300V
17	4	R8, R13, R14, R15	RES TKF 0R 1/10W SMD 0603	Yes	Panasonic	ERJ-3GSY0R00V
18	1	R9	RES TKF 1k 5% 1/10W SMD 0603	Yes	Panasonic	ERJ-3GEYJ102V
19	1	Y1	CRYSTAL 25MHz 10pF SMD ABM8G	Yes	Abracon LLC	ABM8G-25.000MHZ-4Y-T3
20	1	U1	MCHP INTERFACE PCIe-GIGe ETHERNET LAN7430 SQFN-48	Yes	Microchip Technology	LAN7430/YXX
21	1	U2	MCHP MEMORY SERIAL EEPROM 4k Microwire 93AA66A-I/SN SOIC-8	Yes	Microchip	93AA66A-I/SN
22	4	C1, C21, C29, C39	CAP CER 18pF 50V 5% NP0 SMD 0805	NO	Cal-Chip	GMC21CG180J50NTLF
23	1	C36	CAP CER 10UF 25V 20% X5R SMD 0603	NO	Murata Electronics North America	GRM188R61E106MA73D
24	2	C37, C38	CAP CER 0.1uF 50V 10% X7R SMD 0402	NO	TDK Corporation	C1005X7R1H104K050BB
25	1	J2	CON HDR-2.54 Male 1x2 Gold 5.84MH TH VERT	NO	FCI	77311-118-02LF

TABLE C-1: EVB-LAN7430 BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
26	2	J4, J5	CON RF Coaxial SMA Female TH R/A	NO	TE Connectivity AMP Connectors	5-1814400-1
27	3	R4, R6, R7	RES TKF 0R 1/10W SMD 0603	NO	Panasonic	ERJ-3GSY0R00V
28	2	R16, R18	RES MF 100R 5% 1/10W SMD 0805	NO	Panasonic Electronic Components	ERA-S39J101V
29	2	R17, R19	RES TKF 0R 1/8W SMD 0805	NO	Panasonic	ERJ-6GEY0R00V
30	4	JP1, JP2, JP3, JP4	Shunt connectors for J6, J7, J8, and J9	Yes	TE Connectivity AMP	880584-4

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