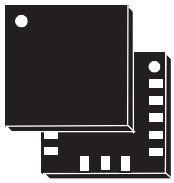
LSM303D

Ultra-compact high-performance eCompass module: 3D accelerometer and 3D magnetometer

Datasheet - production data



LGA-16 (3x3x1 mm)

Features

- 3 magnetic field channels and 3 acceleration channels
- ±2/±4/±8/±12 gauss magnetic full scale
- ±2/±4/±6/±8/±16 *g* linear acceleration full scale
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 2.16 V to 3.6 V
- Power-down mode / low-power mode
- Programmable interrupt generators for free-fall, motion detection and magnetic field detection
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK®, RoHS and “Green” compliant

Applications

- Tilt-compensated compasses
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection
- Click/double-click recognition
- Pedometers
- Intelligent power saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LSM303D is a system-in-package featuring a 3D digital linear acceleration sensor and a 3D digital magnetic sensor.

The LSM303D has linear acceleration full scales of ±2*g* / ±4*g* / ±6*g* / ±8*g* / ±16*g* and a magnetic field full scale of ±2 / ±4 / ±8 / ±12 gauss.

The LSM303D includes an I^2C serial bus interface that supports standard and fast mode (100 kHz and 400 kHz) and SPI serial standard interface.

The system can be configured to generate an interrupt signal for free-fall, motion detection and magnetic field detection. Thresholds and timing of interrupt generators are programmable by the end user.

Magnetic and accelerometer blocks can be enabled or put into power-down mode separately.

The LSM303D is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packaging
LSM303D	-40 to +85	LGA-16	Tray
LSM303DTR	-40 to +85	LGA-16	Tape and reel

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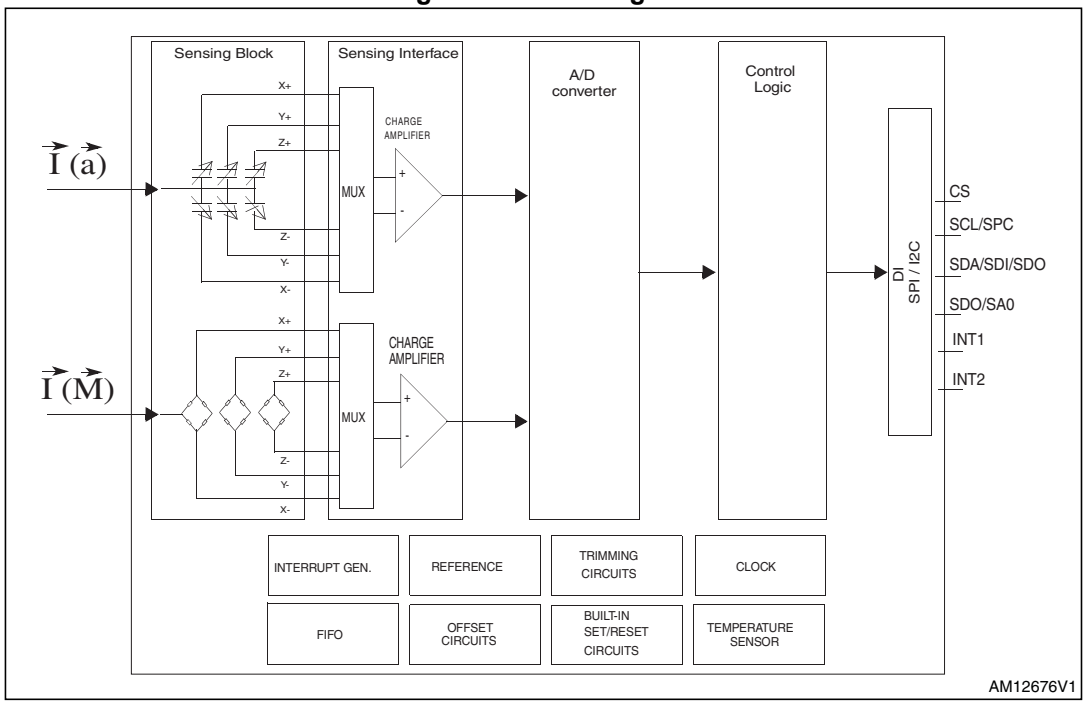
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

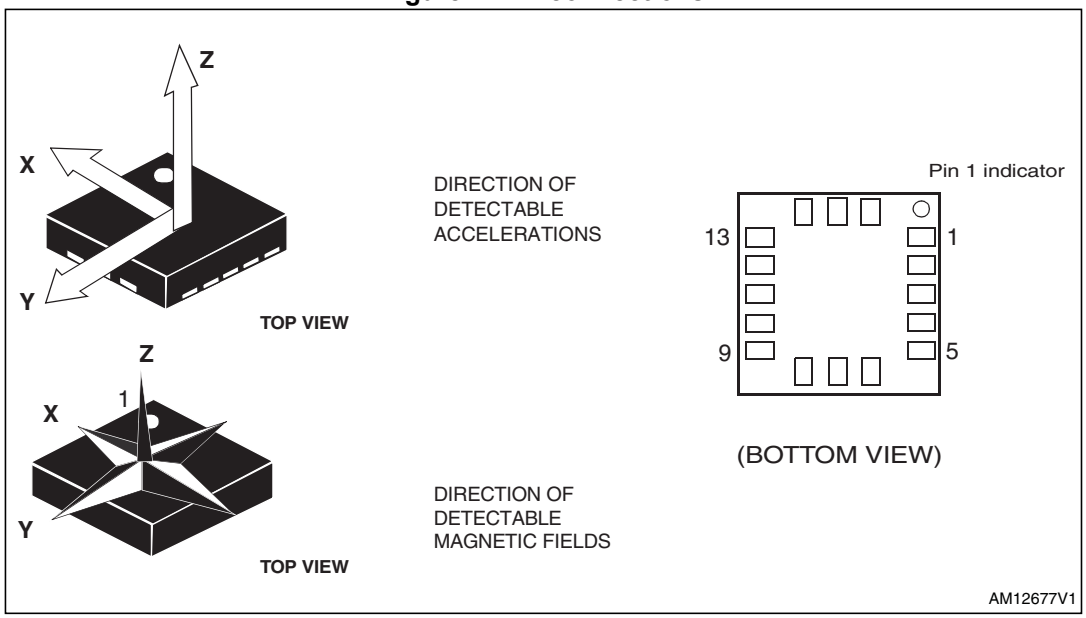


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SETC	S/R capacitor connection (C_2)
3	SETP	S/R capacitor connection (C_2)
4	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
5	GND	0 V supply
6	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
7	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
8	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
9	INT 2	Interrupt 2
10	Reserved	Connect to GND
11	INT 1	Interrupt 1
12	GND	0 V supply
13	GND	0 V supply
14	Vdd	Power supply
15	C1	Capacitor connection (C_1)
16	GND	0 V supply

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted [a].

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_FS	Linear acceleration measurement range(2)			±2		*g*
				±4		
				±6		
				±8		
				±16		
M_FS	Magnetic measurement range			±2		gauss
				±4		
				±8		
				±12		
LA_So	Linear acceleration sensitivity	Linear acceleration FS = ±2 *g*		0.061		mg/LSB
		Linear acceleration FS = ±4 *g*		0.122		
		Linear acceleration FS = ±6 *g*		0.183		
		Linear acceleration FS = ±8 *g*		0.244		
		Linear acceleration FS = ±16 *g*		0.732		
M_So	Magnetic sensitivity	Magnetic FS = ±2 gauss		0.080		mgauss/ LSB
		Magnetic FS = ±4 gauss		0.160		
		Magnetic FS = ±8 gauss		0.320		
		Magnetic FS = ±12 gauss		0.479		
LA_TCSo	Linear acceleration sensitivity change vs. temperature			±0.01		%/°C
M_TCSo	Magnetic sensitivity change vs. temperature			±0.05		%/°C
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy(3),(4)			±60		m*g*
LA_TCOff	Linear acceleration zero-*g* level change vs. temperature	Max delta from 25 °C		±0.5		m*g*/°C
LA_An	Linear acceleration noise density	Linear acceleration FS = 2*g*; ODR = 100 Hz		150		$ug/(\sqrt{Hz})$
M_R	Magnetic noise density	Magnetic FS = 2 gauss; LR setting CTRL5 (M_RES [1,0]) = 00b		5		mgauss/ RMS

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.16 V to 3.6 V.

Table 3. Sensor characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
M_CAS	Magnetic cross-axis sensitivity	Cross field = 0.5 gauss Applied = ±3 gauss		±1		%FS/ gauss
M_EF	Maximum exposed field	No permanent effect on sensor performance			10000	gauss
M_DF	Magnetic disturbance field	Sensitivity starts to degrade. Automatic S/R pulse restores the sensitivity(5)			20	gauss
LA_ST	Linear acceleration self-test positive difference(6)	±2 *g* range, X-, Y-axis AST = 1 see *Table 37*	70		1700	mg
		±2 *g* range, Z-axis AST = 1 see *Table 37*	70		1700	
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.
5. Set/reset pulse is automatically applied at each conversion cycle.
6. “Self-test output change” is defined as: $OUTPUT[mg]_{(CTRL2\ AST\ bit\ =1)}$ - $OUTPUT[mg]_{(CTRL2\ AST\ bit\ =0)}$.

2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted(b).

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		8		LSB/°C
TODR	Temperature refresh rate			M_ODR [2:0](2)		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Refer to *Table 47: Magnetic data rate configuration*.

b. The product is factory calibrated at 2.5 V.

2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.16		3.6	V
Vdd_IO	Module power supply for I/O		1.71	1.8	Vdd+0.1	
Idd	eCompass(2) current consumption in normal mode(3)	LR setting CTRL5 (M_RES [1,0]) = 00b, see *Table 45*		300		µA
IddSL	Current consumption in power-down mode(4)			1		µA
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. eCompass: accelerometer and magnetic sensor.
3. Magnetic sensor setting ODR = 6.25 Hz, accelerometer sensor ODR = 50 Hz and magnetic high-resolution setting.
4. Linear accelerometer and magnetic sensor in power-down mode.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

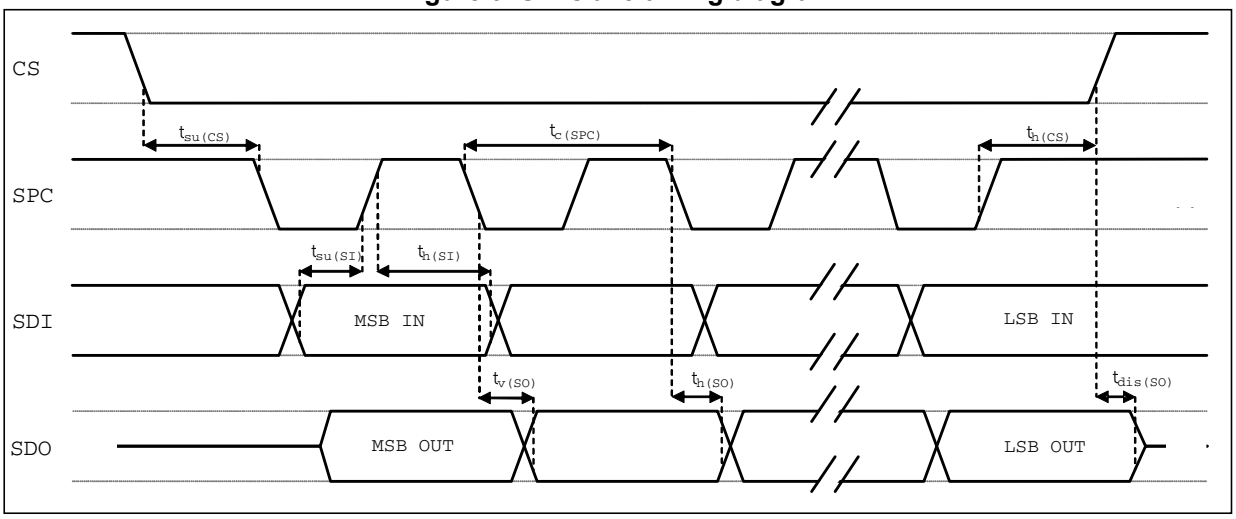
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min.	Max.	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO for both input and output ports.

2.4.2 Sensor I²C - inter-IC control interface

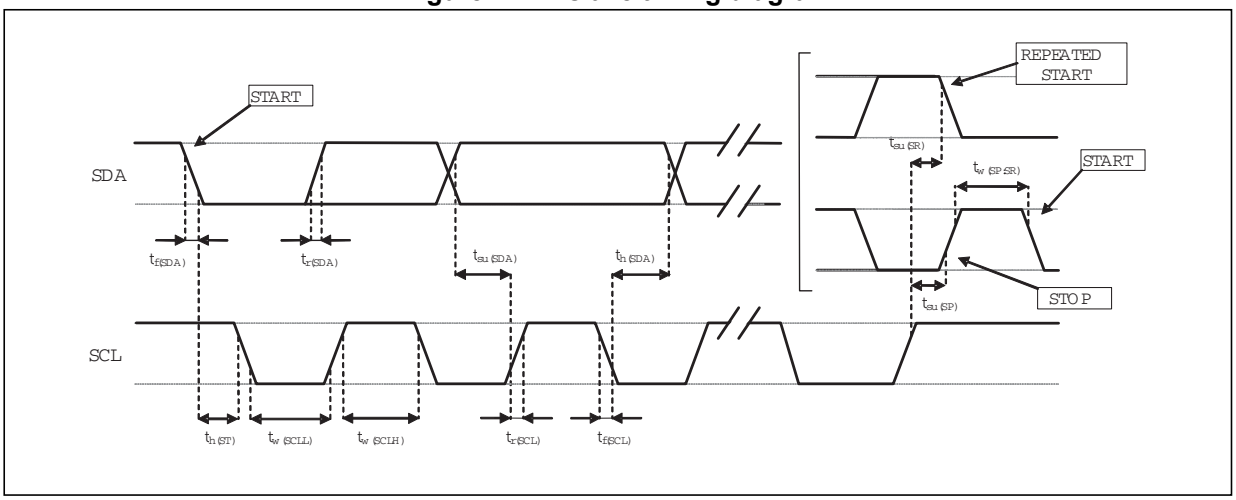
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20 + 0.1C_b (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20 + 0.1C_b (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.
2. C_b = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL/SPC, SDA/SDI/SDO, SDO/SA0, CS)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology

3.1 Set/reset pulse

The set/reset pulse is an automatic operation performed before each magnetic acquisition cycle to recover the initial magnetization state of the sensor and therefore the linearity of the sensor itself.

3.2 Sensitivity

3.2.1 Linear acceleration sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.2.2 Magnetic sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying a magnetic field of 1 *gauss* to it.

3.3 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* on the X-axis and 0 *g* on the Y-axis, whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is, to some extent, a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

3.4 Zero-*gauss* level

Zero-*g*auss level offset describes the deviation of an actual output signal from the ideal output if no magnetic field is present. Thanks to the set/reset pulse and to the magnetic sensor read-out chain, the offset is dynamically cancelled. The Zero-*g*auss level does not show any dependencies on temperature and power supply.

4 Functionality

4.1 Self-test

The self-test allows checking the linear acceleration sensor functionality without moving the sensor. The self-test function is off when the self-test bit (AST) is programmed to '0'. When the self-test bit is programmed to '1', an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Section 2.1*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

4.2 Temperature sensor

The LSM303D features an internal temperature sensor. Temperature data can be enabled by setting the TEMP_EN bit on the *CTRL5 (24h)* register to 1.

Both the TEMP_OUT_H and TEMP_OUT_L registers must be read.

Temperature data is stored inside *TEMP_OUT_L (05h), TEMP_OUT_H (06h)* as two's complement data in 12-bit format, right-justified.

The output data rate of the temperature sensor is set by M_ODR [2:0] in *CTRL5 (24h)* and is equal to the magnetic sensor output data rate.

4.3 FIFO

The LSM303D embeds an acceleration data FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, as the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits. Programmable threshold level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT 1 or INT 2 pin.

Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in *Figure 5*, for each channel only the first address is used. The remaining FIFO slots are empty.

FIFO mode

In FIFO mode, data from X, Y and Z channels are stored in the FIFO. A FIFO threshold interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it is full. When full, the FIFO stops collecting data from the input channels.

Stream mode

In Stream mode, data from X, Y and Z measurements are stored in the FIFO. A FIFO threshold interrupt can be enabled and set as in FIFO mode.The FIFO continues filling until it's full. When full, the FIFO discards the older data as the new arrive.

Stream-to-FIFO mode

In Stream-to-FIFO mode, data from X, Y and Z measurements are stored in the FIFO. A FIFO threshold interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it's full. When full, the FIFO discards the older data as the new arrive. Once a trigger event occurs, the FIFO starts operating in FIFO mode.

Bypass-to-Stream mode

In Bypass-to-Stream mode, the FIFO starts operating in Bypass mode and once a trigger event occurs (related to *IG_CFG1 (30h)* register events), the FIFO starts operating in Stream mode.

Retrieving data from FIFO

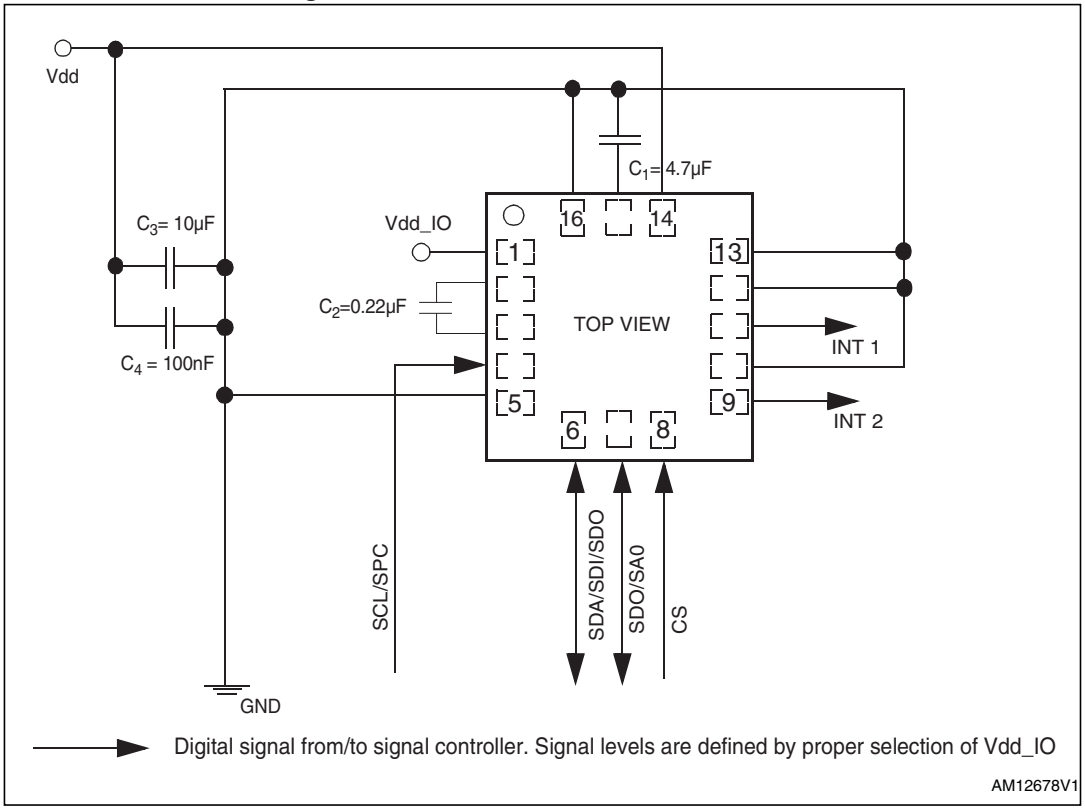
FIFO data is read from the OUT_X_A, OUT_Y_A and OUT_Z_A registers. When the FIFO is in Stream, Stream-to-FIFO, Bypass-to-Stream or FIFO mode, a read operation to the OUT_X_A, OUT_Y_A or OUT_Z_A registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the OUT_X_A, OUT_Y_A and OUT_Z_A registers and both single read and read_burst operations can be used.

4.4 Factory calibration

The IC interface is factory calibrated. The trim values are stored inside the device in nonvolatile memory. Anytime the device is turned on, the trimming parameters are downloaded into the registers to be used during normal operation. This allows the user to use the device without further calibration.

5 Application hints

Figure 5. LSM303D electrical connections



5.1 External capacitors

The C_1 and C_2 external capacitors should be low SR value ceramic type construction (typ. recommended value 200 mΩ). Reservoir capacitor C_1 is nominally 4.7 µF in capacitance, with the set/reset capacitor C_2 nominally 0.22 µF in capacitance.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C_4 = 100 nF ceramic, C_3 = 10 µF Al) should be placed as near as possible to the supply pin of the device (common design practice). All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*).

The functionality of the device and the measured acceleration/magnetic field data is selectable and accessible through the I^2C/SPI interfaces.

The functions, the threshold and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the I^2C/SPI interfaces.

5.2 Pull-up resistors

If an I^2C interface is used, pull-up resistors (recommended value 10 kΩ) must be placed on the two I^2C bus lines.

5.3 Digital Interface power supply

This digital interface, dedicated to the linear acceleration and to the magnetic field signal, is capable of operating with a standard power supply (Vdd) or using a dedicated power supply (Vdd_IO).

5.4 Soldering information

The LGA package is compliant with ECOPACK®, RoHS and “Green” standards.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

5.5 High-current wiring effects

High current in wiring and printed circuit traces can be the cause of errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields add to the Earth’s magnetic field creating errors in compass heading computations.

Keep currents higher than 10 mA a few millimeters further away from the sensor IC.

6 Digital interfaces

The registers embedded in the LSM303D may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL/SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO/SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)

6.1 I^2C serial interface

The LSM303D I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 10. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the START condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a START condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LSM303D is 00111xxb, whereas the xx bits are modified by the SDO/SA0 pin in order to modify the device address. If the SDO/SA0 pin is connected to the voltage supply, the address is 0011101b, otherwise, if the SDO/SA0 pin is connected to ground, the address is 0011110b. This solution permits the connection and addressing of two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LSM303D behaves as a slave device and the following protocol must be adhered to. After the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto-increment. If the MSb of the SUB field is 1, the SUB (register address) is automatically incremented to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is ‘1’ (read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (write) the master transmits to the slave with direction unchanged. *Table 11* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 11. SAD+read/write patterns

Command	SDO/SA0 pin	SAD[6:2]	SAD[1:0]	R/W	SAD+R/W
Read	0	00111	10	1	3D
Write	0	00111	10	0	3C
Read	1	00111	01	1	3B
Write	1	00111	01	0	3A

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data is transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes sent per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to ‘1’ while SUB(6-0) represents the address of the first register to be read.

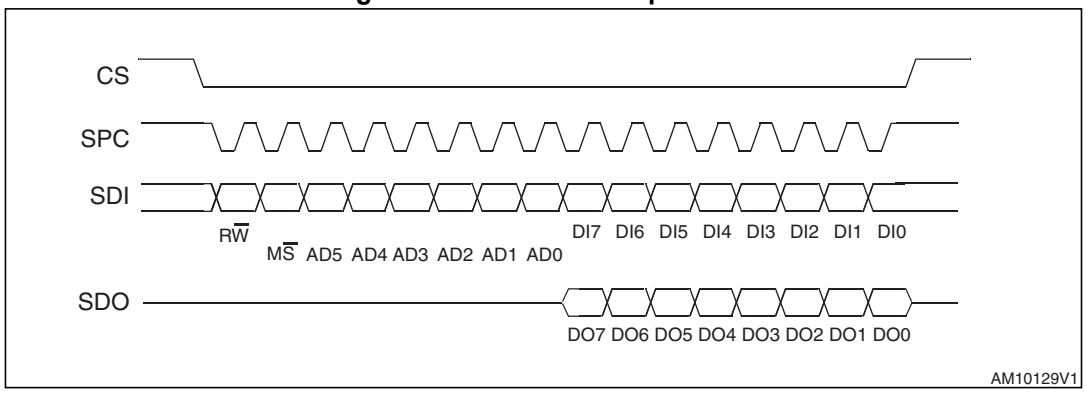
In the communication format presented, MAK is master acknowledge and NMAK is no master acknowledge.

6.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read and write protocol



CS is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

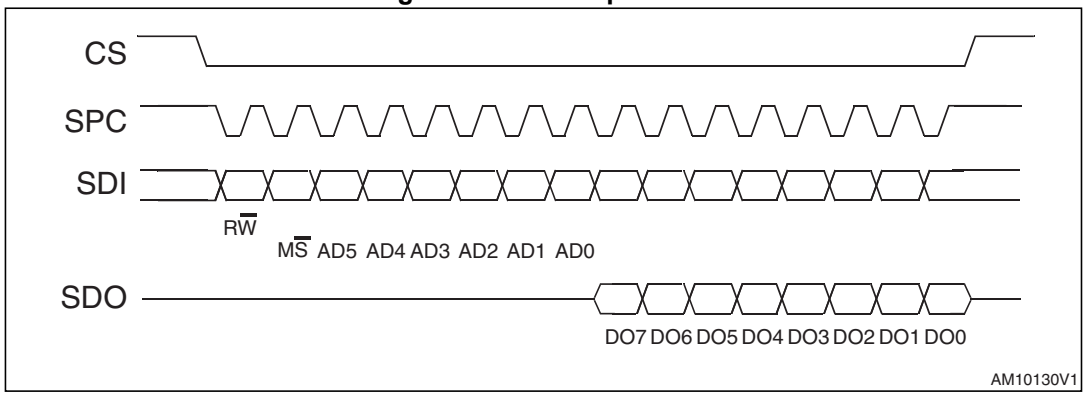
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 7. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

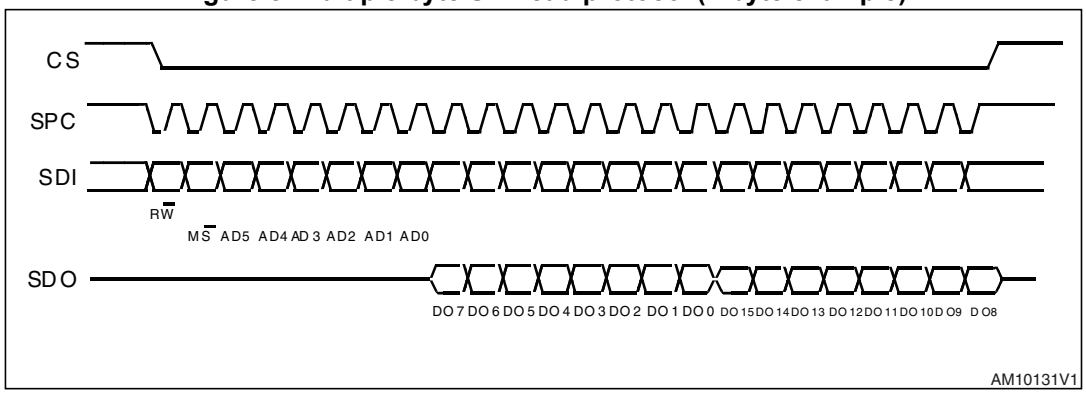
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

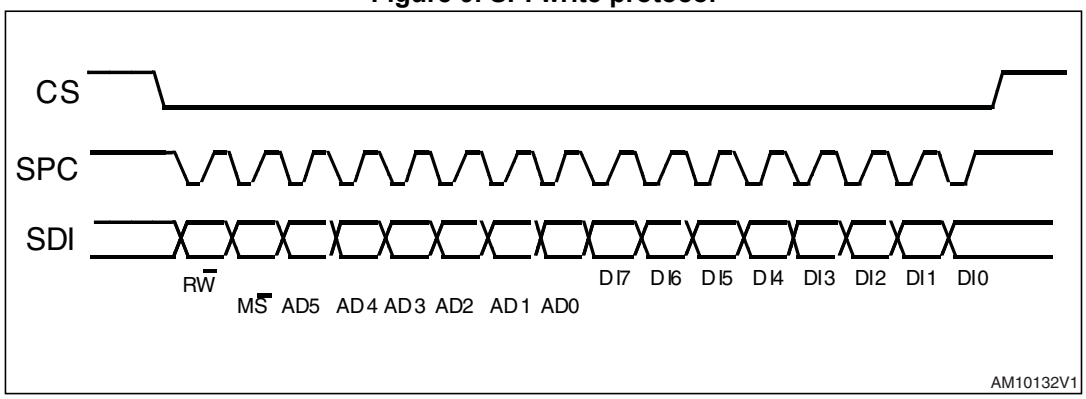
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 8. Multiple byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 9. SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

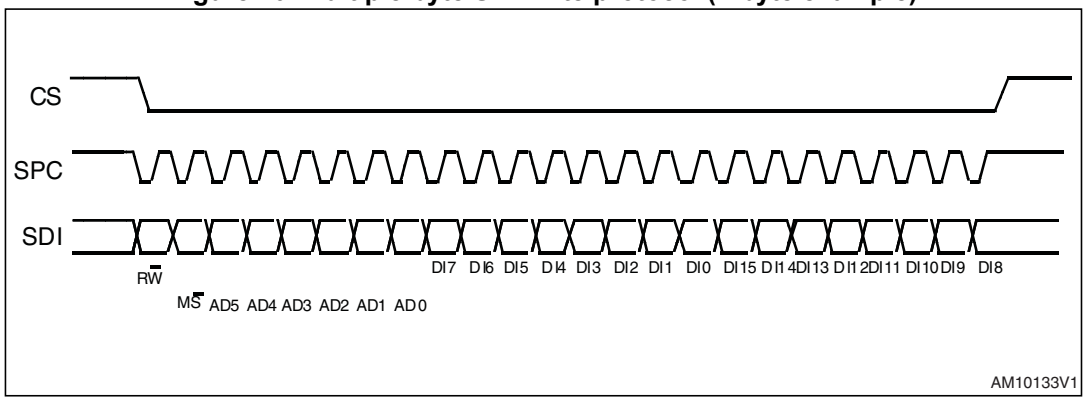
bit 1: MS bit. When 0, do not increment address; when 1, increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

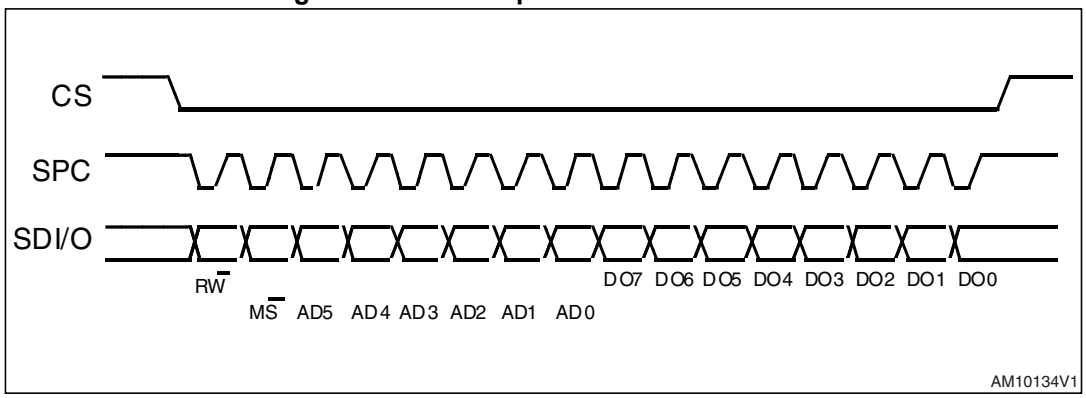
Figure 10. Multiple byte SPI write protocol (2-byte example)



6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the bit SIM (SPI serial interface mode selection) to ‘1’ in *CTRL2 (21h)*.

Figure 11. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

7 Output register mapping

The table below provides a listing of the 8-bit registers embedded in the device and the corresponding addresses.

Table 16. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved	--	00-04	--	--	Reserved
TEMP_OUT_L	r	05	000 0101	Output	
TEMP_OUT_H	r	06	000 0110	Output	
STATUS_M	r	07	000 0111	Output	
OUT_X_L_M	r	08	000 1000	Output	
OUT_X_H_M	r	09	000 1001	Output	
OUT_Y_L_M	r	0A	000 1010	Output	
OUT_Y_H_M	r	0B	000 1011	Output	
OUT_Z_L_M	r	0C	000 1100	Output	
OUT_Z_H_M	r	0D	000 1101	Output	
Reserved	--	0E	000 1110	--	Reserved
WHO_AM_I	r	0F	000 1111	01001001	
Reserved	--	10-11	--	--	Reserved
INT_CTRL_M	rw	12	001 0010	11101000	
INT_SRC_M	r	13	001 0011	Output	
INT_THS_L_M	rw	14	001 0100	00000000	
INT_THS_H_M	rw	15	001 0101	00000000	
OFFSET_X_L_M	rw	16	001 0110	00000000	
OFFSET_X_H_M	rw	17	001 0111	00000000	
OFFSET_Y_L_M	rw	18	001 01000	00000000	
OFFSET_Y_H_M	rw	19	001 01001	00000000	
OFFSET_Z_L_M	rw	1A	001 01010	00000000	
OFFSET_Z_H_M	rw	1B	001 01011	00000000	
REFERENCE_X	rw	1C	001 01100	00000000	
REFERENCE_Y	rw	1D	001 01101	00000000	
REFERENCE_Z	rw	1E	001 01110	00000000	
CTRL0	rw	1F	001 1111	00000000	
CTRL1	rw	20	010 0000	00000111	
CTRL2	rw	21	010 0001	00000000	

Table 16. Register address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
CTRL3	rw	22	010 0010	00000000	
CTRL4	rw	23	010 0011	00000000	
CTRL5	rw	24	010 0100	00011000	
CTRL6	rw	25	010 0101	00100000	
CTRL7	rw	26	010 0110	00000001	
STATUS_A	r	27	010 0111	Output	
OUT_X_L_A	r	28	010 1000	Output	
OUT_X_H_A	r	29	010 1001	Output	
OUT_Y_L_A	r	2A	010 1010	Output	
OUT_Y_H_A	r	2B	010 1011	Output	
OUT_Z_L_A	r	2C	010 1100	Output	
OUT_Z_H_A	r	2D	010 1101	Output	
FIFO_CTRL	rw	2E	010 1110	00000000	
FIFO_SRC	r	2F	010 1111	Output	
IG_CFG1	rw	30	011 0000	00000000	
IG_SRC1	r	31	011 0001	Output	
IG_THS1	rw	32	011 0010	00000000	
IG_DUR1	rw	33	011 0011	00000000	
IG_CFG2	rw	34	011 0100	00000000	
IG_SRC2	r	35	011 0101	Output	
IG_THS2	rw	36	011 0110	00000000	
IG_DUR2	rw	37	011 0111	00000000	
CLICK_CFG	rw	38	011 1000	00000000	
CLICK_SRC	r	39	011 1001	Output	
CLICK_THS	rw	3A	011 1010	00000000	
TIME_LIMIT	rw	3B	011 1011	00000000	
TIME _LATENCY	rw	3C	011 1100	00000000	
TIME_WINDOW	rw	3D	011 1101	00000000	
ACT_THS	rw	3E	011 1110	00000000	
ACT_DUR	rw	3F	011 1111	00000000	

Registers marked as *Reserved* must not be changed. Writing to these registers may cause permanent damage to the device.The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration and magnetic data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

8.1 TEMP_OUT_L (05h), TEMP_OUT_H (06h)

Temperature sensor data. Temperature data is stored as two's complement data in 12-bit format, right-justified.

Refer to *Section 4.2* for details on how to enable and read the temperature sensor output data.

8.2 STATUS_M (07h)

Table 17. STATUS_M register

ZYXMOR/ Tempor	ZMOR	YMOR	XMOR	ZYXMDA / Tempda	ZMDA	YMDA	XMDA

Table 18. STATUS_M register description

ZYXMOR/ Tempor	Magnetic X, Y and Z-axis and temperature data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous data) Temperature data overrun if T_ONLY bit in *CTRL7 (26h)* is set to '1'. Default value: 0.
ZMOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YMOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XMOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXMDA/ Tempda	X, Y and Z-axis and temperature new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available) Temperature new data available if the T_ONLY bit in *CTRL7 (26h)* is set to '1'.
ZMDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YMDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XMDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.3 OUT_X_L_M (08h), OUT_X_H_M (09h)

X-axis magnetic data. The value is expressed in 16-bit as two's complement.

8.4 OUT_Y_L_M (0Ah), OUT_Y_H_M (0Bh)

Y-axis magnetic data. The value is expressed in 16-bit as two's complement.

8.5 OUT_Z_L_M (0Ch), OUT_Z_H_M (0Dh)

Z-axis magnetic data. The value is expressed in 16-bit as two's complement.

8.6 WHO_AM_I (0Fh)

Table 19. WHO_AM_I register

0	1	0	0	1	0	0	1

Device identification register.

8.7 INT_CTRL_M (12h)

Table 20. INT_CTRL_M register

XMIEN	YMIEN	ZMIEN	PP_OD	IEA	MIEL	4D	MIEN

Table 21. INT_CTRL_M register description

XMIEN	Enable interrupt recognition on X-axis for magnetic data. Default value: 0. (0: disable interrupt recognition; 1: enable interrupt recognition)
YMIEN	Enable interrupt recognition on Y-axis for magnetic data. Default value: 0. (0: disable interrupt recognition; 1: enable interrupt recognition)
ZMIEN	Enable interrupt recognition on Z-axis for magnetic data. Default value: 0. (0: disable interrupt recognition; 1: enable interrupt recognition)
PP_OD	Interrupt pin configuration. Default value: 0. (0: push-pull; 1: open drain)
IEA	Interrupt polarity. Default value: 0. (0: interrupt active-low; 1: interrupt active-high)
MIEL	Latch interrupt request on *INT_SRC_M (13h)* register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched) Once the MIEL is set to '1', the interrupt is cleared by reading the *INT_SRC_M (13h)* register.
4D	4D enable: 4D detection on acceleration data is enabled when 6D bit in *IG_CFG1 (30h)* is set to 1. Default value: 0.
MIEN	Enable interrupt generation for magnetic data. Default value: 0. (0: disable interrupt generation; 1: enable interrupt generation)

8.8 INT_SRC_M (13h)

Table 22. INT_SRC_M register

M_PTH_X	M_PTH_Y	M_PTH_Z	M_NTH_X	M_NTH_Y	M_NTH_Z	MROI	MINT

Table 23. INT_SRC_M register description

M_PTH_X	Magnetic value on X-axis exceeds the threshold on the positive side. Default value: 0.
M_PTH_Y	Magnetic value on Y-axis exceeds the threshold on the positive side. Default value: 0.
M_PTH_Z	Magnetic value on Z-axis exceeds the threshold on the positive side. Default value: 0.
M_NTH_X	Magnetic value on X-axis exceeds the threshold on the negative side. Default value: 0.
M_NTH_Y	Magnetic value on Y-axis exceeds the threshold on the negative side. Default value: 0.
M_NTH_Z	Magnetic value on Z-axis exceeds the threshold on the negative side. Default value: 0.
MROI	Internal measurement range overflow on magnetic value. Default value: 0.
MINT	Magnetic interrupt event. The magnetic field value exceeds the threshold. Default value: 0.

8.9 INT_THS_L_M (14h), INT_THS_H_M (15h)

Magnetic interrupt threshold. Default value: 0.

The value is expressed in 16-bit unsigned.

Even if the threshold is expressed in absolute value, the device detects both positive and negative thresholds.

Table 24. INT_THS_L_M register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 25. INT_THS_H_M register

0	THS14	THS13	THS12	THS11	THS10	THS9	THS8

8.10 OFFSET_X_L_M (16h), OFFSET_X_H_M (17h)

Magnetic offset for X-axis. Default value: 0.

The value is expressed in 16-bit as two's complement.

Table 26. OFFSET_X_L_M register

OFF_X_7	OFF_X_6	OFF_X_5	OFF_X_4	OFF_X_3	OFF_X_2	OFF_X_1	OFF_X_0

Table 27. OFFSET_X_H_M register

OFF_X_15	OFF_X_14	OFF_X_13	OFF_X_12	OFF_X_11	OFF_X_10	OFF_X_9	OFF_X_8

8.11 OFFSET_Y_L_M (18h), OFFSET_Y_H_M (19h)

Magnetic offset for Y-axis. Default value: 0.

The value is expressed in 16-bit as two's complement.

Table 28. OFFSET_Y_L_M register

OFF_Y_7	OFF_Y_6	OFF_Y_5	OFF_Y_4	OFF_Y_3	OFF_Y_2	OFF_Y_1	OFF_Y_0

Table 29. OFFSET_Y_H_M register

OFF_Y_15	OFF_Y_14	OFF_Y_13	OFF_Y_12	OFF_Y_11	OFF_Y_10	OFF_Y_9	OFF_Y_8

8.12 OFFSET_Z_L_M (1Ah), OFFSET_Z_H_M (1Bh)

Magnetic offset for Z-axis. Default value: 0.

The value is expressed in 16-bit as two's complement.

Table 30. OFFSET_Z_L_M register

OFF_Z_7	OFF_Z_6	OFF_Z_5	OFF_Z_4	OFF_Z_3	OFF_Z_2	OFF_Z_1	OFF_Z_0

Table 31. OFFSET_Z_H_M register

OFF_Z_15	OFF_Z_14	OFF_Z_13	OFF_Z_12	OFF_Z_11	OFF_Z_10	OFF_Z_9	OFF_Z_8

8.13 REFERENCE_X (1Ch)

Reference value for high-pass filter for X-axis acceleration data.

8.14 REFERENCE_Y (1Dh)

Reference value for high-pass filter for Y-axis acceleration data.

8.15 REFERENCE_Z (1Eh)

Reference value for high-pass filter for Z-axis acceleration data.

8.16 CTRL0 (1Fh)

Table 32. CTRL0 register

BOOT	FIFO_EN	FTH_EN	0(1)	0(1)	HP_Click	HPIS1	HPIS2

1. These bits must be set to '0' for correct operation of the device.

Table 33. CTRL0 register description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO enable)
FTH_EN	FIFO programmable threshold enable. Default value: 0 (0: disable; 1: enable)
HP_Click	High-pass filter enabled for click function. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS1	High-pass filter enabled for interrupt generator 1. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS2	High-pass filter enabled for interrupt generator 2. Default value: 0 (0: filter bypassed; 1: filter enabled)

8.17 CTRL1 (20h)

Table 34. CTRL1 register

AODR3	AODR2	AODR1	AODR0	BDU	AZEN	AYEN	AXEN

Table 35. CTRL1 register description

AODR [3:0]	Acceleration data-rate selection. Default value: 0000 (0000: Power-down mode; Others: Refer to *Table 36*)
BDU	Block data update for acceleration and magnetic data. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
AZEN	Acceleration Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
AYEN	Acceleration Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
AXEN	Acceleration X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

AODR [3:0] is used to set power mode and ODR selection. In the following table bit selection of AODR [3:0] for all frequencies is shown.

Table 36. Acceleration data rate configuration

AODR3	AODR2	AODR1	AODR0	Power mode and ODR selection
0	0	0	0	Power-down mode
0	0	0	1	3.125 Hz
0	0	1	0	6.25 Hz
0	0	1	1	12.5 Hz
0	1	0	0	25 Hz
0	1	0	1	50 Hz
0	1	1	0	100 Hz
0	1	1	1	200 Hz
1	0	0	0	400 Hz
1	0	0	1	800 Hz
1	0	1	0	1600 Hz

8.18 CTRL2 (21h)

Table 37. CTRL2 register

ABW1	ABW0	AFS2	AFS1	AFS0	0(1)	AST	SIM

1. This bit must be set to '0' for correct operation of the device.

Table 38. CTRL2 register description

ABW[1:0]	Accelerometer anti-alias filter bandwidth. Default value: 00 Refer to *Table 39*
AFS[2:0]	Acceleration full-scale selection. Default value: 000 Refer to *Table 40*
AST	Acceleration self-test enable. Default value: 0 (0: self-test disabled; 1: self-test enabled)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

Table 39. Acceleration anti-alias filter bandwidth

ABW1	ABW0	Anti-alias filter bandwidth
0	0	773 Hz
0	1	194 Hz

Table 39. Acceleration anti-alias filter bandwidth

ABW1	ABW0	Anti-alias filter bandwidth
1	0	362 Hz
1	1	50 Hz

Table 40. Acceleration full-scale selection

AFS2	AFS1	AFS0	Acceleration full scale
0	0	0	±2 *g*
0	0	1	±4 *g*
0	1	0	±6 *g*
0	1	1	±8 *g*
1	0	0	±16 *g*

8.19 CTRL3 (22h)

Table 41. CTRL3 register

INT1 _BOOT	INT1 _Click	INT1 _IG1	INT1 _IG2	INT1 _IGM	INT1 _DRDY_A	INT1 _DRDY_M	INT1 _EMPTY

Table 42. CTRL3 register description

INT1_BOOT	Boot on INT1 enable. Default value: 0 (0: disable; 1: enable)
INT1_Click	Click generator interrupt on INT1. Default value: 0 (0: disable; 1: enable)
INT1_IG1	Inertial interrupt generator 1 on INT1. Default value: 0 (0: disable; 1: enable)
INT1_IG2	Inertial interrupt generator 2 on INT1. Default value: 0 (0: disable; 1: enable)
INT1_IGM	Magnetic interrupt generator on INT1. Default value: 0 (0: disable; 1: enable)
INT1_DRDY_A	Accelerometer data-ready signal on INT1. Default value: 0 (0: disable; 1: enable)
INT1_DRDY_M	Magnetometer data-ready signal on INT1. Default value: 0 (0: disable; 1: enable)
INT1_EMPTY	FIFO empty indication on INT1. Default value: 0 (0: disable; 1: enable)

8.20 CTRL4 (23h)

Table 43. CTRL4 register

INT2 _Click	INT2 _INT1	INT2 _INT2	INT2 _INTM	INT2 _DRDY_A	INT2 _DRDY_M	INT2 _Overrun	INT2 _FTH

Table 44. CTRL4 register description

INT2 _Click	Click generator interrupt on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _IG1	Inertial interrupt generator 1 on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _IG2	Inertial interrupt generator 2 on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _IGM	Magnetic interrupt generator on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _DRDY_A	Accelerometer data-ready signal on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _DRDY_M	Magnetometer data-ready signal on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _Overrun	FIFO overrun interrupt on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _FTH	FIFO threshold interrupt on INT2. Default value: 0 (0: disable; 1: enable)

8.21 CTRL5 (24h)

Table 45. CTRL5 register

TEMP_EN	M_RES1	M_RES0	M_ODR2	M_ODR1	M_ODR0	LIR2	LIR1

Table 46. CTRL5 register description

TEMP_EN	Temperature sensor enable. Default value: 0 (0: temperature sensor disabled; 1: temperature sensor enabled)
M_RES [1:0]	Magnetic resolution selection. Default value: 00 (00: low resolution, 11: high resolution)
M_ODR [2:0]	Magnetic data rate selection. Default value: 110 Refer to *Table 47*
LIR2	Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
LIR1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)

Table 47. Magnetic data rate configuration

MODR2	MODR1	MODR0	ODR selection
0	0	0	3.125 Hz
0	0	1	6.25 Hz
0	1	0	12.5 Hz
0	1	1	25 Hz
1	0	0	50 Hz
1	0	1	100 Hz(1)
1	1	0	Do not use
1	1	1	Reserved

1. Available only for accelerometer ODR > 50 Hz or accelerometer in power-down mode (refer to *Table 36,* AODR setting).

8.22 CTRL6 (25h)

Table 48. CTRL6 register

0(1)	MFS1	MFS0	0(1)	0(1)	0(1)	0(1)	0(1)

1. These bits must be set to ‘0’ for correct operation of the device.

Table 49. CTRL6 register description

MFS [1:0]	Magnetic full-scale selection. Default value: 01 Refer to *Table 50*

Table 50. Magnetic full-scale selection

MFS1	MFS0	Magnetic full scale
0	0	±2 gauss
0	1	±4 gauss
1	0	±8 gauss
1	1	±12 gauss

8.23 CTRL7 (26h)

Table 51. CTRL7 register

AHPM1	AHPM0	AFDS	T_ONLY	0(1)	MLP	MD1	MD0

1. This bit must be set to ‘0’ for correct operation of the device.

Table 52. CTRL7 register description

AHPM[1:0]	High-pass filter mode selection for acceleration data. Default value: 00 Refer to *Table 53*
AFDS	Filtered acceleration data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
T_ONLY	Temperature sensor only mode. Default value: 0 If this bit is set to '1', the temperature sensor is on while the magnetic sensor is off.
MLP	Magnetic data low-power mode. Default value: 0 If this bit is '1', the M_ODR [2:0] is set to 3.125 Hz independently from the MODR settings. Once the bit is set to '0', the magnetic data rate is configured by the MODR bits in the *CTRL5 (24h)* register.
MD[1:0]	Magnetic sensor mode selection. Default 10 Refer to *Table 54*

Table 53. High-pass filter mode selection

AHPM1	AHPM0	High-pass filter mode
0	0	Normal mode (reset X, Y and Z-axis, reading respective *REFERENCE_X (1Ch)*, *REFERENCE_Y (1Dh)* and *REFERENCE_Z (1Eh)* registers)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Auto-reset on interrupt event

Table 54. Magnetic sensor mode selection

MD1	MD0	Magnetic sensor mode
0	0	Continuous-conversion mode
0	1	Single-conversion mode
1	0	Power-down mode
1	1	Power-down mode

8.24 STATUS_A (27h)

Table 55. STATUS_A register

ZYXAOR	ZAOR	YAOR	XAOR	ZYXADA	ZADA	YADA	XADA

Table 56. STATUS_A register description

ZYXAOR	Acceleration X, Y and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous data)
ZAOR	Acceleration Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YAOR	Acceleration Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XAOR	Acceleration X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXADA	Acceleration X, Y and Z-axis new value available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZADA	Acceleration Z-axis new value available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YADA	Acceleration Y-axis new value available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XADA	Acceleration X-axis new value available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.25 OUT_X_L_A (28h), OUT_X_H_A (29h)

X-axis acceleration data. The value is expressed in 16-bit as two’s complement.

8.26 OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)

Y-axis acceleration data. The value is expressed in 16-bit as two’s complement.

8.27 OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)

Z-axis acceleration data. The value is expressed in 16-bit as two’s complement.

8.28 FIFO_CTRL (2Eh)

Table 57. FIFO_CTRL register

FM2	FM1	FM0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 58. FIFO_CTRL register description

FM[2:0]	FIFO mode selection. Default value: 000 Refer to *Table 59*
FTH[4:0]	FIFO threshold level. Default value: 00000

Table 59. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

Interrupt generator 2 can change the FIFO mode.

8.29 FIFO_SRC (2Fh)

FiFO status register.

Table 60. FIFO_SRC register

FTH	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 61. FIFO_SRC register description

FTH	FIFO threshold status. FTH bit is set to ‘1’ when FIFO content exceeds threshold level.
OVRN	FIFO overrun status. OVRN bit is set to ‘1’ when FIFO buffer is full.
EMPTY	Empty status. EMPTY bit is set to ‘1’ when all FIFO samples have been read and FIFO is empty.
FSS[4:0]	FIFO stored data level. FSS4-0 bits contain the current number of unread FIFO levels.

8.30 IG_CFG1 (30h)

Inertial interrupt generator 1 configuration register.

Table 62. IG_CFG1 register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 63. IG_CFG1 register description

AOI	And/Or combination of interrupt events. Default value: 0. Refer to *Table 64*
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 64*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/ XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Content of this register is loaded at boot.

Write operation at this address is possible only after system boot.

Table 64. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

Difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when orientation moves from an unknown zone to a known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when orientation is inside a known zone. The interrupt signal stays until orientation is inside the zone.

8.31 IG_SRC1 (31h)

Inertial interrupt generator 1 status register.

Table 65. IG_SRC1 register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 66. IG_SRC1 register description

IA	Interrupt status. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt; 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt; 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt; 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt; 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt; 1: X low event has occurred)

Reading at this address clears the *IG_SRC1 (31h)* IA bit (and the interrupt signal on the corresponding interrupt pin) and allows the refreshment of data in the *IG_SRC1 (31h)* register if the latched option was chosen.

8.32 IG_THS1 (32h)

Table 67. IG_THS1 register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 68. IG_THS1 register description

THS[6:0]	Interrupt generator 1 threshold. Default value: 000 0000

8.33 IG_DUR1 (33h)

Table 69. IG1_DUR1 register

0	D6	D5	D4	D3	D2	D1	D0

Table 70. IG1_DUR1 register description

D[6:0]	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.34 IG_CFG2 (34h)

This register contains the settings for the inertial interrupt generator 2.

Table 71. IG_CFG2 register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 72. IG_CFG2 register description

AOI	And/Or combination of interrupt events. Default value: 0. Refer to *Table 73*
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 73*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/ XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Content of this register is loaded at boot.

Write operation at this address is possible only after system boot.

Table 73. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

Difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal remains for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal remains until the orientation is inside the zone.

8.35 IG_SRC2 (35h)

This register contains the status for the inertial interrupt generator 2.

Table 74. IG_SRC2 register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 75. IG_SRC2 register description

IA	Interrupt generator 2 status. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt; 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt; 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt; 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt; 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt; 1: X low event has occurred)

Reading at this address clears the *IG_SRC2 (35h)* IA bit (and the interrupt signal on the corresponding interrupt pin) and allows the refresh of data in the *IG_SRC2 (35h)* register if the latched option was chosen.

8.36 IG_THS2 (36h)

Table 76. IG2_THS2 register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 77. IG2_THS2 register description

THS[6:0]	Interrupt generator 2 threshold. Default value: 000 0000

8.37 IG_DUR2 (37h)

Table 78. IG_DUR2 register

0	D6	D5	D4	D3	D2	D1	D0

Table 79. IG_DUR2 register description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.38 CLICK_CFG (38h)

Table 80. CLICK_CFG register

--	--	ZD	ZS	YD	YS	XD	XS

Table 81. CLICK_CFG register description

ZD	Enable interrupt double-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enable interrupt single-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enable interrupt double-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enable interrupt single-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XD	Enable interrupt double-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enable interrupt single-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

8.39 CLICK_SRC (39h)

Table 82. CLICK_SRC register

--	IA	DClick	SClick	Sign	Z	Y	X

Table 83. CLICK_SRC register description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
DClick	Double-click enable. Default value: 0 (0: double-click detection disable; 1: double-click detection enable)
SClick	Single-click enable. Default value: 0 (0: single-click detection disable; 1: single-click detection enable)
Sign	Click sign. 0: positive detection; 1: negative detection
Z	Z-click detection. Default value: 0 (0: no interrupt; 1: Z high event has occurred)
Y	Y-click detection. Default value: 0 (0: no interrupt; 1: Y high event has occurred)
X	X-click detection. Default value: 0 (0: no interrupt; 1: X high event has occurred)

8.40 CLICK_THS (3Ah)

Table 84. CLICK_THS register

-	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0

Table 85. CLICK_THS register description

Ths[6:0]	Click threshold. Default value: 000 0000

8.41 TIME_LIMIT (3Bh)

Table 86. TIME_LIMIT register

-	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0

Table 87. TIME_LIMIT register description

TLI[6:0]	Click time limit. Default value: 000 0000

8.42 TIME_LATENCY (3Ch)

Table 88. TIME_LATENCY register

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

Table 89. TIME_LATENCY register description

TLA[7:0]	Double-click time latency. Default value: 0000 0000

8.43 TIME_WINDOW (3Dh)

Table 90. TIME_WINDOW register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

Table 91. TIME_WINDOW register description

TW[7:0]	Double-click time window

8.44 ACT_THS (3Eh)

Table 92. ACT_THS register

--	ACTH6	ACTH5	ACTH4	ACTH3	ACTH2	ACTH1	ACTH0

Table 93. ACT_THS register description

ACTH[6:0]	Sleep-to-Wake, Return-to-Sleep activation threshold 1 LSb = 16 m*g*

8.45 ACT_DUR (3Fh)

Table 94. ACT_DUR register

ActD7	ActD6	ActD5	ActD4	ActD3	ActD2	ActD1	ActD0

Table 95. ACT_DUR register description

ActD[7:0]	Sleep-to-Wake, Return-to-Sleep duration DUR = (Act_DUR + 1)*8/ODR

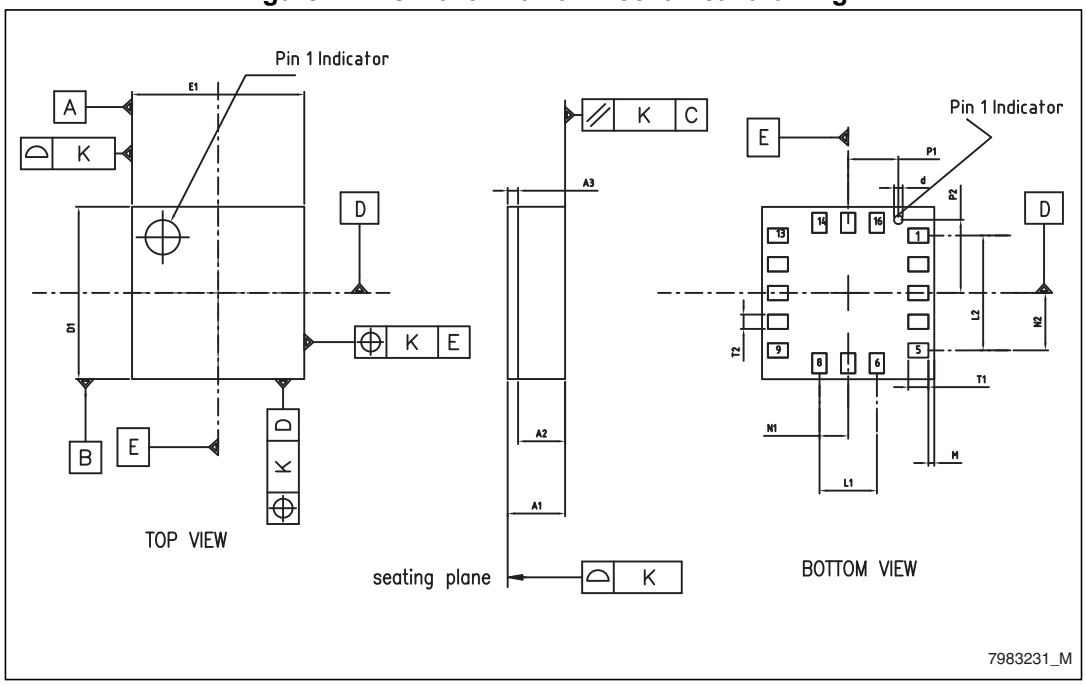
9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 96. LGA 3x3x1.0 16L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1			1
A2		0.785	
A3		0.200	
D1	2.850	3.000	3.150
E1	2.850	3.000	3.150
L1		1.000	1.060
L2		2.000	2.060
N1		0.500	
N2		1.000	
M	0.040	0.100	
P1		0.875	
P2		1.275	
T1	0.290	0.350	0.410
T2	0.190	0.250	0.310
d		0.150	
k		0.050	

Figure 12. LGA 3x3x1.0 16L mechanical drawing



10 Revision history

Table 97. Document revision history

Date	Revision	Changes
22-Jun-2012	1	Initial release
05-Nov-2013	2	Document status promoted from preliminary to production data Changed abbreviation of magnetic sensitivity to M_So and updated footnote *6* in *Table 3: Sensor characteristics* Added ESD to *Table 8: Absolute maximum ratings* Minor textual updates throughout document

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