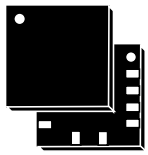
LIS2HH12

MEMS digital output motion sensor: ultra-low-power high-performance 3-axis "pico" accelerometer

Datasheet - production data



LGA-12 (2.0x2.0x1.0 mm)

Features

- Wide supply voltage, 1.71 V to 3.6 V
- Independent IOs supply (1.8 V) and supply voltage compatible
- Ultra-low power consumption
- ±2g/±4g/±8*g* full-scale
- I^2C/SPI digital output interface
- 16-bit data output
- Embedded temperature sensor
- Embedded self-test
- Embedded FIFO
- 10000 *g* high shock survivability
- ECOPACK®, RoHS and “Green” compliant

Applications

- Motion-controlled user interfaces
- Gaming and virtual reality
- Pedometers
- Intelligent power saving for handheld devices
- Display orientation
- Click/double-click recognition
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LIS2HH12 is an ultra-low-power high-performance three-axis linear accelerometer belonging to the “pico” family.

The LIS2HH12 has full scales of ±2g/±4g/±8g and is capable of measuring accelerations with output data rates from 10 Hz to 800 Hz.

The self-test capability allows the user to check the functioning of the sensor in the final application.

The LIS2HH12 has an integrated first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

The LIS2HH12 is available in a small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packaging
LIS2HH12	-40 to +85	LGA-12	Tray
LIS2HH12TR	-40 to +85	LGA-12	Tape and reel

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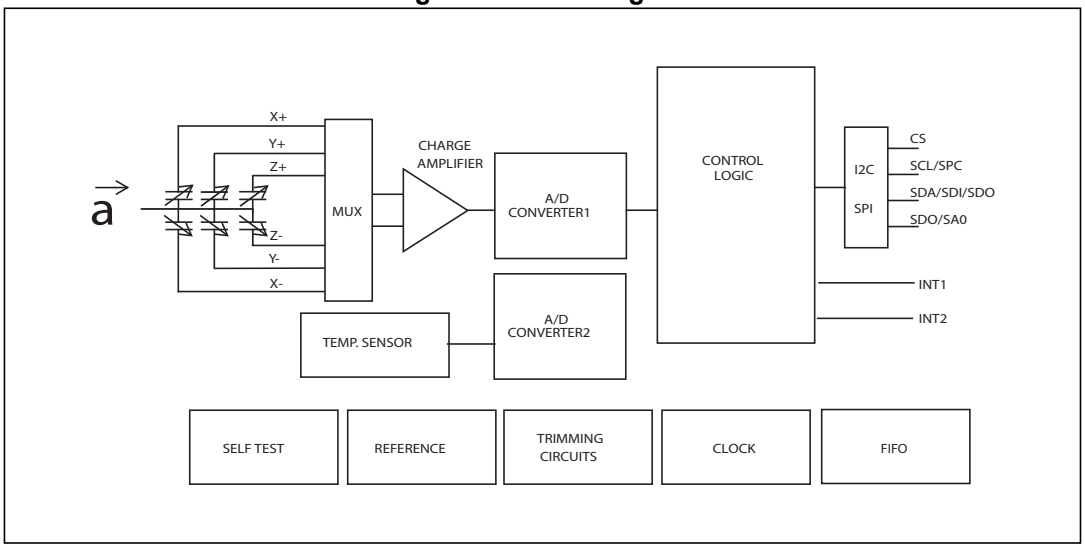
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

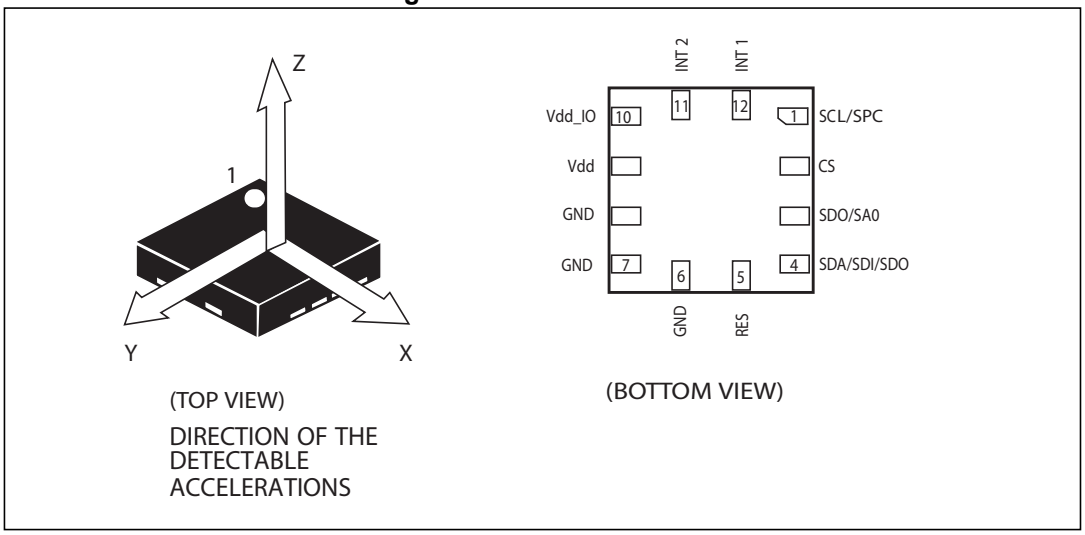


Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
3	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	RES	Connect to GND
6	GND	0 V supply
7	GND	0 V supply
8	GND	0 V supply
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11	INT2	Interrupt pin 2
12	INT1	Interrupt pin 1

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

Table 3. Mechanical characteristics @ Vdd = 2.5 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
FS	Measurement range(3)			±2.0		g
				±4.0		g
				±8.0		g
So	Sensitivity	@ FS ±2.0 *g*		0.061		mg/digit
		@ FS ±4.0 *g*		0.122		mg/digit
		@ FS ±8.0 *g*		0.244		mg/digit
TCSo	Sensitivity change vs. temperature			0.01		%/°C
TyOff	Typical zero-*g* level offset accuracy(4)			±30		mg
TCOff	Zero-*g* level change vs. temperature(4)	Delta from 25 °C		±0.25		mg/°C
Ton	Turn-on time	Number of samples to be discarded from power-down to active mode *CTRL4 (23h)* (BW_SCALE_ODR) = 0	1			# of samples
ST	Self-test positive difference(5)		70		1500	mg
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. Verified by wafer level test and measurement of initial offset and sensitivity.
4. Offset can be eliminated by enabling the built-in high-pass filter.
5. “Self-test positive difference” is defined as: $\text{OUTPUT}[mg]_{(\text{CTRL5 ST2, ST1 bits=01})} - \text{OUTPUT}[mg]_{(\text{CTRL5 ST2, ST1 bits=00})}$.

2.2 Electrical characteristics

Table 4. Electrical characteristics @ Vdd = 2.5 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		1.71	2.5	3.6	V
Vdd_IO	I/O pins supply voltage(3)		1.71		Vdd+0.1	V
IddA	Current consumption in active mode	ODR 100-800 Hz		180		µA
		ODR 50 Hz		110		µA
		ODR 10 Hz		50		µA
IddPdn	Current consumption in power-down mode			5		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
Tboot	Boot time(4)				20	ms
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.
4. Time to complete the entire boot sequence: from Vdd on until all configuration and calibration parameters are correctly loaded into device registers.

2.3 Temperature sensor characteristics

@ Vdd =2.5 V, T=25 °C unless otherwise noted

Table 5. Temperature sensor characteristics

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature		8		digit/°C(2)
TODR	Temperature refresh rate		10		Hz
Top	Operating temperature range	-40		+85	°C

1. Typical specifications are not guaranteed.
2. 11-bit resolution.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

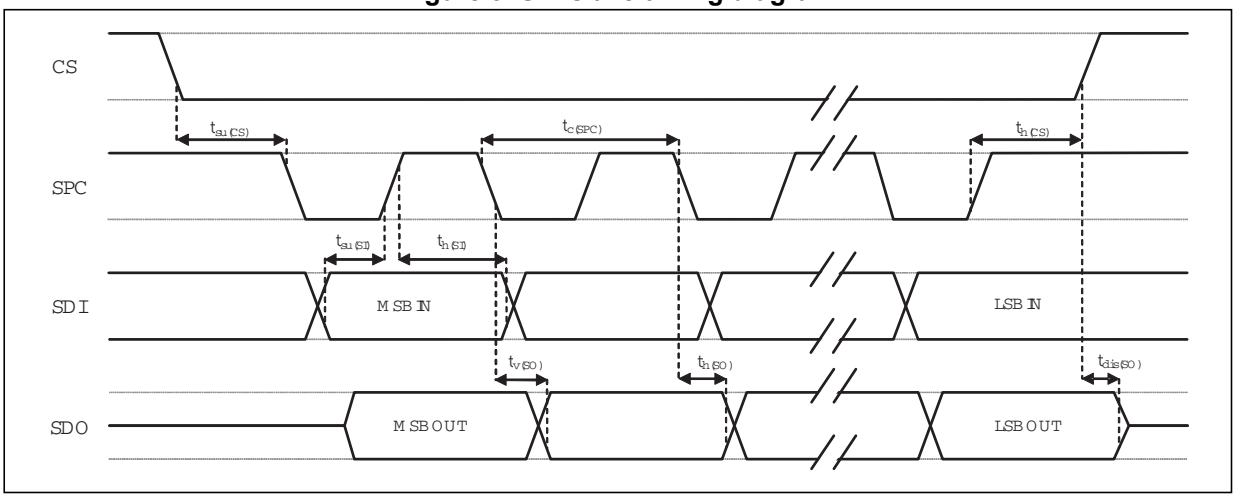
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

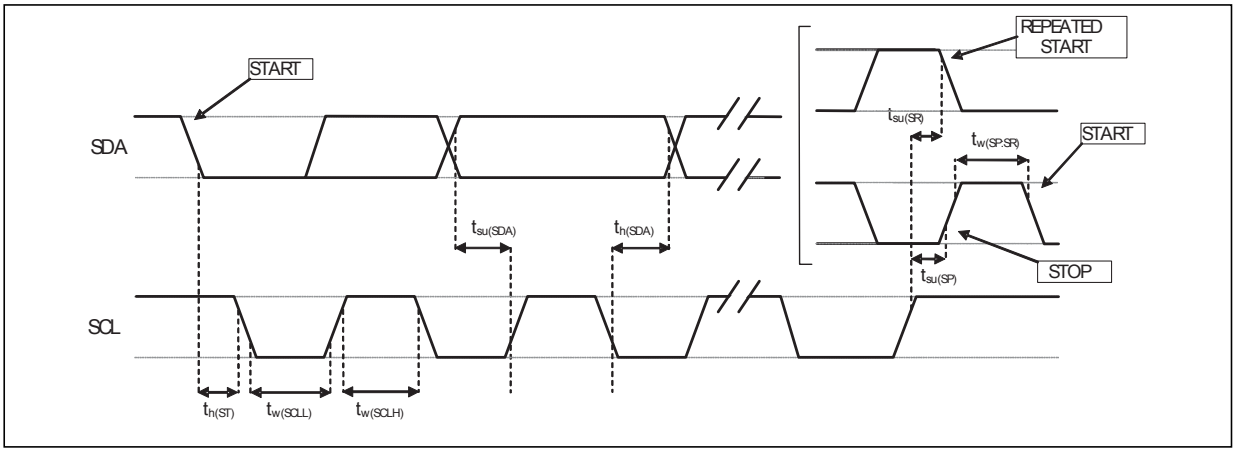
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3000 for 0.5 ms	*g*
		10000 for 0.2 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.2 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology and functionality

Terminology

2.6.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

2.6.2 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

Functionality

2.6.3 Self-test

The self-test allows checking the sensor functionality without moving it. The self-test function is off when the self-test bits (ST) are programmed to '00'. When the self-test bits are changed, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

2.7 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. In order to be compatible with the traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation.

When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

2.8 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS2HH12 features a data-ready signal which indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.

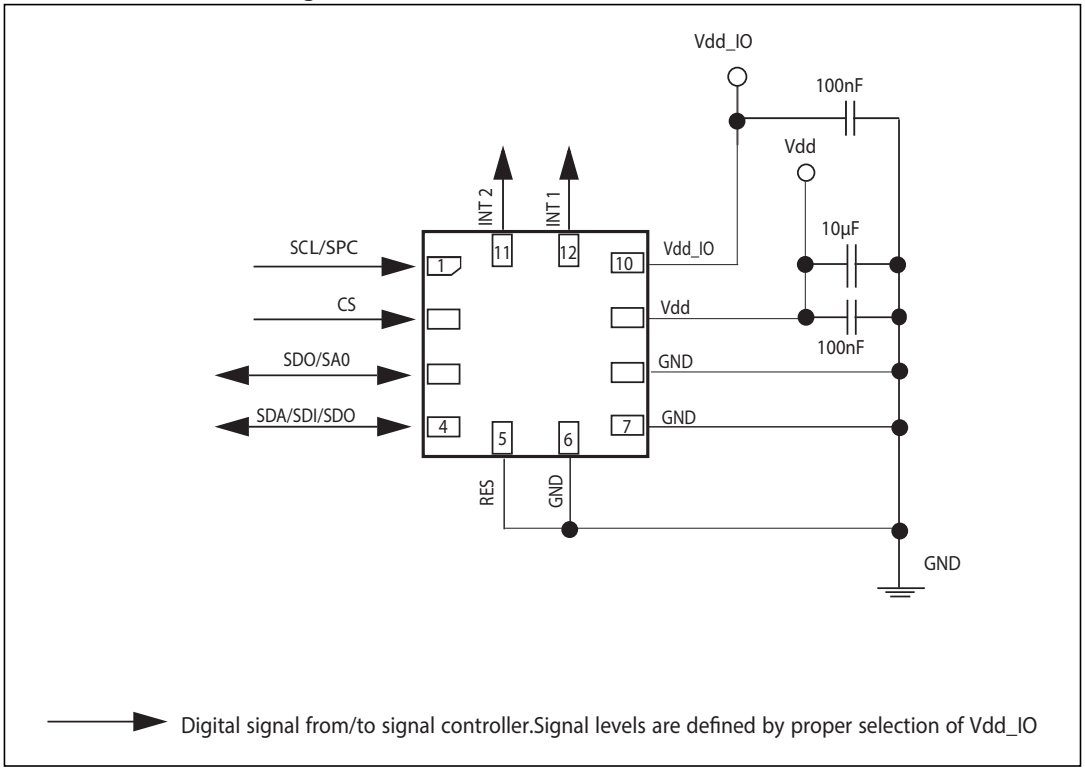
3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-*g* level (TyOff).

The trim values are stored inside the device in nonvolatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the active operation. This allows using the device without further calibration.

4 Application hints

Figure 5. LIS2HH12 electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I^2C/SPI interface.

4.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

5 Digital main blocks

5.1 Activity/Inactivity function

The Activity/Inactivity recognition function allows reducing the power consumption of the system in order to develop new smart applications.

When the Activity/Inactivity recognition function is activated, the LIS2HH12 is able to automatically go to 10Hz sampling rate and to wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Activity/Inactivity recognition function is activated by writing the desired threshold in the *ACT_THS (1Eh)* register. The high-pass filter is automatically enabled.

Table 9. Activity/Inactivity function control registers

Register	LSB value
ACT_THS	Full scale / 128 [mg]
ACT_DUR	8/ODR [s]

When the acceleration falls below the threshold for a duration of at least (8 ACT_DUR +1)/ODR, the *CTRL1 (20h)* (ODR [2:0]) bits of CTRL1 are bypassed (Inactivity) and internally set to 10Hz (ODR [2:0] = 001), but the content of the *CTRL1 (20h)* (ODR [2:0]) bits are left untouched.

When the acceleration exceeds the threshold (*ACT_THS (1Eh)*), the ODR setting in *CTRL1 (20h)* is restored immediately (Activity).

Once the Activity/Inactivity detection function is enabled, the status can be brought out on INT1 by setting the *CTRL3 (22h)* (INT1_INACT) bit to 1.

To disable the Activity/Inactivity detection function, set the content of the *ACT_THS (1Eh)* register to 00h.

5.2 Data stabilization time / ODR change

The data stabilization time required when an ODR change is applied in order to have valid usable data depends on the BW and ODR selected.

The table below provides the number of samples to be discarded in order to obtain valid usable data.

Table 10. Number of samples to be discarded

ODR [Hz]	BW = 400 Hz	BW = 200 Hz	BW = 100 Hz	BW = 50 Hz
10	1	-	-	-
50	1	-	-	-
100	1	1	1	1
200	1	1	1	4
400	1	1	4	7
800	1	4	7	14

5.3 FIFO

The LIS2HH12 embeds an acceleration data FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to the following different modes: Bypass mode, FIFO-mode, Stream mode, Stream-to-FIFO mode, Bypass-to-Stream, Bypass-to-FIFO. Each mode is selected by the FIFO_MODE bits in the *FIFO_CTRL (2Eh)* register. Programmable FIFO threshold level, FIFO empty or FIFO overrun events are available in the *FIFO_CTRL (2Eh)* register and can be set to generate dedicated interrupts on the INT1 or INT2 pin.

FIFO_SRC (2Fh) (EMPTY) is equal to '1' when no samples are available.

FIFO_SRC (2Fh)(FTH) goes to '1' if new data arrives and *FIFO_SRC (2Fh)*(FSS [4:0]) is greater than or equal to *FIFO_CTRL (2Eh)* (FTH [4:0]). *FIFO_SRC (2Fh)* (FTH) goes to '0' if reading X, Y, Z data slot from *FIFO* and *FIFO_SRC (2Fh)* (FSS [4:0]) is less than or equal to *FIFO_CTRL (2Eh)* (FTH [4:0]).

FIFO_SRC (2Fh) (OVR) is equal to '1' if a FIFO slot is overwritten.

The FIFO feature is enabled by writing the *CTRL3 (22h)* (FIFO_EN) bit to '1' in control register 3.

In order to guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

5.3.1 Bypass mode

In Bypass mode (*FIFO_CTRL (2Eh)* (FMODE [2:0])= 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

5.3.2 FIFO mode

In FIFO mode (*FIFO_CTRL (2Eh)* (FMODE [2:0])= 001) data from the X, Y and Z channels are stored in the FIFO until it is full. An overrun interrupt can be enabled, *CTRL3 (22h)* (INT1_OVR)= '1', in order to be raised when the FIFO stops collecting data. When the overrun interrupt occurs, the first set of data has been overwritten and the FIFO stops collecting data from the input channels. To reset the FIFO content, Bypass mode should be written in the *FIFO_CTRL (2Eh)* register, setting the FMODE [2:0] bits to '000'. After this reset command, it is possible to restart FIFO mode, writing the value '001' in *FIFO_CTRL (2Eh)* (FMODE [2:0]).

The FIFO buffer can memorize 32 slots of X, Y and Z data, but the depth of the FIFO can be reduced using the *CTRL3 (22h)* (STOP_ FTH) bit. Setting the STOP_FTH bit to '1', FIFO depth is limited to *FIFO_CTRL (2Eh)* (FTH [4:0]) - 1.

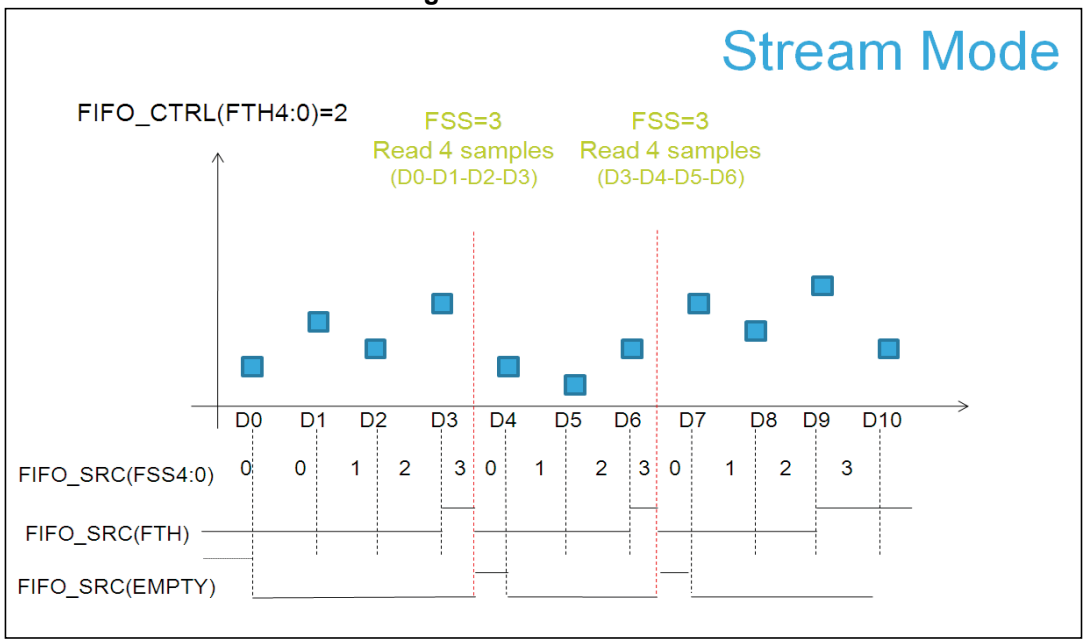
5.3.3 Stream mode

Stream mode (*FIFO_CTRL (2Eh)* (FMODE [2:0]) = 010) provides a continuous FIFO update: as new data arrives, the older data is discarded.

An overrun interrupt can be enabled, *CTRL3 (22h)* (INT1_OVR) = '1', in order to read the entire content of the FIFO at once. If in the application no data can be lost and it is not possible to read at least one sample for each axis within one ODR period, a watermark interrupt can be enabled in order to read partially the FIFO and leave free memory slots for incoming data. Setting the *FIFO_CTRL (2Eh)* (FTH [4:0]) to value N, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt is up to (N+1).

In the latter case, reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last data already read in previous burst, so the number of new data available in the FIFO depends on the previous reading (see *FIFO_SRC (2Fh)*behavior depicted in the following figures).

Figure 6. Stream mode



A watermark interrupt *CTRL3 (22h)* (INT1_FTH), *CTRL6 (25h)*(INT2_FTH) can be enabled in order to read data from the FIFO and leave free memory slots for incoming data. Setting the *FIFO_CTRL (2Eh)* (FTH [4:0]) to value N, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt, in order to read the entire FIFO content, is N + 1.

5.3.4 Stream-to-FIFO mode

In Stream-to-FIFO mode (*FIFO_CTRL (2Eh)*(FMODE2:0) = 011), FIFO behavior changes according to the *IG_SRC1 (31h)* (IA) bit. When the *IG_SRC1 (31h)* (IA) bit is equal to '1' FIFO operates in FIFO mode, when the *IG_SRC1 (31h)* (IA) bit is equal to '0', FIFO operates in Stream mode.

Interrupt generator 1 should be set to the desired configuration using *IG_CFG1 (30h)*, *IG_THS_X1 (32h), IG_THS_Y1 (33h), IG_THS_Z1 (34h)*.

The *CTRL7 (26h)* (LIR1) bit should be set to '1' in order to have latched interrupt.

5.3.5 Bypass-to-Stream mode

In Bypass-to-Stream mode (*FIFO_CTRL (2Eh)* (FMODE [2:0]) = '100'), X, Y and Z measurement storage inside FIFO operates in Stream mode when *IG_SRC1 (31h)* (IA) is equal to '1', otherwise FIFO content is reset (Bypass mode).

Interrupt generator 1 should be set to the desired configuration using *IG_CFG1 (30h)*, *IG_THS_X1 (32h), IG_THS_Y1 (33h), IG_THS_Z1 (34h)*.

The *CTRL7 (26h)* (LIR1) bit should be set to '1' in order to have latched interrupt.

5.3.6 Bypass-to-FIFO mode

In Bypass-to-FIFO mode (*FIFO_CTRL (2Eh)* (FMODE [2:0]) = '111', FIFO behavior changes according to the *IG_SRC1 (31h)* (IA) bit. When the *IG_SRC1 (31h)*(IA) bit is equal to '1', FIFO operates in FIFO mode, when the *IG_SRC1 (31h)* (IA) bit is equal to '0', FIFO operates in Bypass mode (FIFO content reset). If a latched interrupt is generated, FIFO starts collecting data until the first data in the FIFO buffer is overwritten. Interrupt generator 1 should be set to the desired configuration using *IG_CFG1 (30h)*, *IG_THS_X1 (32h), IG_THS_Y1 (33h), IG_THS_Z1 (34h)*.

The *CTRL7 (26h)* (LIR1) bit should be set to '1' in order to have latched interrupt.

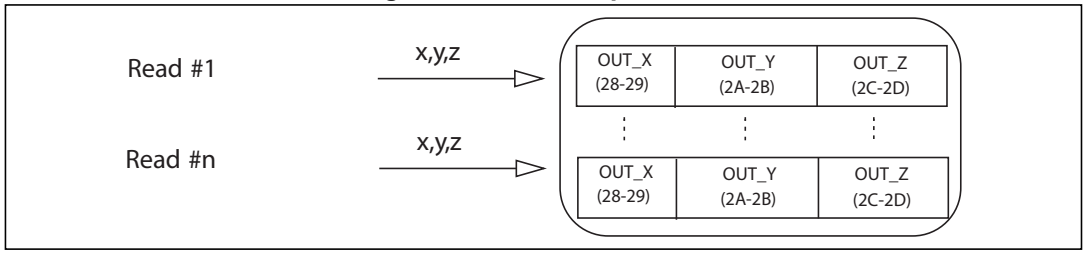
5.3.7 Retrieving data from FIFO

FIFO data is read through the *OUT_X_L (28h) - OUT_X_H (29h)*, *OUT_Y_L (2Ah) - OUT_Y_H (2Bh)*, *OUT_Z_L (2Ch) - OUT_Z_H (2Dh)* registers. A read operation by means of serial interface of OUT_X, OUT_Y or OUT_Z output registers provides the data stored into the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed into the OUT_X, OUT_Y and OUT_Z registers and both single read and read_burst operations can be used.

5.3.8 FIFO multiple reads (burst)

Starting from Addr 28h multiple reads can be performed. Once the read reaches Addr 2Dh the system automatically restarts from Addr 28h.

Figure 7. FIFO multiple reads



6 Digital interfaces

The registers embedded inside the LIS2HH12 may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 11. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0 SDO	I^2C address selection (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The LIS2HH12 I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 12. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

In order to disable the I^2C block, *CTRL4 (23h)* (I2C_DISABLE) = 1 must be set.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave Address (SAD) associated to the LIS2HH12 is 00111xxb where the xx bits are modified by the SA0/SDO pin in order to modify the device address. If the SA0/SDO pin is connected to the supply voltage, the address is 0011101b, otherwise if the SA0/SDO pin is connected to ground, the address is 0011110b. This solution permits to connect and address two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LIS2HH12 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represents the actual register address while the *CTRL4 (23h)* (IF_ADD_INC) bit defines the address increment.

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 13* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 13. SAD+Read/Write patterns

Command	SAD[6:2]	SAD[1] = $\overline{SA0}$	SAD[0] = SA0	R/W	SAD+R/W
Read	00111	1	0	1	00111101
Write	00111	1	0	0	00111100
Read	00111	0	1	1	00111011
Write	00111	0	1	0	00111010

Table 14. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 15. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 16. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 17. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DAT A		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

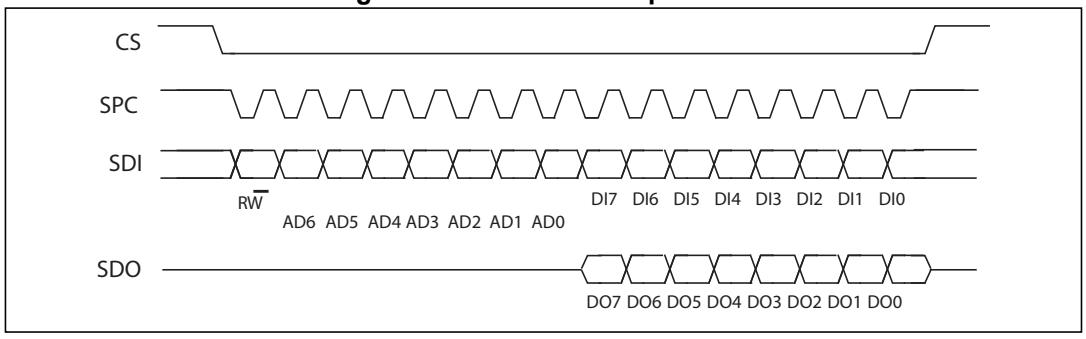
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

6.2 SPI bus interface

The LIS2HH12 SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 8. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

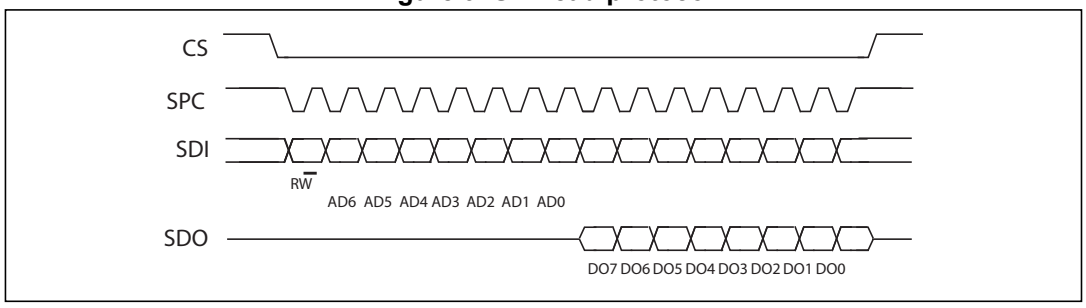
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands additional blocks of 8 clock periods will be added. When the *CTRL4 (23h)* (IF_ADD_INC) bit is '0', the address used to read/write data remains the same for every block. When the *CTRL4 (23h)* (IF_ADD_INC) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 9. SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

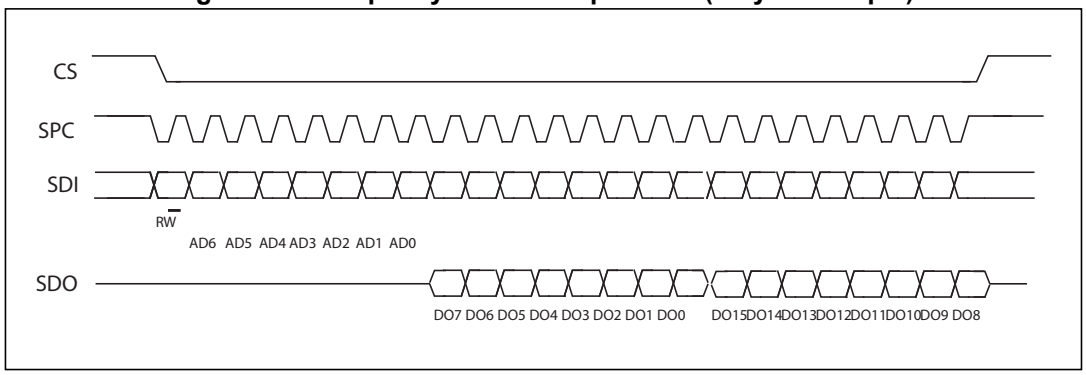
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

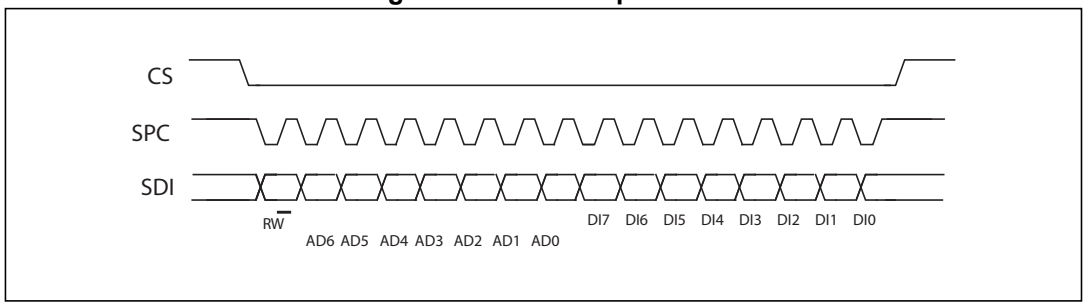
bit 16-... : data DO(...-8). Additional data in multiple byte reads.

Figure 10. Multiple byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 11. SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

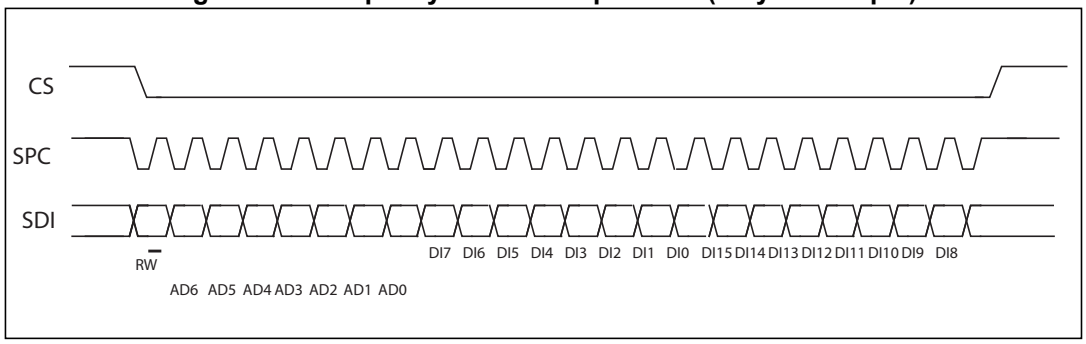
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Additional data in multiple byte writes.

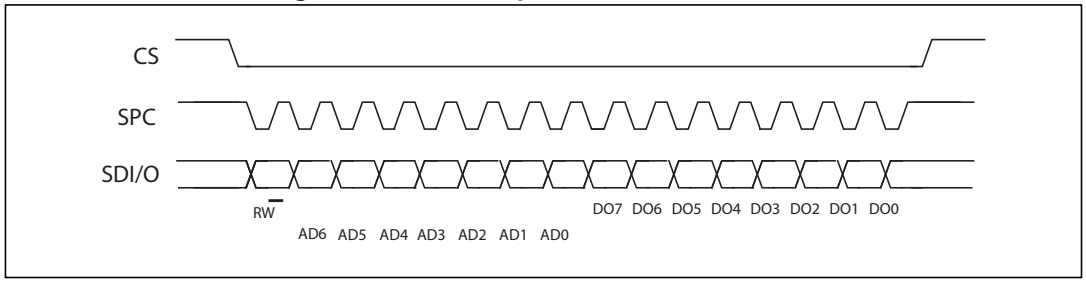
Figure 12. Multiple byte SPI write protocol (2-byte example)



6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the *CTRL4 (23h)* (SIM) bit equal to '1' (SPI serial interface mode selection).

Figure 13. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

7 Register mapping

The table given below provides a list of the 8/16 bit registers embedded in the device and the corresponding addresses.

Table 18. Register map

Name	Type	Register address		Default	Comment
		Hex	Binary		
RESERVED	r	00-0A		-	RESERVED
TEMP_L	r	0B	00001011	output	
TEMP_H	r	0C	00001100	output	
RESERVED	r	0E		-	RESERVED
WHO_AM_I	r	0F	00001111	01000001	Who I am ID
ACT_THS	r/w	1E	00011110	00000000	
ACT_DUR	r/w	1F	00011111	00000000	
CTRL1	r/w	20	00100000	00000111	Control registers
CTRL2	r/w	21	00100001	00000000	
CTRL3	r/w	22	00100010	00000000	
CTRL4	r/w	23	00100011	00000100	
CTRL5	r/w	24	00100100	00000000	
CTRL6	r/w	25	00100101	00000000	
CTRL7	r/w	26	00100110	00000000	
STATUS	r	27	00100111	output	Status data register
OUT_X_L	r	28	00101000	output	Output registers
OUT_X_H	r	29	00101001		
OUT_Y_L	r	2A	00101010		
OUT_Y_H	r	2B	00101011		
OUT_Z_L	r	2C	00101100		
OUT_Z_H	r	2D	00101101		
FIFO_CTRL	r/w	2E	00101110	00000000	FIFO registers
FIFO_SRC	r	2F	00101111	output	
IG_CFG1	r/w	30	00110000	00000000	Interrupt generator 1 configuration
IG_SRC1	r	31	00110001	output	Interrupt generator 1 status register
IG_THS_X1	r/w	32	00110010	00000000	Interrupt generator 1 threshold X

Table 18. Register map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
IG_THS_Y1	r/w	33	00110011	00000000	Interrupt generator 1 threshold Y
IG_THS_Z1	r/w	34	00110100	00000000	Interrupt generator 1 threshold Z
IG_DUR1	r/w	35	00110101	00000000	Interrupt generator 1 duration
IG_CFG2	r/w	36	00110110	00000000	Interrupt generator 2 configuration
IG_SRC2	r	37	00110111	output	Interrupt generator 2 status register
IG_THS2	r/w	38	00111000	00000000	Interrupt generator 2 threshold
IG_DUR2	r/w	39	00111001	00000000	Interrupt generator 2 duration
XL_ REFERENCE	r/w	3A	00111010	00000000	Reference X low
XH_ REFERENCE	r/w	3B	00111011	00000000	Reference X high
YL_ REFERENCE	r/w	3C	00111100	00000000	Reference Y low
YH_ REFERENCE	r/w	3D	00111101	00000000	Reference Y high
ZL_ REFERENCE	r/w	3E	00111110	00000000	Reference Z low
ZH_ REFERENCE	r/w	3F	00111111	00000000	Reference Z high

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

8.1 TEMP_L (0Bh), TEMP_H (0Ch)

Temperature output register (r). The value is expressed in two's complement.

8.2 WHO_AM_I (0Fh)

Who_AM_I register (r). This register is a read-only register. Its value is fixed at 41h.

Table 19. WHO_AM_I register default values

0	1	0	0	0	0	0	1

8.3 ACT_THS (1Eh)

Activity threshold register (r/w). Its value is fixed at 0x00. Inactivity threshold.

Table 20. ACT_THS register default values

0(1)	THS6	THS5	THS4	THS3	THS2	THS1	THS0

1. This bit must be set to '0' for the correct operation of the device.

8.4 ACT_DUR (1Fh)

Activity duration register (r/w). Its value is fixed at 0x00. Activity duration.

Table 21. ACT_DUR register default values

DUR7	DUR6	DUR5	DUR4	DUR3	DUR2	DUR1	DUR0

8.5 CTRL1 (20h)

Control register 1(r/w)

Table 22. Control register 1

HR	ODR2	ODR1	ODR0	BDU	ZEN	YEN	XEN

Table 23. Control register 1 description

HR	High resolution bit. Default value: 0 0: normal mode, 1: high resolution (see *Table*)
ODR [2:0]	Output data rate & power mode selection. Default value: 000 (see *Table*)
BDU	Block data update. Default value: 0 0: continuous update; 1:output registers not updated until MSB and LSB read)
ZEN	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
YEN	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
XEN	X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

ODR [2:0] is used to set the power mode and ODR selection. The following table lists the bit settings for power-down mode and each available frequency.

Table 24. ODR register setting

ODR2	ODR1	ODR0	Power-down and ODR selection
0	0	0	Power-down
0	0	1	10 Hz
0	1	0	50 Hz
0	1	1	100 Hz
1	0	0	200 Hz
1	0	1	400 Hz
1	1	0	800 Hz
1	1	1	N.A.

The BDU bit is used to inhibit the update of the output registers until both upper and lower register parts are read. In default mode (BDU = ‘0’) the output register values are updated continuously. When the BDU is activated (BDU = ‘1’), the content of the output registers is not updated until both MSB and LSB are read which avoids reading values related to different sample times.

Table 25. Low-pass cutoff frequency in high resolution mode (HR = 1)

HR	CTRL2 (DFC [1:0])	LP cutoff freq. [Hz]
1	00	ODR/50
1	01	ODR/100
1	10	ODR/9
1	11	ODR/400

8.6 CTRL2 (21h)

Control register 2 (r/w)

Table 26. Control register 2

0(1)	DFC1	DFC0	HPM1	HPM0	FDS	HPIS1	HPIS2

1. This bit must be set to '0' for the correct operation of the device.

Table 27. Control register 2 description

DFC1 [1:0]	High-pass filter cutoff frequency selection: the bandwidth of the high-pass filter depends on the selected ODR and on the settings of the DFC [1:0] bits
HPM [1:0]	High-pass filter mode selection. Default value: 00 "00" or "10" = Normal mode; "01" = Reference signal for filtering; "11" = Not available
FDS	High-pass filter data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPIS1	High-pass filter enabled for interrupt generator function on Interrupt 1. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS2	High-pass filter enabled for interrupt generator function on Interrupt 2. Default value: 0 (0: filter bypassed; 1: filter enabled)

8.7 CTRL3 (22h)

Control register 3 (r/w). INT1 control register.

Table 28. Control register 3

FIFO_EN	STOP_FTH	INT1 _INACT	INT1 _IG2	INT1 _IG1	INT1 _OVR	INT1 _FTH	INT1 _DRDY

Table 29. Control register 3 description

FIFO_EN	FIFO enable. Default value 0. (0: disable; 1: enable)
STOP_FTH	Enable FIFO threshold level use. Default value 0. (0: disable; 1: enable)
INT1_INACT	Inactivity interrupt on INT1. Default value 0. (0: disable; 1: enable)
INT1_IG2	Interrupt generator 2 on INT1. Default value 0. (0: disable; 1: enable)
INT1_IG1	Interrupt generator 1 on INT1. Default value 0. (0: disable; 1: enable)
INT1_OVR	FIFO overrun signal on INT1.
INT1_FTH	FIFO threshold signal on INT1.
INT1_DRDY	Data Ready signal on INT1.

8.8 CTRL4 (23h)

Control register 4 (r/w)

Table 30. Control register 4

BW2	BW1	FS1	FS0	BW_SCALE_ODR	IF_ADD_INC	I2C_DISABLE	SIM

Table 31. Control register 4 description

BW [2:1]	Anti-aliasing filter bandwidth. Default value: 00 (00: 400 Hz; 01: 200 Hz; 10: 100 Hz; 11: 50 Hz)
FS [1:0]	Full-scale selection. Default value: 00 (00: ±2 *g*; 01: Not available; 10: ±4 *g*; 11: ±8 *g*)
BW_SCALE_ODR	If '0', bandwidth is automatically selected as follows: BW = 400 Hz when ODR = 800 Hz, 50 Hz, 10 Hz; BW = 200 Hz when ODR = 400 Hz; BW = 100 Hz when ODR = 200 Hz; BW = 50 Hz when ODR = 100 Hz; If '1', bandwidth is selected according to BW [2:1] excluding ODR = 50 Hz, 10 Hz, BW = 400 Hz
IF_ADD_INC	Register address automatically incremented during multiple byte access with a serial interface (I^2C or SPI). (0: disabled; 1: enabled)
I2C_DISABLE	Disable I^2C interface. Default value: 0 (0: I^2C enabled; 1: I^2C disabled)
SIM	SPI serial interface mode selection. Default value: 0 0: 4-wire interface; 1: 3-wire interface

8.9 CTRL5 (24h)

Control register 5 (r/w)

Table 32. Control register 5

DEBUG	SOFT_RESET	DEC1	DEC0	ST2	ST1	H_LACTIVE	PP_OD

Table 33. Control register 5 description

DEBUG	Debug stepping action selected. Default value: 0 (0: disabled; 1: enabled)
SOFT_RESET	Soft reset, it acts as POR when 1, then goes to 0
DEC [1:0]	Decimation of acceleration data on OUT REG and FIFO 00 -> no decimation 01 -> update every 2 samples 10 -> update every 4 samples 11 -> update every 8 samples
ST [2:1]	Self-test enable. Default value: 00 (00: Self-test disabled; Other: see table below)
H_LACTIVE	Interrupt active high, low. Default value: 0 (0: active high; 1: active low)
PP_OD	Push-pull/Open-drain selection on interrupt pad. Default value: 0 (0: push-pull; 1: open-drain)

Table 34. Self-test mode selection

ST2	ST1	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

8.10 CTRL6 (25h)

Control register 6 (r/w)

Table 35. Control register 6

BOOT	0(1)	INT2 _BOOT	INT2 _IG2	INT2 _IG1	INT2 _EMPTY	INT2 _FTH	INT2 _DRDY

1. This bit must be set to '0' for the correct operation of the device.

Table 36. Control register 6 description

BOOT	Force reboot, cleared as soon as the reboot is finished. Active high. Default value 0.
INT2_BOOT	BOOT interrupt on INT2. Default value: 0 (0: disable; 1: enable)
INT2_IG2	Interrupt generator 2 on INT2. Default value: 0 (0: disable; 1: enable)
INT2_IG1	Interrupt generator 1 on INT2. Default value: 0 (0: disable; 1: enable)
INT2_EMPTY	FIFO empty flag on INT2. Default value: 0
INT2_FTH	FIFO threshold signal on INT2. Default value: 0
INT2_DRDY	Data Ready signal on INT2. Default value: 0

8.11 CTRL7 (26h)

Control Register 7 (r/w)

Table 37. Control register 7

0(1)	0(1)	DCRM2	DCRM1	LIR2	LIR1	4D_IG2	4D_IG1

1. This bit must be set to '0' for the correct operation of the device.

Table 38. Control register 7 description

DCRM [2:1]	DCRM is used to select the reset mode of the duration counter. Default value: 0 If DCRM = '0', the counter is reset when the interrupt is no longer active, else if DCRM = '1' the duration counter is decremented. 1LSB
LIR [2:1]	Latched Interrupt [2:1] Default value: 00 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading the *IG_SRC1 (31h)* and *IG_SRC2 (37h)* registers.
4D_IG [2:1]	Interrupt [2:1] 4D option enabled. Default value: 00 When set, *IG_CFG1 (30h)* and *IG_CFG2 (36h)* use 4D for position recognition.

8.12 STATUS (27h)

Status register (r/w)

Table 39. Status register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 40. Status register description

ZYXOR	X-, Y- and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X-, Y- and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.13 OUT_X_L (28h) - OUT_X_H (29h)

X-axis output register (r)

8.14 OUT_Y_L (2Ah) - OUT_Y_H (2Bh)

Y-axis output register (r)

8.15 OUT_Z_L (2Ch) - OUT_Z_H (2Dh)

Z-axis output register (r)

8.16 FIFO_CTRL (2Eh)

FIFO control register (r/w)

Table 41. FIFO control register

FMODE2	FMODE1	FMODE0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 42. FIFO control register description

FMODE [2:0]	FIFO mode selection bits. Default: 000. For further details refer to table below
FTH [4:0]	FIFO threshold. Default: 00000. It is the FIFO depth if the STOP_FTH bit in the *CTRL3 (22h)* register is set to '1'.

Table 43. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode. FIFO turned off
0	0	1	FIFO mode. Stops collecting data when FIFO is full.
0	1	0	Stream mode. If the FIFO is full, the new sample overwrites the older one
0	1	1	Stream mode until trigger is deasserted, then FIFO mode
1	0	0	Bypass mode until trigger is deasserted, then Stream mode
1	0	1	Not used
1	1	0	Not used
1	1	1	Bypass mode until trigger is deasserted, then FIFO mode

The FIFO trigger is the *IG_SRC1 (31h)* event. (Refer to *IG_SRC1 (31h)*).

8.17 FIFO_SRC (2Fh)

FIFO status control register (r)

Table 44. FIFO status register

FTH	OVR	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 45. FIFO status register description

FTH	FIFO threshold status. 0: FIFO filling is lower than FTH level; 1: FIFO filling is equal to or higher than threshold level
OVR	Overrun bit status. 0: FIFO is not completely filled; 1: FIFO is completely filled
EMPTY	FIFO empty bit. 0: FIFO not empty; 1: FIFO empty)
FSS [4:0]	FIFO stored data level

8.18 IG_CFG1 (30h)

Interrupt generator 1 configuration register (r/w)

Table 46. IG_CFG1 configuration register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 47. IG_CFG1 configuration register description

AOI	And/Or combination of Interrupt events. Default value: 0
6D	6-direction detection function enabled. Default value: 0
ZHIE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YLIE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XHIE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XLIE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)

8.19 IG_SRC1 (31h)

Interrupt generator 1 status register (r)

Table 48. IG1_SRC1 register

-	IA	ZH	ZL	YH	YL	XH	XL

Table 49. IG1_SRC1 register description

IA	Interrupt Active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt event has been generated)
ZH	Z High. Default value: 0 (0: no interrupt; 1: ZH event has occurred)
ZL	Z Low. Default value: 0 (0: no interrupt; 1: ZL event has occurred)
YH	Y High. Default value: 0 (0: no interrupt; 1: YH event has occurred)
YL	Y Low. Default value: 0 (0: no interrupt; 1: YL event has occurred)
XH	X High. Default value: 0 (0: no interrupt; 1: XH event has occurred)
XL	X Low. Default value: 0 (0: no interrupt; 1: XL event has occurred)

8.20 IG_THS_X1 (32h), IG_THS_Y1 (33h), IG_THS_Z1 (34h)

Interrupt generator 1 threshold registers (r/w)

Table 50. IG1_THS register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 51. IG1_THS description

THS [7:0]	Interrupt 1 thresholds. Default: 00000000

8.21 IG_DUR1 (35h)

Interrupt generator 1 duration register (r/w)

Table 52. IG_DUR1 duration

WAIT1	DUR1_6	DUR1_5	DUR1_4	DUR1_3	DUR1_2	DUR1_1	DUR1_0

Table 53. IG_DUR1 duration description

WAIT1	Wait function enable on duration counter. Default value: 0 (0: Wait function off; 1: Wait function on)
DUR1_[6:0]	Duration value Default: 0000000

8.22 IG_CFG2 (36h)

Interrupt generator 2 configuration register (r/w)

Table 54. IG_CFG2 register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 55. IG_CFG2 register description

AOI	And/Or combination of Interrupt events. Default value: 0
6D	6-direction detection function enabled. Default value: 0
ZHIE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YLIE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XHIE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XLIE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)

8.23 IG_SRC2 (37h)

Interrupt generator 2 status register (r)

Table 56. IG_SRC2 register

-	IA	ZH	ZL	YH	YL	XH	XL

Table 57. IG_SRC2 register description

IA	Interrupt Active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events has been generated)
ZH	Z High. Default value: 0 (0: no interrupt; 1: ZH event has occurred)
ZL	Z Low. Default value: 0 (0: no interrupt; 1: ZL event has occurred)
YH	Y High. Default value: 0 (0: no interrupt; 1: YH event has occurred)
YL	Y Low. Default value: 0 (0: no interrupt; 1: YL event has occurred)
XH	X High. Default value: 0 (0: no interrupt; 1: XH event has occurred)
XL	X Low. Default value: 0 (0: no interrupt; 1: XL event has occurred)

8.24 IG_THS2 (38h)

Interrupt generator 2 threshold register (r/w)

Table 58. IG_THS2 register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 59. IG_THS2 register description

THS [7:0]	Interrupt generator 2 thresholds. Default 00000000

8.25 IG_DUR2 (39h)

Interrupt generator 2 duration register (r/w)

Table 60. IG_DUR2 register

WAIT2	DUR2_6	DUR2_5	DUR2_4	DUR2_3	DUR2_2	DUR2_1	DUR2_0

Table 61. IG_DUR2 register description

WAIT2	Wait function enable on duration counter. Default value: 0 (0: Wait function off; 1: Wait function on)
DUR2_[6:0]	Duration value. Default: 0000000

8.26 XL_REFERENCE (3Ah), XH_REFERENCE (3Bh)

In normal mode (HPM [1:0] = ‘00’ or ‘10’) when one of these registers (XL_REFERENCE or XH_REFERENCE) is read, the x output of the hp filter is set to ‘0’.

In reference mode (HPM [1:0] =”01”) the reference value is subtracted from the X output of the hp filter.

8.27 YL_REFERENCE (3Ch), YH_REFERENCE (3Dh)

See previous section concerning the X Reference (r/w) registers.

8.28 ZL_REFERENCE (3Eh), ZH_REFERENCE (3Fh)

See previous section concerning the X Reference (r/w) registers.

9 Package information

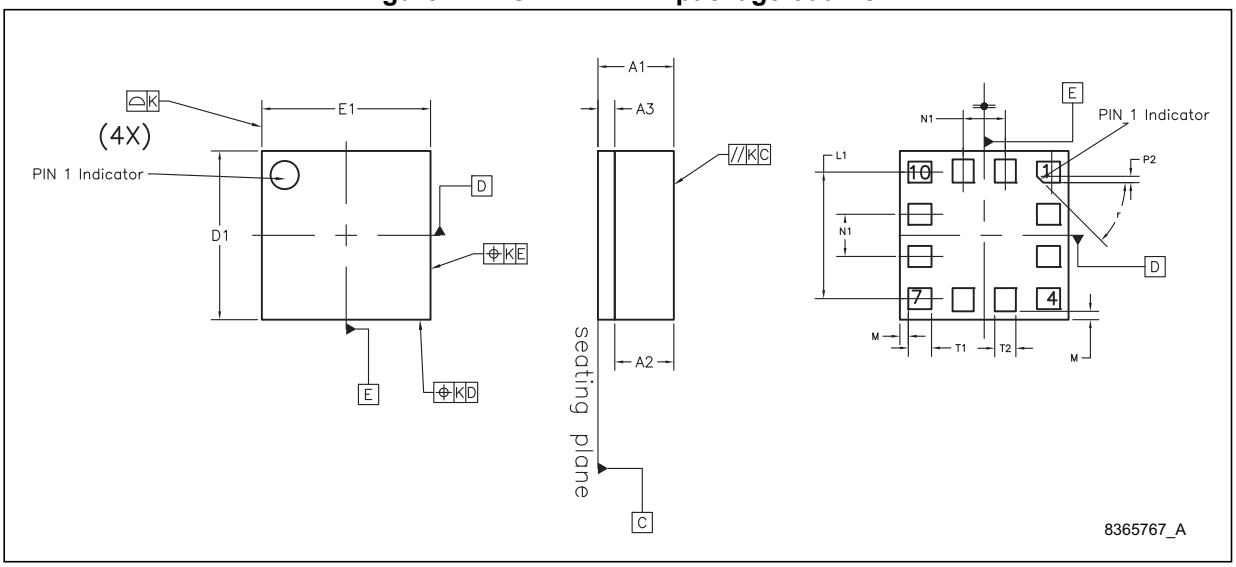
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

9.1 LGA-12 package information

Table 62. LGA-12 2x2x1 package mechanical data

Ref.	Min.	Typ.	Max.
A1			1
A2		0.785	
A3		0.200	
D1	1.850	2.000	2.150
E1	1.850	2.000	2.150
L1		1.500	
N1		0.500	
T1		0.275	
T2		0.250	
P2		0.075	
r		45°	
M		0.100	
K		0.050	

Figure 14. LGA-12 2x2x1 package outline



9.2 LGA-12 packing information

Figure 15. Carrier tape information for LGA-12 package

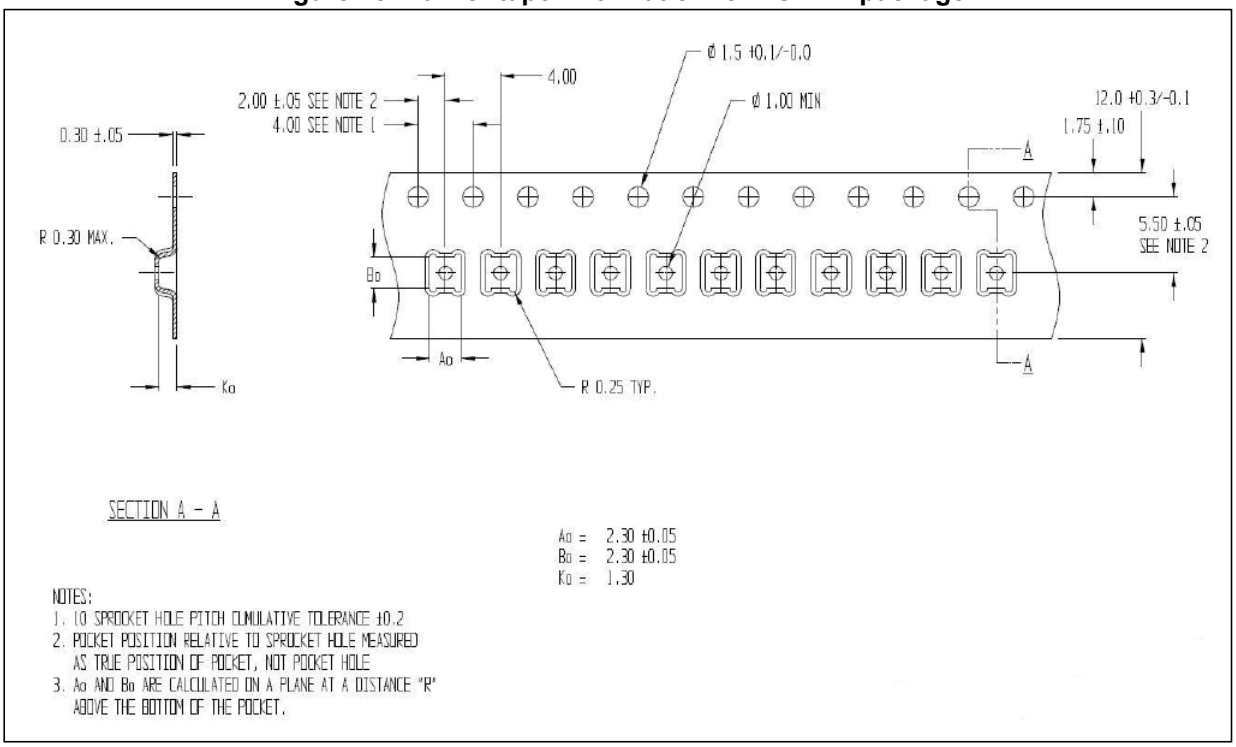


Figure 16. LGA-12 package orientation in carrier tape

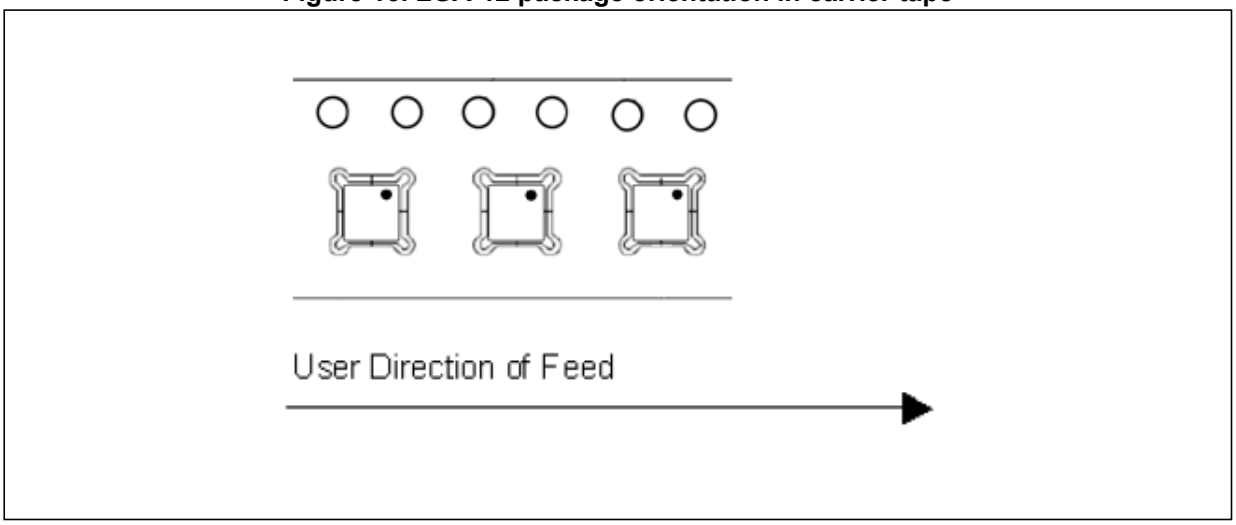


Figure 17. Reel information for carrier tape of LGA-12 package

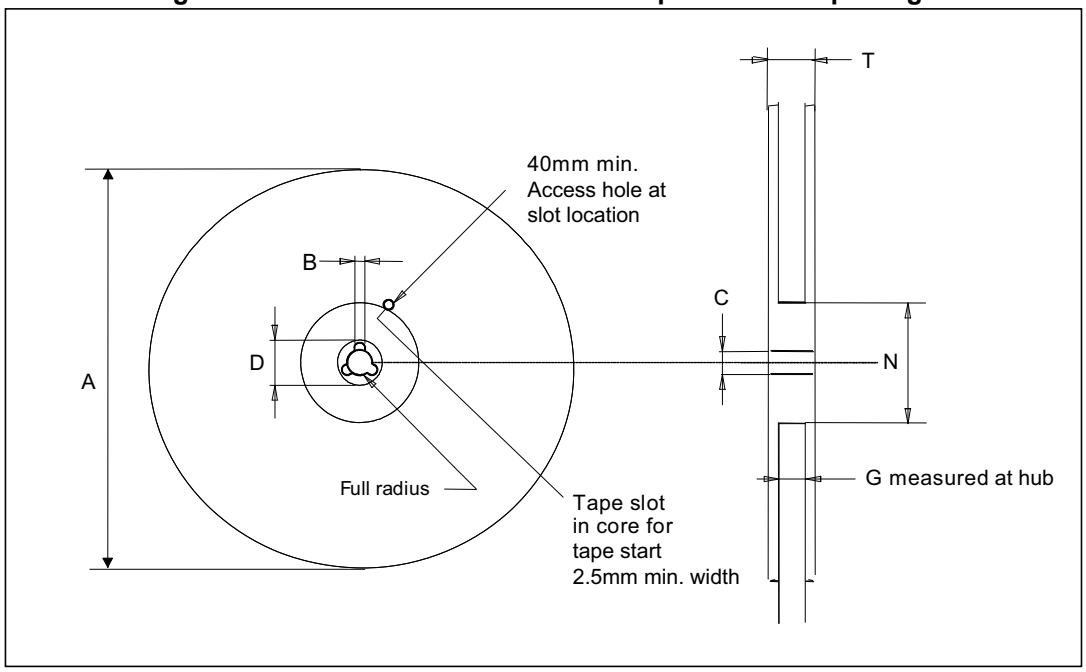


Table 63. Reel dimensions for carrier tape of LGA-12 package

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

10 Revision history

Table 64. Document revision history

Date	Revision	Changes
26-Nov-2013	1	Initial release
27-Nov-2013	2	General document review
24-Sep-2014	3	Document status promoted from preliminary to production data Updated *Figure 2: Pin connections* and *Figure 5: LIS2HH12 electrical connections* Added *Table 9: Activity/Inactivity function control registers*
09-Nov-2015	4	Added *Section 9.2: LGA-12 packing information*
14-Dec-2015	5	Updated HPIS1 and HPIS2 bits in *CTRL2 (21h)* Updated *Table 8: Absolute maximum ratings* Updated *Figure 17: Reel information for carrier tape of LGA-12 package*