ATSAMR30M18A

SAMR30 IEEE® 802.15.4™ Sub-1GHz Module Data Sheet

Introduction

The ATSAMR30M18A is an IEEE® 802.15.4™-2003/2006/2011-compliant RF module for the sub-1 GHz ISM bands, such as 868 MHz (Europe) and 915 MHz (North America), optimized for low-power applications. This module combines the ATSAMR30E18A SiP (System in Package), 16 MHz crystal oscillator, discrete balun, lumped element harmonic reject filter and required RF shielding in a compact 12.7 mm x 11.0 mm design. The module as implemented on the Xplained Pro development board has passed regulatory approvals with chip antenna or SMA connectorized monopole antenna.

This data sheet provides only a brief overview of the necessary sections of the module. For a detailed description of each peripheral, refer to the ATSAMR30E18A Data Sheet.

Features

- Processor
  - ARM® Cortex®-M0+ CPU running at up to 48 MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer (MTB)
- Memories
  - 256 KB in-system self-programmable Flash
  - 32 KB SRAM
  - 8 KB low-power RAM
- System
  - Power-on Reset (POR) and Brown-out Detection (BOD)
  - Internal clock option with 48 MHz Digital Frequency Locked Loop (DFLL48M) and 48 MHz to 96 MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - Up to 14 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle and Standby Sleep modes
  - Sleep walking peripherals
- Integrated Ultra-Low Power Transceiver for 800/900 MHz ISM Band:
  - European SRD band from 863 to 870 MHz
  - North American ISM band from 902 to 928 MHz
- Direct Sequence Spread Spectrum with Different Modulation and Data Rates:
  - BPSK with 20 and 40 kb/s, compliant to IEEE 802.15.4-2003/2006/2011
  - O-QPSK with 100 and 250 kb/s, compliant to IEEE 802.15.4-2006/2011
  - O-QPSK with 200, 400, 500 and 1000 kb/s PSDU data rate
  - Industry-leading link budget:
    - RX sensitivity up to -105 dBm

    - TX output power up to +8.7 dBm
  - Hardware-assisted MAC:
    - Auto-Acknowledge
    - Auto-Retry
    - CSMA-CA and Listen Before Talk (LBT)
    - Automatic address filtering and automated FCS check
  - Special 802.15.4-2011 hardware support:
    - FCS computation and Clear Channel Assessment
    - RSSI measurement, Energy Detection and Link Quality Indication
  - 128 Byte TX/RX Frame Buffer
  - Integrated 16 MHz Crystal Oscillator (external crystal is not needed)
  - Fully integrated, fast settling transceiver PLL to support frequency hopping
  - Hardware Security (AES, True Random Generator)
- Peripherals
  - 16-channel Direct Memory Access Controller (DMAC)
  - 12-channel event system
  - Up to three 16-bit Timer/Counters (TC), including one low-power TC(TC4), each configurable as:
    - 16-bit TC with two compare/capture channels
    - 8-bit TC with two compare/capture channels
    - 32-bit TC with two compare/capture channels, by using two TCs
  - Two 24-bit and one 16-bit Timer/Counters for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5-bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12 Mbps) Universal Serial Bus (USB) 2.0 interface
    - Embedded host and device function
    - Eight endpoints
  - Up to two Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex or single-wire half-duplex configuration
    - I^2C up to 3.4 MHz
    - SPI
    - LIN Client
  - Up to three Serial Communication Interfaces (SERCOM) including one low-power SERCOM (SERCOM5), each configurable to operate as UART with internal clock
  - One Configurable Custom Logic (CCL)
  - One 12-bit, 350 ksps Analog-to-Digital Converter (ADC) with up to four external channels
    - Differential and single-ended input
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - 12-Channel capacitive touch and proximity sensing
- Clock
  - High precision 16 MHz integrated internal crystal
  - 32.768 kHz internal oscillator (OSC32K)

  - 32.768 kHz ultra-low power internal oscillator (OSCULP32K)
  - 16/12/8/4 MHz high-accuracy internal oscillator (OSC16M)
  - 48 MHz Digital Frequency Locked Loop (DFLL48M)
  - 96 MHz Fractional Digital Phased Locked Loop (FDPLL96M)
- I/O and Package
  - 16 programmable I/O pins
  - 25-pin module package (12.7 mm x 11.0 mm) with castellated PCB pads
- Operating Voltage
  - 1.8V – 3.6V
- Temperature Range
  - -40°C to 85°C Industrial
- Power Consumption(1)
  - RX_ON = 10.79 mA
  - BUSY_TX = 26.97 mA
  - Standby = 2.03 µA
  - Backup mode = 0.77 µA

Note:

1. For more details, see 9.3.4. Current Consumption Specifications.

Table of Contents

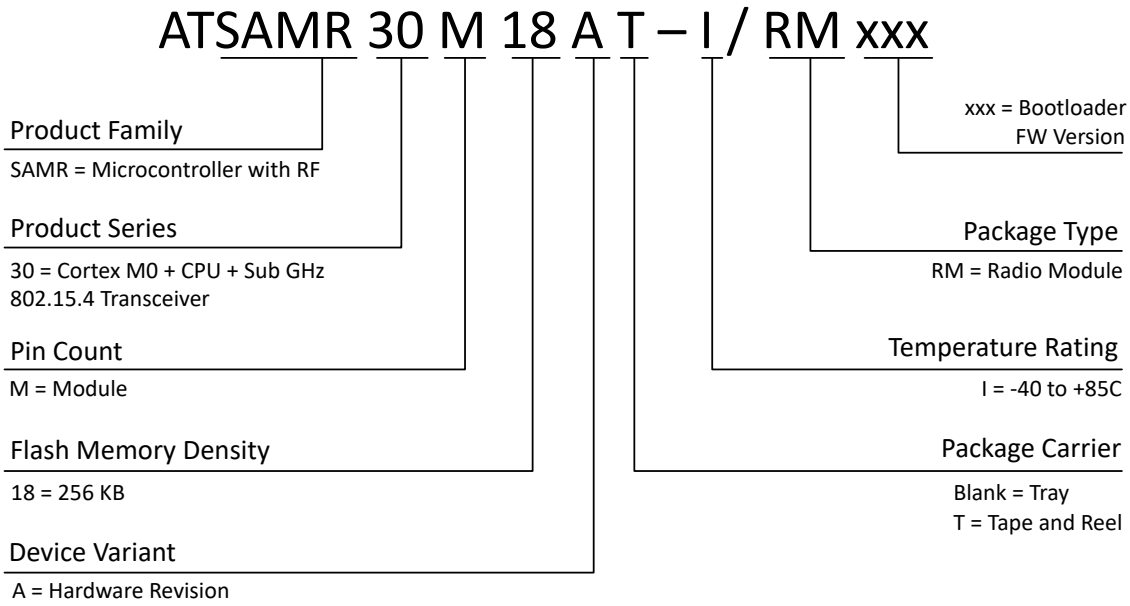
1. Ordering Information and Module Marking

The following table provides the ordering details for the ATSAMR30M18A module.

Table 1-1. Ordering Information for ATSAMR30M18A

Model Number	Ordering Code	Package Dimension	Number of Pins	Description	Regulatory Approval
ATSAMR30M18A	ATSAMR30M18A-I/RMxxx	12.7mm x 11mm x 2.71mm	25	SAM R30 Module in Tray package	FCC, ISED, CE
	ATSAMR30M18AT-I/RMxxx			SAM R30 Module in Tape and Reel package	

Figure 1-1. Module Ordering Code Information



2. Package Information

The following table provides the ATSAMR30M18A module package dimensions.

Table 2-1. ATSAMR30M18A Package Information

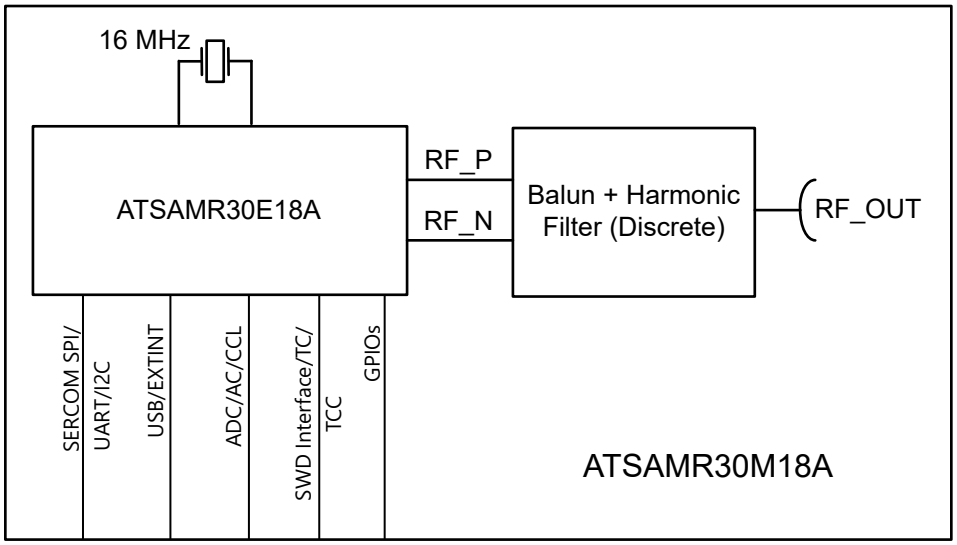
Parameter	Value	Units
Package size	12.7 x 11.0	mm
Pad count	25	—
Total thickness	2.71	mm
Pad pitch	1.2	mm
Pad width	0.8	mm

3. Module Block Diagram

The ATSAMR30M18A module contains ATSAMR30E18A SiP, 16 MHz crystal, discrete Balun and lumped element Harmonic Filter.

The following figure shows the block diagram of the ATSAMR30M18A module.

Figure 3-1. Module Block Diagram



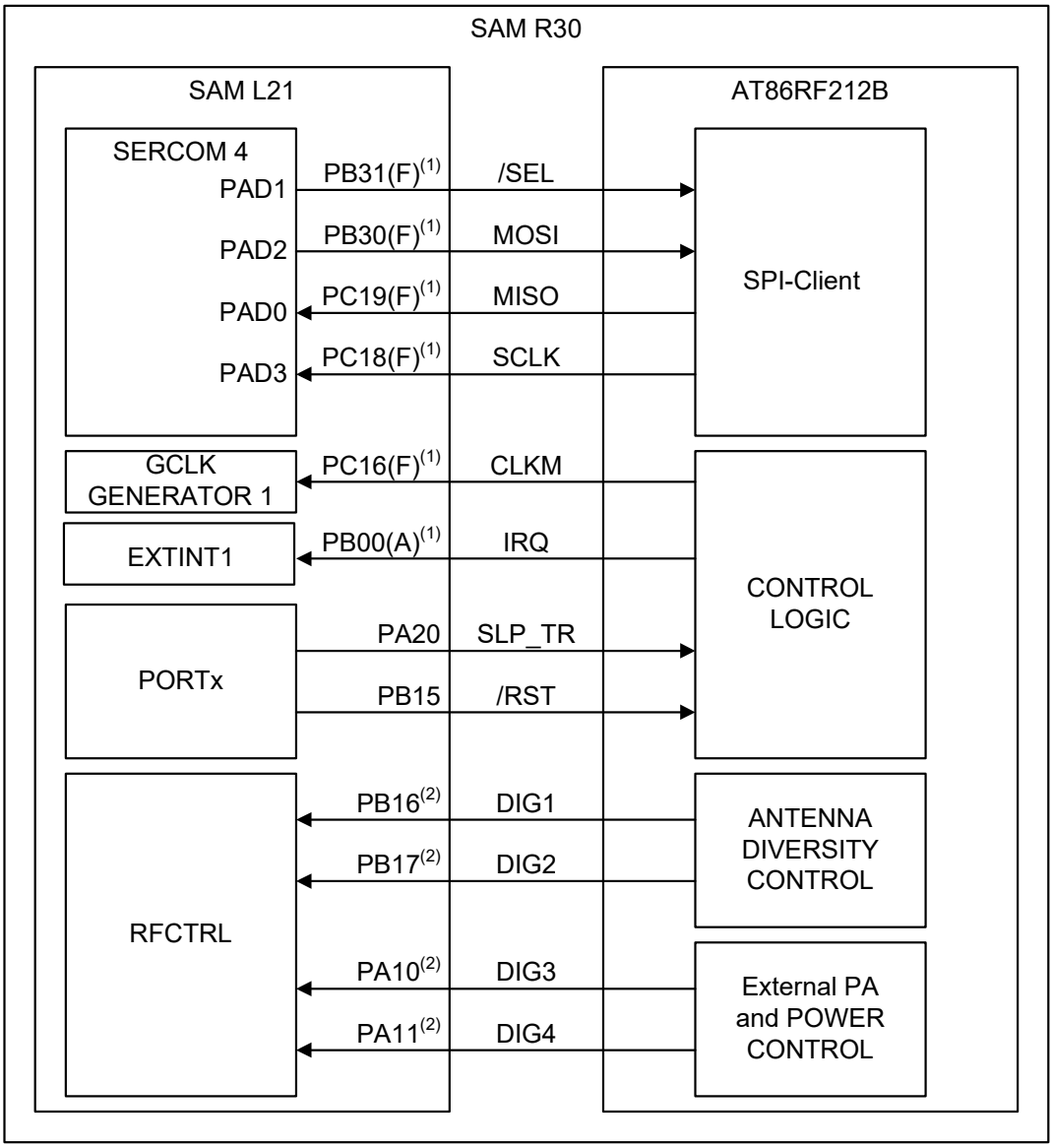
The ATSAMR30E18A SIP consists of two vertically integrated silicon dies:

- SAM L21 ARM Cortex M0+ based microcontroller
- AT86RF212B low-power, low-voltage 700/800/900 MHz transceiver
  The local communication and control interface is wired within the package. Key I/O external signals are exposed as I/O pins.

3.1 Interconnection between SAM L21 and AT86RF212B within ATSAMR30E18A SiP

This section describes the interconnection between SAM L21 and AT86RF212B. The interface comprises a client SPI and additional control signals. This interface is a host SPI interface in SAM L21 as shown in the following figure.

Figure 3-2. Interconnection between SAM L21 and AT86RF212B



1. Alternate pin function and direction has to be configured by software.
2. Pin function is configured by hardware automatically after reset.

The SPI is used for register, Frame Buffer, SRAM and AES access. The additional control signals are connected to the GPIO/IRQ interface of the microcontroller. The following table introduces the radio transceiver I/O signals and their functionality.

Table 3-1. Microcontroller Interface Signal Description

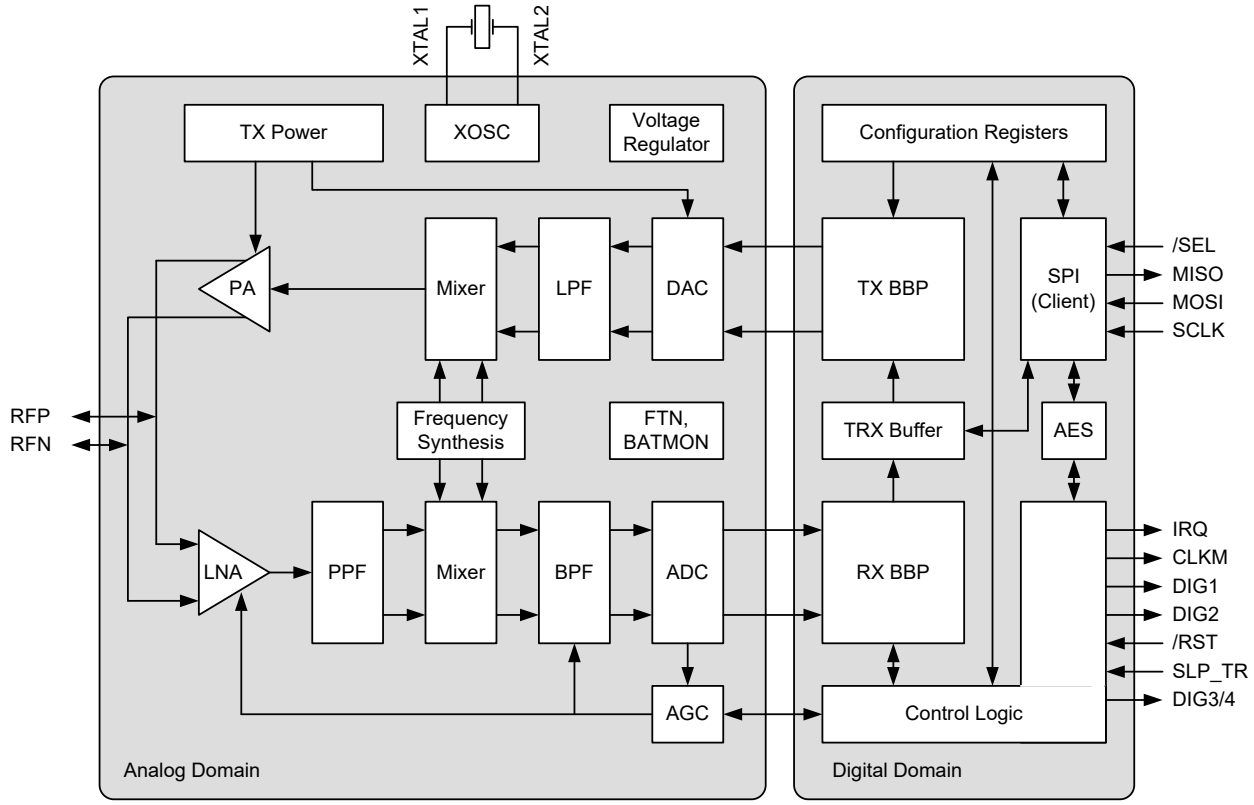
Signal	Description
/SEL	SPI select signal, active-low
MOSI	SPI data (host output client input) signal
MISO	SPI data (host input client output) signal
SCLK	SPI clock signal

.....continued	
Signal	**Description**
CLKM	Optional, clock output, usable as: • Microcontroller clock source and/or MAC timer reference • High precision timing reference
IRQ	Interrupt request signal, further used as: • Frame Buffer Empty indicator
SLP_TR	Multi-purpose control signal (functionality is state dependent): • Sleep/Wake up: enable/disable SLEEP state • TX start: BUSY_TX_(ARET) state • Disable/enable CLKM
/RST	AT86RF212B Reset signal; active-low
DIG2	Optional: • IRQ_2 (RX_START) for RX Frame Time Stamping

3.2 AT86RF212B Transceiver Circuit Description

The AT86RF212B single-chip radio transceiver provides a complete radio transceiver interface between radio frequency signals and the baseband microcontroller. It comprises a bidirectional analog RF front end, direct-conversion mixers, low-noise fractional-n PLL, quadrature digitizer, DSP modem and baseband packet-handler optimized for IEEE 802.15.4 MAC/PHY automation and low power. An SPI accessible 128-byte TRX buffer stores receive or transmit data. Radio communication between transmitter and receiver is based on DSSS Spread Spectrum with OQPSK or BPSK modulation schemes as defined by the IEEE 802.15.4 standard. Additional proprietary modulation modes include high-data rate payload encoding and wideband BPSK-40-ALT.

Figure 3-3. AT86RF212B Block Diagram



The number of required external components is minimal. The basic requirements are an antenna, a balun, harmonic filter, crystal oscillator and bypass capacitors. The RF Ports are bidirectional differential signals that do not require external TX/RX switches. Hardware control signals are automatically generated for TX/RX arbitration of high-powered PA/LNA front ends and transmitter diversity for systems with dual antennas.

The AT86RF212B supports the IEEE 802.15.4-2006 [2] standard mandatory BPSK modulation and optional O-QPSK modulation in the 868.3 MHz and 915 MHz bands. For applications not targeting IEEE compliant networks, the radio transceiver supports proprietary High Data Rate Modes based on O-QPSK. Additionally, the AT86RF212B provides BPSK-40-ALT wideband BPSK mode for compliance with FCC rule 15.247 and backward compatibility with legacy BPSK networks.

The AT86RF212B features hardware-supported 128-bit security operation. The standalone AES encryption/decryption engine can be accessed in parallel to all PHY operational modes. Configuration of the AT86RF212B, reading and writing of data memory, as well as the AES hardware engine are controlled by the SPI interface and additional control signals.

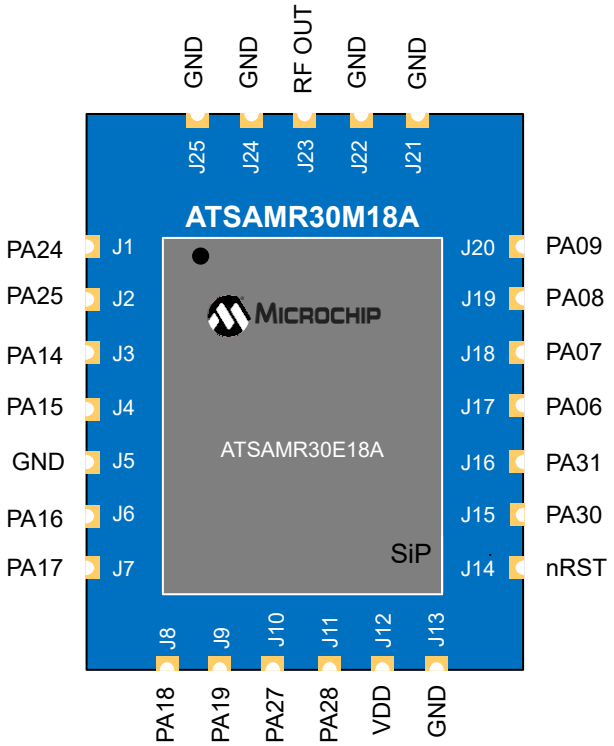
On-chip low-dropout linear regulators provide clean 1.8 V_{DC} power for critical analog and digital sub-systems. To conserve power, these rails are automatically sequenced by the transceiver's state machine. This feature greatly improves EMC in the RF domain and reduces external power supply complexity to the simple addition of frequency compensation capacitors on the AVDD and DVDD pins.

Additional features of the Extended Feature Set are provided to simplify the interaction between the radio transceiver and microcontroller.

4. Pinout Information

The ATSAMR30M18A module pin assignment is shown in the following figure.

Figure 4-1. ATSAMR30M18A Module Pin Assignment



The module pin assignment is shown in the following table. The **SiP pin** column is a reference to the ATSAMR30E18 datasheet (ATSAMR30E18A).

Table 4-1. ATSAMR30M18A Module Pin Assignment

Module			SAMR30E	
Pin No.	Pin Name	Possible Peripheral Function(1)	SiP Pin	Pin Description
J1	PA24	UART5_Tx	22	EXTINT[12], SERCOM3 or 5/PAD[2], TC1/WO[0], TCC1/WO[2], USB/DM, CCL2/IN[2]
J2	PA25	UART5_Rx	23	EXTINT[13], SERCOM3 or 5/PAD[3], TC1/WO[1], TCC1/WO[3], USB/DP, CCL2/OUT

.....continued

Module			SAMR30E	
Pin No.	Pin Name	Possible Peripheral Function(1)	SiP Pin	Pin Description
J3	PA14	UART2_Tx	15	EXTINT[14], SERCOM2/PAD[2], TC4/WO[0], TCC0/WO[4], GCLK/IO[0]
J4	PA15	UART2_Rx	16	EXTINT[15], SERCOM2/PAD[3], TC4/WO[1], TCC0/WO[5], GCLK/IO[1]
J5	GND	—	3, 6, 11, 14, 28	Ground
J6	PA16(2)	SPI1_MISO	17	EXTINT[0], PTC_X[4], SERCOM1 or 3/PAD[0], TCC2/WO[0], TCC0/WO[6], GCLK/IO[2], CCL0/IN[0]
J7	PA17(2)	SPI1_SS	18	EXTINT[1], PTC_X[5], SERCOM1 or 3/PAD[1], TCC2/WO[1], TCC0/WO[7], GCLK/IO[3], CCL0/IN[1]
J8	PA18	SPI1_MOSI	19	EXTINT[2], PTC_X[6], SERCOM1 or 3/PAD[2], TC4/WO[0], TCC0/WO[2], AC/CMP[0], CCL0/IN[2]
J9	PA19	SPI1_SCK	20	EXTINT[3], PTC_X[7], SERCOM1 or 3/PAD[3], TC4/WO[1], TCC0/WO[3], AC/CMP[1], CCL0/OUT
J10	PA27	GPIO	25	EXTINT[15], GCLK/IO[0]
J11	PA28	GPIO	27	EXTINT[8], GCLK/IO[0]
J12	VDD	—	4, 24, 30	Power (VDDANA, VDDIO, VDDIN)
J13	GND	GND	3, 6, 11, 14, 28	Ground
J14	RESET#	nRST	26	CPU Reset
J15	PA30	SWCLK	31	EXTINT[10], SERCOM1/PAD[2], TCC1/WO[0], CM0P/SWCLK, GCLK/IO[0], CCL1/IN[0]

.....continued

Module			SAMR30E	
Pin No.	Pin Name	Possible Peripheral Function(1)	SiP Pin	Pin Description
J16	PA31	SWDIO	32	EXTINT[11], SERCOM1/PAD[3], TCC1/WO[1], SWDIO(3), CCL1/OUT
J17	PA06	AIN[6]	7	EXTINT[6], EXTWAKE[6], AC_AIN[2], ADC_AIN[6], PTC_Y[4], SERCOM0/PAD[2], TCC1/WO[0], CCL0/IN[2]
J18	PA07	GPIO	8	EXTINT[7], EXTWAKE[7], AC_AIN[3], ADC_AIN[7], SERCOM0/PAD[3], TCC1/WO[1], CCL0/OUT
J19	PA08(2)	I2C2_SDA	9	NMI, ADC_AIN[16], PTC_X[0] or Y[6], SERCOM0 or 2/PAD[0], TCC0/WO[0], TCC1/WO[2], CCL1/IN[0]
J20	PA09(2)	I2C2_SCL	10	EXTINT[9], ADC_AIN[17], PTC_X[1] or Y[7], SERCOM0 or 2/PAD[1], TCC0/WO[1], TCC1/WO[3], CCL1/IN[1]
J21	GND	—	3, 6, 11, 14, 28	Ground
J22	GND	—	3, 6, 11, 14, 28	Ground
J23	RF OUT	RFP, RFN	12,13	50 ohm single-ended RF Output
J24	GND	—	3, 6, 11, 14, 28	Ground
J25	GND	—	3, 6, 11, 14, 28	Ground

Notes:

1. The peripheral function indicated in this column is based on the reference design. This is one of the possibilities as each ATSAMR30E18A pin supports several multiplexed peripheral functions mentioned in the Pin description column.
2. Only these pins can be used for the SERCOM I2C mode: PA08, PA09, PA16 and PA17.
3. This function is only activated in the presence of a debugger.

5. Nonvolatile Memory Information

The ATSAMR30M18A provides the user a readable Nonvolatile Memory (NVM) space called user row, programmed in the factory. The base address for the application is 0x804008. The following table shows the implemented data structure.

Table 5-1. NVM (User Row) Data

Address Offset	Field Name	Field Description	Length
BaseAddr. + 0x00	MIB_REVISION	Data structure revision. 0x1501	2 bytes
+0x02	MAC_IEEE_ADDRESS	Module specific IEEE MAC Address	8 bytes
+0x0A	BOARD_SERIAL	Module specific serial number	10 bytes
+0x14	PART_NO	Product specific part number	8 bytes
+0x1C	PCBA_REV	Product PCB/assembly revision	1 byte
+0x1D	XTAL_TRIM	Reference crystal calibration value	1 byte
+0x1E	CRC16	Checksum for this data structure	2 bytes

BOARD_SERIAL and PART_NO for this ATSAMR30M18A will be programmed with 0xFF. The end user application software must copy two data fields to radio transceiver registers. The data in MAC_IEEE_ADDRESS must be copied to the registers IEEE_ADDR_0 to IEEE_ADDR_7 of AT86RF212B. The MAC_IEEE_ADDRESS is stored little-endian with the first byte stored at the lowest address.

The XTAL_TRIM value is determined during the production test and must be copied to the transceiver XTAL_TRIM bits of XOSC_CTRL register (AT86RF212B). For more information on registers, see the SAM R30 Datasheet. Programming the XTAL_TRIM value reduces the absolute deviation for the 16 MHz reference crystal. CRC16 is calculated using CRC-CCITT with the polynomial $x^{16} + x^{12} + x^5 + 1$ and initial value as 0xFFFF.

6. Boot Loader

The module is delivered with a pre-flashed boot loader. The bootloader memory section (8 kB) is write-protected at factory. To overwrite the write-protection, program the BOOTPROT bits[2:0] of NVM User Row with the default value of 0x7.

Customers not using the bootloader must program the BOOTPROT bits to default value to program the complete Flash of the SAMR30 device. For detailed information, refer to the boot loader manual. The related information is available in the AVR2054 Application Note.

7. Module Description

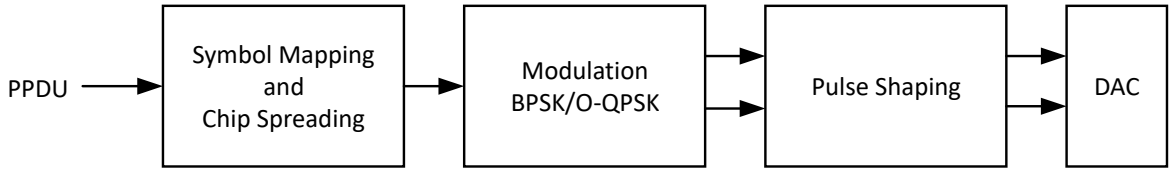
This section provides an overview of the major features of AT86RF212B. For detailed information, refer to Reference guide - AT86RF212B section of the SAM R30 datasheet.

7.1 Physical Layer Modes

7.1.1 Spreading, Modulation and Pulse Shaping

The AT86RF212B supports various physical layer (PHY) modes independent of the RF channel selection. Symbol mapping along with chip spreading, modulation and pulse shaping are a part of the digital baseband processor as shown in the following figure.

Figure 7-1. Base Band Transmitter Architecture



The combination of spreading, modulation and pulse shaping are restricted to several combinations, as shown in the following table.

The AT86RF212B is fully compliant to the IEEE 802.15.4 low data rate modes of 20 kb/s or 40 kb/s, employing binary phase-shift keying (BPSK) and spreading with a fixed chip rate of 300 kchip/s or 600 kchip/s, respectively. The symbol rate is 20 ksymbol/s or 40 ksymbol/s, respectively. In both cases, pulse shaping is approximating a raised cosine filter with roll-off factor 1.0 (RC-1.0).

For optional data rates according to IEEE 802.15.4-2006, offset quadrature phase-shift keying (O-QPSK) is supported by the AT86RF212B with a fixed chip rate of either 400 kchip/s or 1000 kchip/s.

At a chip rate of 400 kchip/s, there is a choice between two different Pulse Shaping modes. One Pulse Shaping mode uses a combination of both half-sine shaping (SIN) and raised cosine filtering with roll-off factor 0.2 (RC-0.2) according to IEEE 802.15.4-2006 [2] for the 868.3 MHz band. The other uses raised cosine filtering with roll-off factor 0.2 (RC-0.2).

At a chip rate of 1000 kchip/s, pulse shaping is either half-sine filtering (SIN), as specified in IEEE 802.15.4-2006 [2], or, alternatively, raised cosine filtering with roll-off factor 0.8 (RC-0.8), as specified in IEEE 802.15.4c™-2009 [3] and IEEE 802.15.4-2011 [4].

For O-QPSK, the AT86RF212B supports spreading according to IEEE 802.15.4-2006 with data rates of either 100 kb/s or 250 kb/s depending on the chip rate, leading to a symbol rate of either 25 ksymbol/s or 62.5 ksymbol/s, respectively.

Additionally, the AT86RF212B supports two more spreading codes for O-QPSK with shortened code lengths. This leads to higher but non-IEEE 802.15.4-compliant data rates for PSDU transmission at 200, 400, 500 and 1000 kb/s.

Table 7-1. Modulation and Pulse Shaping

Modulation	Chip Rate [kchip/s]	Supported Data Rate for PPDU Header [kb/s]	Supported Data Rates for PSDU [kb/s]	Pulse Shaping
BPSK	300	20	20	RC-1.0
	600	40	40(1)	RC-1.0

.....continued				
Modulation	**Chip Rate [kchip/s]**	**Supported Data Rate for PPDU Header [kb/s]**	**Supported Data Rates for PSDU [kb/s]**	**Pulse Shaping**
O-QPSK	400	100	100, 200, 400	SIN and RC-0.2
	400	100	100, 200, 400	RC-0.2
	1000	250	250, 500(1), 1000	SIN
	1000	250	250, 500(1), 1000	RC-0.8

1. Support of two different spreading codes.

7.1.2 Recommended PHY Modulation Modes for Different Frequency Bands

The following are the recommended PHY modes for North American band:

- BPSK-40
- BPSK-40-ALT
- OQPSK-SIN-250/500/1000

The following are the recommended PHY modes for European band:

- BPSK-20
- OQPSK-SIN-RC-100/200/400
- OQPSK-RC-100/200/400

7.1.3 Configuration

The PHY mode can be selected by setting the appropriate BPSK_OQPSK, SUB_MODE, OQPSK_DATA_RATE and ALT_SPECTRUM bits in the TRX_CTRL_2. During configuration, the transceiver needs to be in TRX_OFF state.

7.1.4 Symbol Period

Within IEEE 802.15.4 and, accordingly, within this document, time references are often specified in units of symbol periods, leading to a PHY mode independent description. The table below shows the duration of the symbol period.

Table 7-2. Duration of the Symbol Period

Modulation	PSDU Data Rate [kb/s]	Duration of Symbol Period [µs]
BPSK	20	50
	40	25
O-QPSK	100, 200, 400	40
	250, 500, 1000	16

1. For the proprietary High Data Rate Modes, the symbol period is (by definition) the same as the symbol period of the corresponding base mode.

7.1.5 Proprietary High Data Rate Modes

The main features are:

- High data rates up to 1000 kb/s
- Support of Basic and Extended Operating Mode
- Reduced ACK timing (optional)

7.1.5.1 Overview

The AT86RF212B supports alternative data rates of 200, 400, 500 and 1000 kb/s for applications not necessarily targeting IEEE 802.15.4 compliant networks.

The High Data Rate Modes utilize the same RF channel bandwidth as the IEEE 802.15.4-2006 sub-1 GHz O-QPSK modes. Higher data rates are achieved by using the modified O-QPSK spreading codes having reduced code lengths. The lengths are reduced by the factor of two or by the factor of four.

For O-QPSK with 400 kchip/s, this leads to a data rate of 200 kb/s (2-fold) and 400 kb/s (4-fold), respectively.

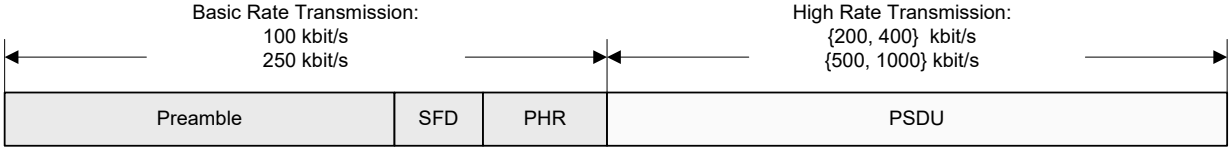
For O-QPSK with 1000 kchip/s, the resulting data rate is 500 kb/s (2-fold) and 1000 kb/s (4-fold), respectively.

Due to the decreased spreading factor, the sensitivity of the receiver is reduced. The P_{SENS} parameter in the *Receiver Characteristics* shows typical values of the sensitivity for different data rates.

7.1.5.2 High Data Rate Frame Structure

In order to allow robust frame synchronization, the AT86RF212B high data rate modulation is restricted to the PSDU part only. The PPDU header (the preamble, the SFD and the PHR field) are transmitted with a rate of either 100 kb/s or 250 kb/s (basic rates).

Figure 7-2. High Date Rate Frame Structure



Due to the overhead caused by the PPDU header and the FCS, the effective data rate is less than the selected data rate, depending on the length of the PSDU.

Consequently, high data rate transmission is useful for large PSDU lengths due to the higher effective data rate, or in order to reduce the power consumption of the system.

7.1.5.3 High Data Rate Mode Options

Reduced Acknowledgment Time

If the AACK_ACK_TIME bit in the XAM_CTRL_1 register (XAH_CTRL_1.AACK_ACK_TIME) is set, the acknowledgment time is reduced to the duration of two symbol periods for 200 and 400 kb/s data rates, and to three symbol periods for 500 and 1000 kb/s data rates. The reduced acknowledgment time is untouched in IEEE 802.15.4. Otherwise, it defaults to 12 symbol periods according to IEEE 802.15.4.

Receiver Sensitivity Control

The different data rates between PPDU header (SHR and PHR) and PHY payload (PSDU) cause a different sensitivity between header and payload. This can be adjusted by defining sensitivity threshold levels of the receiver. With a sensitivity threshold level set, the AT86RF212B does not synchronize to frames with an RSSI level below that threshold. The sensitivity threshold is configured by the RX_PDT_LEVEL bits in the RX_SYN register (RX_SYN.RX_PDT_LEVEL).

Scrambler

For data rates 400 kb/s and 1000 kb/s, additional chip scrambling is applied default in order to mitigate data dependent spectral properties. Scrambling can be disabled if the OQPSK_SCRAM_EN bit in the TRX_CTRL_2 register (TRX_CTRL_2.OQPSK_SCRAM_EN) is set to '0'.

Energy Detection

The Energy Detection (ED) measurement time span is eight symbol periods according to IEEE 802.15.4. For frames operated at a higher data rate, the automated measurement duration is reduced to two symbol periods taking reduced frame durations into account. This means, the ED measurement time is 80 µs for modes 200 kb/s and 400 kb/s, and 32 µs for modes 500 kb/s and 1000 kb/s. For manually initiated ED measurements in these modes, the measurement time is still eight-symbol periods.

Carrier Sense

For clear channel assessment, IEEE 802.15.4-2006 specifies several modes which may either apply "energy above threshold" or "carrier sense" (CS) or a combination of both. Since signals of the High Data Rate Modes are not compliant to IEEE 802.15.4-2006, CS is not supported when the AT86RF212B is operating in these modes. However, "energy above threshold" is supported.

Link Quality Indicator (LQI)

For the High Data Rate Modes, the link quality value does not contain useful information; therefore, discarding it is recommended.

7.2 Receiver (RX)

7.2.1 Overview

The AT86RF212B transceiver is split into an analog radio front-end and a digital domain. Referring to the receiver part of the analog domain, the differential RF signal is amplified by a low noise amplifier (LNA) and split into quadrature signals by a poly-phase filter (PPF). Two mixer circuits convert the quadrature signal down to an intermediate frequency. Channel selectivity is achieved by an integrated band-pass filter (BPF). The subsequent analog-to-digital converter (ADC) samples the receive signal and additionally generates a digital RSSI signal. The ADC output is then further processed by the digital baseband receiver (RX BBP), which is part of the digital domain.

The BBP performs further filtering and signal processing. In RX_ON state, the receiver searches for the synchronization header. Once the synchronization is established and the SFD is found, the received signal is demodulated and provided to the Frame Buffer. Upon synchronization the receiver performs a state change from RX_ON to BUSY_RX, which is indicated by the TRX_STATUS bits in the TRX_STATUS register (TRX_STATUS.TRX_STATUS). Once the frame is received, the receiver switches back to RX_ON in the listen mode on the selected channel. A similar scheme applies to the Extended Operating Mode.

The receiver is designed to handle reference oscillator accuracies up to ±60ppm; refer to the f_{SRD} parameter in the *General RF Specifications* section. This results in the estimation and correction of frequency and symbol rate errors up to ±120 ppm.

Several status information are generated during the receive process: LQI, ED and RX_STATUS. They are automatically appended during Frame Read Access. Some information is also available through register access, for example the PHY_ED_LEVEL.ED_LEVEL and FCS correctness with the PHY_RSSI.RX_CRC_VALID.

The Extended Operating Mode of the AT86RF212B supports frame filtering and pending data indication.

7.2.2 Frame Receive Procedure

The frame receive procedure, including the radio transceiver setup for reception and reading PSDU data from the Frame Buffer, is described in the *Frame Receive Procedure* section.

7.2.3 Configuration

In Basic Operating Mode, the receiver is enabled by writing command RX_ON to the TRX_CMD bits in the TRX_STATE register (TRX_STATE.TRX_CMD) in states TRX_OFF or PLL_ON. In Extended Operating Mode, the receiver is enabled for RX_AACK operation from state PLL_ON by writing the command RX_AACK_ON.

There is no additional configuration required to receive IEEE 802.15.4 compliant frames in Basic Operating Mode. However, the frame reception in the AT86RF212B Extended Operating Mode requires further register configurations.

For specific applications, the receiver can additionaly be configured to handle critical environment to simplify the interaction with the microcontroller, or to operate in different data rates.

There are scenarios where CSMA-CA is not used before a transmission or where CSMA-CA is not really reliable, for example in hidden node scenarios. As two transceivers compete for the use of one channel they may interfere with each other which may produce unreliable transmission. Receiver Override can be used to cope with such scenarios. The level of interference (which can be caused by a new incoming frame) is continuously measured while decoding a frame. The synchronization to the potential new frame starts if the interference level does not allow for a reliable detection.

The AT86RF212B receiver has an outstanding sensitivity performance. At certain environmental conditions or for High Data Rate Modes it may be useful to manually decrease this sensitivity. This is achieved by adjusting the synchronization header detector threshold using register the RX_PDT_LEVEL bits in the RX_SYN register (RX_SYN.RX_PDT_LEVEL). Received signals with a RSSI value below the threshold do not activate the demodulation process.

Furthermore, at times it may be useful to protect a received frame against overwriting by a new subsequent data frame, when the receive data buffer has not been read on time. A Dynamic Frame Buffer Protection is enabled with

the RX_SAFE_MODE bit in the TRX_CTRL_2 register (TRX_CTRL_2.RX_SAFE_MODE) set. The receiver remains in RX_ON or RX_AACK_ON state until the whole frame is uploaded by the microcontroller, indicated by pin 23 (/SEL) = H during the SPI Frame Receive Mode. The Frame Buffer content is only protected if the FCS is valid.

A Static Frame Buffer Protection is enabled with the RX_PDT_DIS bit in the RX_SYN register (RX_SYN.RX_PDT_DIS) set. The receiver remains in RX_ON or RX_AACK_ON state and no further SHR is detected until the register bit RX_PDT_DIS is set back.

7.3 Transmitter (TX)

7.3.1 Overview

The AT86RF212B transmitter utilizes a direct up-conversion topology. The digital transmitter (TX BBP) generates the in-phase (I) and quadrature (Q) component of the modulation signal. A Digital-to-Analog converter (DAC) forms the analog modulation signal. A quadrature mixer pair converts the analog modulation signal to the RF domain. The Power Amplifier (PA) provides signal power delivered to the differential antenna pins (RFP, RFN). Both, the LNA of the receiver input and the PA of the transmitter output are internally connected to the bidirectional differential antenna pins so that no external antenna switch is needed.

Using the default settings, the PA incorporates an equalizer to improve its linearity. The enhanced linearity keeps the spectral side lobes of the transmit spectrum low in order to meet the requirements of the European 868.3MHz band.

If the PA Boost mode is turned on, the equalizer is disabled. This allows delivery of a higher transmit power of up to +9 dBm at the cost of higher spectral side lobes and higher harmonic power.

In Basic Operating Mode, a transmission is started from PLL_ON state by either writing TX_START to the TRX_CMD bits in the TRX_STATE regoster (TRX_STATE.TRX_CMD) or by a rising edge of pin 11 (SLP_TR).

In Extended Operating modes, a transmission might be started automatically depending on the transaction phase of either RX_AACK or TX_ARET.

7.3.2 Frame Transmit Procedure

The frame transmit procedure, including writing PSDU data into the Frame Buffer and initiating a transmission, is described in the *Radio Transceiver Usage - Frame Transmit Procedure* section.

7.3.3 TX Output Power

The maximum output power of the transmitter is typically +3.2 dBm in normal mode and +8.7 dBm in boost mode. The TX output power can be set via the TX_PWR bits in the PHY_TX_PWR register (PHY_TX_PWR.TX_PWR). The output power of the transmitter can be controlled down to -27 dBm with 1 dB resolution.

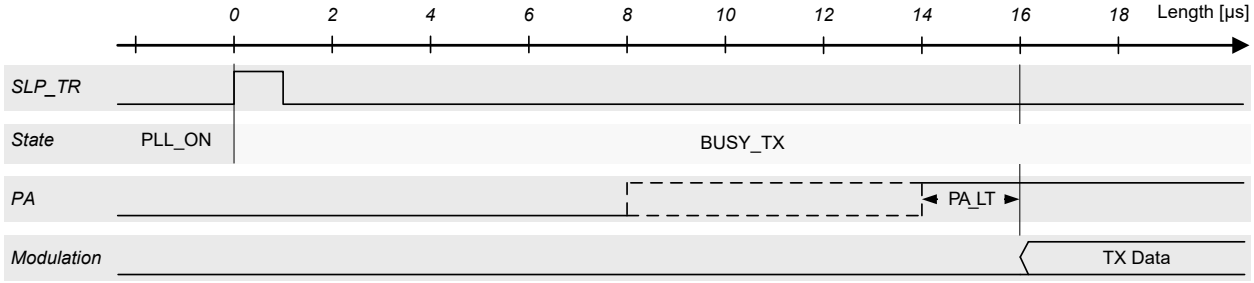
To meet the spectral requirements of the European bands, it is necessary to limit the TX power by appropriate setting of the TX_PWR and GC_PA bits in the PHY_TX_PWR register (PHY_TX_PWR.TX_PWR and PHY_TX_PWR.GC_PA), and the GC_TX_OFFS bits in the RF_CTRL_0 register (RF_CTRL_0.GC_TX_OFFS).

7.3.4 TX Power Ramping

To optimize the output Power Spectral Density (PSD), individual transmitter blocks are enabled sequentially. A transmit action is started by either the rising edge of pin 11 (SLP_TR) or by writing TX_START command to the TRX_CMD bits in the TRX_STATE register (TRX_STATE.TRX_CMD). One symbol period later the data transmission begins. During this time period, the PLL settles to the frequency used for transmission. The PA is enabled prior to the data transmission start. This PA lead time can be adjusted with the PA_LT bits in the RF_CTRL_0 register (RF_CTRL_0.PA_LT). The PA is always enabled at the lowest gain value corresponding to GC_PA = 0. Then the PA gain is increased automatically to the value set by the GC_PA bits in the PHY_TX_PWR register (PHY_TX_PWR.GC_PA). After transmission is completed, TX power ramping down is performed in an inverse order.

The control signals associated with TX power ramping are shown in the figure below. In this example, the transmission is initiated with the rising edge of pin 11 (SLP_TR). The radio transceiver state changes from PLL_ON to BUSY_TX.

Figure 7-3. TX Power Ramping Example (O-QPSK 250kb/s Mode)



Using an external RF front-end, it may be required to adjust the start-up time of the external PA relative to the internal building blocks to optimize the overall PSD. This can be achieved using the RF_CTRL_0.PA_LT bits.

For more details on actual TX power for each gain settings, see Table 9-5.

Table 7-3. Recommended Mapping of TX Power, Frequency Band and PHY_TX_PWR (register 0x05).

		PHY_TX_PWR (register 0x05)
TX Power Setting	915 MHz North American Band PHY Modes: BPSK-40 (GC_TX_OFFS = 3), BPSK-40-ALT (GC_TX_OFFS = 3), OQPSK-SIN-{250, 500, 1000} (GC_TX_OFFS = 2)	868.3 MHz European Band PHY Modes: BPSK-20 (GC_TX_OFFS = 3), OQPSK-SIN-RC-{100, 200, 400} (GC_TX_OFFS = 2) OQPSK-RC-{100, 200, 400} (GC_TX_OFFS = 3)
11	0xC0	0xA0
10	0xC1	0x80
9	0x80	0xE4
8	0x82	0xE6
7	0x83	0xE7
6	0x84	0xE8
5	0x40	0xE9
4	0x86	0xEA
3	0x00	0xCB
2	0x01	0xCC
1	0x02	0xCC
0	0x03	0xAD
-1	0x04	0x47
-2	0x27	0x48
-3	0x05	0x49
-4	0x07	0x29
-5	0x08	0x90
-6	0x91	0x91
-7	0x09	0x93
-8	0x0B	0x94
-9	0x0C	0x2F
-10	0x0D	0x30

.....continued

		PHY_TX_PWR (register 0x05)
TX Power Setting	915 MHz North American Band PHY Modes: BPSK-40 (GC_TX_OFFS = 3), BPSK-40-ALT (GC_TX_OFFS = 3), OQPSK-SIN-{250, 500, 1000} (GC_TX_OFFS = 2)	868.3 MHz European Band PHY Modes: BPSK-20 (GC_TX_OFFS = 3), OQPSK-SIN-RC-{100, 200, 400} (GC_TX_OFFS = 2) OQPSK-RC-{100, 200, 400} (GC_TX_OFFS = 3)
-11	0x0E	0x31
-12	0x0F	0x0F
-13	0x10	0x10
-14	0x11	0x11
-15	0x12	0x12
-16	0x13	0x13
-17	0x14	0x14
-18	0x15	0x15
-19	0x16	0x17
-20	0x17	0x18
-21	0x19	0x19
-22	0x1A	0x1A
-23	0x1B	0x1B
-24	0x1C	0x1C
-25	0x1D	0x1D

7.4 Frame Buffer

The AT86RF212B contains a 128-byte dual port SRAM. One port is connected to the SPI interface, the other one to the internal transmitter and receiver modules. For data communication, both ports are independent and simultaneously accessible.

The Frame Buffer utilizes the SRAM address space 0x00 to 0x7F for RX and TX operation of the radio transceiver and can keep a single IEEE 802.15.4 RX or a single TX frame of maximum length at a time.

Frame Buffer access conflicts are indicated by an underrun interrupt IRQ_6 (TRX_UR).

Note: The IRQ_6 (TRX_UR) interrupt also occurs on the attempt to write frames longer than 127 octets to the Frame Buffer (overflow). In that case, the content of the Frame Buffer cannot be determined.

Frame Buffer access is only possible if the digital voltage regulator (DVREG) is turned on. This is valid in all device states except in SLEEP state. An access in P_ON state is possible if pin 17 (CLKM) provides the 1 MHz host clock.

7.4.1 Data Management

Data in Frame Buffer (received data or data to be transmitted) remains valid as long as:

- No new frame or other data are written into the buffer over SPI
- No new frame is received (in any BUSY_RX state)
- No state change into SLEEP state is made
- No RESET took place

By default, there is no protection of the Frame Buffer against overwriting. Therefore, if a frame is received during Frame Buffer read access of a previously received frame, interrupt IRQ_6 (TRX_UR) is issued and the stored data might be overwritten.

Even so, the old frame data can be read, if the SPI data rate is higher than the effective over air data rate. For a data rate of 250 kb/s, a minimum SPI clock rate of 1 MHz is recommended. Finally, the microcontroller checks the transferred frame data integrity by an FCS check.

To protect the Frame Buffer content against being overwritten by newly incoming frames, change the radio transceiver state to PLL_ON state after reception. This can be achieved by writing the command PLL_ON to the TRX_CMD bits in the TRX_STATE register (TRX_STATE.TRX_CMD) immediately after receiving the frame, indicated by IRQ_3 (TRX_END). Alternatively, Dynamic Frame Buffer Protection can be used to protect received frames against overwriting. Both procedures do not protect the Frame Buffer from overwriting by the microcontroller.

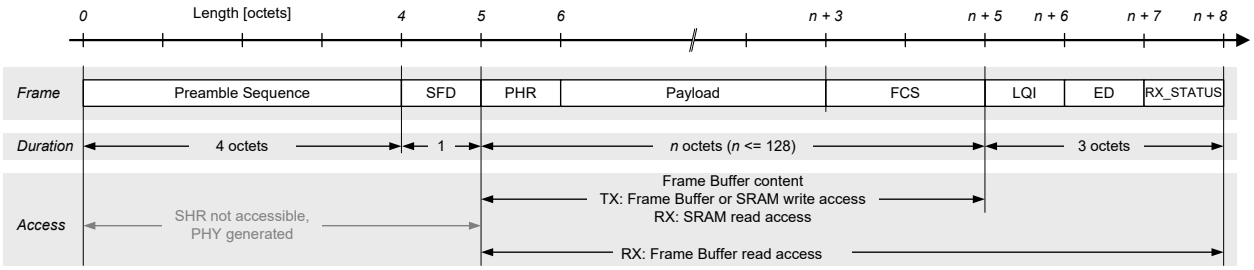
In Extended Operating Mode, during TX_ARET operation, the radio transceiver switches to the receive state if an acknowledgment of a previously transmitted frame was requested. During this period, received frames are evaluated but not stored in the Frame Buffer. This allows the radio transceiver to wait for an acknowledgment frame and retry the frame transmission without writing the frame again.

A radio transceiver state change, except a transition to SLEEP state or a reset, does not affect the Frame Buffer content. If the radio transceiver is taken into SLEEP, the Frame Buffer is powered off and the stored data are lost.

7.4.2 User accessible Frame Content

The AT86RF212B supports an IEEE 802.15.4 compliant frame format as shown in the figure below.

Figure 7-4. AT86RF212B Frame Structure



A frame comprises two sections, the radio transceiver internally generated SHR field and the user accessible part stored in the Frame Buffer. The SHR contains the preamble and the SFD field. The variable frame section contains the PHR and the PSDU including the FCS.

To access the data, follow the procedures described in *Frame Check Sequence (FCS)*.

The frame length information (PHR field) and the PSDU are stored in the Frame Buffer. During frame reception, the link quality indicator (LQI) value, the energy detection (ED) value and the status information (RX_STATUS) of a received frame are additionally stored. The radio transceiver appends these values to the frame data during Frame Buffer read access.

If the SRAM read access is used to read an RX frame, the frame length field (PHR) can be accessed at address zero. The SHR (except the SFD value used to generate the SHR) cannot be read by the microcontroller.

For frame transmission, the PHR and the PSDU needs to be stored in the Frame Buffer. The maximum Frame Buffer size supported by the radio transceiver is 128 bytes. If the TX_AUTO_CRC_ON bit in the TRX_CTRL_1 register (TRX_CTRL_1.TX_AUTO_CRC_ON) is set , the FCS field of the PSDU is replaced by the automatically calculated FCS during frame transmission.

To manipulate individual bytes of the Frame Buffer a SRAM write access can be used instead.

For non IEEE 802.15.4 compliant frames, the minimum frame length supported by the radio transceiver is one byte (Frame Length Field + one byte of data).

7.4.3 Interrupt Handling

Access conflicts may occur when reading and writing data simultaneously at the two independent ports of the Frame Buffer, TX/RX BBP and SPI. These ports have their own address counter that points to the Frame Buffer's current address.

Access violations may cause data corruption and are indicated by IRQ_6 (TRX_UR) interrupt when using the Frame Buffer access mode. Note that access violations are not indicated when using the SRAM access mode.

While receiving a frame, first the data need to be stored in the Frame Buffer before reading it. This can be ensured by accessing the Frame Buffer at least eight symbols (BPSK) or two symbols (O-QPSK) after interrupt IRQ_2 (RX_START). When reading the frame data continuously, the SPI data rate shall be lower than the current TRX bit rate to ensure no underrun interrupt occurs. To avoid access conflicts and to simplify the Frame Buffer read access, Frame Buffer Empty indication may be used.

When writing data to the Frame Buffer during frame transmission, the SPI data rate shall be higher than the PHY data rate avoiding underrun. The first byte of the PSDU data must be available in the Frame Buffer before SFD transmission is complete, which takes 41 symbol periods for BPSK (one symbol PA ramp up + 40 symbols SHR) and 11 symbol periods for O-QPSK (one symbol PA ramp up + 10 symbols SHR) from the rising edge of pin 11 (SLP_TR).

Notes:

1. Interrupt IRQ_6 (TRX_UR) is valid two octets after IRQ_2 (RX_START).
2. If a Frame Buffer read access is not finished until a new frame is received, an IRQ_6 (TRX_UR) interrupt occurs. Nevertheless the old frame data can be read, if the SPI data rate is higher than the effective PHY data rate. A minimum SPI clock rate of 1MHz is recommended in this case. Finally, the microcontroller checks the integrity of the transferred frame data by calculating the FCS.
3. When writing data to the Frame Buffer during frame transmission, the SPI data rate shall be higher than the PHY data rate to ensure no under run interrupt. The first byte of the PSDU data must be available in the Frame Buffer before SFD transmission is complete.

7.5 Crystal Oscillator (XOSC) and Clock Output (CLKM)

The main crystal oscillator features are:

- 16 MHz amplitude-controlled crystal oscillator
- Fast settling time after leaving SLEEP state
- Configurable trimming capacitance array
- Configurable clock output (CLKM)

7.5.1 Overview

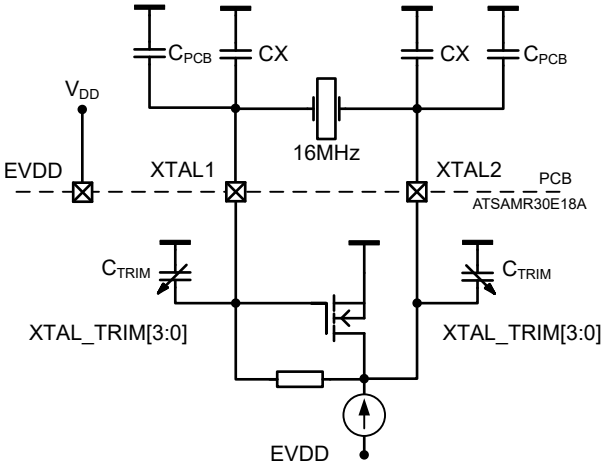
The internal 16 MHz crystal oscillator to the module generates the reference frequency for the AT86RF212B. All other internally generated frequencies of the radio transceiver are derived from this frequency. The XOSC_CTRL register provides access to the control signals of the oscillator.

7.5.2 Integrated Oscillator Setup

Using the internal oscillator, the oscillation frequency depends on the load capacitance between the crystal pin 2 (XTAL1) and pin 1 (XTAL2) of ATSAMR30E18A. The total load capacitance C_L must be equal to the specified load capacitance of the crystal itself. It consists of the internal capacitors CX and parasitic capacitances connected to the XTAL nodes inside the module.

The figure below shows all parasitic capacitances, such as PCB stray capacitances and the pin input capacitance, summarized to C_{PAR}.

Figure 7-5. Simplified XOSC Schematic with External Components



Additional internal trimming capacitors C_{TRIM} are available. Any value in the range from 0 pF to 4.5 pF with a 0.3 pF resolution is selectable using the XTAL_TRIM bits in the XOSC_CTRL register (XOSC_CTRL.XTAL_TRIM). To calculate the total load capacitance, the following formula can be used:

$C_L[pF] = 0.5 \times (CX[pF] + C_{TRIM}[pF] + C_{PAR}[pF])$.

The ATSAMR30E18A trimming capacitors provide the possibility of reducing frequency deviations caused by production process variations or by external components' tolerances. Note that the oscillation frequency can only be reduced by increasing the trimming capacitance. The frequency deviation caused by one step of C_{TRIM} decreases with increasing crystal load capacitor values.

An amplitude control circuit is included to ensure stable operation under different operating conditions and for different crystal types. Enabling the crystal oscillator in P_ON state and after leaving SLEEP state causes a slightly higher current during the amplitude build-up phase to ensure a short start-up time. At stable operation, the current is reduced to the amount necessary for a robust operation. This also keeps the drive level of the crystal low.

The XTAL_TRIM value is determined during the production test and stored in NVM user row. This value needs to be loaded into the register during initialization. For more details, see NVM Information.

7.5.3 Clock Jitter

The ATSAMR30M18A provides receiver sensitivities up to -105 dBm. Detection of such small RF signals requires very clean scenarios with respect to noise and interference. Harmonics of digital signals may degrade the performance if they interfere with the wanted RF signal. A small clock jitter of digital signals can spread harmonics over a wider frequency range, thus reducing the power of certain spectral lines. The ATSAMR30M18A provides such a clock jitter as an optional feature. The jitter module is working for the receiver part and all I/O signals, for example CLKM if enabled. The transmitter part and RF frequency generation are not influenced.

7.6 Frequency Synthesizer (PLL)

The main PLL features are:

- Generate RX/TX frequencies for all supported channels
- Autonomous calibration loops for stable operation within the operating range
- Two PLL interrupts for status indication
- Fast PLL settling to support frequency hopping

7.6.1 Overview

The PLL generates the RF frequencies for the ATSAMR30M18A. During receive and transmit operations, the frequency synthesizer operates as a local oscillator. The frequency synthesizer is implemented as a fractional-N PLL with analog compensation of the fractional phase error. The Voltage Controlled Oscillator (VCO) is running at double the RF frequency.

Two calibration loops ensure correct PLL functionality within the specified operating limits.

7.6.2 RF Channel Selection

The PLL is designed to support:

- One channel in the European SRD band from 863 MHz to 870 MHz at 868.3 MHz according to IEEE 802.15.4 (channel k = 0)
- 10 channels in the North American ISM band from 902 MHz to 928 MHz with a channel spacing of 2 MHz according to IEEE 802.15.4. The center frequency of these channels is defined as:
  F_C [MHz] = 906 [MHz] + 2 [MHz] x(k – 1), for k = 1, 2, ..., 10

  where k is the channel number.

Additionally, the PLL supports all frequencies from 769 MHz to 935 MHz with 1MHz frequency spacing and four bands with 100 kHz spacing from 769.0 MHz to 794.5 MHz, 857.0 MHz to 882.5 MHz and 902.0 MHz to 928.5 MHz. The frequency is selected by the CC_BAND bits in the CC_CTRL_1 register (CC_CTRL_1.CC_BAND) and CC_NUMBER bits in the CC_CTRL_0 register (CC_CTRL_0.CC_CTRL_0).

The table below shows the settings of CC_BAND and CC_NUMBER.

Table 7-4. Frequency Bands and Numbers

CC_BAND	CC_NUMBER	Description
0	Not used	European and North American channels according to IEEE 802.15.4; Frequency selected by the CHANNEL bits in the PHY_CC_CCA register (PHY_CC_CCA.CHANNEL)
1	0x00 – 0xFF	769.0 MHz – 794.5 MHz Fc [MHz] = 769.0 [MHz] + 0.1 [MHz] x CC_NUMBER
2	0x00 – 0xFF	857.0 MHz – 882.5 MHz Fc [MHz] = 857.0 [MHz] + 0.1 [MHz] x CC_NUMBER
3	0x00 – 0xFF	903.0 MHz – 928.5 MHz Fc [MHz] = 903.0 [MHz] + 0.1 [MHz] x CC_NUMBER
4	0x00 – 0x5E	769 MHz – 863 MHz Fc [MHz] = 769 [MHz] + 1 [MHz] x CC_NUMBER
5	0x00 – 0x66	833 MHz – 935 MHz Fc [MHz] = 833 [MHz] + 1 [MHz] x CC_NUMBER
6	0x00 – 0xFF	902.0 MHz – 927.5 MHz Fc [MHz] = 902.0 [MHz] + 0.1 [MHz] x CC_NUMBER
7	0x00 – 0xFF	Reserved

Bits 4:0 of register PHY_CC_CCA (0x08 – AT86RF212B) control the selection of IEEE802.15.4 Channels.

Table 7-5. CHANNEL Assignment

Value	Description
0x00	868.3 MHz
0x01	906 MHz
0x02	908 MHz
0x03	910 MHz
0x04	912 MHz

.....continued	
Value	**Description**
0x05	914 MHz
0x06	916 MHz
0x07	918 MHz
0x08	920 MHz
0x09	922 MHz
0x0A	924 MHz
Reserved	All other values are reserved

7.6.3 PLL Settling Time and Frequency Agility

When the PLL is enabled during state transition from TRX_OFF to PLL_ON or RX_ON, the settling time is typically t_{TR4} = 170 µs, including PLL self calibration. A lock of the PLL is indicated with an interrupt IRQ_0 (PLL_LOCK).

Switching between channels within a frequency band in PLL_ON or RX_ON states is typically done within t_{PLL_SW} = 11 µs. This makes the radio transceiver highly suitable for frequency hopping applications.

The PLL frequency in PLL_ON and receive states is 1 MHz below the PLL frequency in transmit states. When starting the transmit procedure, the PLL frequency is changed to the transmit frequency within a period of t_{RX_TX} = 16 µs before really starting the transmission. After the transmission, the PLL settles back to the receive frequency within a period of t_{TX_RX} = 32 µs. This frequency step does not generate an interrupt IRQ_0 (PLL_LOCK) or IRQ_1 (PLL_UNLOCK) within these periods.

7.6.4 Calibration Loops

Due to variation of temperature, supply voltage and part-to-part variations of the radio transceiver the VCO characteristics may vary.

To ensure a stable operation, two automated control loops are implemented:

- Center Frequency (CF) tuning
- Delay Cell (DCU) calibration

Both calibration loops are initiated automatically when the PLL is enabled during state transition from TRX_OFF to PLL_ON or RX_ON state. Additionally, both calibration loops are initiated when the PLL changes to a different frequency setting.

If the PLL operates for a long time on the same channel, for example more than five minutes, or the operating temperature changes significantly, it is recommended to initiate the calibration loops manually.

Both calibration loops can be initiated manually by an SPI command. To start the calibration, it is recommended that the device be in the PLL_ON state. The center frequency calibration can be initiated by setting the PLL_CF_START bit in the PLL_CF register to '1' (PLL_CF.PLL_CF_START = 1). The calibration loop is completed when the IRQ_0 (PLL_LOCK) occurs, if enabled. The duration of the center frequency calibration loop depends on the difference between the current CF value and the final CF value. During the calibration, the CF value is incremented or decremented. Each step takes t_{PLL_CF} = 8 µs. The minimum time is 8 µs; the maximum time is 270 µs. The recommended procedure to start the center frequency calibration is to read the register 0x1A (PLL_CF), to set the PLL_CF_START register bit to '1' and to write the value back to the register.

The delay cell calibration can be initiated by setting the PLL_DCU_START bit in the PLL_DCU register (PLL_DCU.PLL_DCU_START) to '1'. The delay time of the programmable delay unit is adjusted to the correct value. The calibration works as successive approximation and is independent of the values in the PLL_DCU register. The duration of the calibration is t_{PLL_DCU} = 10 µs.

During both calibration processes, no correct receive or transmit operation is possible. The recommended state for the calibration is therefore PLL_ON, but calibration is not blocked at receive or transmit states.

Both calibrations can be executed concurrently.

7.6.5 Interrupt Handling

Two different interrupts indicate the PLL status (refer to the IRQ_STATUS register). IRQ_0 (PLL_LOCK) indicates that the PLL is locked. IRQ_1 (PLL_UNLOCK) interrupt indicates an unexpected unlock condition. A PLL_LOCK interrupt clears any preceding PLL_UNLOCK interrupt automatically and vice versa.

An IRQ_0 (PLL_LOCK) interrupt is supposed to occur in the following situations:

- State change from TRX_OFF to PLL_ON / RX_ON
- Frequency setting change in states PLL_ON / RX_ON
- A manually started center frequency calibration completed

All other PLL_LOCK interrupt events indicate that the PLL locked again after a prior unlock happened.

An IRQ_1 (PLL_UNLOCK) interrupt occurs in the following situations:

- A manually initiated center frequency calibration in states PLL_ON / (RX_ON)
- Frequency setting change in states PLL_ON / RX_ON

Any other occurrences of IRQ_1 (PLL_UNLOCK) indicate erroneous behavior and require checking of the actual device status.

PLL_LOCK and PLL_UNLOCK affect the behavior of the transceiver:

In states BUSY_TX and BUSY_TX_ARET, the transmission is stopped and the transceiver returns into state PLL_ON. During BUSY_RX and BUSY_RX_AACK, the transceiver returns to state RX_ON and RX_AACK_ON, respectively, once the PLL is locked.

Notes:

1. An AT86RF212B interrupt IRQ_0 (PLL_LOCK) clears any preceding IRQ_1 (PLL_UNLOCK) interrupt automatically and vice versa.
2. The state transition from BUSY_TX / BUSY_TX_ARET to PLL_ON / TX_ARET_ON after successful transmission does not generate an IRQ_0 (PLL_LOCK) within the settling period.

7.7 Automatic Filter Tuning (FTN)

The Automatic Filter Tuning (FTN) is incorporated to compensate device tolerances for temperature and supply voltage variations, as well as part-to-part variations of the radio transceiver. The filter-tuning result is used to correct the analog baseband filter transfer function and the PLL loop-filter time constant.

An FTN calibration cycle is initiated automatically when entering the TRX_OFF state from the P_ON, SLEEP or RESET state.

Although receiver and transmitter are very robust against these variations, it is recommended to initiate the FTN manually if the radio transceiver does not use the SLEEP state. If necessary, a calibration cycle is to be initiated in states TRX_OFF, PLL_ON or RX_ON. This applies in particular for the High Data Rate modes with a much higher sensitivity against Band-Pass Filter (BPF) transfer function variations. The recommended calibration interval is five minutes or less, if the ATSAMR30M18A operates always in an active state (PLL_ON, TX_ARET_ON, RX_ON and RX_AACK_ON).

7.7.1 Overview

The Automatic Filter Tuning (FTN) is incorporated to compensate device tolerances for temperature, supply voltage variations as well as part-to-part variations of the radio transceiver. The filter-tuning result is used to correct the analog baseband filter transfer function and the PLL loop-filter time constant.

An FTN calibration cycle is initiated automatically when entering the TRX_OFF state from the P_ON, SLEEP or RESET state.

Although receiver and transmitter are very robust against these variations, it is recommended to initiate the FTN manually if the radio transceiver does not use the SLEEP state. If necessary, a calibration cycle is to be initiated in states TRX_OFF, PLL_ON or RX_ON. This applies in particular for the High Data Rate Modes with a much higher sensitivity against Band-Pass Filter (BPF) transfer function variations. The recommended calibration interval is five minutes or less, if the AT86RF212B operates always in an active state (PLL_ON, TX_ARET_ON, RX_ON and RX_AACK_ON).

8. Radio Transceiver Usage

This section describes basic procedures to receive and transmit frames using the ATSAMR30M18A. For a detailed description of different states of AT86RF212B, refer to the ATSAMR30E18A data sheet.

8.1 Frame Receive Procedure

A frame reception comprises of two actions: The transceiver listens for, receives and demodulates the frame to the Frame Buffer and signals the reception to the microcontroller. After or during that process, the microcontroller can read the available frame data from the Frame Buffer via the SPI interface.

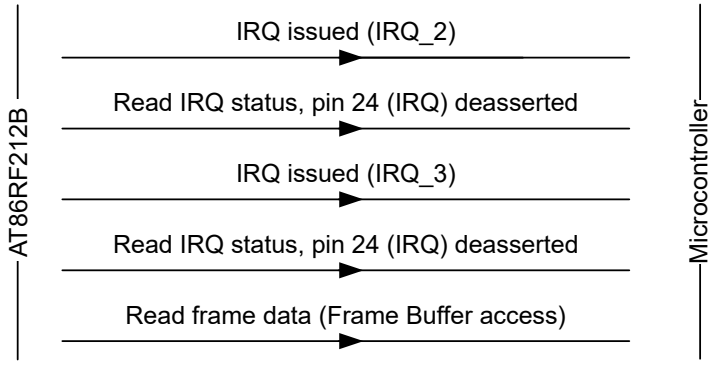
While being in state RX_ON or RX_AACK_ON, the radio transceiver searches for incoming frames with the selected modulation scheme and data rate on the selected channel. Assuming the appropriate interrupts are enabled, the detection of a frame is indicated by interrupt IRQ_2 (RX_START). When the frame reception is completed, interrupt IRQ_3 (TRX_END) is issued.

Different Frame Buffer read access scenarios are recommended for:

- Non-time critical applications:
  - Read access starts after IRQ_3 (TRX_END)
- Time-critical applications:
  - Read access starts after IRQ_2 (RX_START)

For non-time-critical operations, it is recommended to wait for interrupt IRQ_3 (TRX_END) before starting a Frame Buffer read access. The figure below illustrates the frame receive procedure using IRQ_3 (TRX_END).

Figure 8-1. Transactions between AT86RF212B and Microcontroller during Receive



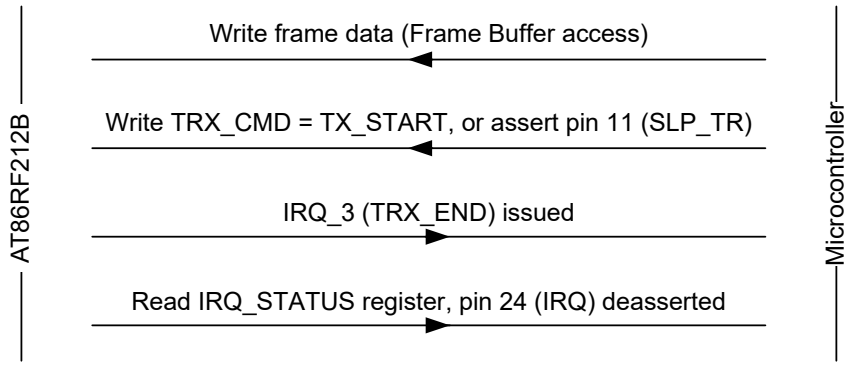
Critical protocol timing could require starting the Frame Buffer read access after interrupt IRQ_2 (RX_START). The first byte of the frame data can be read 32µs after the IRQ_2 (RX_START) interrupt. The microcontroller must be sure to read slower than the frame is received. Otherwise, a Frame Buffer underrun occurs, IRQ_6 (TRX_UR) is issued and the frame data may be not valid. To avoid this, the Frame Buffer read access can be controlled by using a Frame Buffer Empty Indicator.

8.2 Frame Transmit Procedure

A frame transmission comprises of two actions, a write to Frame Buffer and the transmission of its contents. Both actions can be run in parallel if required by critical protocol timing.

The following figure illustrates the ATSAMR30M18A frame transmit procedure, when writing and transmitting the frame consecutively. After a Frame Buffer write access, the frame transmission is initiated by asserting pin 11 (SLP_TR) or writing command TX_START to the TRX_CMD bits in the TRX_STATE register (TRX_STATE.TRX_CMD). For more information on registers, see the SAM R30 Data Sheet. The transceiver must be either in PLL_ON state for Basic Operating mode or TX_ARET_ON state for Extended Operating mode. The completion of the transaction is indicated by interrupt IRQ_3 (TRX_END).

Figure 8-2. Transaction between AT86RF212B and Microcontroller during Transmit

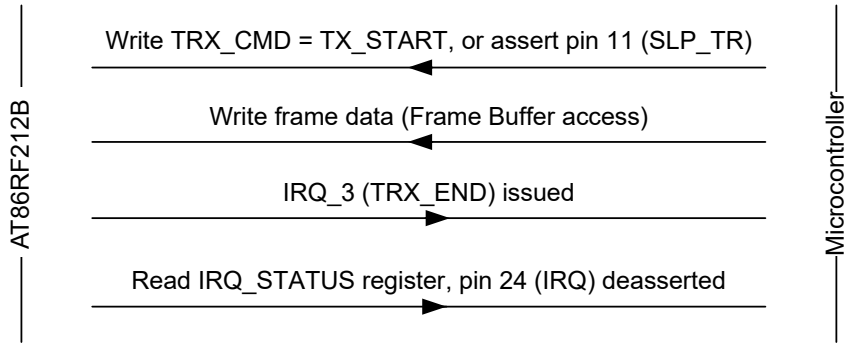


Alternatively, for time critical applications when the frame start transmission time needs to be minimized, a frame transmission task can be started first. Then it can be followed by the Frame Buffer write access event (populating PSDU data). This way the data to be transmitted needs to be written in the transmit frame buffer as the transceiver initializes and begins the SHR transmission.

By initiating a transmission, either by asserting pin 11 (SLP_TR) or writing a TX_START command to the TRX_CMD bits, the radio transceiver starts transmitting the SHR, which is internally generated.

Front end initialization takes one symbol period to settle PLL and ramp up the PA. SHR transmission takes another 40 symbol periods for BPSK or 10 symbol periods delay for O-QPSK. By this time, the PHR must be available in the Frame Buffer. Furthermore, the SPI data rate must be higher than the PHY data rate to avoid a Frame Buffer underrun, which is indicated by IRQ_6 (TRX_UR).

Figure 8-3. Time Optimized Frame Transmit Procedure



For more details about the internal interface lines like the SPI_Client Front End control, see the Microcontroller Interface section in the SAM R30 Data Sheet.

For more details about BUSY_TX, BUSY_RX, RX_ON, PLL_ON, SLEEP, RESET and other extended operating modes, see the Operating Modes section in the SAM R30 Data Sheet.

For more details about IEEE 802.15.4 Frame Format, Frame Filter, Frame Check Sequence, Received Signal Strength Indicator, Energy Detection, Clear Channel Assessment, Listen Before Talk (LBT) and Link Quality Indication (LQI), see the Functional Description section in the SAM R30 Data Sheet.

For more details about Security Module (AES), Random Number Generator and RX/TX Indicator, see the Extended Feature Set section in the SAM R30 Data Sheet.

In addition, refer to the available documentation, software sources and application notes for AT86RF212B.

9. Electrical Characteristics

This section outlines the main parameters required to build applications. The module characteristics are determined by the implemented parts.

9.1 Absolute Maximum Ratings

The values listed in this section are the ratings that can be peaked by the device, but not sustained without causing irreparable damage to the device.

Table 9-1. ATSAMR30M18A Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{STOR}	Storage temperature	—	-50	—	+150	°C
V_{PIN}	Pin voltage with respect to GND and VDD	—	GND – 0.6 V	—	VDD + 0.6 V	V
V_{ESD}	ESD robustness(1)	Module IO is routed to ATSAMR30 human body model	—	—	4	kV
		Charged device model	—	—	450	V
P_{RF}	Input RF level	—	—	—	+12	dBm

Note:

1. This value is derived from the ATSAMR30E18A IC.

9.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for the ATSAMR30M18A module.

Table 9-2. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{OP}	Operating temperature range	-40	25	85	°C
VDD	Supply voltage	1.8	3.3	3.63	V

9.3 Module Performance

This section provides the module characteristics.

9.3.1 General RF Specifications

The following table provides the ATSAMR30M18A general RF specifications.

Test Conditions (unless otherwise stated):

V_{DD} = 3.3V, f_{RF} = 914 MHz, T_{OP} = +25°C

Table 9-3. General RF Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{RF}	Frequency range	As specified in [1]	868.3	914	924	MHz
		1 MHz spacing	769	—	935	MHz
		100 kHz spacing	857.0	—	882.5	MHz
		100 kHz spacing	902.0	—	928.5	MHz
f_{CH}	Channel spacing	As specified in [1] except CHANNEL = 0	—	2	—	MHz
		1 MHz spacing	—	1000	—	kHz
		100 kHz spacing	—	100	—	kHz
f_{CHIP}	Chip rate	BPSK as specified in [1](1)	—	300	—	kchip/s
		BPSK as specified in [1](2)	—	600	—	kchip/s
		O-QPSK as specified in [2](1)	—	400	—	kchip/s
		O-QPSK as specified in [2], [3](2)	—	1000	—	kchip/s
f_{HDR}	Header bit rate (SHR, PHR)	BPSK as specified in [1](1)	—	20	—	kb/s
		BPSK as specified in [1](2)	—	40	—	kb/s
		O-QPSK as specified in [2](1)	—	100	—	kb/s
		O-QPSK as specified in [2], [3](2)	—	250	—	kb/s
f_{PSDU}	PSDU bit rate	BPSK as specified in [1](1)	—	20	—	kb/s
		BPSK as specified in [1](2)	—	40	—	kb/s
		O-QPSK as specified in [2](1)	—	100	—	kb/s
		O-QPSK as specified in [2], [3](2)	—	250	—	kb/s
		OQPSK_DATA_RATE = 1(1)	—	200	—	kb/s
		OQPSK_DATA_RATE = 2(1)	—	400	—	kb/s
		OQPSK_DATA_RATE = 1(2)	—	500	—	kb/s
		OQPSK_DATA_RATE = 2(2)	—	1000	—	kb/s
f_{CLK}	Crystal oscillator frequency	Reference oscillator	—	16	—	MHz
f_{SRD}	Symbol rate deviation	PSDU bit rate	—	—	—	—
	Reference frequency accuracy for correct functionality	20/40/100/250 kb/s	-60(3)	—	+60	ppm
		200/400/500/1000 kb/s	-40	—	+40	ppm

1. TRX_CTRL_2.SUB_MODE = 0
2. TRX_CTRL_2.SUB_MODE = 1
3. A reference frequency accuracy of ±40 ppm is required by [1], [2], [3], [4].

9.3.2 Transmitter Characteristics

The following table provides the ATSAMR30M18A transmitter characteristics.

Test Conditions (unless otherwise stated):

V_{DD} = 3.3V, f_{RF} = 914 MHz, T_{OP} = +25°C, Measurement setup in Application Reference Design.

Table 9-4. Transmitter Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_{TX_MAX}	TX Output power	BPSK-20 f_{RF} = 868.3 MHz (TX_PWR setting: 11)	—	8.7	—	dBm
		BPSK-40 f_{RF} = 914 MHz (TX_PWR setting: 11)	—	8.6	—	dBm
		OQPSK-SIN-RC-100 f_{RF} = 868.3 MHz (TX_PWR setting: 9)	—	5.3	—	dBm
		OQPSK-SIN-250 f_{RF} = 914 MHz (TX_PWR setting: 11)	—	7.3	—	dBm
P_{RANGE}	Output power range	36 steps, configurable in the PHY_TX_PWR register	—	35	—	dB
P_{1dB}	1 dB compression point	Normal mode	—	4	—	dBm
		Boost mode	—	9	—	dBm
EVM	Error vector magnitude(1)	BPSK-20	—	6.2	—	%rms
		BPSK-40	—	5.9	—	%rms
		BPSK-40-ALT	—	5.9	—	%rms
		OQPSK-SIN-RC-100(2)(3)	—	21.31	—	%rms
		OQPSK-SIN-250	—	15.81	—	%rms
		OQPSK-RC-100(3)	—	11.2	—	%rms
		OQPSK-RC-250	—	12.1	—	%rms
P_{2nd_HARM}	2nd Harmonics	TX_PWR setting: 11	—	—	—	—
		906 MHz	—	–52.43	—	dBm
		868.3 MHz	—	–51.35	—	dBm
P_{3rd_HARM}	3rd Harmonics	TX_PWR setting: 11	—	—	—	—
		906 MHz	—	–61.64	—	dBm
		868.3 MHz	—	–69.31	—	dBm
P_{SPUR_TX}	Spurious Emissions(4)	30 – ≤ 1000 MHz	—	—	-54.38	dBm
		>1 – 12.75 GHz	—	—	-46.72	dBm

1. Power settings according to the TX_PWR bits in the PHY_TX_PWR register (PHY_TX_PWR.TX_PWR).
2. The EVM of OQPSK-SIN-RC-100 is significantly higher than the EVM of the other modulation schemes. This phenomenon can be explained by the fact that the combination of SIN and RC shaping as specified in IEEE 802.15.4-2006/2011 inherently shows some inter-chip interference.
3. The EVM is valid up to +5 TX power setting.
4. Complies with EN 300 220, FCC 47CFR Part 15: Subpart C Section 15.247, RSS-247.

Table 9-5. TX Power Mapping for Frequency Bands and PHY_TX_PWR (register 0x05) Values

TX Power Setting	f_{RF} = 914 MHz PHY Modes: BPSK – 40		f_{RF} = 868.3 MHz PHY Modes: BPSK – 20	
	PHY_TX_PWR	Typical TX Power (dBm)	PHY_TX_PWR	Typical TX Power (dBm)
11	0xC0	8.6	0xA0	8.65

.....continued

TX Power Setting	f_{RF} = 914 MHz PHY Modes: BPSK – 40		f_{RF} = 868.3 MHz PHY Modes: BPSK – 20	
	PHY_TX_PWR	Typical TX Power (dBm)	PHY_TX_PWR	Typical TX Power (dBm)
10	0xC1	8	0x80	7.75
9	0x80	7.53	0xE4	6.61
8	0x82	5.91	0xE6	5.08
7	0x83	4.93	0xE7	4.04
6	0x84	4.02	0xE8	3.18
5	0x40	3.57	0xE9	2.16
4	0x86	2.31	0xEA	1.49
3	0x00	1.87	0xCB	0.01
2	0x01	0.73	0xCC	-0.91
1	0x02	-0.33	0xCC	-1.93
0	0x03	-1.62	0xAD	-2.8
-1	0x04	-2.69	0x47	-3.34
-2	0x27	-4	0x48	-4.34
-3	0x05	-3.9	0x49	-5.44
-4	0x07	-5.9	0x29	-6.65
-5	0x08	-7	0x90	-7.43
-6	0x91	-8.22	0x91	-8.48
-7	0x09	-8.11	0x93	-10.12
-8	0x0B	-9.92	0x94	-11.01
-9	0x0C	-10.91	0x2F	-12.17
-10	0x0D	-11.96	0x30	-13.14
-11	0x0E	-12.64	0x31	-14.16
-12	0x0F	-13.73	0x0F	-14.74
-13	0x10	-14.68	0x10	-15.72
-14	0x11	-15.74	0x11	-16.78
-15	0x12	-16.42	0x12	-17.43
-16	0x13	-17.5	0x13	-18.5
-17	0x14	-18.42	0x14	-19.46
-18	0x15	-19.46	0x15	-20.48
-19	0x16	-20.2	0x17	-22.23
-20	0x17	-21.24	0x18	-23.17
-21	0x19	-23.2	0x19	-24.22
-22	0x1A	-23.9	0x1A	-24.86
-23	0x1B	-24.92	0x1B	-25.92

.....continued

TX Power Setting	f_{RF} = 914 MHz PHY Modes: BPSK – 40		f_{RF} = 868.3 MHz PHY Modes: BPSK – 20	
	PHY_TX_PWR	Typical TX Power (dBm)	PHY_TX_PWR	Typical TX Power (dBm)
-24	0x1C	-25.87	0x1C	-26.83
-25	0x1D	-26.91	0x1D	-27.85

9.3.3 Receiver Characteristics

The following table provides the ATSAMR30M18A Receiver characteristics.

Test Conditions (unless otherwise stated):

- V_{DD} = 3.3V
- f_{RF} = 914 MHz
- T_{OP} = +25°C
- Measurement setup in Application Reference Design

Table 9-6. Receiver Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_{SENS}	Receiver sensitivity	**f_{RF} = 868.3 MHz**				
		BPSK-20(1)(3)	—	-105	—	dBm
		OQPSK-SIN-RC-100(1)(4)	—	-96	—	dBm
		OQPSK-SIN-RC-200(2)	—	-94	—	dBm
		OQPSK-SIN-RC-400(2)	—	-86	—	dBm
		OQPSK-RC-100(1)	—	-97	—	dBm
		OQPSK-RC-200(2)	—	-95	—	dBm
		OQPSK-RC-400(2)	—	-92	—	dBm
		f_{RF} = 914 MHz				
		BPSK-40(1)(3)	—	-103.3	—	dBm
		OQPSK-SIN-250(1)(4)	—	-95	—	dBm
		OQPSK-SIN-500(2)	—	-93	—	dBm
		OQPSK-SIN-1000(2)	—	-88	—	dBm
P_{RX_MAX}	Maximum RX input level(1)	—	—	9	12	dBm
P_{CRSB20}	Channel rejection/selectivity: BPSK-20(3)	**f_{RF} = 868.3 MHz and P_{RF} = -89 dBm(1)**				
		-2 MHz	—	39	—	dB
		-1 MHz	—	33	—	dB
		+1 MHz	—	19	—	dB
		+2 MHz	—	39	—	dB

.....continued

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$P_{CRSO100}$	Channel rejection/selectivity: OQPSK-SIN-RC-100(4)	**f_{RF} = 868.3 MHz and P_{RF} = -82 dBm(1)**				
		-2 MHz	—	35	—	dB
		-1 MHz	—	24	—	dB
		+1 MHz	—	17	—	dB
		+2 MHz	—	35	—	dB
P_{ACRB40}	Adjacent channel rejection: BPSK-40(3)	**P_{RF} = -89 dBm(1)**				
		-2 MHz	—	38	—	dB
		+2 MHz	—	38	—	dB
$P_{AACRB40}$	Alternate channel rejection: BPSK-40(3)	**P_{RF} = -89 dBm(1)**				
		-4 MHz	—	56	—	dB
		+4 MHz	—	56	—	dB
$P_{ACROS250}$	Adjacent channel rejection: OQPSK-SIN-250(4)	**P_{RF} = -82 dBm(1)**				
		-2 MHz	—	30(6)	—	dB
		+2 MHz	—	30(6)	—	dB
$P_{AACROS250}$	Alternate channel rejection: OQPSK-SIN-250(4)	**P_{RF} = -82 dBm(1)**				
		-4 MHz	—	47(6)	—	dB
		+4 MHz	—	47(6)	—	dB
$P_{ACROR250}$	Adjacent channel rejection: OQPSK-RC-250(5)	**P_{RF} = -82 dBm(1)**				
		-2 MHz	—	32	—	dB
		+2 MHz	—	32	—	dB
$P_{AACROR250}$	Alternate channel rejection: OQPSK-RC-250(5)	**P_{RF} = -82 dBm(1)**				
		-4 MHz	—	50	—	dB
		+4 MHz	—	50	—	dB
RX_{BL}	Blocking	**f_{RF} = 868.3 MHz and P_{RF} = -90 dBm(1)** (Refer to ETSI EN 300 220-1)				
		BPSK-20, ±2 MHz	—	38	—	dB
		BPSK-20, ±10 MHz	—	71	—	dB
		OQPSK-SIN-RC-100, ±2 MHz	—	34	—	dB
		OQPSK-SIN-RC-100, ±10 MHz	—	68	—	dB
P_{SPUR_RX}	Spurious emissions	LO leakage	—	-74	—	dBm
		30 – ≤ 1000 MHz	—	—	-60.45	dBm
		>1 – 12.75 GHz	—	—	-60.74	dBm
$RSSI_{TOL}$	RSSI tolerance	Tolerance within gain step	—	—	±6	dB
$RSSI_{RANGE}$	RSSI dynamic range	—	—	87	—	dB
$RSSI_{RES}$	RSSI resolution	—	—	3.1	—	dB

.....continued						
Symbol	**Parameter**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
$RSSI_{BASE\_VAL}$	RSSI sensitivity	Defined as RSSI_BASE_VAL	—	—	—	—
		BPSK with 300 kchips/s	—	-95	—	dBm
		BPSK with 600 kchips/s	—	-94	—	dBm
		O-QPSK with 400 kchips/s, SIN and RC-0.2 shaping	—	-93	—	dBm
		O-QPSK with 400 kchips/s, RC-0.2 shaping	—	-93	—	dBm
		O-QPSK with 1000 kchips/s, SIN shaping	—	-93	—	dBm
		O-QPSK with 1000 kchips/s, RC-0.8 shaping	—	-92	—	dBm
$RSSI_{MIN}$	Minimum RSSI value	P_{RF}≤ RSSI_BASE_VAL	—	0	—	—
$RSSI_{MAX}$	Maximum RSSI value	P_{RF}≥ RSSI_BASE_VAL + 87 dB	—	28	—	—

1. AWGN channel, PER ≤ 1%, PSDU length 20 octets.
2. AWGN channel, PER ≤ 1%, PSDU length 127 octets.
3. Compliant to [1].
4. Compliant to [2].
5. Compliant to [4].
6. Channel rejection is limited by modulation side lobes of interfering signal.

9.3.4 Current Consumption Specifications

The values in this section are measured values of power consumption under the following conditions, except where noted:

- Operating Conditions
  - VDD = 3.3V
  - Temperature at 25°C
  - CPU is running on Flash with one Wait state in PL0 and two Wait states in PL2
  - Low power cache is enabled
  - BOD33 is disabled
  - State of AT86RF212B is as specified in the following table
- Oscillators
  - XOSC (crystal oscillator) is disabled
  - When MCU (ATSAML21) is in Active Performance Level 2 (PL2) mode, the DFLL48M is running at 48 MHz in Open-Loop mode
  - When MCU is in Active Performance Level 0 (PL0) mode, the internal multi RC oscillator is running at 8 MHz
- Clocks
  - In the PL2 mode, DFLL48M is running in the Open-Loop mode and is used as main clock source
  - In the PL0 mode, OSC16M is used at 8 MHz
  - Clock masks and dividers are at Reset values: All AHB and APB clocks enabled, CPUDIV = 1, BUPDIV = 1 and LPDIV = 1
  - I/Os are configured in the Digital Functionality Disabled mode. Except for PA24 and PA25, which are used to provide UART input to device

Table 9-7. Current Consumption under Different Conditions(1)

Mode/Parameter	MCU Conditions	Transceiver Conditions	Measured Current (Typical)	Units
I_{BUSY_TX}	PL0	North American band, BPSK-40, f_{RF} = 914 MHz	—	mA
		TX_PWR setting = 11	26.97	
		TX_PWR setting = 5	18.71	
		TX_PWR setting = 0	14.5	
		TX_PWR setting = -25	11.1	
	PL2	North American band, BPSK-40, f_{RF} = 914 MHz	—	
		TX_PWR setting = 11	32.74	
		TX_PWR setting = 5	24.49	
		TX_PWR setting = 0	20.29	
		TX_PWR setting = -25	16.88	
I_{RX_ON}	PL0	RX_PDT_LEVEL = 0x0; BPSK-20 f_{RF} = 868.3 MHz	10.79	
	PL2	RX_PDT_LEVEL = 0x0, BPSK-20, f_{RF} = 868.3 MHz	16.47	
I_{PLL_ON}	PL0	PLL_ON	6.41	
	PL2	PLL_ON	12.12	
I_{TRX_OFF}	PL0	TRX_OFF	1.68	
	PL2	TRX_OFF	7.39	
$I_{STANDBY}$	Standby; LPEFF Enable; PD0, PD1 and PD2 in Retention state with RTC running on OSCULP32K	Sleep	2.03	µA
I_{BACKUP}	Backup with RTC running on OSCULP32K	Sleep	0.77	

Notes:

1. These values are based on characterization.
2. All power consumption measurements are performed with CLKM disabled.

10. Mechanical Description

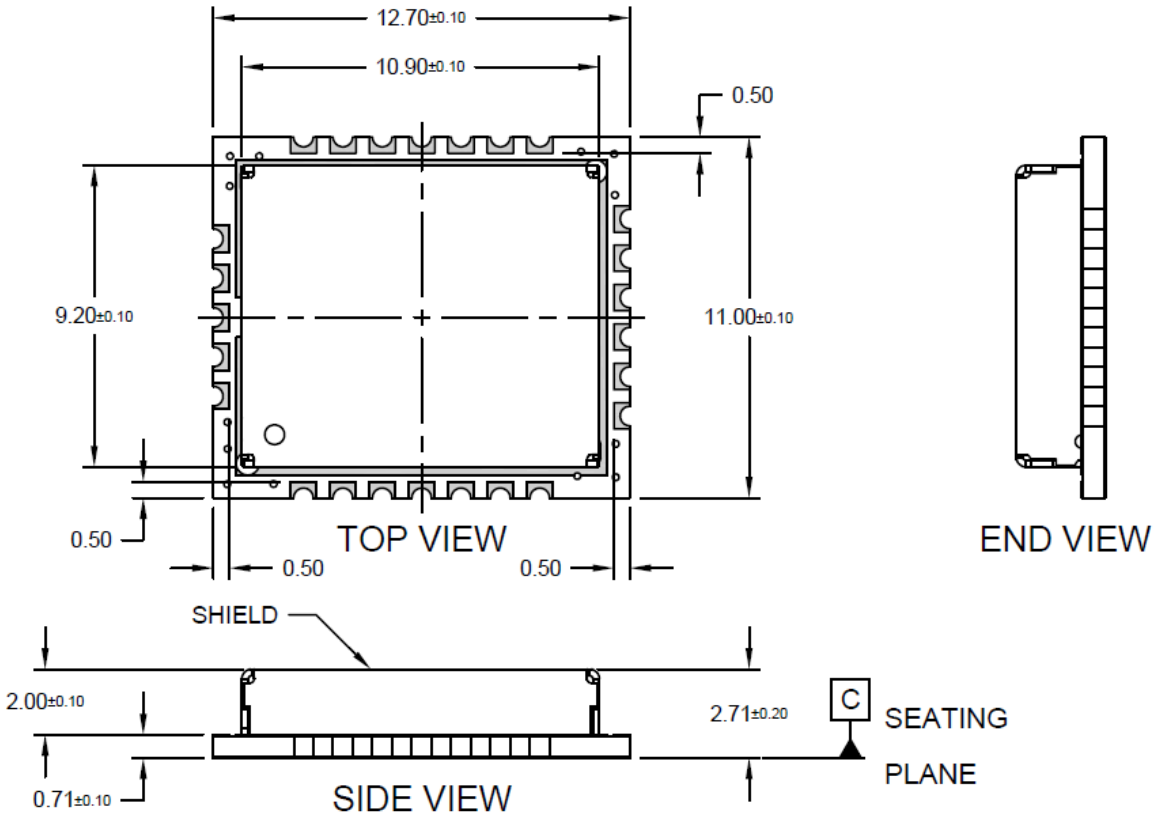
This section provides module outline drawings, footprint, application reference design and layout recommendation.

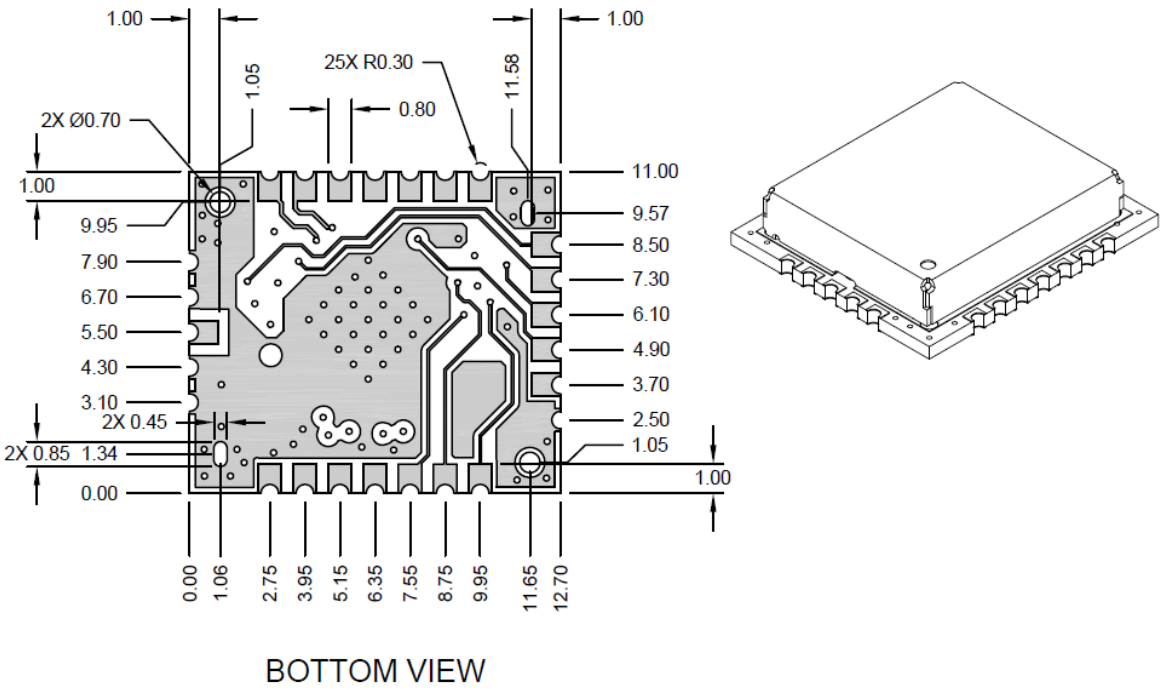
10.1 Module Outline Drawings

The ATSAMR30M18A module package details are outlined in the following figure.

The module pins are arranged with a 1.2 mm pitch distance. The module is designed in a symmetric way. Dimensions missing in the following figure can be considered as identical to the opposite side.

Figure 10-1. Module Bottom Dimensions - Top View in CAD Perspective



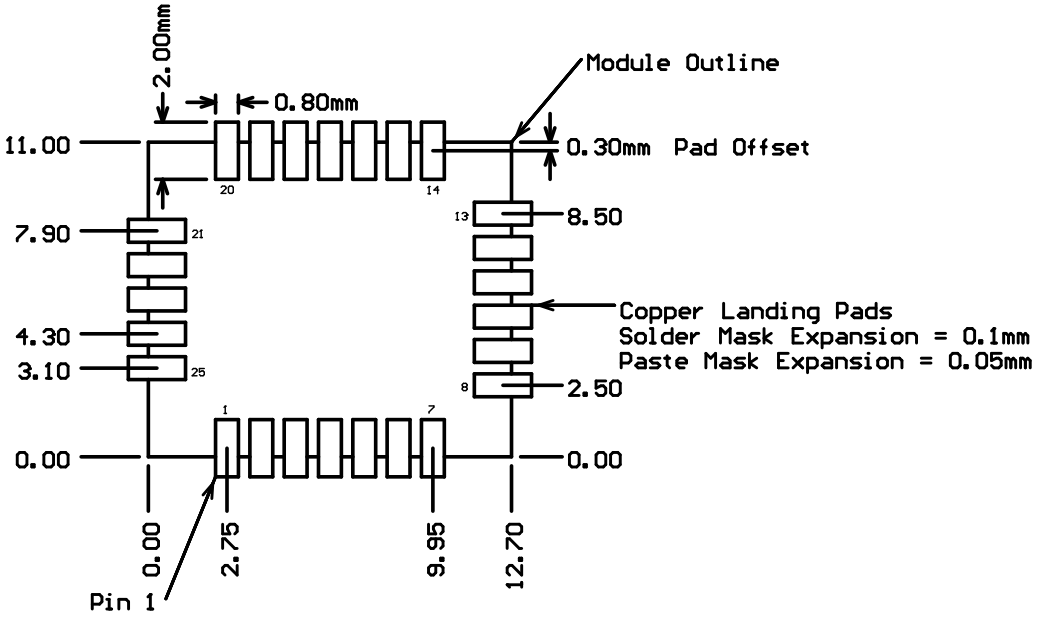


The module can be mounted to a base board with a soldered RF connection.

10.2 Footprint

The recommended land pattern is shown in the following figure.

Figure 10-2. Recommended Base Board Footprint



11. Design Considerations

11.1 Approved Antennas

The ATSAMR30M18A is tested and approved to use with the antennas listed in the following table.

If other antenna types are used, the OEM installer must authorize the antenna with the respective regulatory agencies and ensure its compliance. The used antenna is to be connected to the ATSAMR30M18A module via PCB trace in the host board as in the SAMR30 Module XPRO board or SAMR30M Sensor board.

Table 11-1. List of Approved Antennas

Manufacturer	Part Number	Antenna Type	Peak Gain	Operating Frequency
Linx technologies	ANT-916-CW-QW-SMA/ANT-916-CW-QW(1)	Monopole Antenna	1.8 dBi	865-965 MHz
Pulse Electronics	W1910/W1911(1)	Monopole Antenna	1.0 dBi	824-960 MHz and 1710-2170 MHz
Johanson Technology Inc.	0900AT43A0070	Chip Antenna	2.0 dBi	858-928 MHz
—	—	PCB Antenna	0.44 dBi	868-928 MHz

Notes:

1. If the end product using the module is designed to have an antenna port that is accessible to the end user, a unique (nonstandard) antenna connector (refer to FCC KDB 353028) must be used; for example, Reverse Polarity – SMA.
2. If an RF coaxial cable is used between the module RF output and the enclosure, a unique (nonstandard) antenna connector must be used in the enclosure wall for interfacing with the antenna.
3. Contact the antenna vendor for detailed antenna specifications to review suitability to end-product operating environment and to identify equivalent alternatives.

11.2 Module Assembly Considerations

The ATSAMR30M18A module is assembled with an EMI Shield to ensure compliance with EMI emission and immunity rules. The EMI shield is made of a Cold Rolled Steel (common or ordinary low carbon steel) material with Matte Tin Pre-plating. Use IPA solutions and similar solvents to clean the ATSAMR30M18A module. However, cleaning solutions that contain acid must never be used on the module.

11.2.1 Conformal Coating

The modules are not intended for use with a conformal coating and the customer assumes all risks (such as the module reliability, performance degradation and so on) if a conformal coating is applied to the modules.

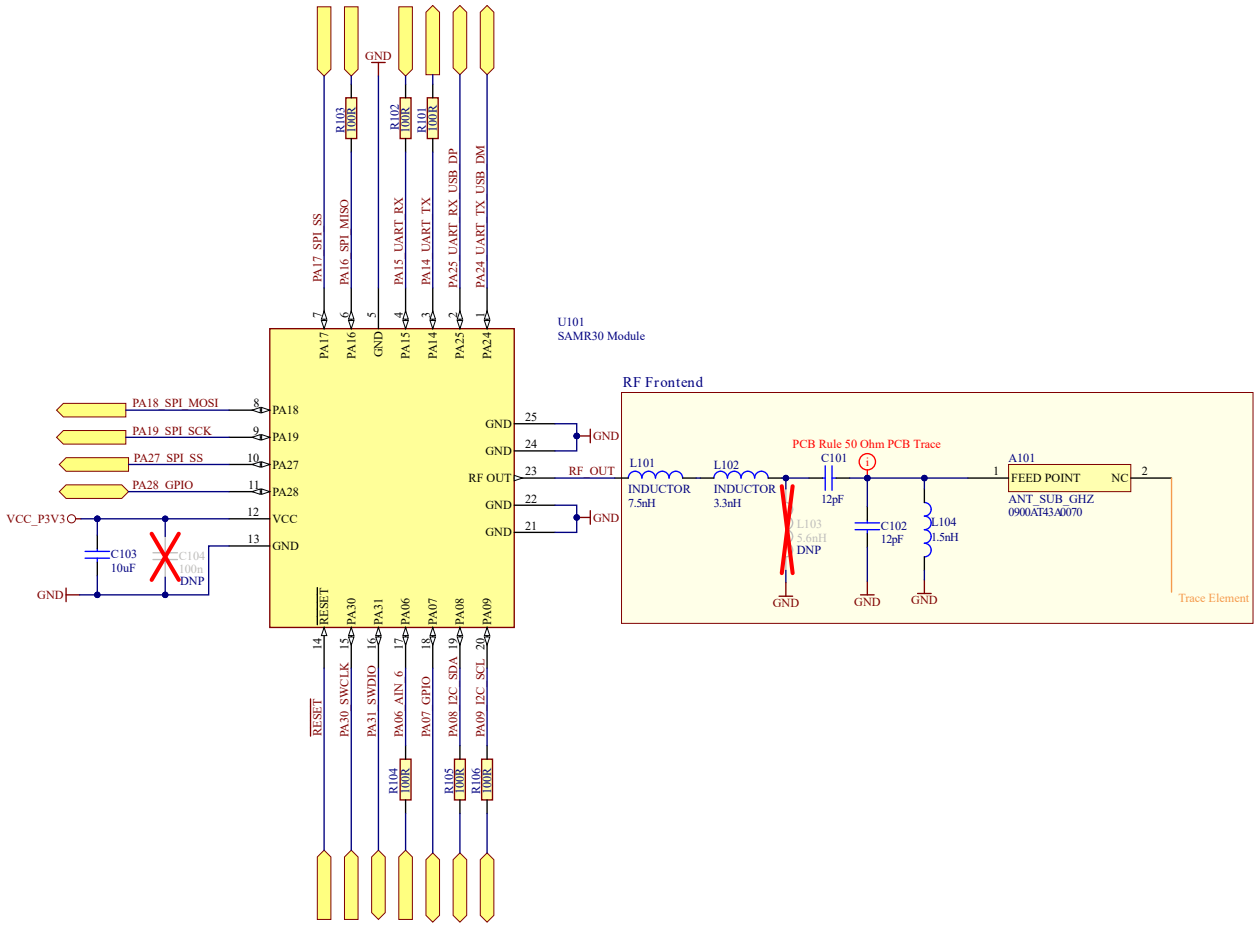
11.2.2 Reflow Profile Information

For information on the reflow process guidelines, refer to the “Solder Reflow Recommendation” Application Note (www.microchip.com/DS00233).

12. Application Reference Design

This section shows the ATSAMR30M18A module application schematics for different supported host interfaces. It is required to add 100Ω series resistors for module pins 3, 4, 6, 17, 19 and 20 to minimize radiated emission from the open-ended connectors/traces. Place these resistors (R101, R102, R103, R104, R105 and R106) as close as possible to the specific module pin in the PCB layout. If any of these module pins (3, 4, 6, 17, 19 and 20) are left unused in the design, it is recommended these pins be terminated through a 10 kΩ resistor to GND. Additionally, drive the pins to logic low during the firmware initialization.

Figure 12-1. Application Reference Design



12.1 RF Trace Layout Design Instructions

The ATSAMR30M18A module transmitter is certified with:

1. SMA(1) connector and micro strip layout
2. On-board chip antenna and micro strip layout
3. On-board PCB antenna and micro strip layout

Note:

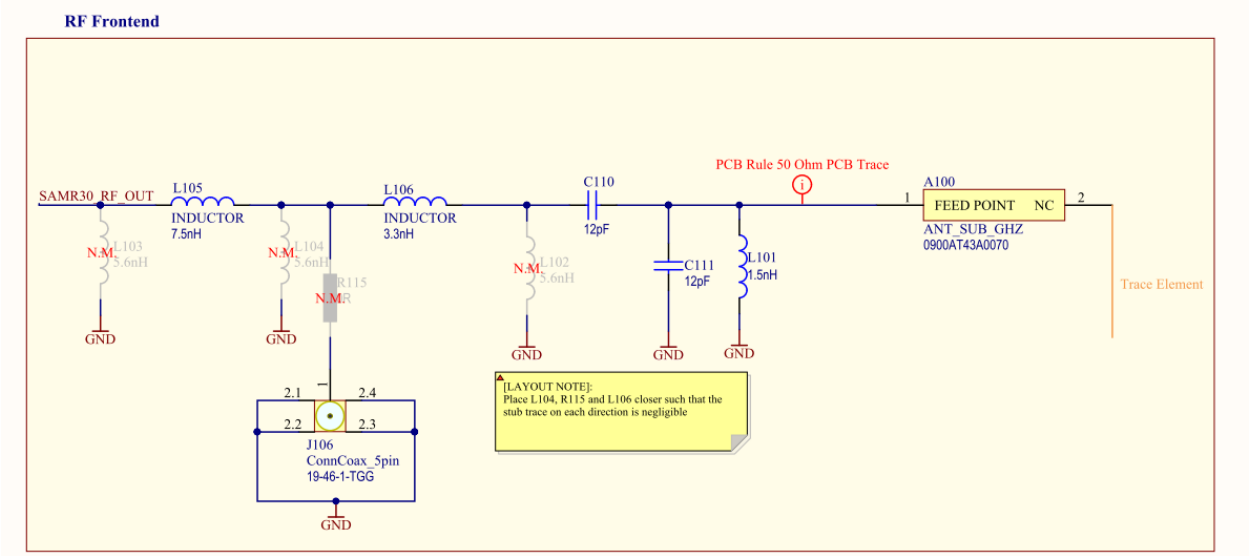
1. If the host board of ATSAMR30M18A is designed to have an antenna port that is accessible to the end user, an RP (Reverse Polarity)-SMA socket must be used. If an RF coaxial cable is used between the module RF output and the enclosure, an RP-SMA connector must be used in the enclosure wall for interface with antenna.

12.1.1 Chip Antenna and External Antenna (SMA Connector)

This section describes the PCB stack-up, mechanical details of the PCB trace leading up to SMA connector for case 1 and up to chip antenna for case 2. The host PCB can follow either of these trace designs to maintain compliance under the modular grant (FCC) and certificate (ISED). Schematics, BoM, Layout source files and Gerber files are available for download on the ATSAMR30M18A product web page.

The following is a snapshot of the schematic diagram for the host board showing the RF front end. For case 1, R115 is populated and L106 is not populated. For case 2, L106 is populated and R115 is not populated.

Figure 12-2. RF Front End



Trace layout dimensions:

- Trace width – 0.22 mm
- Trace gap – 0.42 mm
- Finished copper weight – 1 ounce

The following figure shows the top layer routing of the complete reference board (SAMR30 Module XPRO). The complete design documentation of the reference board is available on the SAMR30 Module XPRO Product web page.

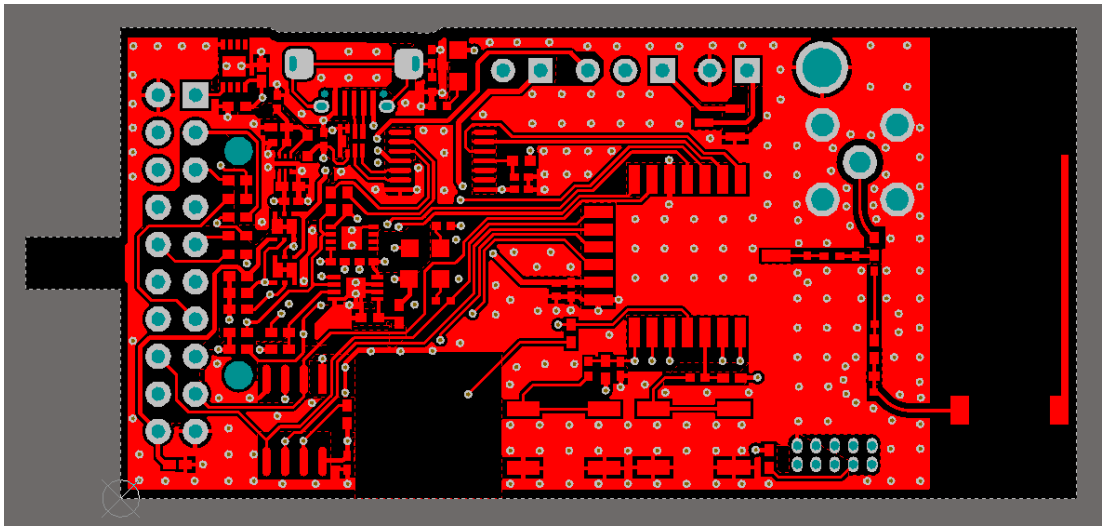
Follow the module placement and RF trace design as in the following figure. The module must be placed in the host board such that the chip antenna or the RF connector(1) is at one of the edges of the host PCB.

- For a design with an external antenna through the RF connector(1), the RF trace running from L106 to chip antenna can be replaced with GND polygon pour (with distributed GND Vias). The PCB area containing the chip antenna footprint and the RF trace can be cut out.
- For a design using a chip antenna, the RF trace running from R115 to the RF connector(1), the RF connector(1) footprint can be replaced with a GND polygon pour (with distributed GND Vias).

Note:

1. If the host board of ATSAMR30M18A is designed to have an antenna port that is accessible to the end-user, an RP (Reverse Polarity)-SMA socket must be used. If an RF coaxial cable is used between the module RF output and the enclosure, an RP-SMA connector must be used in the enclosure wall for interface with the antenna.

Figure 12-3. Top Layer Routing of the SAMR30 Module XPRO



The following figure shows the top layer layout of the reference board focused on the RF traces. The snapshot also indicates the critical dimensions that are required to be replicated in the design to maintain compliance.

Figure 12-4. Top Layer Layout

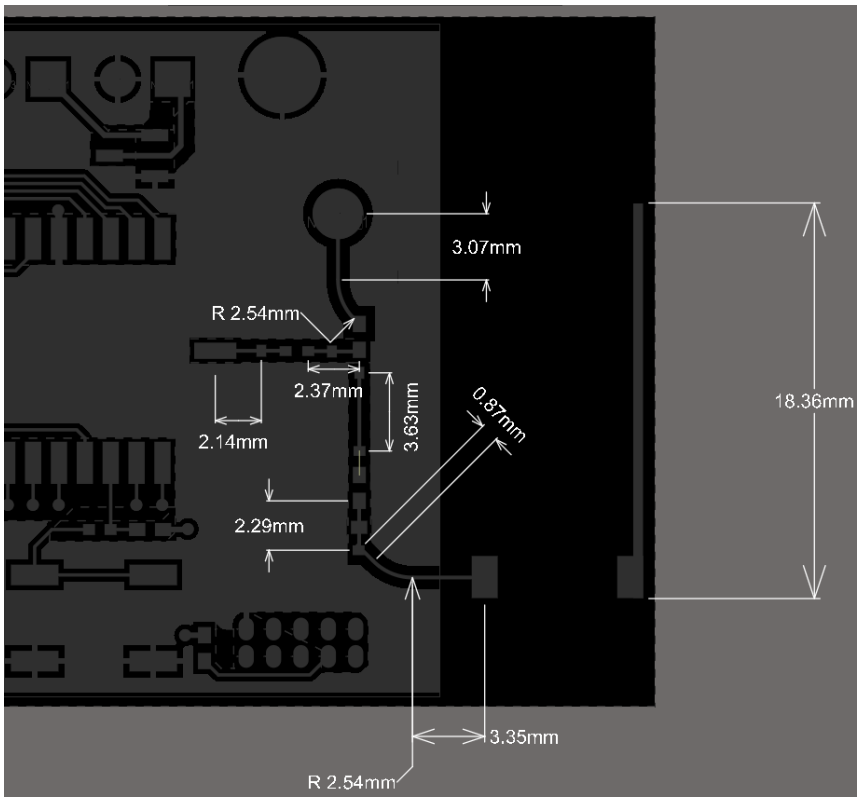
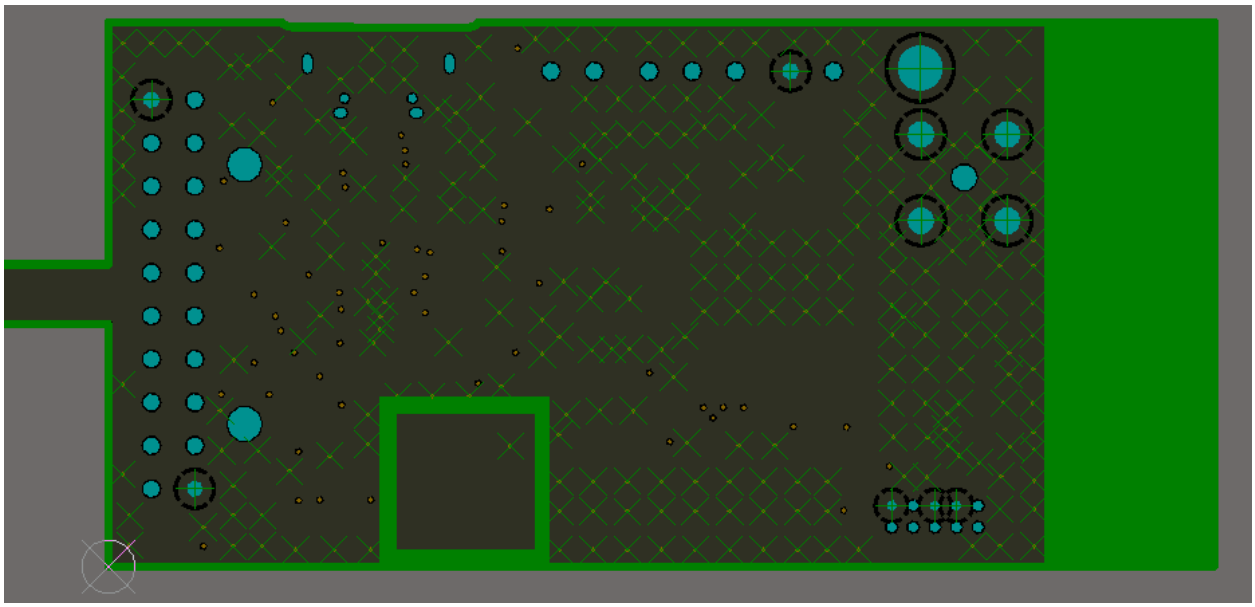
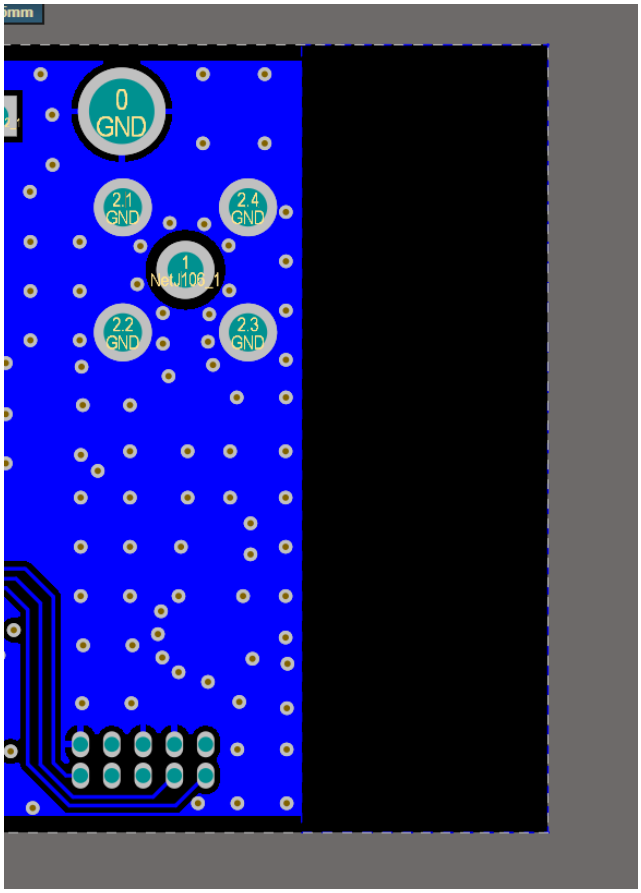


Figure 12-5. Layer 2 (GND) Layout



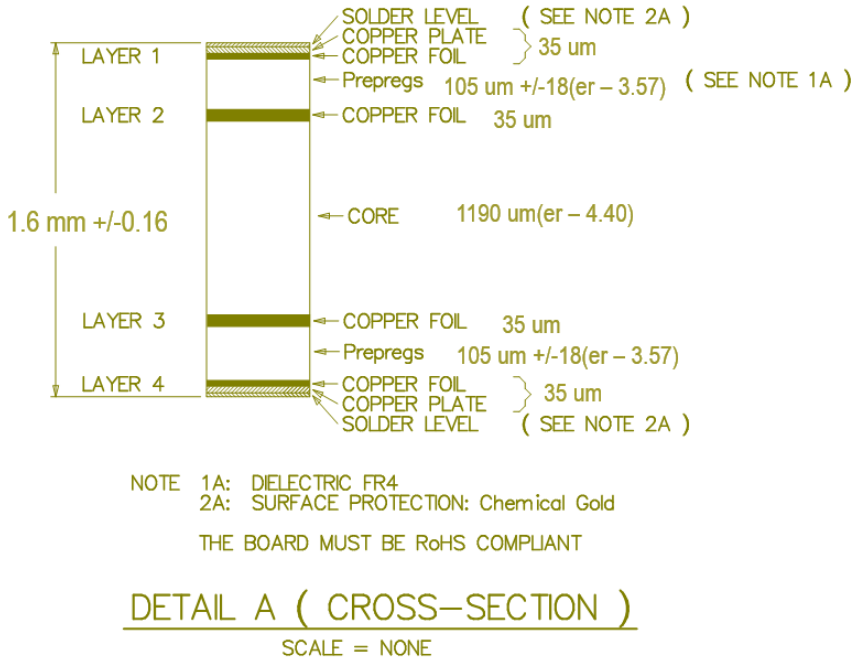
The following figure shows the bottom layer layout of the reference board directly beneath the RF traces.

Figure 12-6. Bottom Layer Layout



The following image shows the PCB stack-up for the reference board. Layer 1 (Top Layer) and Layer 2 specifications are critical to the RF Trace Layout specification.

Figure 12-7. PCB Stack Up



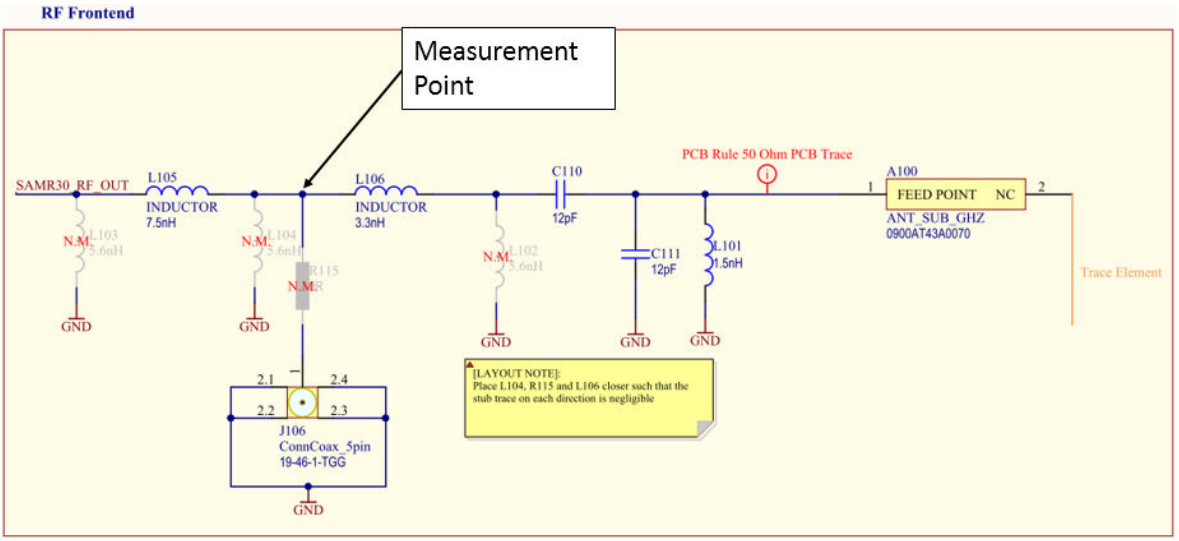
The technical specification of the approved chip and external antenna is listed in Table 11-1.

12.1.1.1 Test Procedure for Ensuring Compliance

The following test must be performed both at the design verification stage and in production to ensure compliance.

1. Initiate Continuous Transmission in the appropriate modulation mode from the device that is, 868.3 MHz; BPSK-20 for European band and 914 MHz; BPSK-ALT-40 for North American band.
2. Verify RF power through conducted measurement at junction between L106 and L105.
3. Remove L106 and R115 to isolate the antenna path from the measurement point. It is recommended that the measured TX power be within the data sheet specification for the Transmit output power. For good measurement, it is recommended that there be a firm connection between the copper core of the coaxial cable and the measurement point. Ensure the copper shield of the coaxial cable is firmly connected to the GND of the PCB.

Figure 12-8. RF Front End with Measurement Point

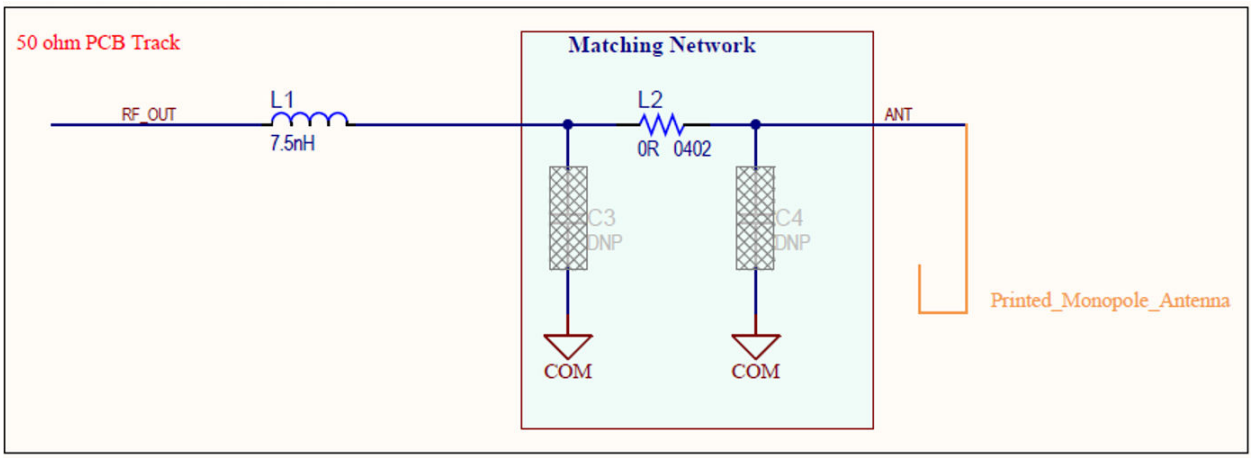


12.1.2 PCB Antenna (ATSAMR30 Sensor Board)

This section describes the PCB stack up, mechanical details of the PCB trace leading up to PCB antenna for case 3 in 12.1. RF Trace Layout Design Instructions. The host PCB can follow these trace design to maintain compliance under the modular grant (FCC) and Canada certificate (IC). Schematics, Bill of Materials (BoM), layout source files and gerber files are available for download from the SAMR30M Sensor board product page.

The following is a snapshot of the schematic diagram for the host SAMR30M Sensor board showing the PCB Antenna section.

Figure 12-9. PCB Antenna



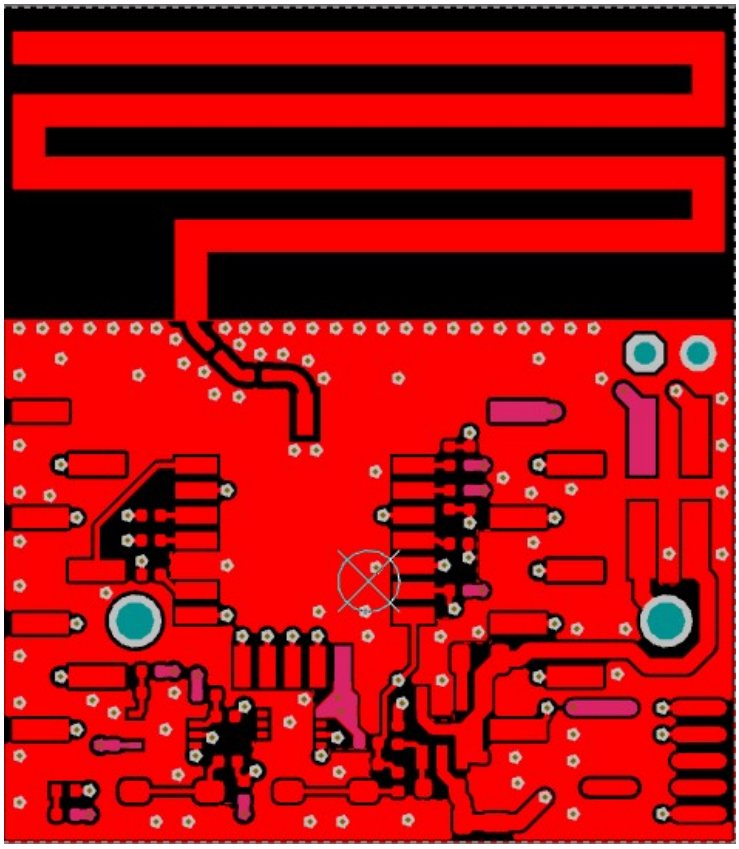
Trace layout dimensions

- Trace width – 0.533 mm
- Trace gap – 0.381 mm
- Finished copper thickness – 47 µm

Layout of Trace design:

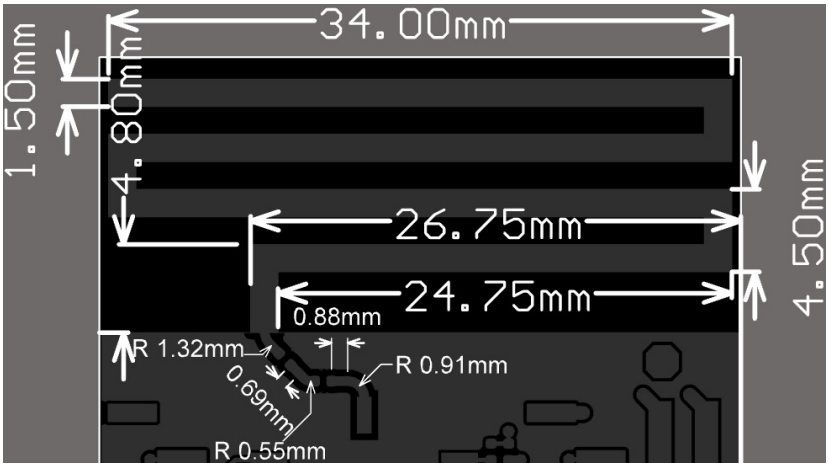
The following figure shows the top layer routing of the complete reference board.

Figure 12-10. Top Layer Routing of the Reference Board



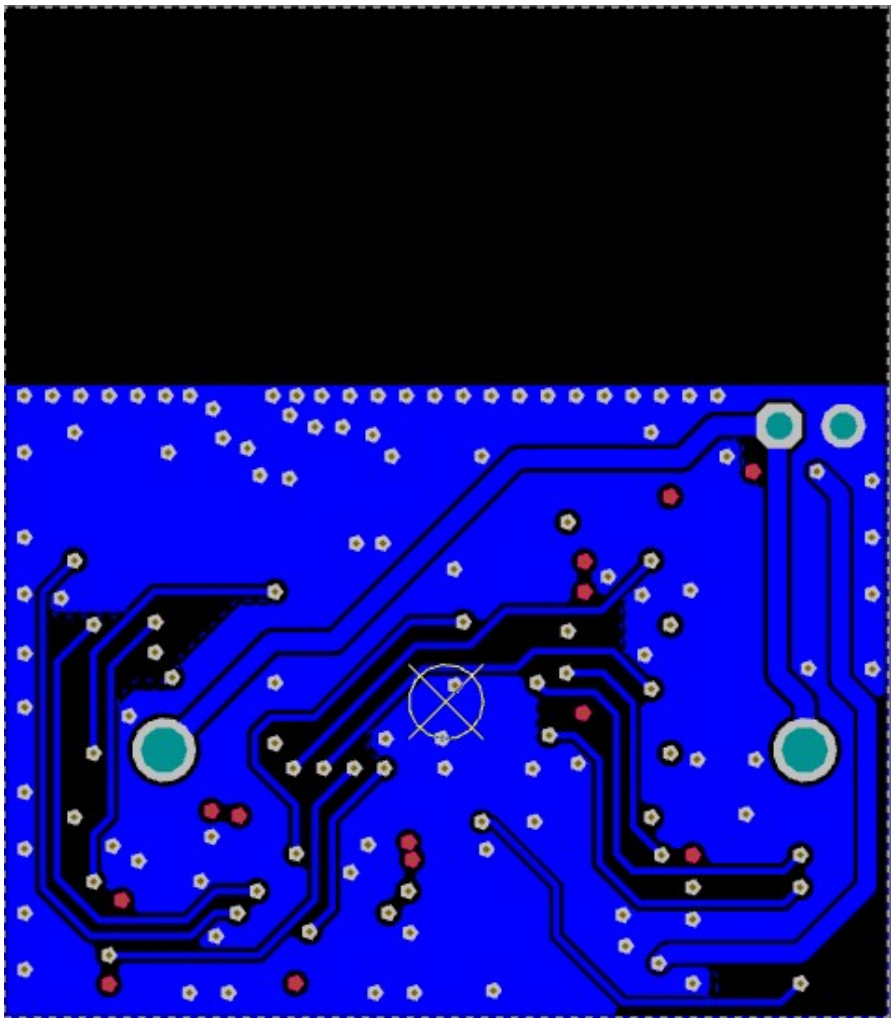
The following figure shows the top layer layout of the reference host Sensor board focussed on RF traces and PCB antenna. The snapshot also indicates the critical dimensions that are required to be replicated in the design to maintain compliance.

Figure 12-11. Top Layer Layout of the Reference Board



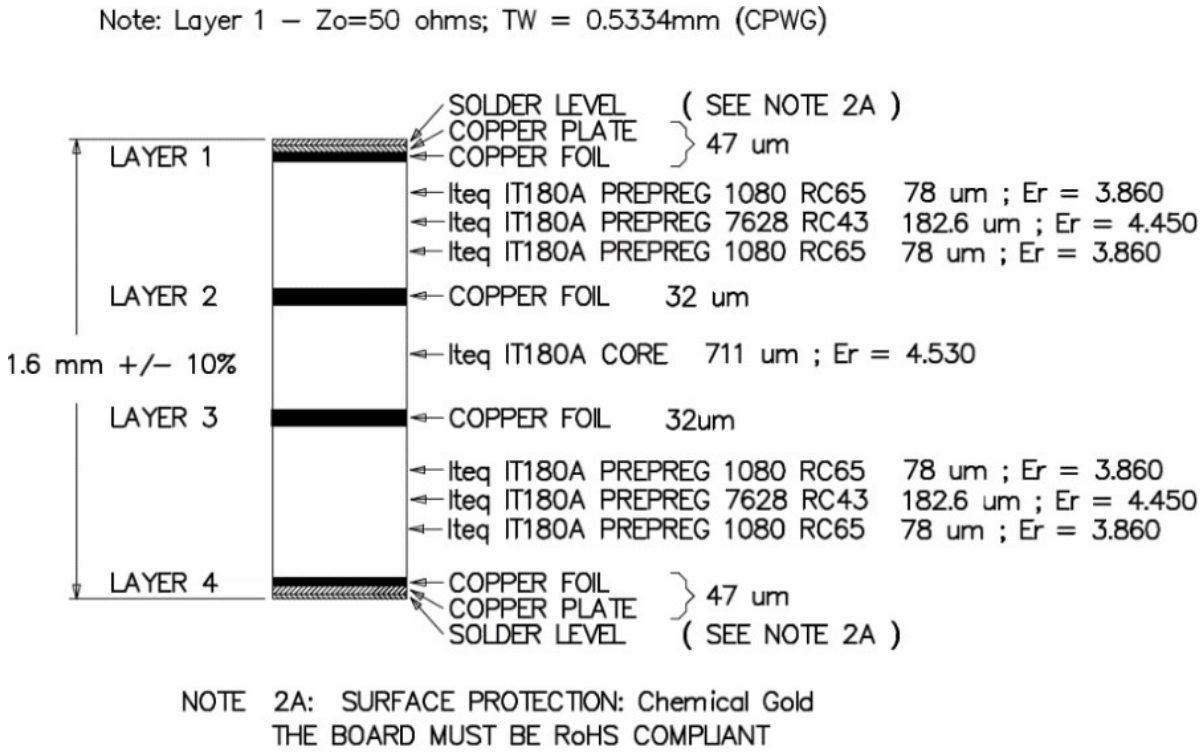
The following figure shows the bottom layer layout of the reference board directly beneath the RF traces.

Figure 12-12. Bottom Layer Layout of the Reference Board



The following figure shows the PCB stack-up for the reference board. Layer 1 (Top layer) and Layer 2 specifications are critical to the RF Trace Layout specification.

Figure 12-13. PCB Stack-up for the Reference Board



12.1.2.1 Test Procedure for Ensuring Compliance

The following test procedure must be performed both at design verification stage and in production to ensure compliance.

- Initiate Continuous Transmission in the appropriate modulation mode from the device, in other words, 868.3 MHz; BPSK-20 for European band and 914 MHz; BPSK-ALT-40 for North American band.
- Remove the 0Ω resistor mounted at L2 to isolate the PCB antenna and verify the RF power through conducted measurement at pad1 of L2.

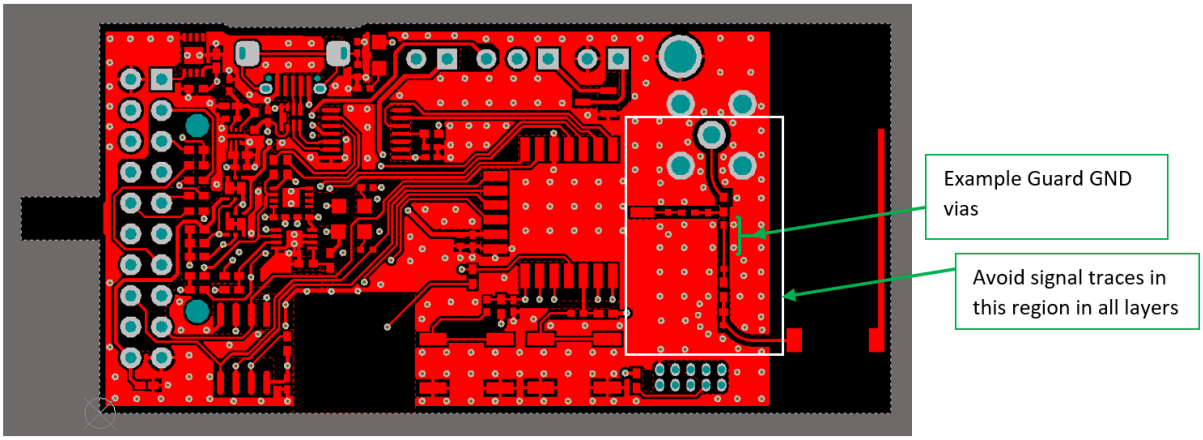
12.2 Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- Follow the RF trace design as highlighted in RF Trace Layout Design Instructions for leveraging the ATSAMR30M18A certifications.
- In a four or higher layer PCB design, dedicate the layer immediately below the layer containing the ATSAMR30M18A module for GND.
- Avoid routing any traces in the region on the top layer of the host board which will be directly below the module area.
- Place GND polygon pour below the module covering the entire area. Do not have any breaks in this GND plane. Place sufficient GND vias in this polygon pour for better RF performance.
  For optimal performance, the GND plane of the host board must have an minimum area of:
  - 30 mm x 35 mm (for chip antenna - 0900AT43A0070)
  - 70 mm x 50 mm (for external antenna - W1910)
  - 101 mm x 101 mm (for external antenna - ANT-916-CW-QW-SMA)
- Place at least one GND via next to the GND module pinout.
- The RF trace from RF OUT of the ATSAMR30M18A module to the antenna feed point must be 50Ω single ended controlled impedance trace.

- Place guard GND vias along the RF trace running from module to feed point of the antenna, in the host PCB. The area directly below the RF trace must have a GND polygon pour, at least in the immediate layer below Top layer.
- Do not have any signal traces below/adjacent to the RF trace in the host PCB. This is applicable to all layers below the highlighted region in the following image.
- Do not use thermal relief pads for the GND pads of all components in the RF path. These component pads must be completely filled with GND copper polygon. Place individual vias to the GND pads of these components.
- It is recommended that the antenna in the host board not be placed in direct contact or close proximity to plastic casing/objects. Keep a minimum clearance of >7 mm in all directions around the antenna.
- Do not enclose the antenna in the host board within a metal shield.
- Keep any components which may radiate noise or signals within the 850-950 MHz frequency band away from the antenna and if possible, shield those components. Any noise radiated from the host board in this frequency band degrades the sensitivity of the module.
- Make sure the width of the traces routed to GND and VCC rails are larger for handling the peak TX current consumption.

Figure 12-14. Top Layer Routing



13. Regulatory Approval

The ATSAMR30M18A has received the regulatory approval from the following countries:

- United States/FCC ID: 2ADHKR30M
- Canada
  - IC: 20266-R30M
  - HVIN: ATSAMR30M18A
  - PMN: ATSAMR30M18A
- Europe - CE

For USA/Canada, the module has been certified for the modulation modes listed below. The user must ensure that the module will only work on the 902-928 MHz frequency band and with one of the modulation modes listed below, when used in USA and Canada.

- BPSK-ALT-40(1)
- OQPSK-SIN-250(1)
- OQPSK-SIN-500
- OQPSK-SIN-1000-SCR-ON(1)

The host product manufacturer must ensure that the RF behavior adheres to the certification (e.g. FCC, ISED) requirements when the module is installed in the final host product.

For Europe, the module has been certified for the modulation modes listed below. The user must ensure that the module will only work on the 868-868.6 MHz frequency band and with one of the modulation modes listed below, when used in Europe. For OQPSK-SIN-RC-100/200/400 modes, the maximum certified TX_PWR setting is 9.

- BPSK-20(1)
- OQPSK-SIN-RC-100(1)
- OQPSK-SIN-RC-200
- OQPSK-SIN-RC-400

Note:

1. Tests are done for only these modes which are chosen as the worst case modes.

The availability of some specific channels and/or operating frequency bands are country dependent and should be programmed at the Host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via Host implementation.

13.1 United States (FCC)

The ATSAMR30M18A module has received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C “Intentional Radiators” modular approval in accordance with Part 15.212 Modular Transmitter approval. Modular approval allows the end user to integrate the ATSAMR30M18A module into a finished product without obtaining subsequent and separate FCC approvals for intentional radiation, provided no changes or modifications are made to the module circuitry. Changes or modifications could void the user’s authority to operate the equipment.

The user must comply with all of the instructions provided by the Grantee, which indicate the installation and/or operating conditions necessary for compliance.

The finished product is required to comply with all applicable FCC equipment authorization regulations, requirements and equipment functions that are not associated with the transmitter module portion. For example, compliance must be demonstrated: to regulations for other transmitter components within a host product; to requirements for unintentional radiators (Part 15 Subpart B), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non transmitter functions on the transmitter module (i.e., SDoC or certification) as appropriate (e.g., Bluetooth and Wi-Fi® transmitter modules may also contain digital logic functions).

13.1.1 Labeling and User Information Requirements

Due to the limited module size of ATSAMR30M18A (12.7 mm x 11 mm), the FCC identifier is displayed only in the datasheet and packaging box label. FCC identifier cannot be displayed on the module label. When the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label should use the following wording:

For the ATSAMR30M18A:

> Contains Transmitter Module FCC ID: 2ADHKR30M
>
> or
>
> Contains FCC ID: 2ADHKR30M
>
> This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

A user's manual for the finished product should include the following statement:

> This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
>
> - Reorient or relocate the receiving antenna
> - Increase the separation between the equipment and receiver
> - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
> - Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) apps.fcc.gov/oetcf/kdb/index.cfm

13.1.2 RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power listed is conducted. This grant is valid only when the module is sold to OEM integrators and must be installed by the OEM or OEM integrators. This transmitter is restricted for use with the specific antenna(s) tested in this application for Certification and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with FCC multi-transmitter product procedures.

These modules are approved for installation into mobile or/and portable host platforms.

This module can only be used with a host antenna circuit trace layout design in strict compliance with the OEM instructions provided.

13.1.3 Approved Antennas

To maintain modular approval in the United States, only the antenna types that were tested shall be used. Testing of the ATSAMR30M18A module was performed with the antenna types listed in Table 11-1.

According to KDB 178919 (Policy), it is allowed to substitute approved antennas through equivalent antennas of the same type with equal or less antenna gain:

'Equivalent antennas must be of the same type (e.g., yagi, dish, etc.), must be of equal or less gain than an antenna previously authorized under the same FCC ID, and must have similar in band and out-of-band characteristics (consult specification sheet for cutoff frequencies).'

13.1.4 Module Integration in the Host Product

Host products are to ensure continued compliance as per KDB 996369 Module Integration Guide.

13.1.5 Helpful Websites

Federal Communications Commission (FCC): www.fcc.gov/.

FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB): apps.fcc.gov/oetcf/kdb/index.cfm.

13.2 Canada (ISED)

The ATSAMR30M18A module has been certified for use in Canada under Innovation, Science, and Economic Development (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

13.2.1 Labeling and User Information Requirements

Labeling Requirements (from RSP-100 - Issue 12, Section 5): The host product shall be properly labeled to identify the module within the host device.

Due to the limited module size of ATSAMR30M18A (12.7 mm x 11 mm), the Innovation, Science, and Economic Development Canada certification number identifier is displayed only in the datasheet and packaging box label, and it cannot be displayed on the module. Therefore, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number of the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:

• For ATSAMR30M18A:
Contains IC: 20266-R30M

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 5, February 2021): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

This device contains license-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's license-exempt RSS(s). Operation is subject to the following two conditions:

(1) This device may not cause interference;

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage;

2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Transmitter Antenna (From Section 6.8 RSS-GEN, Issue 5, February 2021): User manuals, for transmitters shall display the following notice in a conspicuous location:

This radio transmitter [IC: 20266-R30M] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Le présent émetteur radio [IC: 20266-R30M] a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés cidessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué pour tout type figurant sur la liste, sont strictement interdits pour l'exploitation de l'émetteur.

Immediately following the above notice, the manufacturer shall provide a list of all antenna types approved for use with the transmitter, indicating the maximum permissible antenna gain (in dBi) and required impedance for each.

13.2.2 RF Exposure

All transmitters regulated by Innovation, Science and Economic Development Canada (ISED) must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radiocommunication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

The device operates at an output power level which is within ISED SAR test exemption limits at any user distance.

13.2.3 Approved Antennas

The testing of the ATSAMR30M18A module was performed with the antenna types listed in Table 11-1.

13.2.4 Helpful Websites

Innovation, Science and Economic Development Canada (ISED): www.ic.gc.ca/

13.3 Europe

The ATSAMR30M18A is a Radio Equipment Directive (RED) assessed radio module that is CE marked and has been manufactured and tested with the intention of being integrated into a final product.

The ATSAMR30M18A module has been tested to RED 2014/53/EU Essential Requirements mentioned in the following European Compliance table.

Table 13-1. European Compliance

Certification	Standards	Article
Safety	EN 62368	3.1a
Health	EN 62479	
EMC	EN 301 489-1	3.1b
	EN 301 489-3	
Radio	EN 300 220	3.2

The ETSI provides guidance on modular devices in the "*Guide to the application of harmonised standards covering articles 3.1b and 3.2 of the RED 2014/53/EU (RED) to multi-radio and combined radio and non-radio equipment*" document available at http://www.etsi.org/deliver/etsi_eg/203300_203399/20 3367/01.01.01_60/eg_203367v010101p.pdf.

Note: To maintain conformance to the standards listed in the preceding European Compliance table, the module shall be installed in accordance with the installation instructions in this data sheet and shall not be modified. When integrating a radio module into a completed product, the integrator becomes the manufacturer of the final product and is therefore responsible for demonstrating compliance of the final product with the essential requirements against the RED.

13.3.1 Labeling and User Information Requirements

The label on the final product that contains the ATSAMR30M18A module must follow CE marking requirements.

13.3.2 Conformity Assessment

From ETSI Guidance Note EG 203367, section 6.1, when non-radio products are combined with a radio product:

If the manufacturer of the combined equipment installs the radio product in a host non-radio product in equivalent assessment conditions (i.e. host equivalent to the one used for the assessment of the radio product) and according to the installation instructions for the radio product, then no additional assessment of the combined equipment against article 3.2 of the RED is required.

13.3.2.1 Simplified EU Declaration of Conformity

Hereby, Microchip Technology Inc. declares that the radio equipment type ATSAMR30M18A is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity for this product is available at www.microchip.com/wwwproducts/en/ATSAMR30M18 (available under *Documents* > *Certifications*).

13.3.3 Approved Antennas

The testing of the ATSAMR30M18A module was performed with the antenna types listed in Table 11-1.

13.3.4 Helpful Websites

A document that can be used as a starting point in understanding the use of Short Range Devices (SRD) in Europe is the European Radio Communications Committee (ERC) Recommendation 70-03 E, which can be downloaded from the European Communications Committee (ECC) at: http://www.ecodocdb.dk/.

Additional helpful web sites are:

- Radio Equipment Directive (2014/53/EU):
  https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/red_en
- European Conference of Postal and Telecommunications Administrations (CEPT):
  http://www.cept.org
- European Telecommunications Standards Institute (ETSI):
  http://www.etsi.org
- The Radio Equipment Directive Compliance Association (REDCA):
  http://www.redca.eu/

14. Continuous Transmission Test Mode Errata

14.1 Overview

The AT86RF212B offers a Continuous Transmission Test Mode to support application and production tests as well as certification tests. Using this test mode, the radio transceiver transmits continuously a previously transferred frame (PRBS mode) or a continuous wave signal (CW mode).

The AT86RF212B uses I/Q modulation for both, PRBS mode and CW mode. In CW mode, this results in a signal which is not placed at the selected channel center frequency F_C, but at 0.1 or 0.25 MHz apart this frequency. One out of four different signal frequencies per channel can be transmitted:

- $f_1 = F_C + 0.25$ MHz using O-QPSK 1000 kb/s mode
- $f_2 = F_C – 0.25$ MHz using O-QPSK 1000 kb/s mode
- $f_3 = F_C + 0.1$ MHz using O-QPSK 400 kb/s mode
- $f_4 = F_C – 0.1$ MHz using O-QPSK 400 kb/s mode

As a side effect of I/Q modulation, CW mode shows some unwanted signal components based on finite image rejection and non-linearities.

In addition to the above mentioned modes, there is a CW mode that directly uses the PLL signal without I/Q modulation. This is the recommended mode because the signal is placed at the selected channel center frequency F_C and unwanted signal components are significantly lower.

PRBS mode requires data in the frame buffer, that is a valid PHR followed by PSDU data. After transmission of two non-PSDU octets, PSDU data is repeated continuously.

14.2 Configuration

The tables below show detailed programming sequences for PRBS, CW and additional CW mode. The R/W column indicates writing (W) or reading (R) a register or the Frame Buffer.

Table 14-1. PRBS and CW Mode Programming Sequence

Step	Action	Register	R/W	Value	Description
1	RESET	—	—	—	Reset AT86RF212B
2	Register access	0x0E	W	0x01	Set IRQ mask register, enable IRQ_0 (PLL_LOCK)
3	Register access	0x02	W	0x03	Set radio transceiver state TRX_OFF
4	Register access	—	W	—	Set channel
5	Register access	—	W	—	Set TX output power. For CW mode, it is recommended GC_TX_OFFS be set to three(1).
6	Register access	0x01	R	0x08	Verify TRX_OFF state
7	Register access	0x36	W	0x0F	—

.....continued

Step	Action	Register	R/W	Value	Description
8	Register access	0x0C	W	0x00 0x04 0x08 0x0C 0x1C 0x0A 0x0E	Select PRBS mode with modulation scheme or CW mode with carrier position: PRBS mode, BPSK-20 PRBS mode, BPSK-40 PRBS mode, OQPSK-SIN-RC-100 PRBS mode, OQPSK-SIN-250 PRBS mode, OQPSK-RC-250 CW mode, CW at Fc – 0.1 MHz or CW at Fc + 0.1 MHz, see step 9 CW mode, CW at Fc – 0.25 MHz or CW at Fc + 0.25 MHz, see step 9
9	Frame Buffer write access	—	W	{PHR, PSDU} {0x01,0x00}{0x01, 0xFF}{0x01, 0x00} {0x01, 0xFF}	PRBS mode: Write PHR value (0x01 … 0x7F) followed by PSDU data. PHR determines how many bytes of the PSDU data are repeated continuously. CW mode, CW at Fc – 0.1 MHz CW mode, CW at Fc + 0.1 MHz CW mode, CW at Fc – 0.25 MHz CW mode, CW at Fc + 0.25 MHz
10	Register access	0x1C	W	0x54	—
11	Register access	0x1C	W	0x46	—
12	Register access	0x02	W	0x09	Enable PLL_ON state
13	Interrupt event	0x0F	R	0x01	Wait for IRQ_0 (PLL_LOCK)
14	Register access	0x02	W	0x02	Initiate transmission, enter BUSY_TX state
15	Measurement	—	—	—	Perform measurement
16	Register access	0x1C	W	0x00	Disable Continuous Transmission Test Mode
17	Reset	—	—	—	Reset AT86RF212B

Table 14-2. Additional CW Mode Programming Sequence

Step	Action	Register	R/W	Value	Description
1	Reset	—	—	—	Reset AT86RF212B rev. C
2	Register access	0x0E	W	0x01	Set IRQ mask register, enable IRQ_0 (PLL_LOCK)
3	Register access	0x02	W	0x03	Set radio transceiver state TRX_OFF
4	Register access	—	W	—	Set channel
5	Register access	—	W	—	Set TX output power. For CW mode, set GC_TX_OFFS to three(1).
6	Register access	0x01	R	0x08	Verify TRX_OFF state

.....continued					
Step	**Action**	**Register**	**R/W**	**Value**	**Description**
7	Register access	0x36	W	0x0F	—
8	Register access	0x1C	W	0x54	—
9	Register access	0x1C	W	0x42	—
10	Register access	0x34	W	0x00	—
11	Register access	0x3F	W	0x08	—
12	Register access	0x02	W	0x09	Enable PLL_ON state
13	Interrupt event	0x0F	R	0x01	Wait for IRQ_0 (PLL_LOCK)
14	Register access	0x02	W	0x02	Initiate transmission, enter BUSY_TX state
15	Measurement	—	—	—	Perform measurement
16	Register access	0x1C	W	0x00	Disable Continuous Transmission Test Mode
17	Reset	—	—	—	Reset AT86RF212B rev. C

1. Changing the output power during continuous transmission is not allowed.

15. Reference Documentation

The following table provides the set of collateral documents to ease integration and device ramp.

Table 15-1. Reference Documents

Title	Content
IEEE Standard 802.15.4™–2003	Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs).
IEEE Standard 802.15.4™–2006	Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs).
IEEE Standard 802.15.4c™–2009	Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs): Amendment 2: Alternative Physical Layer Extension to support one or more of the Chinese 314-316 MHz, 430-434 MHz and 779-787 MHz bands.
IEEE Standard 802.15.4™–2011	Low-Rate Wireless Personal Area Networks (WPANs).
ATSAMR30E18A Data Sheet	IEEE 802.15.4 Sub-GHz System in Package Datasheet.
ATSAMR30M18A Product Page	SAMR30 module's product page
SAMR30 Module Xplained Pro Design Documentation	Provides the complete design documentation of the reference board.
ATSAMR30M Sensor Board Design Documentation	Provides the complete design documentation of the reference board.
Solder Reflow Recommendation	Provides guidelines for the reflow process in soldering the module to the customer's design.

16. Document Revision History

Revision	Date	Section	Description
C	11/2022	Introduction	Removed support for Chinese band
		Features	Removed support for Chinese and Japanese bands
		3.2. AT86RF212B Transceiver Circuit Description	Removed support for Chinese band
		7.3.3. TX Output Power	Removed support for Chinese band
		7.3.4. TX Power Ramping	Removed support for Chinese band
		7.6.2. RF Channel Selection	Removed support for Chinese band
		9.3.3. Receiver Characteristics	Updated the section
B	07/2021	7.1.1. Spreading, Modulation and Pulse Shaping	Editorial updates
		12. Application Reference Design	• Updated the Chip antenna and external antenna details • Added PCB antenna details and its test procedure • Updated the figure with DNP details
		10.2. Footprint	Updated Recommended Base Board Footprint
		11.1. Approved Antennas	Updated the antenna details
		13.1.3. Approved Antennas	Updated antenna details for FCC
		13.1.4. Module Integration in the Host Product	Added new section
		13.1.5. Helpful Websites	Updated the section
		13.3. Europe	Updated the CE certification details
		13.1.1. Labeling and User Information Requirements	Updated the date of amendment for RSS-Gen
A	12/2018	Document	Initial release

Note: Microchip is aware that some terminologies used in the technical documents and existing software codes of this product are outdated and unsuitable. This document may use these new terminologies, which may or may not reflect on the source codes, software GUIs, and the documents referenced within this document. The following table shows the relevant terminology changes made in this document.

Table 16-1. Terminology Related Changes

Old Terminology	New Terminology	Section
LIN Slave	LIN Client	Features is updated with the new terminology.
Slave SPI	Client SPI	3.1. Interconnection between SAM L21 and AT86RF212B within ATSAMR30E18A SiP is updated with the new terminology.
Master SPI	Host SPI	
Master output	Host output	
Master input	Host input	

.....continued		
Old Terminology	**New Terminology**	**Section**
SPI (Slave)	SPI (Client)	3.2. AT86RF212B Transceiver Circuit Description is updated with the new terminology.
Master clock	Host clock	7.4. Frame Buffer is updated with the new terminology.
SPI_Slave	SPI_Client	8.2. Frame Transmit Procedure is updated with the new terminology.

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