SAMA5D27 MPU, 1Gbit (128MB) DDR2 SDRAM, 10/100 Ethernet PHY, 64Mbit (8MB) Flash, Power Management IC, 1Kbit EEPROM

SAMA5D27 SOM1

Introduction

The Microchip SAMA5D27 SOM1 is a small single-sided System-On-Module (SOM) based on the high-performance System-in-Package 32-bit Arm® Cortex®-A5 processor-based MPU SAMA5D27 and 1Gb DDR2 SDRAM running up to 500 MHz.

The SAMA5D27 SOM1 is built on a common set of proven Microchip components to reduce time to market by simplifying hardware design and software development.

The SOM also limits design rules of the main application board, reducing overall PCB complexity and cost. The SAMA5D27 SOM1 is delivered with a free Linux® distribution and bare metal C examples.

Figure 1. SAMA5D27 SOM1

Features

- System-in-Package (SAMA5D27C-D1G-CU) including:
  - Arm Cortex-A5 processor-based SAMA5D2 MPU
  - 1 Gbit DDR2 SDRAM
- On-Board Power Management Unit (MIC2800-G1JJYML)
- 1 Kb Serial EEPROM with EUI-48™ Node Identity (24AA02E48T-I/OT)
- 64 Mb Serial Quad I/O Flash Memory (SST26VF064BT-104I/MF)
- 10Base-T/100Base-TX Ethernet PHY (KSZ8081RNAIA)
- 40 x 38 mm Module, Pitch 0.8 mm, solderable by hand

- 103 I/Os
- Up to 7 Tampers
- One USB Device, One USB Host and One HSIC Interface
- Shutdown and Reset Control Pins
- Up to 24-bit LCD Interface
- Independent Power Supplies Available for Camera Sensor, for SD Card and for Backup depending on Voltage Domains
- Operational Specifications:
  - Main operating voltage: 3.3V ± 5%
  - Temperature range: -40°C to 85°C
  - Integrated crystals, internal voltage regulators
  - Multiple interfaces and I/Os for easy application development

Applications

- Healthcare/Patient Monitoring
- IoT Secure Gateways
- Human Machine Interface, Control Panel
- Home and Building Automation, Thermostat, Industrial Gateways

1.   Description

The SAMA5D27 SOM1 is a high-performance System-On-Module based on the 32-bit ARM Cortex-A5 RISC SAMA5D2 processor. The SAMA5D27 SOM1 is certified for industrial operating conditions over a -40 to 85°C temperature range.

The system of the SAMA5D27 SOM1 operates at a maximum CPU operating frequency of 500 MHz and a maximum bus speed of 166 MHz. It features up to:

- 1 Gbit of DDR2 SDRAM memory (SAMA5D27C-D1G-CU)
- 1 Kb of EEPROM memory (24AA02E48T-I/OT) with EUI-48
- 64 Mb of QSPI Flash (SST26VF064BT-104I/MF) memory

The SAMA5D27 SOM1 is a 176-pin, 0.8mm pad pitch module, 40 mm x 38 mm in size.

The SAMA5D27 SOM1 offers an extensive peripheral set, including High-speed USB Host and Device, HSIC Interface, 10Base-T/100Base-TX Ethernet Interface, system control and up to 103 I/Os featuring:

- Up to 4 UARTs
- Up to 4 FLEXCOMs
- Up to 6 capacitive touch lines for up to 9 touch buttons
- Up to 10 ADC inputs
- Up to 2 CAN interfaces
- Up to 7 tamper pins
- Serial interfaces such as SPI, TWI, QSPI, SSC and I²S
- SD/MMC, eMMC, SDIO interfaces
- Up to 24-bit LCD RGB interface
- CMOS camera interface
- Mono PDMIC and Full-Bridge Class-D Stereo
- Up to 6 capacitive touch lines

> **Tip:** Each I/O of the SAMA5D27 SOM1 is configurable, as either a general-purpose I/O line only, or as an I/O line multiplexed with up to six peripheral I/Os. As the multiplexing is hardware-defined, the hardware designer and programmer must carefully determine the configuration of the PIO Controllers required by their application.


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2. Reference Documents

The SAMA5D27 SOM1 is equipped with various Microchip silicon devices. The relevant documentation is listed in the table below.

Type	Document Title	Available	Ref. No./Product
Data sheet	SAMA5D2	www.microchip.com/SAMA5D2	DS60001476
Data sheet	SAMA5D2 System-in-Package (SiP)	www.microchip.com/SAMA5D2 SiP	DS60001484
Data sheet	Serial EEPROMs with EUI-48 Node Identity	www.microchip.com/24AA02E48	24AA02E48T-I/OT
Data sheet	10BASE-T/100BASE-TX Ethernet PHY	www.microchip.com/ksz8081	KSZ8081RNAIA
Data sheet	Serial Quad I/O (SQI) Flash Memory	www.microchip.com/sst26vf064b	SST26VF064BT-104I/MF
Data sheet	Digital Power Management IC	www.microchip.com/mic2800	MIC2800-G1JJYML

3.   Block Diagram

**Figure 3-1.** SAMA5D27 SOM1 Block Diagram
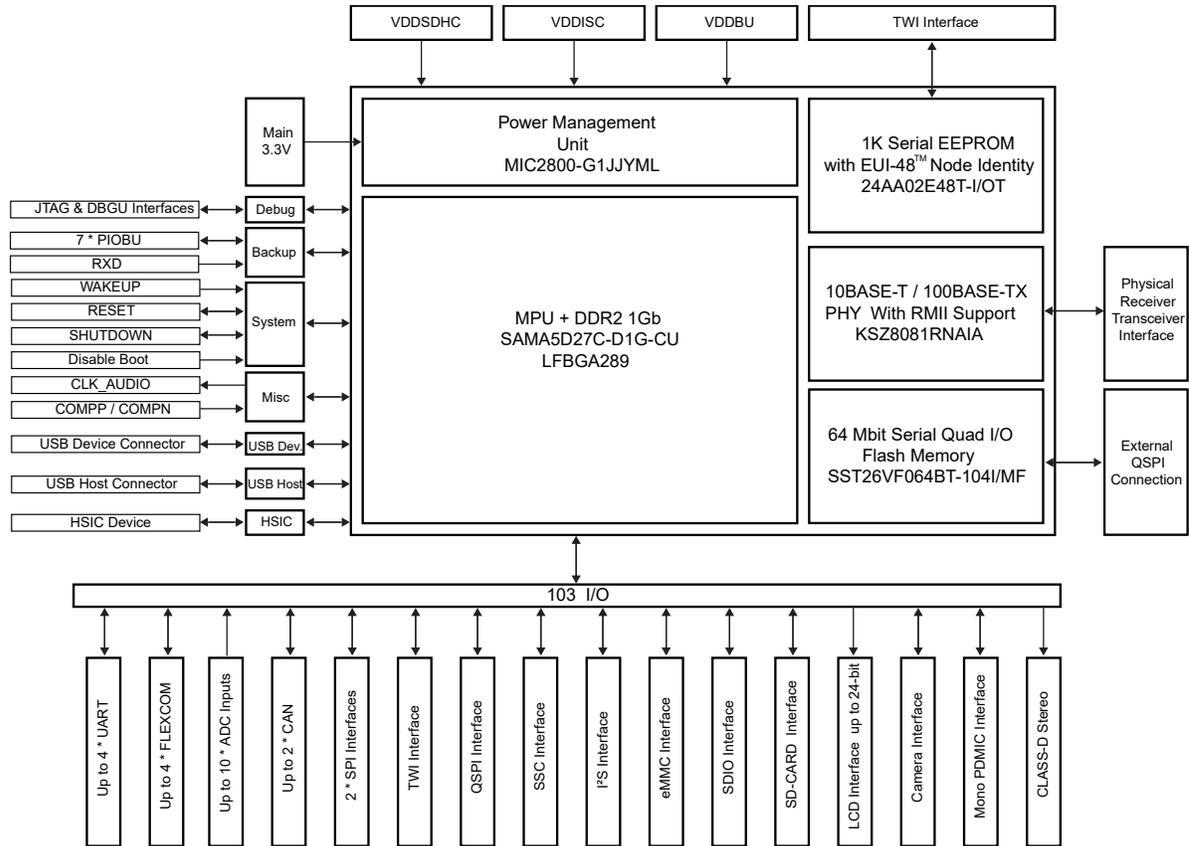
4. Pinout

4.1 Pinout Overview

The categories of pins are listed below:

- Red: Power Supplies
- Black: Ground
- Blue: Signals
- Orange: Reserved for future use

Figure 4-1. SAMA5D27 SOM1 Pinout Overview
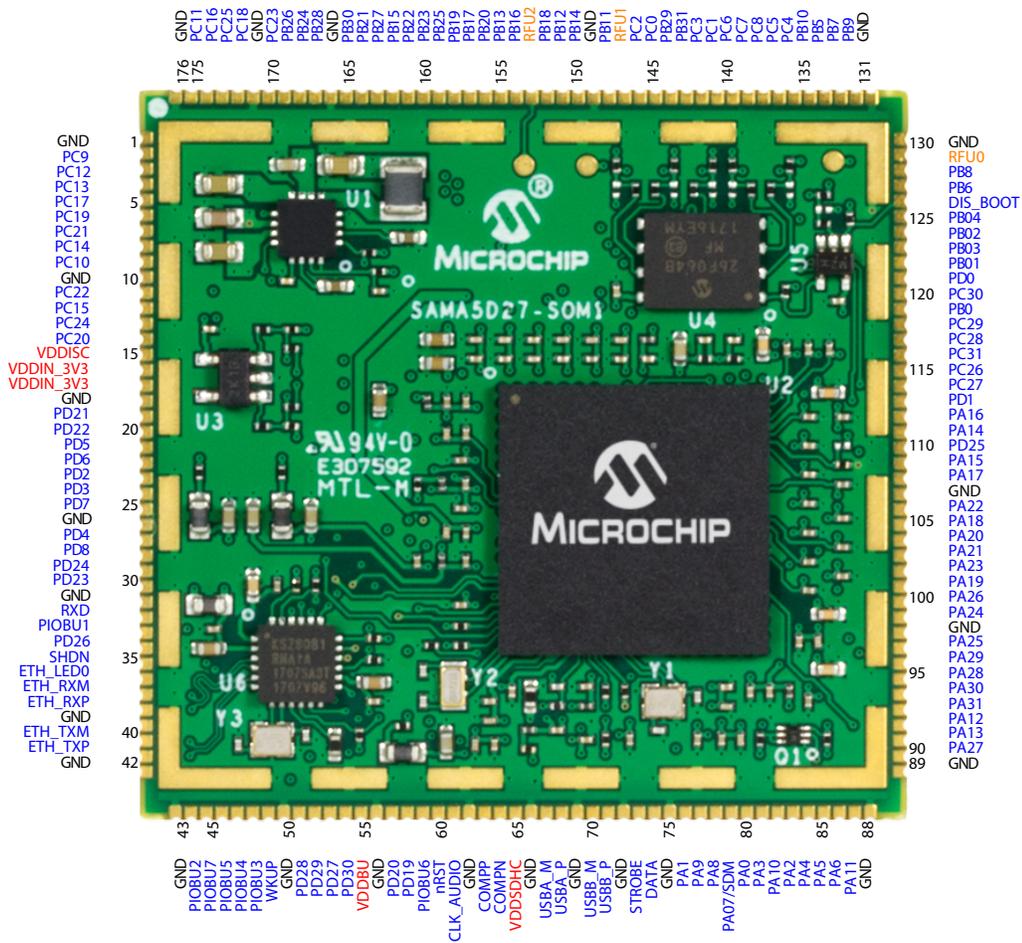
4.2 Pin List

The pin list of the SAMA5D27 SOM1 is provided in the following tables.

Important: Compared to SAMA5D2 Series devices, some PIO features are not listed. These features are used internally on the SOM and cannot be shared with other PIOs for purposes of features or signal integrity.

4.2.1 PIOA Pin Description

Table 4-1. System-On-Module Pin Description: PIOA

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
80	VDDSDHC	GPIO_EMMC	PA0	I/O	–	–	A	SDMMC0_CK	I/O	1	PIO, I, PU, ST
							B	QSPI0_SCK	O	1	
							F	D0	I/O	2	
76	VDDSDHC	GPIO_EMMC	PA1	I/O	–	–	A	SDMMC0_CMD	I/O	1	PIO, I, PU, ST
							B	QSPI0_CS	O	1	
							F	D1	I/O	2	
83	VDDSDHC	GPIO_EMMC	PA2	I/O	–	–	A	SDMMC0_DAT0	I/O	1	PIO, I, PU, ST
							B	QSPI0_IO0	I/O	1	
							F	D2	I/O	2	
81	VDDSDHC	GPIO_EMMC	PA3	I/O	–	–	A	SDMMC0_DAT1	I/O	1	PIO, I, PU, ST
							B	QSPI0_IO1	I/O	1	
							F	D3	I/O	2	
84	VDDSDHC	GPIO_EMMC	PA4	I/O	–	–	A	SDMMC0_DAT2	I/O	1	PIO, I, PU, ST
							B	QSPI0_IO2	I/O	1	
							F	D4	I/O	2	
85	VDDSDHC	GPIO_EMMC	PA5	I/O	–	–	A	SDMMC0_DAT3	I/O	1	PIO, I, PU, ST
							B	QSPI0_IO3	I/O	1	
							F	D5	I/O	2	
86[2]	VDDSDHC	GPIO_EMMC	PA6	I/O	–	–	A	SDMMC0_DAT4	I/O	1	PIO, I, PU, ST
							D	TIOA5	I/O	1	
							E	FLEXCOM2_IO0	I/O	1	
							F	D6	I/O	2	
79[2]	VDDSDHC	GPIO_EMMC	PA7	I/O	–	–	A	SDMMC0_DAT5	I/O	1	PIO, I, PU, ST
							D	TIOB5	I/O	1	
							E	FLEXCOM2_IO1	I/O	1	
							F	D7	I/O	2	
78[2]	VDDSDHC	GPIO_EMMC	PA8	I/O	–	–	A	SDMMC0_DAT6	I/O	1	PIO, I, PU, ST
							D	TCLK5	I	1	
							E	FLEXCOM2_IO2	I/O	1	
							F	NWE/NANDWE	O	2	
77[2]	VDDSDHC	GPIO_EMMC	PA9	I/O	–	–	A	SDMMC0_DAT7	I/O	1	PIO, I, PU, ST
							D	TIOA4	I/O	1	
							E	FLEXCOM2_IO3	O	1	
							F	NCS3	O	2	

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
82[2]	VDDSDHC	GPIO_EMMC	PA10	I/O	–	–	A	SDMMC0_RSTN	O	1	PIO, I, PU, ST
							D	TIOB4	I/O	1	
							E	FLEXCOM2_IO4	O	1	
							F	A21/NANDALE	O	2	
87[2]	VDDIN_3V3	GPIO	PA11	I/O	–	–	A	SDMMC0_VDDSEL	O	1	PIO, I, PU, ST
							D	TCLK4	I	1	
							F	A22/NANDCLE	O	2	
92	VDDIN_3V3	GPIO	PA12	I/O	–	–	A	SDMMC0_WP	I	1	PIO, I, PU, ST
							B	IRQ	I	1	
							F	NRD/NANDOE	O	2	
91	VDDIN_3V3	GPIO	PA13	I/O	–	–	A	SDMMC0_CD	I	1	PIO, I, PU, ST
							E	FLEXCOM3_IO1	I/O	1	
							F	D8	I/O	2	
111	VDDIN_3V3	GPIO_QSPI	PA14	I/O	–	–	A	SPI0_SPCK	I/O	1	PIO, I, PU, ST
							B	TK1	I/O	1	
							C	QSPI0_SCK	O	2	
							D	I2SMCK1	O	2	
							E	FLEXCOM3_IO2	I/O	1	
							F	D9	I/O	2	
109	VDDIN_3V3	GPIO	PA15	I/O	–	–	A	SPI0_MOSI	I/O	1	PIO, I, PU, ST
							B	TF1	I/O	1	
							C	QSPI0_CS	O	2	
							D	I2SCK1	I/O	2	
							E	FLEXCOM3_IO0	I/O	1	
							F	D10	I/O	2	
112	VDDIN_3V3	GPIO_IO	PA16	I/O	–	–	A	SPI0_MISO	I/O	1	PIO, I, PU, ST
							B	TD1	O	1	
							C	QSPI0_IO0	I/O	2	
							D	I2SWS1	I/O	2	
							E	FLEXCOM3_IO3	O	1	
							F	D11	I/O	2	
108	VDDIN_3V3	GPIO_IO	PA17	I/O	–	–	A	SPI0_NPCS0	I/O	1	PIO, I, PU, ST
							B	RD1	I	1	
							C	QSPI0_IO1	I/O	2	
							D	I2SDI1	I	2	
							E	FLEXCOM3_IO4	O	1	
							F	D12	I/O	2	
105	VDDIN_3V3	GPIO_IO	PA18	I/O	–	–	A	SPI0_NPCS1	O	1	PIO, I, PU, ST
							B	RK1	I/O	1	
							C	QSPI0_IO2	I/O	2	
							D	I2SDO1	O	2	
							E	SDMMC1_DAT0	I/O	1	
							F	D13	I/O	2	

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
101	VDDIN_3V3	GPIO_IO	PA19	I/O	–	–	A	SPI0_NPCS2	O	1	PIO, I, PU, ST
							B	RF1	I/O	1	
							C	QSPI0_IO3	I/O	2	
							D	TIOA0	I/O	1	
							E	SDMMC1_DAT1	I/O	1	
							F	D14	I/O	2	
104	VDDIN_3V3	GPIO_IO	PA20	I/O	–	–	A	SPI0_NPCS3	O	1	PIO, I, PU, ST
							D	TIOB0	I/O	1	
							E	SDMMC1_DAT2	I/O	1	
							F	D15	I/O	2	
103	VDDIN_3V3	GPIO_IO	PA21	I/O	–	–	A	IRQ	I	2	PIO, I, PU, ST
							B	PCK2	O	3	
							D	TCLK0	O	1	
							E	SDMMC1_DAT3	I/O	1	
							F	NANDRDY	I	2	
106	VDDIN_3V3	GPIO_QSPI	PA22	I/O	–	–	A	FLEXCOM1_IO2	I/O	1	PIO, I, PU, ST
							B	D0	I/O	1	
							C	TCK	I	4	
							D	SPI1_SPCK	I/O	2	
							E	SDMMC1_CK	I/O	1	
							F	QSPI0_SCK	O	3	
102	VDDIN_3V3	GPIO	PA23	I/O	–	–	A	FLEXCOM1_IO1	I/O	1	PIO, I, PU, ST
							B	D1	I/O	1	
							C	TDI	I	4	
							D	SPI1_MOSI	I/O	2	
							F	QSPI0_CS	O	3	
99	VDDIN_3V3	GPIO_IO	PA24	I/O	–	–	A	FLEXCOM1_IO0	I/O	1	PIO, I, PU, ST
							B	D2	I/O	1	
							C	TDO	O	4	
							D	SPI1_MISO	I/O	2	
							F	QSPI0_IO0	I/O	3	
97	VDDIN_3V3	GPIO_IO	PA25	I/O	–	–	A	FLEXCOM1_IO3	O	1	PIO, I, PU, ST
							B	D3	I/O	1	
							C	TMS	I	4	
							D	SPI1_NPCS0	I/O	2	
							F	QSPI0_IO1	I/O	3	
100	VDDIN_3V3	GPIO_IO	PA26	I/O	–	–	A	FLEXCOM1_IO4	O	1	PIO, I, PU, ST
							B	D4	I/O	1	
							C	NTRST	I	4	
							D	SPI1_NPCS1	O	2	
							F	QSPI0_IO2	I/O	3	

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Pad No.	Power Rail	I/O Type	Primary Signal	Primary Dir	Alternate Signal	Alternate Dir	PIO Peripheral Func	PIO Peripheral Signal	PIO Peripheral Dir	PIO Peripheral IO Set	Reset State (Signal, Dir, PU, PD, HiZ, ST)
90	VDDIN_3V3	GPIO_IO	PA27	I/O	–	–	A	TIOA1	I/O	2	PIO, I, PU, ST
							B	D5	I/O	1	
							C	SPI0_NPCS2	O	2	
							D	SPI1_NPCS2	O	2	
							E	SDMMC1_RSTN	O	1	
							F	QSPI0_IO3	I/O	3	
95	VDDIN_3V3	GPIO	PA28	I/O	–	–	A	TIOB1	I/O	2	PIO, I, PU, ST
							B	D6	I/O	1	
							C	SPI0_NPCS3	O	2	
							D	SPI1_NPCS3	O	2	
							E	SDMMC1_CMD	I/O	1	
							F	CLASSD_L0	O	1	
96	VDDIN_3V3	GPIO	PA29	I/O	–	–	A	TCLK1	I	2	PIO, I, PU, ST
							B	D7	I/O	1	
							C	SPI0_NPCS1	O	2	
							E	SDMMC1_WP	I	1	
							F	CLASSD_L1	O	1	
94	VDDIN_3V3	GPIO	PA30	I/O	–	–	B	NWE / NANDWE	O	1	PIO, I, PU, ST
							C	SPI0_NPCS0	I/O	2	
							D	PWMH0	O	1	
							E	SDMMC1_CD	I	1	
							F	CLASSD_L2	O	1	
93	VDDIN_3V3	GPIO	PA31	I/O	–	–	B	NCS3	O	1	PIO, I, PU, ST
							C	SPI0_MISO	I/O	2	
							D	PWML0	O	1	
							F	CLASSD_L3	O	1	

Notes:
1. Fixed feature due to the SOM internal connection.
2. Limited feature compared to SAMA5D2 due to the SOM internal use of specific functionality, for example, QSPI, GMAC.
3. Limited feature compared to SAMA5D2 due to the use of a part of the functionality for other features in the SOM, for example, GMAC, ISC, Flexcom, etc.

4.2.2 PIOB Pin Description

Table 4-2. System-On-Module Pin Description: PIOB

Pad No.	Power Rail	I/O Type	Primary Signal	Primary Dir	Alternate Signal	Alternate Dir	PIO Peripheral Func	PIO Peripheral Signal	PIO Peripheral Dir	PIO Peripheral IO Set	Reset State (Signal, Dir, PU, PD, HiZ, ST)
119	VDDIN_3V3	GPIO	PB0	I/O	–	–	B	A21 / NANDALE	O	1	PIO, I, PU, ST
							C	SPI0_MOSI	I/O	2	
							D	PWMH1	O	1	

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
122	VDDIN_3V3	GPIO	PB1	I/O	–	–	B	A22 / NANDCLE	O	1	PIO, I, PU, ST
							C	SPI0_SPCK	I/O	2	
							D	PWML1	O	1	
							F	CLASSD_R0	O	1	
124	VDDIN_3V3	GPIO	PB2	I/O	–	–	B	NRD/NANDOE	O	1	PIO, I, PU, ST
							D	PWMFI0	I	1	
							F	CLASSD_R1	O	1	
123	VDDIN_3V3	GPIO	PB3	I/O	–	–	A	URXD4	I	1	PIO, I, PU, ST
							B	D8	I/O	1	
							C	IRQ	I	3	
							D	PWMEXTRG0	I	1	
							F	CLASSD_R2	O	1	
125	VDDIN_3V3	GPIO	PB4	I/O	–	–	A	UTXD4	O	1	PIO, I, PU, ST
							B	D9	I/O	1	
							C	FIQ	I	4	
							F	CLASSD_R3	O	1	
134[2]	VDDIN_3V3	GPIO_QSPI	PB5	I/O	–	–	A	TCLK2	I	1	PIO, I, PU, ST
							C	PWMH2	O	1	
							D	QSPI1_SCK	O	2	
127[2]	VDDIN_3V3	GPIO	PB6	I/O	–	–	A	TIOA2	I/O	1	PIO, I, PU, ST
							C	PWML2	O	1	
							D	QSPI1_CS	O	2	
133[2]	VDDIN_3V3	GPIO_IO	PB7	I/O	–	–	A	TIOB2	I/O	1	PIO, I, PU, ST
							C	PWMH3	O	1	
							D	QSPI1_IO0	I/O	2	
128[2]	VDDIN_3V3	GPIO_IO	PB8	I/O	–	–	A	TCLK3	I	1	PIO, I, PU, ST
							C	PWML3	O	1	
							D	QSPI1_IO1	I/O	2	
132[2]	VDDIN_3V3	GPIO_IO	PB9	I/O	–	–	A	TIOA3	I/O	1	PIO, I, PU, ST
							C	PWMFI1	I	1	
							D	QSPI1_IO2	I/O	2	
135[2]	VDDIN_3V3	GPIO_IO	PB10	I/O	–	–	A	TIOB3	I/O	1	PIO, I, PU, ST
							C	PWMEXTRG1	I	1	
							D	QSPI1_IO3	I/O	2	
148[3]	VDDIN_3V3	GPIO	PB11	I/O	–	–	A	LCDDAT0	O	1	PIO, I, PU, ST
							B	A0/NBS0	O	1	
							C	URXD3	I	3	
							D	PDMDAT0	I/O	2	
151[3]	VDDIN_3V3	GPIO	PB12	I/O	–	–	A	LCDDAT1	O	1	PIO, I, PU, ST
							B	A1	O	1	
							C	UTXD3	O	3	
							D	PDMCLK0	O	2	

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
155[3]	VDDIN_3V3	GPIO	PB13	I/O	–	–	A	LCDDAT2	O	1	PIO, I, PU, ST
							B	A2	O	1	
							C	PCK1	I/O	3	
150[2], [3]	VDDIN_3V3	GPIO_QSPI	PB14	I/O	–	–	A	LCDDAT3	O	1	PIO, I, PU, ST
							B	A3	O	1	
							C	TK1	I/O	2	
							D	I2SMCK1	O	1	
162[2], [3]	VDDIN_3V3	GPIO	PB15	I/O	–	–	A	LCDDAT4	O	1	PIO, I, PU, ST
							B	A4	O	1	
							C	TF1	I/O	2	
							D	I2SCK1	I/O	1	
154[2], [3]	VDDIN_3V3	GPIO_IO	PB16	I/O	–	–	A	LCDDAT5	O	1	PIO, I, PU, ST
							B	A5	O	1	
							C	TD1	O	2	
							D	I2SWS1	I/O	1	
157[2], [3]	VDDIN_3V3	GPIO_IO	PB17	I/O	–	–	A	LCDDAT6	O	1	PIO, I, PU, ST
							B	A6	O	1	
							C	RD1	I	2	
							D	I2SDI1	I	1	
152[2], [3]	VDDIN_3V3	GPIO_IO	PB18	I/O	–	–	A	LCDDAT7	O	1	PIO, I, PU, ST
							B	A7	O	1	
							C	RK1	I/O	2	
							D	I2SDO1	O	1	
158[2], [3]	VDDIN_3V3	GPIO_IO	PB19	I/O	–	–	A	LCDDAT8	O	1	PIO, I, PU, ST
							B	A8	O	1	
							C	RF1	I/O	2	
							D	TIOA3	I/O	2	
156[3]	VDDIN_3V3	GPIO	PB20	I/O	–	–	A	LCDDAT9	O	1	PIO, I, PU, ST
							B	A9	O	1	
							C	TK0	I/O	1	
							D	TIOB3	I/O	2	
							E	PCK1	O	4	
164[3]	VDDIN_3V3	GPIO	PB21	I/O	–	–	A	LCDDAT10	O	1	PIO, I, PU, ST
							B	A10	O	1	
							C	TF0	I/O	1	
							D	TCLK3	I	2	
							E	FLEXCOM3_IO2	I/O	3	
161[3]	VDDIN_3V3	GPIO	PB22	I/O	–	–	A	LCDDAT11	O	1	PIO, I, PU, ST
							B	A11	O	1	
							C	TD0	O	1	
							D	TIOA2	I/O	2	
							E	FLEXCOM3_IO1	I/O	3	

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
160[3]	VDDIN_3V3	GPIO	PB23	I/O	–	–	A	LCDDAT12	O	1	PIO, I, PU, ST
							B	A12	O	1	
							C	RD0	I	1	
							D	TIOB2	I/O	2	
							E	FLEXCOM3_IO0	I/O	3	
168	VDDIN_3V3	GPIO	PB24	I/O	–	–	A	LCDDAT13	O	1	PIO, I, PU, ST
							B	A13	O	1	
							C	RK0	I/O	1	
							D	TCLK2	I	2	
							E	FLEXCOM3_IO3	O	3	
							F	ISI_D10	I	3	
159	VDDIN_3V3	GPIO	PB25	I/O	–	–	A	LCDDAT14	O	1	PIO, I, PU, ST
							B	A14	O	1	
							C	RF0	I/O	1	
							E	FLEXCOM3_IO4	O	3	
							F	ISI_D11	I	3	
169	VDDIN_3V3	GPIO	PB26	I/O	–	–	A	LCDDAT15	O	1	PIO, I, PU, ST
							B	A15	O	1	
							C	URXD0	I	1	
							D	PDMDAT0	I/O	1	
							F	ISI_D0	I	3	
163	VDDIN_3V3	GPIO	PB27	I/O	–	–	A	LCDDAT16	O	1	PIO, I, PU, ST
							B	A16	O	1	
							C	UTXD0	O	1	
							D	PDMCLK0	O	1	
							F	ISI_D1	I	3	
167	VDDIN_3V3	GPIO	PB28	I/O	–	–	A	LCDDAT17	O	1	PIO, I, PU, ST
							B	A17	O	1	
							C	FLEXCOM0_IO0	I/O	1	
							D	TIOA5	I/O	2	
							F	ISI_D2	I	3	
144	VDDIN_3V3	GPIO	PB29	I/O	–	–	A	LCDDAT18	O	1	PIO, I, PU, ST
							B	A18	O	1	
							C	FLEXCOM0_IO1	I/O	1	
							D	TIOB5	I/O	2	
							F	ISI_D3	I	3	
165	VDDIN_3V3	GPIO	PB30	I/O	–	–	A	LCDDAT19	O	1	PIO, I, PU, ST
							B	A19	O	1	
							C	FLEXCOM0_IO2	I/O	1	
							D	TCLK5	I	2	
							F	ISI_D4	I	3	

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	(Signal, Dir, PU, PD, HiZ, ST)
143[2]	VDDIN_3V3	GPIO	PB31	I/O	–	–	A	LCDDAT20	O	1	PIO, I, PU, ST
							B	A20	O	1	
							C	FLEXCOM0_IO3	O	1	
							F	ISI_D5	I	3	

Notes:
1. Fixed feature due to the SOM internal connection.
2. Limited feature compared to SAMA5D2 due to the SOM internal use of specific functionality, for example, QSPI, GMAC.
3. Limited feature compared to SAMA5D2 due to the use of a part of the functionality for other features in the SOM, for example, GMAC, ISC, Flexcom, etc.

4.2.3   PIOC Pin Description

Table 4-3. System-On-Module Pin Description: PIOC

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	(Signal, Dir, PU, PD, HiZ, ST)
145[2]	VDDIN_3V3	GPIO	PC0	I/O	–	–	A	LCDDAT21	O	1	PIO, I, PU, ST
							B	A23	O	1	
							C	FLEXCOM0_IO4	O	1	
							F	ISI_D6	I	3	
141	VDDIN_3V3	GPIO	PC1	I/O	–	–	A	LCDDAT22	O	1	PIO, I, PU, ST
							B	A24	O	1	
							C	CANTX0	O	1	
							D	SPI1_SPCK	I/O	1	
							E	I2SCK0	I/O	1	
							F	ISI_D7	I	3	
146	VDDIN_3V3	GPIO	PC2	I/O	–	–	A	LCDDAT23	O	1	PIO, I, PU, ST
							B	A25	O	1	
							C	CANRX0	I/O	1	
							D	SPI1_MOSI	I/O	1	
							E	I2SMCK0	O	1	
							F	ISI_D8	I	3	
142	VDDIN_3V3	GPIO	PC3	I/O	–	–	A	LCDPWM	O	1	PIO, I, PU, ST
							B	NWAIT	I	1	
							C	TIOA1	I/O	1	
							D	SPI1_MISO	I/O	1	
							E	I2SWS0	I/O	1	
							F	ISI_D9	I	3	
136	VDDIN_3V3	GPIO	PC4	I/O	–	–	A	LCDDISP	O	1	PIO, I, PU, ST
							B	NWR1/NBS1	O	1	
							C	TIOB1	I/O	1	
							D	SPI1_NPCS0	I/O	1	
							E	I2SDI0	I	1	
							F	ISI_PCK	I	3	

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
137	VDDIN_3V3	GPIO	PC5	I/O	–	–	A	LCDVSYNC	O	1	PIO, I, PU, ST
							B	NCS0	O	1	
							C	TCLK1	I	1	
							D	SPI1_NPCS1	O	1	
							E	I2SDO0	O	1	
							F	ISI_VSYNC	I	3	
140	VDDIN_3V3	GPIO	PC6	I/O	–	–	A	LCDHSYNC	O	1	PIO, I, PU, ST
							B	NCS1	O	1	
							C	TWD1	I/O	1	
							D	SPI1_NPCS2	O	1	
							F	ISI_HSYNC	I	3	
139	VDDIN_3V3	GPIO_CLK	PC7	I/O	–	–	A	LCDPCK	O	1	PIO, I, PU, ST
							B	NCS2	O	1	
							C	TWCK1	I/O	1	
							D	SPI1_NPCS3	O	1	
							E	URXD1	I	2	
							F	ISI_MCK	O	3	
138	VDDIN_3V3	GPIO	PC8	I/O	–	–	A	LCDDEN	O	1	PIO, I, PU, ST
							B	NANDRDY	I	1	
							C	FIQ	I	1	
							D	PCK0	O	3	
							E	UTXD1	O	2	
							F	ISI_FIELD	I	3	
2[2]	VDDISC	GPIO	PC9	I/O	–	–	A	FIQ	I	3	PIO, I, PU, ST
							C	ISI_D0	I	1	
							D	TIOA4	I/O	2	
9[2]	VDDISC	GPIO	PC10	I/O	–	–	A	LCDDAT2	O	2	PIO, I, PU, ST
							C	ISI_D1	I	1	
							D	TIOB4	I/O	2	
							E	CANTX0	O	2	
175[2]	VDDISC	GPIO	PC11	I/O	–	–	A	LCDDAT3	O	2	PIO, I, PU, ST
							C	ISI_D2	I	1	
							D	TCLK4	I	2	
							E	CANRX0	I	2	
							F	A0/NBS0	O	2	
3[2]	VDDISC	GPIO	PC12	I/O	–	–	A	LCDDAT4	O	2	PIO, I, PU, ST
							C	ISI_D3	I	1	
							D	URXD3	I	1	
							E	TK0	I/O	2	
							F	A1	O	2	

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
4[2]	VDDISC	GPIO	PC13	I/O	–	–	A	LCDDAT5	O	2	PIO, I, PU, ST
							C	ISI_D4	I	1	
							D	UTXD3	O	1	
							E	TF0	I/O	2	
							F	A2	O	2	
8[2]	VDDISC	GPIO	PC14	I/O	–	–	A	LCDDAT6	O	2	PIO, I, PU, ST
							C	ISI_D5	I	1	
							E	TD0	O	2	
							F	A3	O	2	
12[2]	VDDISC	GPIO	PC15	I/O	–	–	A	LCDDAT7	O	2	PIO, I, PU, ST
							C	ISI_D6	I	1	
							E	RD0	I	2	
							F	A4	O	2	
174[2]	VDDISC	GPIO	PC16	I/O	–	–	A	LCDDAT10	O	2	PIO, I, PU, ST
							C	ISI_D7	I	1	
							E	RK0	I/O	2	
							F	A5	O	2	
5[2]	VDDISC	GPIO	PC17	I/O	–	–	A	LCDDAT11	O	2	PIO, I, PU, ST
							C	ISI_D8	I	1	
							E	RF0	I/O	2	
							F	A6	O	2	
172[2]	VDDISC	GPIO	PC18	I/O	–	–	A	LCDDAT12	O	2	PIO, I, PU, ST
							C	ISI_D9	I	1	
							E	FLEXCOM3_IO2	I/O	2	
							F	A7	O	2	
6[2]	VDDISC	GPIO	PC19	I/O	–	–	A	LCDDAT13	O	2	PIO, I, PU, ST
							C	ISI_D10	I	1	
							E	FLEXCOM3_IO1	I/O	2	
							F	A8	O	2	
14[2]	VDDISC	GPIO	PC20	I/O	–	–	A	LCDDAT14	O	2	PIO, I, PU, ST
							C	ISI_D11	I	1	
							E	FLEXCOM3_IO0	I/O	2	
							F	A9	O	2	
7[2]	VDDISC	GPIO	PC21	I/O	–	–	A	LCDDAT15	O	2	PIO, I, PU, ST
							C	ISI_PCK	I	1	
							E	FLEXCOM3_IO3	O	2	
							F	A10	O	2	
11[2]	VDDISC	GPIO	PC22	I/O	–	–	A	LCDDAT18	O	2	PIO, I, PU, ST
							C	ISI_VSYNC	I	1	
							E	FLEXCOM3_IO4	O	2	
							F	A11	O	2	
170[2]	VDDISC	GPIO	PC23	I/O	–	–	A	LCDDAT19	O	2	PIO, I, PU, ST
							C	ISI_HSYNC	I	1	
							F	A12	O	2	

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| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State |
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	(Signal, Dir, PU, PD, HiZ, ST)
13[2]	VDDISC	GPIO_CLK	PC24	I/O	–	–	A	LCDDAT20	O	2	PIO, I, PU, ST
							C	ISI_MCK	O	1	
							F	A13	O	2	
173[2]	VDDISC	GPIO	PC25	I/O	–	–	A	LCDDAT21	O	2	PIO, I, PU, ST
							C	ISI_FIELD	I	1	
							F	A14	O	2	
115[2]	VDDIN_3V3	GPIO	PC26	I/O	–	–	A	LCDDAT22	O	2	PIO, I, PU, ST
							D	CANTX1	O	1	
							F	A15	O	2	
114[2]	VDDIN_3V3	GPIO	PC27	I/O	–	–	A	LCDDAT23	O	2	PIO, I, PU, ST
							C	PCK1	O	2	
							D	CANRX1	I/O	1	
							F	A16	O	2	
117[2]	VDDIN_3V3	GPIO	PC28	I/O	–	–	A	LCDPWM	O	2	PIO, I, PU, ST
							B	FLEXCOM4_IO0	I/O	1	
							C	PCK2	O	1	
							F	A17	O	2	
118	VDDIN_3V3	GPIO	PC29	I/O	–	–	A	LCDDISP	O	2	PIO, I, PU, ST
							B	FLEXCOM4_IO1	I/O	1	
							F	A18	O	2	
120	VDDIN_3V3	GPIO	PC30	I/O	–	–	A	LCDVSYNC	O	2	PIO, I, PU, ST
							B	FLEXCOM4_IO2	I/O	1	
							F	A19	O	2	
116	VDDIN_3V3	GPIO	PC31	I/O	–	–	A	LCDHSYNC	O	2	PIO, I, PU, ST
							B	FLEXCOM4_IO3	O	1	
							C	URXD3	I	2	
							F	A20	O	2	

Notes:
1. Fixed feature due to the SOM internal connection.
2. Limited feature compared to SAMA5D2 due to the SOM internal use of specific functionality, for example, QSPI, GMAC.
3. Limited feature compared to SAMA5D2 due to the use of a part of the functionality for other features in the SOM, for example, GMAC, ISC, Flexcom, etc.

4.2.4   PIOD Pin Description

Table 4-4. System-On-Module Pin Description: PIOD

| Pad No. | Power Rail | I/O Type | Primary | | Alternate | | PIO Peripheral | | | | Reset State |
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	(Signal, Dir, PU, PD, HiZ, ST)
121[2]	VDDIN_3V3	GPIO_CLK	PD0	I/O	–	–	A	LCDPCK	O	2	PIO, I, PU, ST
							B	FLEXCOM4_IO4	O	1	
							C	UTXD3	O	2	
							F	A23	O	2	

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Pad No.	Power Rail	I/O Type	Primary Signal	Dir	Alternate Signal	Dir	Func	PIO Peripheral Signal	Dir	IO Set	Reset State (Signal, Dir, PU, PD, HiZ, ST)
113[2]	VDDIN_3V3	GPIO	PD1	I/O	–	–	A	LCDDEN	O	2	PIO, I, PU, ST
							F	A24	O	2	
23[2], [3]	VDDIN_3V3	GPIO_CLK	PD2	I/O	–	–	A	URXD1	I	1	PIO, I, PU, ST
							F	A25	O	2	
24[2], [3]	VDDIN_3V3	GPIO_AD	PD3	I/O	PTCROW0	–	A	UTXD1	O	1	PIO, I, PU, ST
							B	FIQ	I	2	
							F	NWAIT	I	2	
27[2], [3]	VDDIN_3V3	GPIO_AD	PD4	I/O	PTCROW1	–	A	TWD1	I/O	2	PIO, I, PU, ST
							B	URXD2	I	1	
							F	NCS0	O	2	
21[2], [3]	VDDIN_3V3	GPIO_AD	PD5	I/O	PTCROW2	–	A	TWCK1	I/O	2	PIO, I, PU, ST
							B	UTXD2	O	1	
							F	NCS1	O	2	
22[2], [3]	VDDIN_3V3	GPIO_AD	PD6	I/O	PTCROW3	–	B	PCK1	O	1	PIO, I, PU, ST
							F	NCS2	O	2	
25[2], [3]	VDDIN_3V3	GPIO_AD	PD7	I/O	PTCROW4	–	F	NWR1/NBS1	O	2	PIO, I, PU, ST
28[2], [3]	VDDIN_3V3	GPIO_AD	PD8	I/O	PTCROW5	–	F	NANDRDY	I	2	PIO, I, PU, ST
N/A[1]	VDDIN_3V3	GPIO_AD	PD9	I/O	–	–	D	GTXCK	O	2	PIO, I, PU, ST
N/A[1]	VDDIN_3V3	GPIO_AD	PD10	I/O	–	–	D	GTXEN	O	2	PIO, I, PU, ST
N/A[1]	VDDIN_3V3	GPIO_AD	PD11	I/O	–	–	D	GRXDV	I	2	PIO, I, PU, ST
N/A[1]	VDDIN_3V3	GPIO_AD	PD12	I/O	–	–	D	GRXER	I	2	PIO, I, PU, ST
N/A[1]	VDDIN_3V3	GPIO_AD	PD13	I/O	–	–	D	GRX0	I	2	PIO, I, PU, ST
N/A[1]	VDDIN_3V3	GPIO_AD	PD14	I/O	–	–	D	GRX1	I	2	PIO, I, PU, ST
N/A[1]	VDDIN_3V3	GPIO_AD	PD15	I/O	–	–	D	GTX0	O	2	PIO, I, PU, ST
N/A[1]	VDDIN_3V3	GPIO_AD	PD16	I/O	–	–	D	GTX1	O	2	PIO, I, PU, ST
N/A[1]	VDDIN_3V3	GPIO_AD	PD17	I/O	–	–	D	GMDC	O	2	PIO, I, PU, ST
N/A[1]	VDDIN_3V3	GPIO_AD	PD18	I/O	–	–	D	GMDIO	I/O	2	PIO, I, PU, ST
58[3]	VDDIN_3V3	GPIO_AD	PD19	I/O	AD0	–	A	PCK0	O	1	PIO, I, PU, ST
							B	TWD1	I/O	3	
							C	URXD2	I	3	
57[3]	VDDIN_3V3	GPIO_AD	PD20	I/O	AD1	–	A	TIOA2	I/O	3	PIO, I, PU, ST
							B	TWCK1	I/O	3	
							C	UTXD2	O	3	
19[1, 4]	VDDIN_3V3	GPIO_AD	PD21	I/O	–	–	B	TWD0	I/O	4	PIO, I, PU, ST
20[1, 4]	VDDIN_3V3	GPIO_AD	PD22	I/O	–	–	B	TWCK0	I/O	4	PIO, I, PU, ST
30[3]	VDDIN_3V3	GPIO_AD	PD23	I/O	AD4	–	A	URXD2	I	2	PIO, I, PU, ST
29[3]	VDDIN_3V3	GPIO_AD	PD24	I/O	AD5	–	A	UTXD2	O	2	PIO, I, PU, ST
110	VDDIN_3V3	GPIO_AD	PD25	I/O	AD6	–	A	SPI1_SPCK	O	3	PIO, I, PU, ST
34	VDDIN_3V3	GPIO_AD	PD26	I/O	AD7	–	A	SPI1_MOSI	I/O	3	PIO, I, PU, ST
							C	FLEXCOM2_IO0	I/O	2	
53	VDDIN_3V3	GPIO_AD	PD27	I/O	AD8	–	A	SPI1_MISO	I/O	3	PIO, I, PU, ST
							B	TCK	I	3	
							C	FLEXCOM2_IO1	I/O	2	

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
51	VDDIN_3V3	GPIO_AD	PD28	I/O	AD9	–	A	SPI1_NPCS0	I/O	3	PIO, I, PU, ST
							B	TDI	I	3	
							C	FLEXCOM2_IO2	I/O	2	
52[2]	VDDIN_3V3	GPIO_AD	PD29	I/O	AD10	–	A	SPI1_NPCS1	O	3	PIO, I, PU, ST
							B	TDO	O	3	
							C	FLEXCOM2_IO3	O	2	
							D	TIOA3	I/O	3	
54[2]	VDDIN_3V3	GPIO_AD	PD30	I/O	AD11	–	A	SPI1_NPCS2	O	3	PIO, I, PU, ST
							B	TMS	I	3	
							C	FLEXCOM2_IO4	O	2	
							D	TIOB3	I/O	3	
N/A[1]	VDDIN_3V3	GPIO_AD	PD31	I/O	–	–	C	IRQ	I	4	PIO, I, PU, ST

Notes:

1. Fixed feature due to the SOM internal connection.
2. Limited feature compared to SAMA5D2 due to the SOM internal use of specific functionality, for example, QSPI, GMAC.
3. Limited feature compared to SAMA5D2 due to the use of a part of the functionality for other features in the SOM, for example, GMAC, ISC, Flexcom, etc.
4. Signal is internally pulled up with a 2.2 kΩ resistor.

4.2.5 System Pin Description

Table 4-5. System-On-Module Pin Description: System

Pin Number	PIO	Power Rail	Designation	Type
61	CLK_AUDIO	VDDIN_3V3	Audio clock	Output
64	COMPN	VDDBU	External analog comparator input	Input
63	COMPP	VDDBU	External analog comparator input	Input
126	DIS_BOOT[1]	VDDIN_3V3	QSPI Interface Disable pin	Input
67	USBA_M	VDDIN_3V3	USB Device High-speed Data -	–
68	USBA_P	VDDIN_3V3	USB Device High-speed Data +	–
70	USBB_M	VDDIN_3V3	USB Host Port B High-speed Data -	–
71	USBB_P	VDDIN_3V3	USB Host Port B High-speed Data +	–
74	DATA	VDDHSIC	USB High-speed Inter-Chip Data	–
73	STROBE	VDDHSIC	USB High-speed Inter-Chip Strobe	–
60	NRST[1]	VDDIN_3V3	Microprocessor reset	Input / Active Low
33	PIOBU1	VDDBU	Tamper or Wake-up input	Input
44	PIOBU2	VDDBU	Tamper or Wake-up input	Input
48	PIOBU3	VDDBU	Tamper or Wake-up input	Input
47	PIOBU4	VDDBU	Tamper or Wake-up input	Input
46	PIOBU5	VDDBU	Tamper or Wake-up input	Input
59	PIOBU6	VDDBU	Tamper or Wake-up input	Input
45	PIOBU7	VDDBU	Tamper or Wake-up input	Input
32	RXD	VDDBU	Low-Power Asynchronous Receiver	Input

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Pin Number	PIO	Power Rail	Designation	Type
35	SHDN[2]	VDDBU	Shutdown Control	Output
49	WKUP	VDDBU	Wake-up	Input
36	ETH_LED0[1]	VDDIN_3V3	Status LED control for Ethernet ports	Output
37	ETH_RXM	± 2.5V	Physical receive or transmit signal (–differential)	I/O
38	ETH_RXP	± 2.5V	Physical receive or transmit signal (+differential)	I/O
40	ETH_TXM	± 2.5V	Physical receive or transmit signal (–differential)	I/O
41	ETH_TXP	± 2.5V	Physical receive or transmit signal (+differential)	I/O

Notes:
1. The signal is internally pulled up with a 10 kΩ resistor.
2. The signal is internally pulled up with a 100 kΩ resistor.

4.2.6   Power Pin Description

Table 4-6. System-On-Module Pin Description: Power

Pin Number	PIO	Description	Comments
16,17	VDDIN_3V3	Main 3.3V Supply inputs. Used for Peripheral I/O lines and MIC2800-G1JJYML supplies.	–
55	VDDBU	Input supply for Slow Clock Oscillator, internal 32 kHz RC Oscillator and a part of the System Controller	–
65	VDDSDHC	SDMMC I/O lines supply input	–
15	VDDISC	Image Sensor I/O lines supply input	–
1, 10, 18, 26, 31, 39, 42, 43, 50, 56, 62, 66, 69, 72, 75, 88, 89, 98, 107, 130, 131, 149, 166, 171, 176	GND	Ground connections	Must be connected together
129	RFU0	Reserved for future use	Must be left floating
147	RFU1	Reserved for future use	Must be left floating
153	RFU2	Reserved for future use	Must be left floating

5. Functional Description

5.1 SAMA5D27 System-in-Package

The SAMA5D2 System-in-Package (SiP) (SAMA5D27C-D1G-CU) integrates the ARM Cortex-A5 processor-based SAMA5D2 MPU with 1 Gbit DDR2-SDRAM in a single package.

By combining the high-performance, ultra-low power SAMA5D2 with DDR2-SDRAM in a single package, PCB routing complexity, area and number of layers are reduced. This makes board design easier and lowers the overall cost of materials. Board design is more robust by facilitating design for EMI, ESD and signal integrity.

For more information about the SiP, see Reference Documents. This section lists the sole reference documents for product information on the SAMA5D2 and the DDR2-SDRAM memory.

The SAMA5D27C-D1G-CU is available in a 289-ball TFBGA package.

5.2 MPU Clocks

Two clock sources are necessary for the module microprocessor:

- 24-MHz main oscillator for the SAMA5D27 MPU
- 32.768-kHz oscillator for slow clock oscillator input and embedded RTC of the SAMA5D27 MPU

The 24-MHz clock is generated by a small size crystal. It delivers a 24-MHz clock to the SAMA5D27 Oscillator IP.

The 32.768-kHz clock is generated by a small size crystal. It delivers an accurate 32.768-kHz clock to the SAMA5D27 for its embedded RTC.

5.3 Power Supplies

The SAMA5D27 SOM1 is supplied by an external 3.3V and generates its own internal supplies by interfacing with the Microchip MIC2800-G1JJYML Power Management Unit.

The MIC2800 is a high-performance power management IC, providing three output voltages with maximum efficiency and is optimized to respect the MPU power-up and power-down cycles.

Integrating a 2 MHz DC/DC converter with an LDO post regulator, the MIC2800 gives two high-efficiency outputs with a second, 300mA LDO for maximum flexibility. The DC-to-DC converter uses small values of L and C to reduce board space while still retaining efficiency over 90% at load currents up to 600mA.

The three outputs supply the following internal nodes:
- DCDC set @ 1.8V supplies SAMA5D27C-D1G-CU DDR2 pads and device.
- LDO1 set @ 1.25V supplies SAMA5D27C-D1G-CU Core.
- LDO2 set @ 2.5V supplies SAMA5D27C-D1G-CU VDDFUSE pad.

The MIC2800 is a µCap design, operating with very small ceramic output capacitors and inductors for stability.

It is available in fixed output voltages in the 16-pin 3mm x 3mm MLF® lead-less package. For more information, refer to the product web page.

Figure 5-1. Power Management Unit Block Diagram
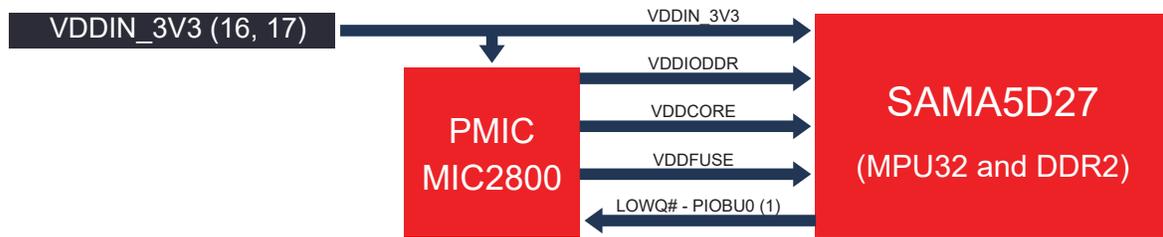
Note:

1. The LOWQ# signal is connected to the PIOBU0 function of the SAMA5D27 device. This signal is internally pulled up at VDDBU level with a 100kΩ resistor.

5.4   System Control

The SAMA5D27 SOM1 provides global system Reset (nRST) and Shutdown (SHDN) pins to the application board.

- The nRST pin is an output pin generated by the internal Power Management Unit (MIC2800-G1JJYML) in respect with power sequence timing. It can be forced externally in case of a system crash and must be connected as described in the example schematic below.
- The SHDN pin is an output pin and is managed by the software application. It switches the Main 3.3V Supply ON or OFF.

Figure 5-2. Internal System Control Schematic
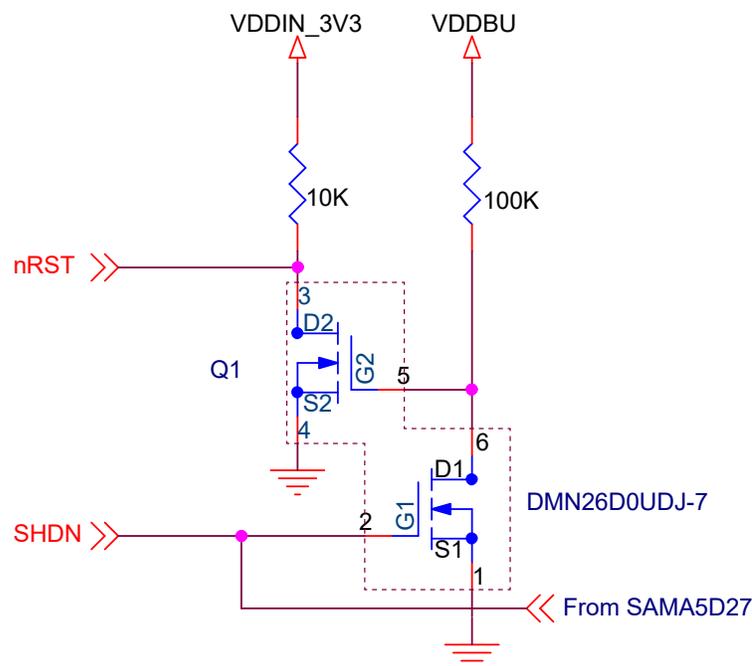
5.5 Ethernet PHY

The Microchip SAMA5D27 SOM1 embeds a single-supply 10BASE-T/100BASE-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081RNAIA is a highly-integrated PHY solution. The KSZ8081RNAIA offers the Reduced Media Independent Interface (RMII) for direct connection to RMII-compliant MACs in Ethernet processors.

The KSZ8081RNAIA is available in 24-pin, lead-free QFN packages. For more information, refer to the product web page.

Figure 5-3. Ethernet PHY Block Diagram
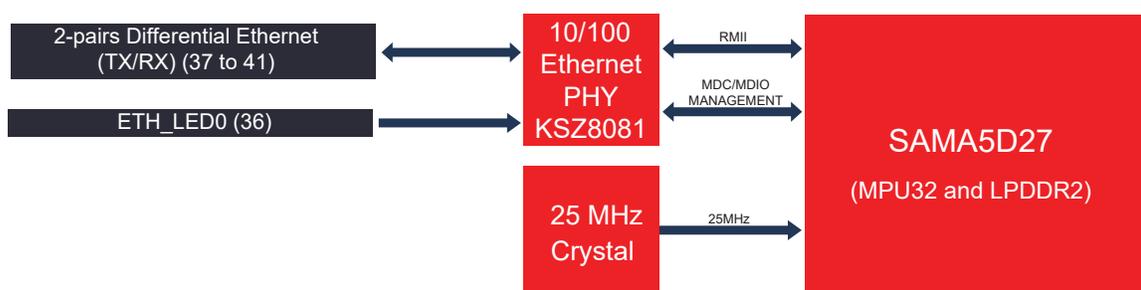
Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State	Note
		Signal	Type	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER	
VDDIN_3V3	GPIO	PD9	I/O	–	–	D	GTXCK	O	2	PIO, I, PU, ST	Used for RMII Interface
VDDIN_3V3	GPIO	PD10	I/O	–	–	D	GTXEN	O	2	PIO, I, PU, ST	
VDDIN_3V3	GPIO	PD11	I/O	–	–	D	GRXDV	I	2	PIO, I, PU, ST	
VDDIN_3V3	GPIO	PD12	I/O	–	–	D	GRXER	I	2	PIO, I, PU, ST	
VDDIN_3V3	GPIO	PD13	I/O	–	–	D	GRX0	I	2	PIO, I, PU, ST	
VDDIN_3V3	GPIO	PD14	I/O	–	–	D	GRX1	I	2	PIO, I, PU, ST	
VDDIN_3V3	GPIO	PD15	I/O	–	–	D	GTX0	O	2	PIO, I, PU, ST	
VDDIN_3V3	GPIO	PD16	I/O	–	–	D	GTX1	O	2	PIO, I, PU, ST	
VDDIN_3V3	GPIO	PD17	I/O	–	–	D	GMDC	O	2	PIO, I, PU, ST	Used for MDIO Interface
VDDIN_3V3	GPIO	PD18	I/O	–	–	D	GMDIO	I/O	2	PIO, I, PU, ST	
VDDIN_3V3	GPIO	PD31	I/O	–	–	–	PB24	--	--	PIO, I, PU, ST	Interrupt Line

5.6 QSPI Memory

The SAMA5D27 SOM1 embeds the SST26VF064BT-104I/MF, a 64Mb Serial Quad I/O Flash memory.

The SST26VF064BT-104I/MF SQI features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package.

The SST26VF064BT-104I/MF is available in 8-lead WDFN package with 6mm × 5mm dimensions.

For more information, refer to the product web page.

Figure 5-4. QSPI Memory Block Diagram
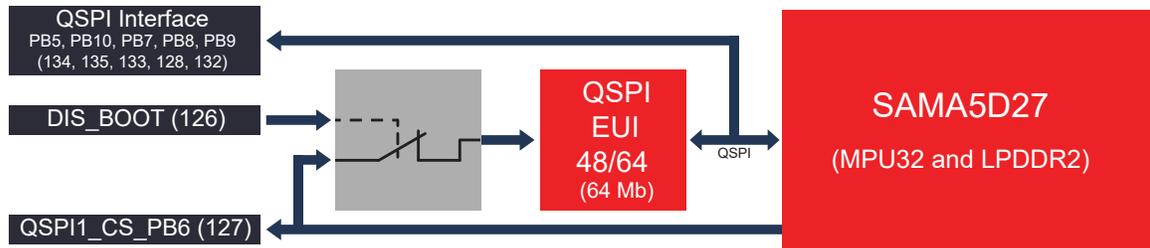
Power Rail	Primary		Alternate			PIO Peripheral			Reset State	Note
	Signal	Type	Signal	Dir	Func	Signal	Dir	IO Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER	
VDDIN_3V3	PB5	I/O	–	–	D	QSPI1_SCK	O	2	PIO, I, PU, ST	
VDDIN_3V3	PB6	I/O	–	–	D	QSPI1_CS	O	2	PIO, I, PU, ST	
VDDIN_3V3	PB7	I/O	–	–	D	QSPI1_IO0	I/O	2	PIO, I, PU, ST	
VDDIN_3V3	PB8	I/O	–	–	D	QSPI1_IO1	I/O	2	PIO, I, PU, ST	Used for QSPI Interface
VDDIN_3V3	PB9	I/O	–	–	D	QSPI1_IO2	I/O	2	PIO, I, PU, ST	
VDDIN_3V3	PB10	I/O	–	–	D	QSPI1_IO3	I/O	2	PIO, I, PU, ST	

> **Tip:** In case of non-use at application level of the QSPI embedded in SAMA5D27 SOM1, it is possible to reassign the signals dedicated to QSPI memory to another PIO function as defined in the table below. To do so, the DIS_BOOT pin (SAMA5D27 SOM1 pad 126) must be forced to ground.

5.7 EEPROM Memory

The SAMA5D27 SOM1 embeds the 24AA02E48T-I/OT, a 1Kb Serial EEPROM with pre-programmed EUI-48 MAC address.

The device is organized as one block of 128 x 8-bit memory with a 2-wire serial interface. The second block is reserved for MAC Address storage.

The 24AA02E48T-I/OT also has a page write capability for up to 8 bytes of data.

The 24AA02E48T-I/OT is available in the standard 5-lead SOT-23 package. For more information, see the product web page.

Figure 5-5. EEPROM Memory Block Diagram

Tip: The 2-Wire serial interface can be externally shared with another device. 2-Wire Data Signal (SAMA5D27 SOM1 Pad 19) and 2-Wire Clock Signal (SAMA5D27 SOM1 Pad 20) are used.

Important: If the 2-Wire serial interface is used externally, the device connected must have a different I²C address than the embedded EEPROM. For more details, refer to the device data sheet.

6. Power Supply Connections and Timing Sequences

The SAMA5D27 SOM1 can be supplied in different ways depending on application needs.

Four power domains must be supplied and can be connected differently. The four different power connections are described below:

- Power Configuration #1: All supplies are connected to the Main 3.3V Supply.
- Power Configuration #2: Backup domain is connected to a coin-cell and the rest to the Main 3.3V Supply.
- Power Configuration #3: Backup domain is connected to a coin-cell. Camera sensor is connected to a separate power supply and the rest to the Main 3.3V Supply.
- Power Configuration #4: All supply domains are connected to separate power supplies.

For each power configuration, the power-on and power-off timing sequences to respect are described below.

6.1 Power Supply Configuration #1

The SAMA5D27 SOM1 is supplied by only one main supply.

In this configuration mode, all supplies are connected together and supplied by the main 3.3V supply. All PIOs have VDDIN_3V3 Power Rail as voltage reference.

Figure 6-1. Power Configuration #1
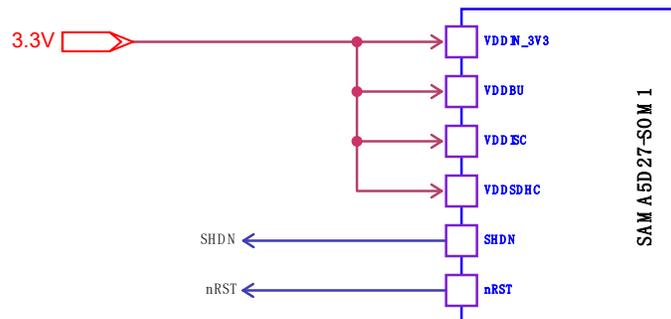
In this configuration mode, the two following timing sequences are applied.

Figure 6-2. Power-On Sequence Timing Diagram
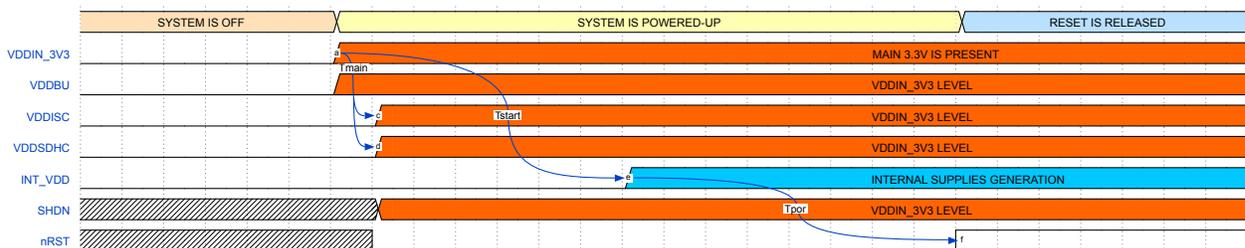
Figure 6-3. Power-Off Sequence Timing Diagram
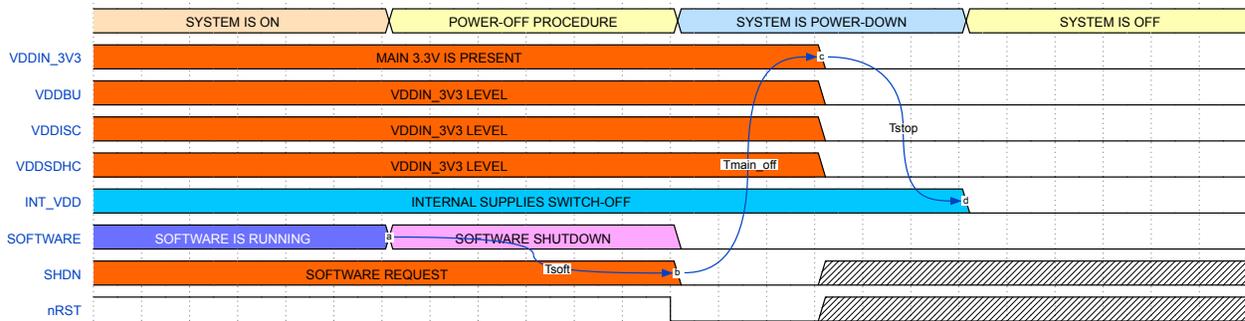
Table 6-1. Timing Values

Symbol	Description	Min.	Typ.	Max.	Unit
t_{main}[1]	Main 3.3V Start-up Time	–	–	1	ms
t_{start}	Internal Delay before starting System Core Supplies	1	–	3	ms
t_{por}	Power-on Reset Delay	–	10	11	ms
t_{soft}	Software Shutdown Time	Depending on system off time			ms
t_{main_off}	Main 3.3V Power-off Time	–	–	1	ms
t_{stop}	Internal Delay before switching off System Core Supplies	1	–	3	ms

Note:
1. The three supplies VDDIN_3V3, VDDISC and VDDSDHC must be applied at the same time. If a delay is implemented, it must be lower than 800µs. VDDBU must be applied at the same time as VDDIN_3V3 or just before. It is forbidden to apply VDDBU after VDDIN_3V3.

6.2 Power Supply Configuration #2

The SAMA5D27 SOM1 is supplied by different power supplies.

- Backup domain is connected to a coin-cell supply.
- The rest of the power inputs are connected to the main 3.3V supply.

In this configuration, the following PIOs have VDDBU Power Rail as reference. All other PIO have VDDIN_3V3 Power Rail as reference.
- COMPP and COMPN
- PIOBU1 to PIOBU7
- RXD, SHDN and WKUP

Figure 6-4. Power Configuration #2
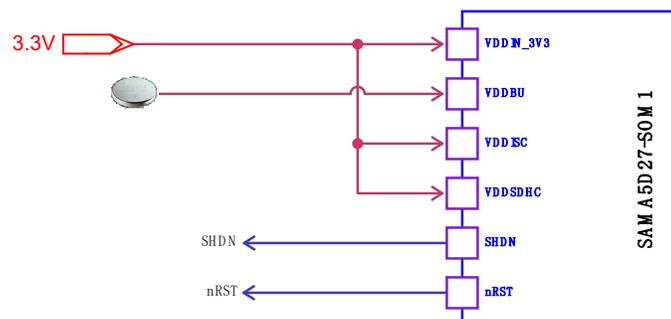
In this configuration, the two following timing sequences are applied.

Figure 6-5. Power-On Sequence Timing Diagram
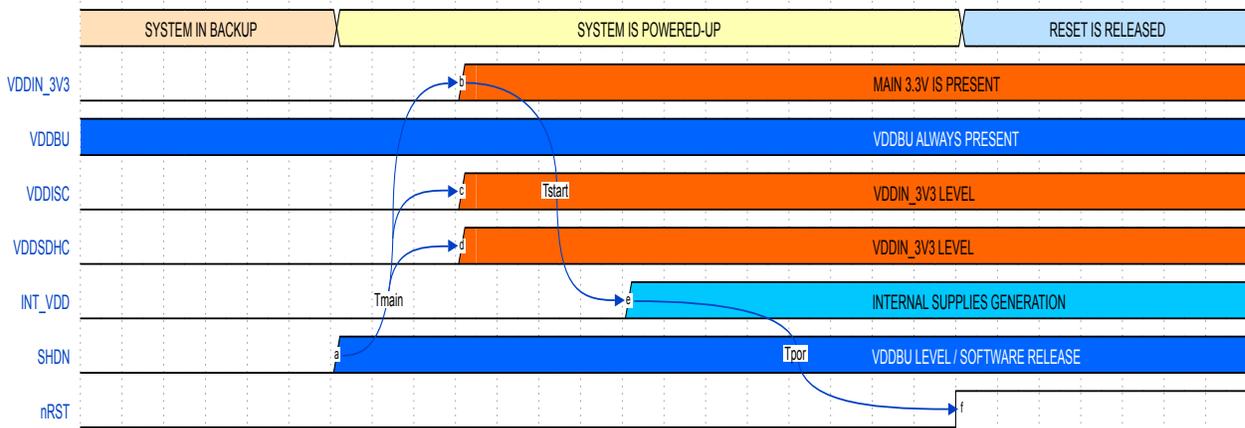
Figure 6-6. Power-Off Sequence Timing Diagram
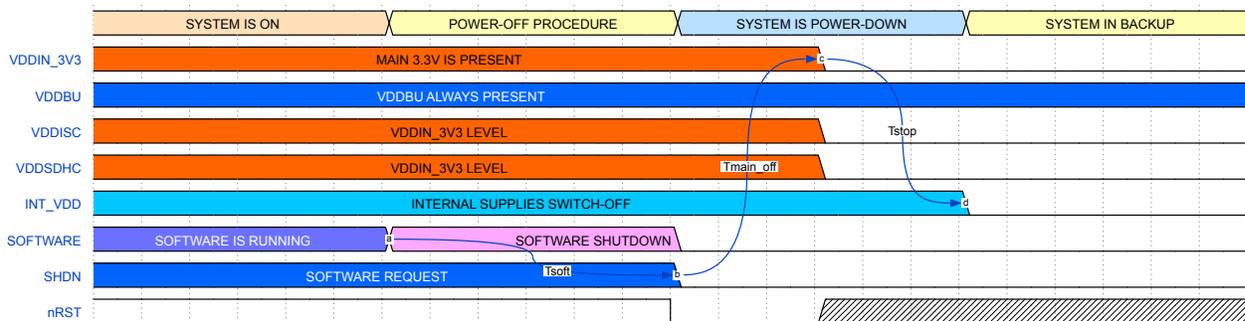
Table 6-2. Timing Values

Symbol	Description	Min.	Typ.	Max.	Unit
t_{main}[1]	Main 3.3V Start-up Time	–	–	1	ms
t_{start}	Internal Delay before starting System Core Supplies	1	–	3	ms
t_{por}	Power-on Reset Delay	–	10	11	ms
t_{soft}	Software Shutdown Time	Depending on system off time			ms
t_{main_off}	Main 3.3V Power-off Time	–	–	1	ms
t_{stop}	Internal Delay before switching-off System Core Supplies	1	–	3	ms

Note:

1. The three supplies VDDIN_3V3, VDDISC and VDDSDHC must be applied at the same time. If a delay is implemented, it must be lower than t_{start}.

6.3   Power Supply Configuration #3

Some power inputs of the SAMA5D27 SOM1 are grouped and others are supplied by a separated power supplies.

- Backup domain is connected to a coin cell.
- Camera sensor power input (VDDISC) is connected to a separate power supply set at one of the following voltage levels (1.8V/2.5V/2.8V/3.0V or 3.3V) depending on the camera sensor technology used in the application.
- The remaining power inputs are connected to the main 3.3V supply.

In this configuration, the following PIOs have:

- VDDBU Power Rail as reference
  - COMPP and COMPN
  - PIOBU1 to PIOBU7
  - RXD, SHDN and WKUP
- VDDISC Power Rail as reference
  - PC9 to PC25
- All other PIOs have VDDIN_3V3 Power Rail as reference.

Figure 6-7. Power Configuration #3
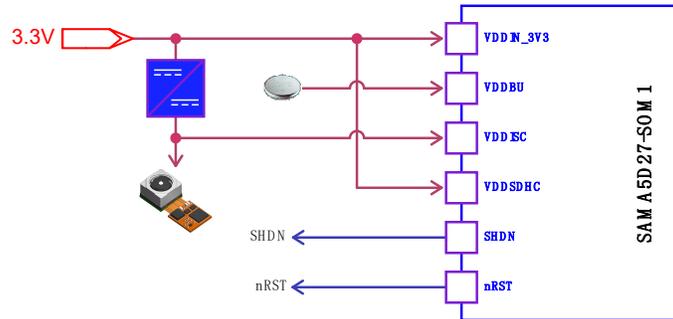
In this configuration mode, the two following timing sequences are applied.

Figure 6-8. Power-On Sequence Timing Diagram
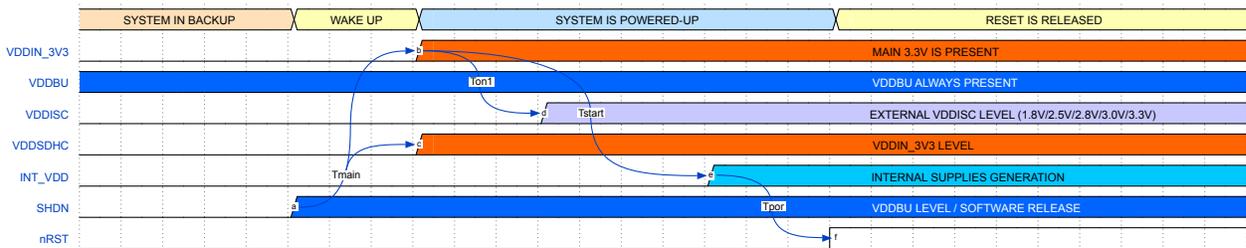
Figure 6-9. Power-Off Sequence Timing Diagram
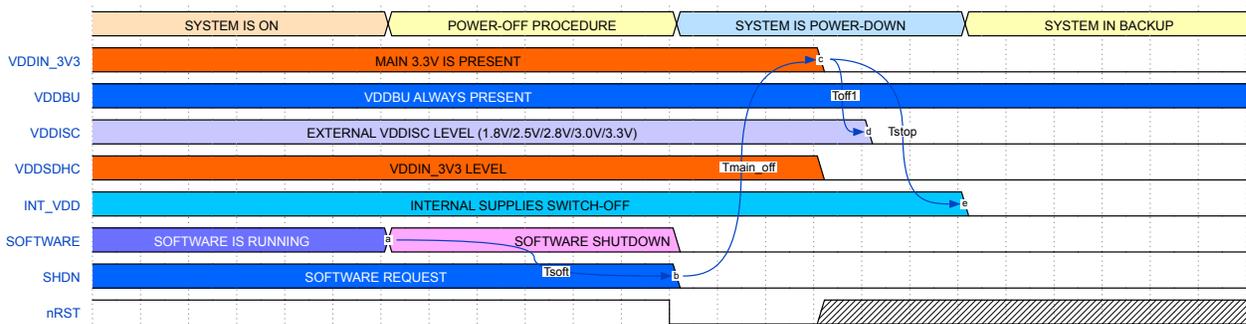
Table 6-3. Timing Values

Symbol	Description	Min.	Typ.	Max.	Unit
t_{main} [1]	Main 3.3V Start-up Time (From regulator available on the motherboard)	–	–	1	ms
t_{on1}	VDDISC Regulator Start-up Time (From regulator available on the motherboard)	–	–	800	µs
t_{start}	Internal Delay before starting System Core Supplies	1	–	3	ms

Symbol	Description	Min.	Typ.	Max.	Unit
..........continued					
t_{por}	Power-on Reset Delay	–	10	11	ms
t_{soft}	Software Shutdown Time	Depending on system off time			ms
t_{main_off}	Main 3.3V Power-off Time (From regulator available on the motherboard)	–	–	1	ms
t_{off1}	VDDISC Regulator Power-off Time (From regulator available on the motherboard)	–	–	1	ms
t_{stop}	Internal Delay before switching off System Core Supplies	1	–	3	ms

Note:

1. The supplies VDDIN_3V3 and VDDSDHC must be applied at the same time. If a delay is implemented, it must be lower than t_{start}.

6.4 Power Supply Configuration #4

Each power input of the SAMA5D27 SOM1 is supplied by separate power supplies.

- Backup domain is connected to a coin cell.
- Camera sensor power input (VDDISC) is connected to a separate power supply set at one of the following voltage levels (1.8V/2.5V/2.8V/3.0V or 3.3V) depending on the camera sensor technology used in the application.
- SD Card power input (VDDSDHC) is connected to a separate power supply set at one of the following voltage levels (1.8V or 3.3V) depending on the SD Card Technology/Speed used in the application.
- VDDIN_3V3 power input is connected to the main 3.3V supply.

In this configuration, the following PIOs have:
- VDDBU Power Rail as reference
  - COMPP and COMPN
  - PIOBU1 to PIOBU7
  - RXD, SHDN and WKUP
- VDDISC Power Rail as reference
  - PC9 to PC25
- VDDSDHC Power Rail as reference
  - PA0 to PA10
- All other PIOs have VDDIN_3V3 Power Rail as reference.

Figure 6-10. Power Configuration #4
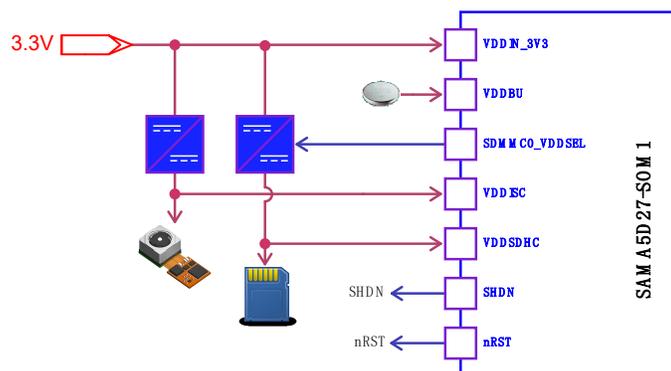
In this configuration mode, the two following timing sequences are applied.

Figure 6-11. Power-On Sequence Timing Diagram
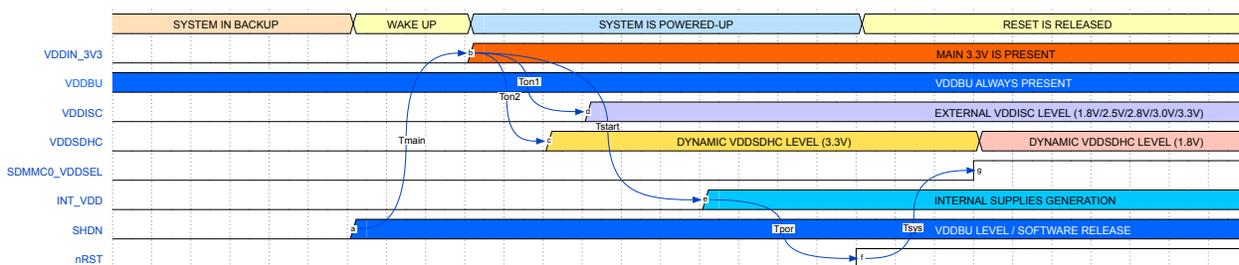
Figure 6-12. Power-Off Sequence Timing Diagram
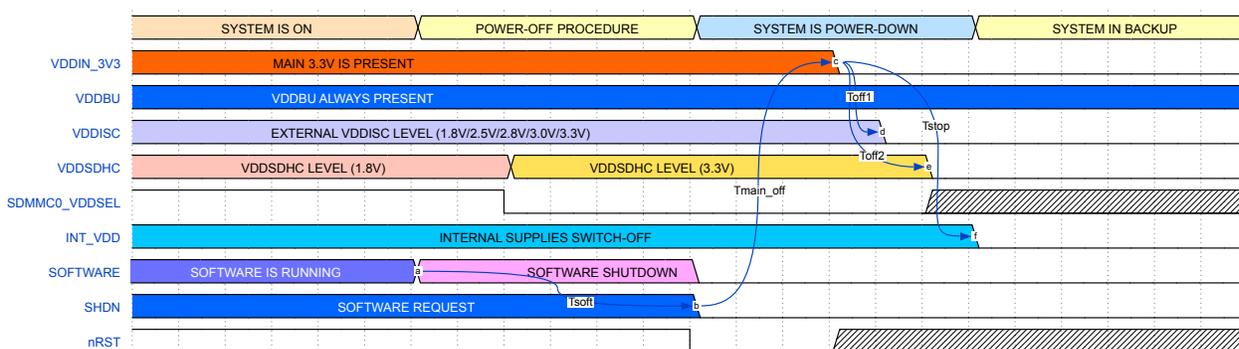
Table 6-4. Timing Values

Symbol	Description	Min.	Typ.	Max.	Unit
t_{main}	Main 3.3V Start-up Time (From regulator available on the mother board)	–	–	1	ms
t_{on1}	VDDISC Regulator Start-up Time (From regulator available on the mother board)	–	–	800	µs
t_{on2}	VDDSDHC Regulator Start-up Time (From regulator available on the mother board)	–	–	800	µs
t_{start}	Internal Delay before starting System Core Supplies	1	–	3	ms
t_{por}	Power-on Reset Delay	–	10	11	ms
t_{sys}	Low-speed to High-speed Card Timing[1]	Depending on system on time			ms
t_{soft}	Software Shutdown Time	Depending on system off time			ms
t_{main_off}	Main 3.3V Power-off Time (From regulator available on the motherboard)	–	–	1	ms
t_{off1}	VDDISC Regulator Power-off Time (From regulator available on the motherboard)	–	–	1	ms
t_{off2}	VDDSDHC Regulator Power-off Time (From regulator available on the motherboard)	–	–	1	ms
t_{stop}	Internal Delay before switching off System Core Supplies	1	–	3	ms

Note:

1. Timing depends on the system boot time. No particular recommendations to apply.

7. Booting Guidelines

This section provides an overview of how to program a Non-Volatile Memory (NVM) and boot from it.

The SAMA5D27 SOM1 embeds a Quad I/O Flash Memory as a source for boot. Another type of NVM may be located on the motherboard. This section explains how to program, select and boot from an NVM.

7.1 Boot Process

The system always boots from the ROM memory at address 0x0. The ROM code is a boot program contained in the embedded ROM. It is also called "First level bootloader". The SAMA5D2 can be configured to run a Standard Boot mode or a Secure Boot mode. More information on how the Secure Boot mode can be enabled, and how the chip operates in this mode, is provided in the document *SAMA5D2x Secure Boot Strategy*. To obtain this application note and additional information about the secure boot and related tools, contact a Microchip sales representative.

By default, the chip starts in Standard Boot Mode.

The ROM code standard sequence is executed as follows:
- Basic chip initialization: crystal or external clock frequency detection.
- Attempt to retrieve a valid code from external non-volatile memories (NVM).
- Execution of a monitor called SAM-BA® Monitor, in case no valid application has been found on any NVM [1].

Note:
1. This may be the case during the first start-up or after an NVM erase or when a "boot disable jumper" is used on the memory Chip Select, in order to force an update.

7.2 Boot Configuration

The boot sequence is controlled using a Boot Configuration Word in the Fuse area or in the backup registers BUREG.

For details, refer to the section "Boot Configuration" of the *SAMA5D2 Data Sheet*, document no. DS60001476.

7.3 NVM Programming

The SAMA5D27 SOM1 is delivered with SAM-BA® In-System Programmer, a comprehensive tool to program boot memories.

In case the boot code does not find a valid program in NVM, the SAM-BA monitor is launched in order to program the considered NVM.

The SAM-BA monitor principle is to:
- Initialize DBGU and USB.
- Check if USB Device enumeration occurred.
- Check if characters are received on the DBGU.

Once the communication interface is identified, the application runs in an infinite loop waiting for different commands.

The firmware can be sent and programmed in the NVM.

For more information, refer to the following link: www.at91.com/linux4sam/bin/view/Linux4SAM/Sama5d2XplainedMainPage#Using_SAM_BA_to_flash_components.

7.4   Boot From External Memory

Several types of external memories such as NAND Flash, SDCard, SPI Flash, QSPI Flash, etc. can be connected to the SAMA5D27 SOM1 and placed on the motherboard.

For details of the Boot sequence, refer to the "NVM Bootloader Program Description for MRL C Parts" diagram of the SAMA5D2 data sheet, document no. DS60001476.

The table below provides the list of external memory types and interfaces that may be used to boot the SAMA5D27 SOM1:

Table 7-1. External Memory Connections

Memory Type	Interface	PIO	Comments
SDCard	SDMMC0	PA0 to PA13	If external SDMMC0 interface is not used, bit SDMMC_0 in **Boot Configuration Word** must be set to 1.
	SDMMC1	PA18 to PA22, PA27 to PA30	If external SDMMC1 Interface is not used, bit SDMMC_1 in **Boot Configuration Word** must be set to 1.
eMMC	SDMMC0	PA0 to PA10, PA13	If external SDMMC0 Interface is not used, bit SDMMC_0 in **Boot Configuration Word** must be set to 1.
	SDMMC1	PA18 to PA22, PA27, PA30	If external SDMMC0 interface is not used, bit SDMMC_1 in **Boot Configuration Word** must be set to 1.
NAND Flash	NFC	PA0 to PA12	Field NFC in **Boot Configuration Word** must be set to "01". IOSET2 is selected. (See Notes below)
		PA22 to PA31, PB0 to PB2, PC8	Field NFC in **Boot Configuration Word** must be set to "00". IOSET1 is selected. (See Notes below)
QSPI Flash	QSPI0	PA0 to PA5	Field QSPI_0 in **Boot Configuration Word** must be set to "00". IOSET1 is selected. (See Notes below)
		PA14 to PA19	Field QSPI_0 in **Boot Configuration Word** must be set to "01". IOSET2 is selected. (See Notes below)
		PA22 to PA27	Field QSPI_0 in **Boot Configuration Word** must be set to "10". IOSET3 is selected. (See Notes below)
	QSPI1	PB5 to PB10	Need to tie DIS-BOOT pin to GND. Bits QSPI_1 in **Boot Configuration Word** must be set to "01". IOSET2 is selected. (See Notes below)
SPI Flash	SPI0	PA14 to PA17	Bits SPI_0 in **Boot Configuration Word** must be set to "00". IOSET1 is selected. (See Notes below)
		PA30, PA31, PB0, PB1	Bits SPI_0 in **Boot Configuration Word** must be set to "01". IOSET2 is selected. (See Notes below)
	SPI1	PA22 to PA25	Bits SPI_1 in **Boot Configuration Word** must be set to "01". IOSET2 is selected. (See Notes below)
		PC1 to PC4	Bits SPI_1 in **Boot Configuration Word** must be set to "00". IOSET1 is selected. (See Notes below)

Note: For these external memory configurations, set the EXT_MEM_BOOT_ENABLE bit to "1" in **Boot Configuration Word**.

Note: The Boot Configuration Word allows several customizations of the boot sequence. For details, refer to the section "Boot Configuration" in the *SAMA5D2 Data Sheet*, document no. DS60001476.

8. Debug Considerations

The SAMA5D27 SOM1 JTAG access is disabled during the execution of the ROM code sequence. It is re-enabled when jumping into SRAM when a valid code has been found on an external NVM, at the same time the ROM memory and fuses are hidden. If no valid boot is found on an external NVM, the ROM code

- enables the USB connection and one UART serial port
- starts the standard SAM-BA monitor
- locks access to the ROM memory
- re-enables the JTAG connection

The SAMA5D27 SOM1 has multiple debug and JTAG settings. For more information, refer to the *SAMA5D2 Data Sheet*, document no. DS60001476, "SECUMOD JTAG Protection Control Register", "Customer Fuse Matrix" and "Special Function Bits".

The JTAG I/O set can be configured. For correct operations, the I/O set to be used is JTAG_IOSET_3, i.e., the field JTAG_IO_SET in the Boot Configuration Word must be written with value '2'.[1]

Note: Due to IO conflict on line PA22, JTAG_IOSET_4 must not be implemented when SDMMC1 is used as an NVM boot media. See the *SAMA5D2 Data Sheet*, document no. DS60001476, "Boot Configuration Word".

9. Electrical Characteristics

This section provides an overview of the electrical characteristics of the SAMA5D27 SOM1 module. Absolute maximum ratings for the SAMA5D27 SOM1 module are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the module at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

9.1 Absolute Maximum Ratings

Table 9-1. Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.
Storage Temperature	–	-60°C	+150°C
Maximum Operating Temperature	–	-40°C	+85°C
Voltage on Inputs Pins	With respect to ground	-0.3V	+4.0V
Maximum Voltage	On VDDIN_3V3 Pads	–	+4.0V
	On VDDBU Pad	–	+4.0V
	On VDDSDHC Pad	–	+4.0V
	On VDDISC Pad	–	+4.0V

Important: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 Operational Characteristics

The following characteristics are applicable to the operating temperature range T_A = -40°C to +85°C, unless otherwise specified.

Table 9-2. Table 7. Power Supplies Operating Conditions

Pad	Parameters	Conditions	Min.	Typ.	Max.
VDDIN_3V3	DC Supply	–	3.0V	3.3V	3.6V
	Maximum Input Current	–	–	–	450mA
VDDBU	DC Supply	Must be established first or at the same time as VDDIN_3V3.	1.65V	3.3V	3.6V
	Maximum Input Current	–	–	–	0.1 mA
VDDSDHC	DC Supply	SDHC I/Os Lines	1.65V	3.3V	3.6V
	Maximum Input Current	–	–	–	30mA
VDDISC	DC Supply	ISC I/Os Lines	1.65V	3.3V	3.6V
	Maximum Input Current	–	–	–	30mA

9.3 DC Electrical Characteristics

9.3.1 Standard Interfaces

The following characteristics are applicable to the operating temperature range T_A = -40°C to +85°C, unless otherwise specified.

Table 9-3. DC Electrical Characteristicsfor GPIO Inputs

Pad	Parameters	Conditions	Min.	Typ.	Max.
V_{IL}	Low-level Input Voltage	All GPIO @ 3.3V	-0.3V	–	0.4V
V_{IH}	High-level Input Voltage	All GPIO @ 3.3V	2.3V	–	3.6V
V_{OL}	Low-level Output Voltage	I_O Max.	–	–	0.41V
V_{OH}	High-level Output Voltage	I_O Max.	2.9V	–	--
I_{IL}	Low-level Input Current	All GPIO @ 3.3V	-1µA	–	1µA
I_{IH}	High-level Input Current	All GPIO @ 3.3V	-1µA	–	1µA
I_{OL}	Low-level Output Current	All GPIO @ 3.3V / Low	-2mA	–	--
		All GPIO @ 3.3V / High	-32mA	–	--
I_{OH}	High-level Output Current	All GPIO @ 3.3V / Low	–	–	2mA
		All GPIO @ 3.3V / High	–	–	32mA
R_{PULLUP}	Pull-up Resistors	All GPIO @ 3.3V and PDxx in AD mode.	280kΩ	380kΩ	480kΩ
		All IOs in GPIO mode @3.3V.	40kΩ	66kΩ	130kΩ
$R_{PULLDOWN}$	Pull-down Resistors	All GPIO @ 3.3V and PDxx in AD mode	280 kΩ	380kΩ	480kΩ
		All IOs in GPIO mode @3.3V.	40kΩ	77kΩ	160kΩ

Note: This table applies to all the following pads: PA0–PA31, PB0–PB31, PC0–PC31, PD0–PD8, PD19-PD30.

9.3.2 Other PIOs

The following characteristics are applicable to the operating temperature range T_A = -40°C to +85°C, unless otherwise specified.

Table 9-4. Table 7. DC Electrical Characteristics for System Inputs

Pad	Parameters	Conditions	Min.	Typ.	Max.
V_{IL}	Low-level Input Voltage	DIS_BOOT	–	–	1.0V
V_{IH}	High-level Input Voltage	DIS_BOOT	2.3V	–	–

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10.   Mechanical Characteristics

10.1   Module Dimensions

The SAMA5D27 SOM1 has dimensions of 40mm x 38mm with specific mechanical characteristics listed below.

Figure 10-1. System-On-Module Dimensions
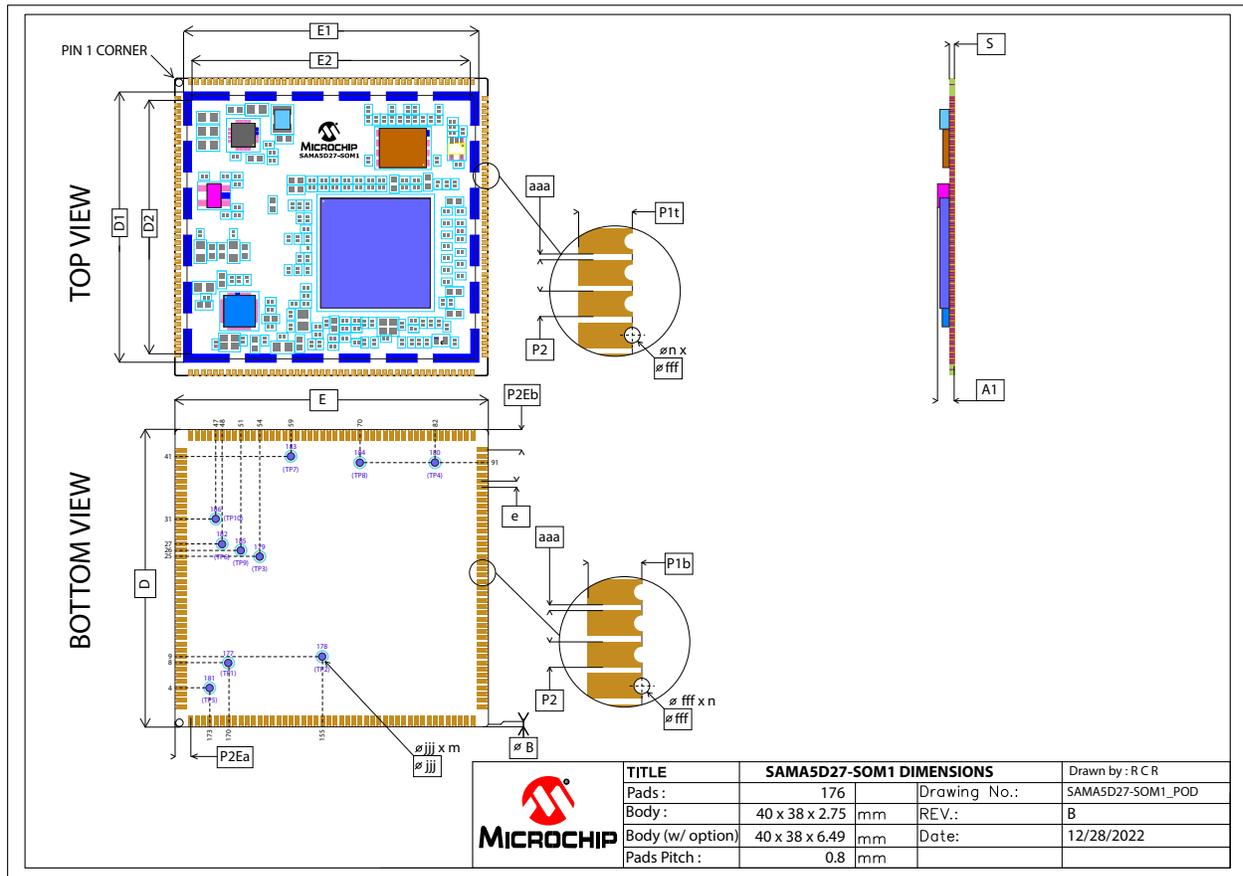
Table 10-1. System-On-Module Dimensions

		Symbol	Common Dimensions			Comments
			Min.	Typ.	Max.	
Body Size	X	E	39.900	40.000	40.100	–
	Y	D	37.900	38.000	38.100	–
Pad Pitch		e	–	0.800	--	–
PCB Thickness		S	1.150	1.200	1.250	–
Total Thickness		A1	–	2.750	2.800	–
PCB Angle Hole Diameter		B	–	0.200	–	–
Pad Length	Bottom Side	P1b	–	1.500	–	–
	Top Side	P1t	–	0.800	–	–
Pad Width		P2	–	0.600	–	Solder Mask defined 0.550
Pad Space		aaa	–	0.200	–	–

...........continued

		Symbol	Common Dimensions			Comments
			Min.	Typ.	Max.	
Opening Drilling Diameter		fff	–	0.400	–	0.400 typic minus metallization
Pad Count		n	–	176	–	–
Edge Center to Center	X	E1	37.550	37.630	37.700	–
	Y	D1	34.400	34.480	34.550	–
	X	E2	35.550	35.630	35.700	–
	Y	D2	32.400	32.480	32.550	–
Pad Axis to Edge	X	P2Ea	–	2.000	–	–
	Y	P2Eb	–	2.600	–	–

⚠ WARNING Test points placed on the bottom side are used for factory test only. It is not possible to connect external devices on these test points.

11.   Ordering Information

Table 11-1. Ordering Information

Ordering Code	Version	Package	Carrier Type	Operating Temperature Range
ATSAMA5D27-SOM1	1	176-pin 38x40mm	Tray	-40°C to +85°C

12.   Revision History

Table 12-1. SAMA5D27 SOM1 Data Sheet, Rev. DS60001521E, Feb-2024

Changes
4.2.4. PIOD Pin Description: added note 4. 4.2.5. System Pin Description : added notes. 5.1. SAMA5D27 System-in-Package: removed schematics. 5.2. MPU Clocks: added. 5.3. Power Supplies: updated figure. Updated 10.1. Module Dimensions. Deleted sections Module Land Pattern, Production Settings.

Table 12-2. SAMA5D27 SOM1 Data Sheet, Rev. DS60001521D, June-2020

Changes
Description and Block Diagram: updated number of ADC inputs. Pinout Overview: updated figure. Pin List: updated PIO muxing tables for PIOA, PIOB, PIOC and PIOD. Table Other GPIO Possibilities for QSPI Interface in Case of Non-use: updated primary signal column. Table External Memory Connections: updated eMMC and NAND Flash.

Table 12-3. SAMA5D27 SOM1 Data Sheet, Rev. DS60001521C, Oct-2018

Changes
Deleted all references to PTC in Features, Block Diagram, Pinout Overview and Pin List. Editorial corrections throughout.

Table 12-4. SAMA5D27 SOM1 Data Sheet, Rev. DS60001521B, Feb-2018

Changes
Features: added PTC support and LCD interface. Applications: updated list. 1. Description: added PTC support. 2. Reference Documents: corrected datasheet cross-reference. Pinout Overview: updated figure with correct color key. SAMA5D27-D1G-CU Supplies Decoupling Schematic: updated all occurrences of 1V2 to 1V25. 5.1. SAMA5D27 System-in-Package: removed table "SAMA5D27C-D1G-CU External Crystal". 5.3. Power Supplies: LDO1 output changed to 1.25V 5.5. Ethernet PHY: removed table "KSZ8081RNAIA External Crystal". QSPI Memory Schematic: updated QSPI memory reference. 5.7. EEPROM Memory: updated Important Note. Module Land Pattern: added Warning. Added Production Settings. Updated Reflow Profile. Updated 11. Ordering Information.

Table 12-5. SAMA5D27 SOM1 Data Sheet, Rev. DS60001521A, Oct-2017

Changes
First issue.

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ATSAMA5   D27 - SOM1

Architecture

Product Group

System on Module
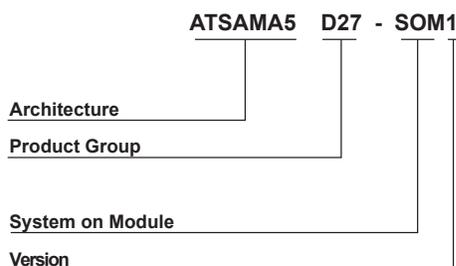
Version

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Product Group:	D27
System on Module:	SOM
Version:	1

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