SAMA5D27 SOM1 Kit1 User's Guide

ATSAMA5D27-SOM1-EK1

Scope

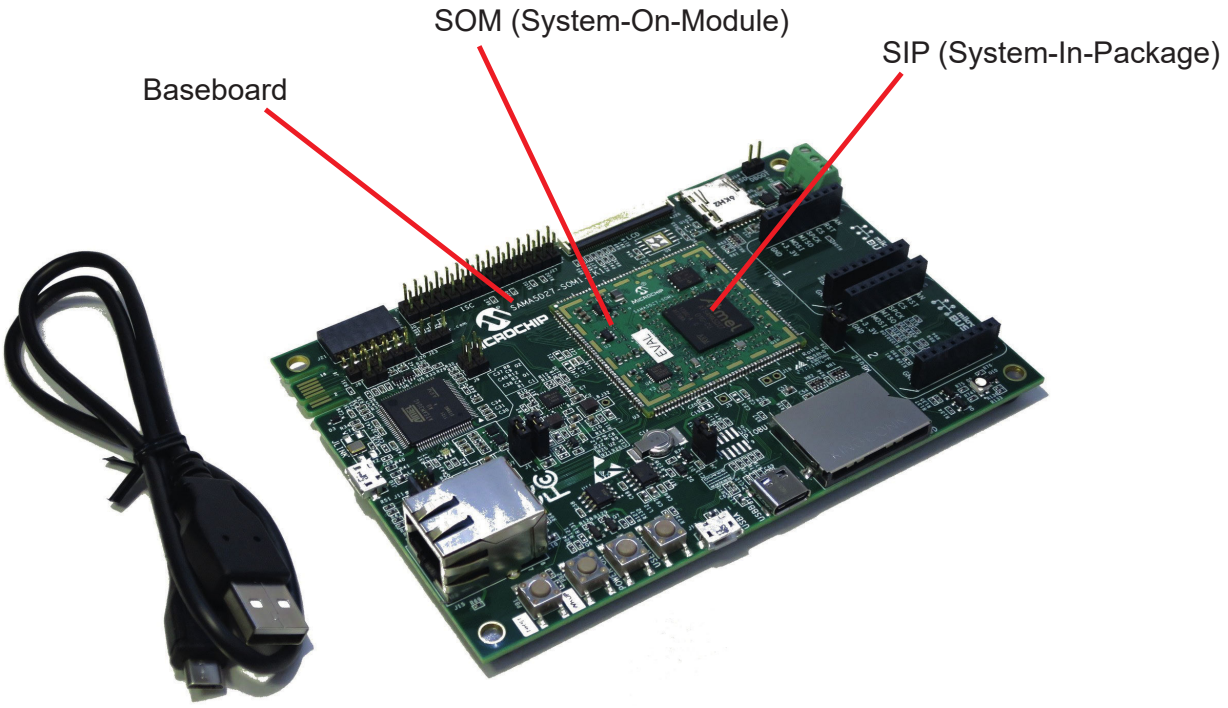
This user's guide provides detailed information on the overall design of the SAMA5D27 SOM1 Kit1 and describes how to use the kit.

The kit is the evaluation platform for the SAMA5D27 SIP (System-In-Package) and SOM (System-On-Module), and comprises:

- a baseboard
- a SAMA5D27 SOM soldered on the baseboard
- a SAMA5D27 SIP soldered on the SOM
- a USB cable

See the figure below.

Figure 1. SAMA5D27 SOM1 Kit1 Overview



1. Introduction

1.1 Document Layout

The document is organized as follows:

- Introduction
- Product Overview – Important information about the kit
- Board Components – Specifications of the kit and high-level description of the major components and interfaces
- Installation and Operation – Instructions on how to get started with the kit
- Errata
- Appendix: Schematics and Layouts – Kit schematics and layout diagrams

1.2 Reference Documents

The following Microchip documents are available and recommended as supplemental reference resources:

Type	Document Title	Available	Ref. No./Product
Data Sheet	SAMA5D2	www.microchip.com/SAMA5D2	DS60001476
Data Sheet	SAMA5D2 System-On-Module (SOM)	www.microchip.com/ATSAMA5D27-SOM1	DS60001521
Data Sheet	SAMA5D2 System-In-Package (SIP)	www.microchip.com/SAMA5D2 SIP	DS60001484

2. Product Overview

2.1 Kit Contents

The kit includes the following:

- One baseboard with soldered SOM
- One USB cable

2.2 Features

The kit comprises a baseboard with a soldered SAMA5D27 SOM1 module. The module features a SAMA5D27-D1G-CU SIP embedding a 1-Gbit DDR2 SDRAM. The SOM offers a reliable and cost-effective embedded platform for building end products, as well as a small form factor, complemented by many connectivity interfaces. The SOM is a fully-featured industrially-certified single board computer designed for integration into customer applications.

The SOM module is a purpose-built small footprint hardware platform equipped with a wide array of high-speed connectivity engineered to support various applications such as IoT endpoints, wearables, appliances or industrial equipment.

The SOM integrates a 1-Gbit DDR2 SDRAM, a QSPI memory and a 10/100 Mbps Ethernet controller. 128 GPIO pins are provided by the SOM for general use in the system. All GPIO pins are independent and can be configured as inputs or outputs, with or without pull-up/pull-down resistors.

The baseboard features a wide range of peripherals, as well as a user interface and expansion options, including two mikroBUS™ click interface headers to support over 300 MikroElektronika click boards™ and one Pmod™ interface.

Table 2-1. Baseboard Features

Characteristics	Specifications	Components
Memory	One QSPI Flash (unmounted)	Tested with Macronix MX25L25673GM2I-08G
Crypto	One CryptoAuthentication™ device	ATECC608
USB Com Port	One USB host One USB device One USB HSIC	Connector type C Connector type microAB 2-pin header (not populated)
Ethernet	One Ethernet interface	RJ45 connector
CAN	One CAN interface	ATA6561
Video	One LCD RGB 24-bit interface One ISC 12-bit interface	50-pin FPC connector 2x15 male connector
Storage	One standard SD card interface One microSD card interface	With 3.3V/1.8V power switch –
Debug port	One J-Link-OB and J-Link-CDC One JTAG interface	Microchip SAM3U micro-controller with embedded J-Link firmware –
Board Monitor	One RGB (Red, Green, Blue) LED Four push button switches	– Power ON, Reset, Wakeup, User Free
Expansion	One tamper connector One Pmod connector Two mikroBUS interfaces	10-pin male connector 6-pin female connector 2x8-pin female connector
Board Supply	From USB A and/or USB J-Link-OB	5 VDC
Power saving	SuperCap	–

Refer to www.microchip.com for:

- Sample code and technical support

- Linux® software and demos

2.3 Specifications

Table 2-2. Kit Specifications

Characteristic	Specification
Ordering code	ATSAMA5D27-SOM1-EK1
Board supply voltage	USB-powered
Temperature	Operating: 0°C to +70°C Storage: –40°C to +85°C
Relative humidity	0 to 90% (non-condensing)
Baseboard dimensions	135 × 90 × 20 mm
RoHS status	Compliant

2.4 Power Sources

Two options are available to power up the baseboard:

- USB powering through the USB Micro-AB connector (J17 - default configuration)
- Powering through the USB Micro-AB connector on the J-Link-OB Embedded Debugger interface (J10)

The two power sources can coexist. A priority mechanism manages the automatic switching between the two. The priority source is J-Link (J10), the secondary source is the USB port (J17).

Table 2-3. Electrical Characteristics

Electrical Parameter	Value
Input voltage	5VCC
Maximum input voltage	6VCC
Maximum 3.3VDC current available	1.2A
I/O voltage	3.3V only

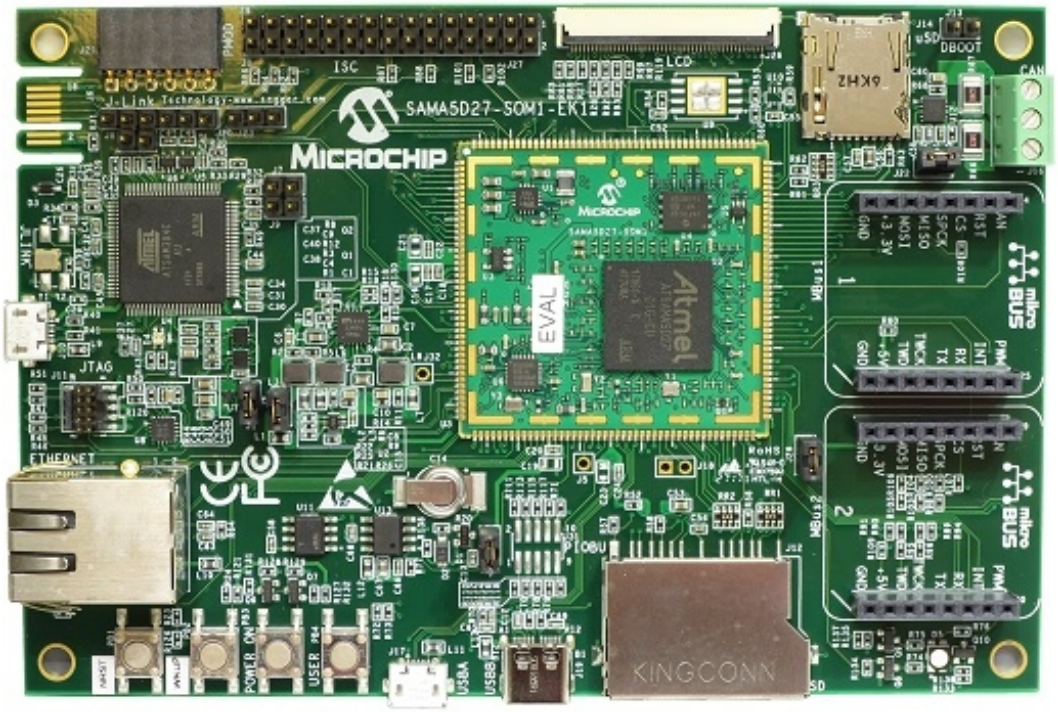
3. Baseboard Components

This section covers the specifications of the SAMA5D27 SOM1 Kit1 baseboard and provides a high-level description of the baseboard's major components and interfaces. This document is not intended to provide a detailed documentation about the processor or about any other component used on the baseboard. It is expected that the user will refer to the appropriate documents of these devices to access detailed information.

3.1 Baseboard Overview

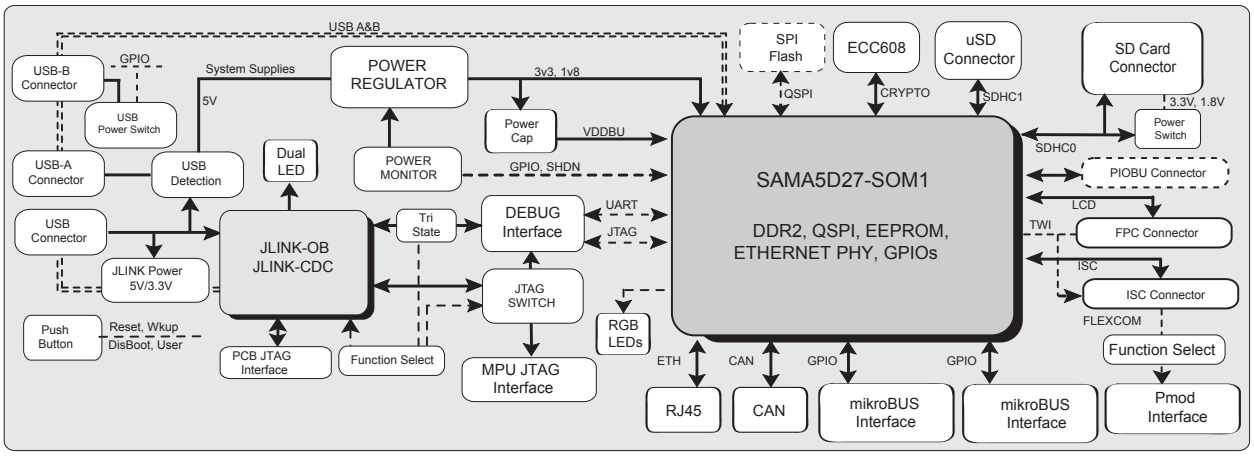
The fully-featured SAMA5D27 SOM1 Kit1 baseboard integrates multiple peripherals and interface connectors, as shown in the figure below.

Figure 3-1. SAMA5D27 SOM1 Kit1 Baseboard Overview



The following picture illustrates the kit block diagram.

Figure 3-2. SAMA5D27 SOM1 Kit1 Block Diagram



3.1.1 Default Jumper Settings

The figure below shows the default jumper settings. Jumpers in red are configuration items and current measurement points. The following table describes the functionality of the jumpers.

Figure 3-3. Default Jumper Settings

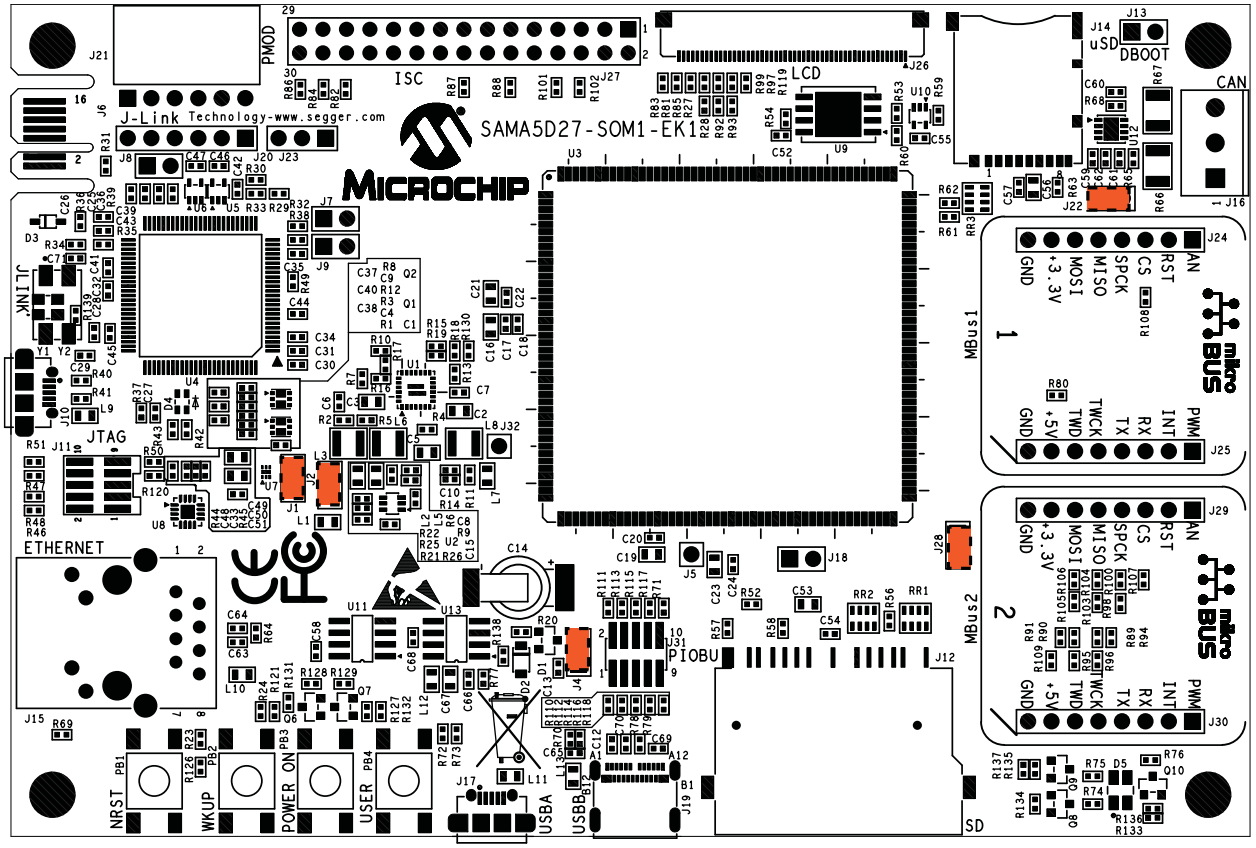


Table 3-1. Jumper Settings

Jumper	Default	Function
J1	Closed	VDD_MAIN_5V current measurement
J2	Closed	VDD_3V3 SOM current measurement
J4	Closed	VDDBU current measurement
J7	Open	Enables J-Link-OB (closed=disable)
J8	Open	Erases SAM3U firmware code (closed=erase at power-up) **⚠WARNING** Must remain open. If closed, the SAM3U contents are erased and J-Link functionality is discarded.
J9	Open	Enables JTAG-CDC (closed=disable)
J13	Open	Disables SOM boot memories (closed=disable)
J22	Closed	Enables 3.3V power mikroBUS1 (closed=enable)
J28	Closed	Enables 3.3V power mikroBUS2 (closed=enable)

3.1.2 Baseboard Connectors

The following table describes the interface connectors on the SAMA5D27 SOM1 Kit1 baseboard.

Table 3-2. Baseboard Interface Connectors

Connector	Interfaces to
J5	CLK_AUDIO test point (not populated)
J6	PCB-edge JTAG connector for factory-programming the J-Link-OB
J10	USB-A MicroAB, J-Link-OB port
J11	MPU SAMA5D27 JTAG 10-pin IDC connector
J12	Standard SDMMC0 connector
J14	microSD connector
J15	Ethernet RJ45 connector
J16	CAN 3-pin screw connector
J17	USB-A MicroAB connector
J18	HSIC 2-point header
J19	USB-B type C connector
J20-J23	Jumper to select Pmod functions
J21	Pmod connector
J24-25	mikroBUS1 connectors
J26	Expansion TFT LCD connector for display module
J27	ISC connector
J29-J30	mikroBUS2 connectors
J31	Tamper and analog comparator connector
J32	SHDN test point (not populated)

3.2 Function Blocks

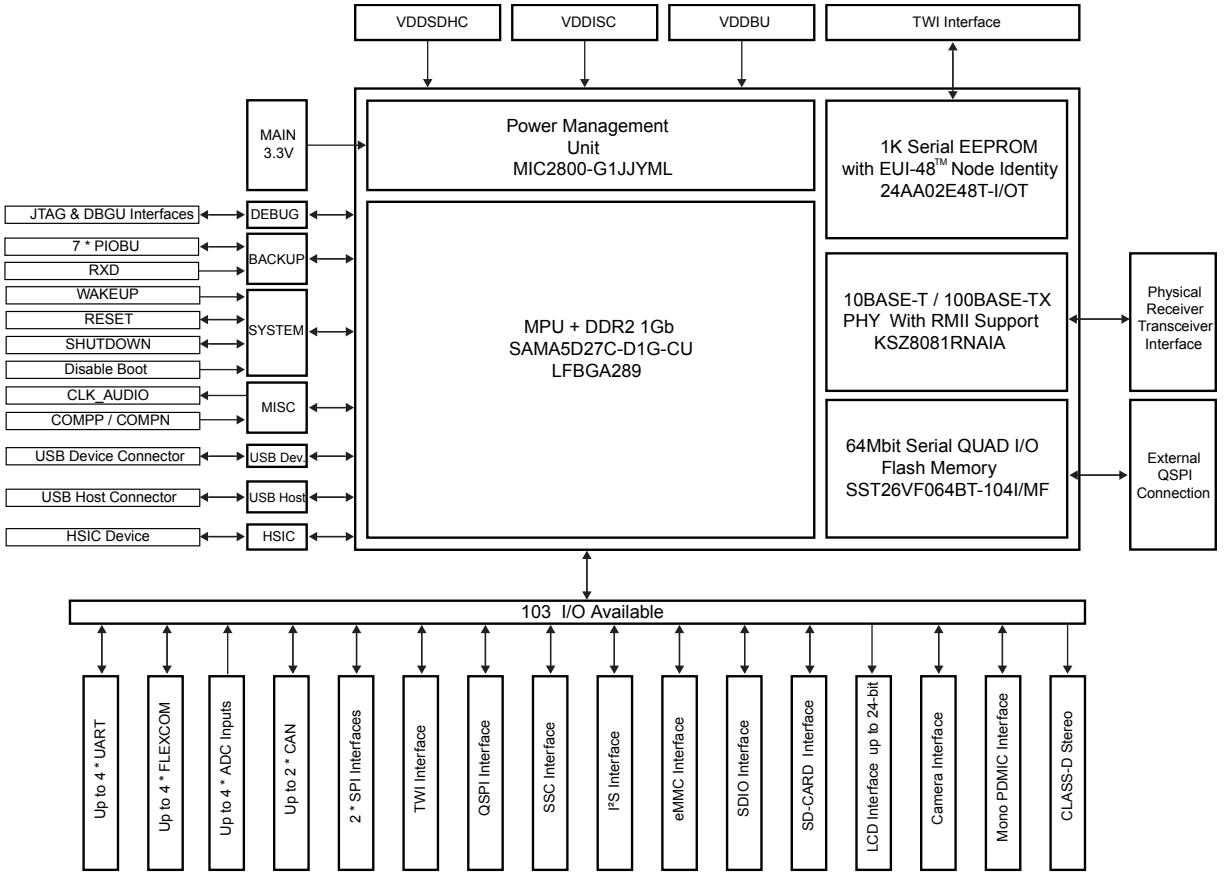
3.2.1 SAMA5D27 SOM1

The SAMA5D27 SOM1 main features are as follows:

- Ultra-small SIP (SAMA5D27-D1G-CU) embedding an ultra-low-power SAMA5D27 Arm® Cortex®-A5 processor and a 1 Gbit DDR2 SDRAM memory
- SST26VF064 64 Mb QSPI Flash
- 24AA02E48 2 Kb serial E^2PROM with preprogrammed EUI node identity
- MIC2800 power management device
- KSZ8081RNA Ethernet Phy 10/100 MHz RMII

Refer to the SAMA5D27 SOM1 datasheet for more information.

Figure 3-4. SAMA5D27 SOM1 Block Diagram



3.2.2 Power Supply Topology and Power Distribution

3.2.2.1 Input Power Options

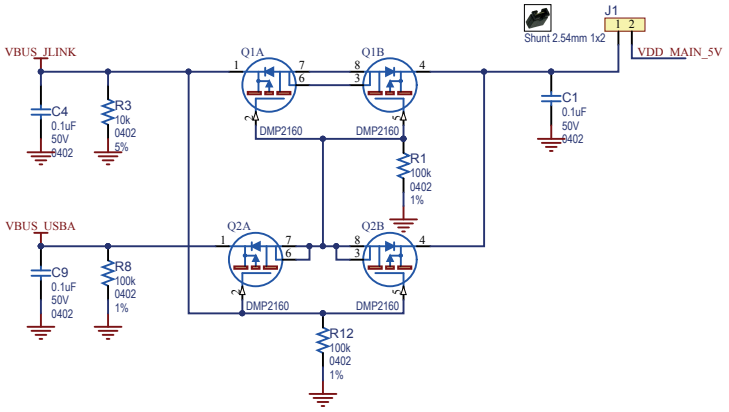
The board power source can come through either a USB connector (J10 or J17) connected to a PC or a 5V DC-USB power supply unit. These USB power sources are sufficient to supply the board in most applications.

Important: In case of an external device connected through the USB-B port, it is recommended to use the 5V DC-USB power supply unit as the main power source for the entire system rather than a PC or a USB hub, which are limited to 500 mA typical.

The baseboard embeds a local power management stage comprising two sets of load switches, respectively implemented by MOSFET DMP2160 and DC/DC converter MIC23451.

The following figure is a schematic of the power options.

Figure 3-5. Input Powering



Note: PC/USB-powered operation eliminates additional wires and batteries. It is the preferred mode of operation for any project that requires only a 5V source at up to 500 mA.

Jumper J1 is used to perform MAIN_5V current measurements on the baseboard.

3.2.2.2 Power Supply Requirements and Restrictions

Detailed information on the device power supplies is provided in tables “SAMA5D2 Power Supplies” and “Power Supply Connections” in the SAMA5D2 Series datasheet.

3.2.2.3 Power-up and Power-down Considerations

Power-up and power-down considerations are described in section “Power Considerations” of the SAMA5D2 Series datasheet.

⚠ CAUTION The power-up and power-down sequences provided in the SAMA5D2 Series datasheet must be respected for reliable operation of the device. These are respected by the on-board MIC23451.

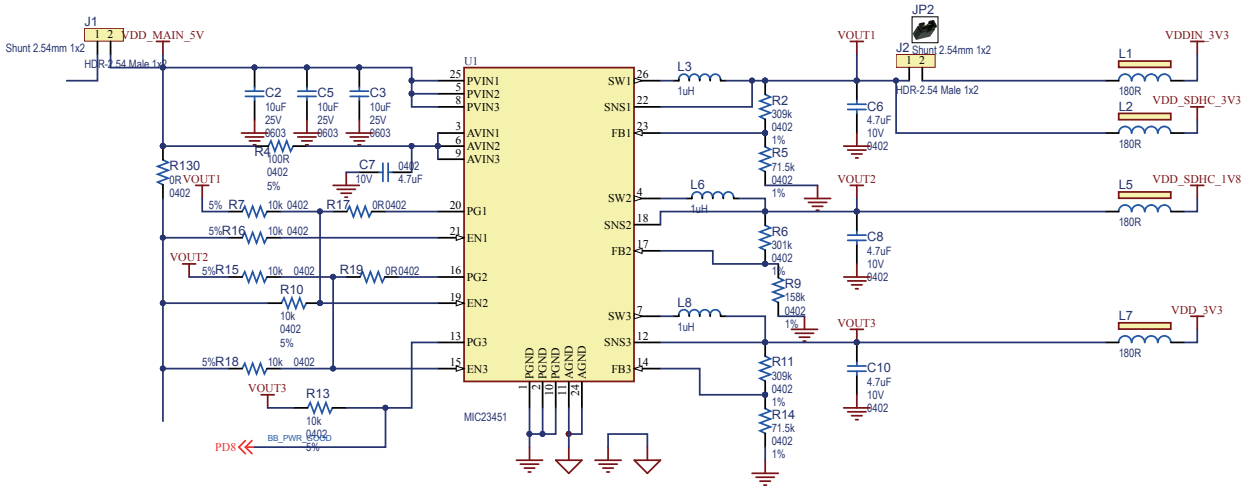
3.2.2.4 Power Management

The baseboard power management uses a MIC23451 PMIC, which is a triple synchronous buck regulator with HyperLight Load® mode featuring a power good indicator. The triple DC-DC step down power regulator delivers two outputs: 3.3V/2A and 1.8V/2A.

While the external power is being applied, the baseboard can be shut down by software and then woken up by action on the PB2 push button, which activates the WKUP signal.

The figure below shows the power management scheme.

Figure 3-6. Baseboard Power Management



One PIO (PD8) is used to check the status of the main regulator.

Table 3-3. Power Good Signal

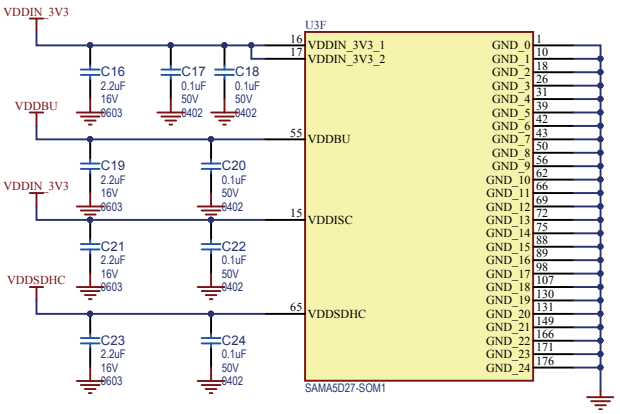
PIO	Mnemonic	Signal Description
PD8	BB_PWR_GOOD	High level = power is established and at correct level

3.2.2.5 Supply Group Configuration

The main regulator provides the 3.3V for the SOM and all power supplies required by the baseboard:

- 3.3V SOM (VDDIN_3V3)
- 3.3V VDDSDHC (3.3V or 1.8V)
- 3.3V baseboard (VDD_3V3)
- 3.3V VDDBU

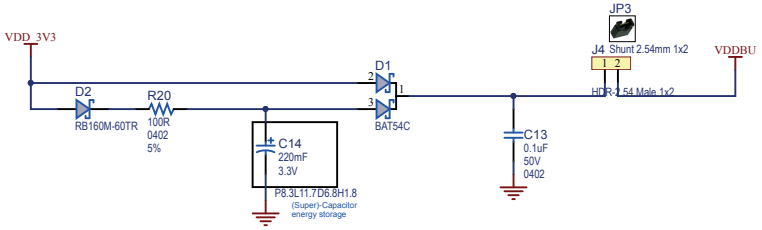
Figure 3-7. SOM Power Lines



3.2.2.6 Backup Power Supply

The baseboard features a power source in order to permanently power the backup area of the SAMA5D2 device (refer to the SAMA5D2 Series datasheet). A super capacitor (C14) sustains such permanent power to VDDBU when all system power sources are off.

Figure 3-8. VDDBU Powering Options



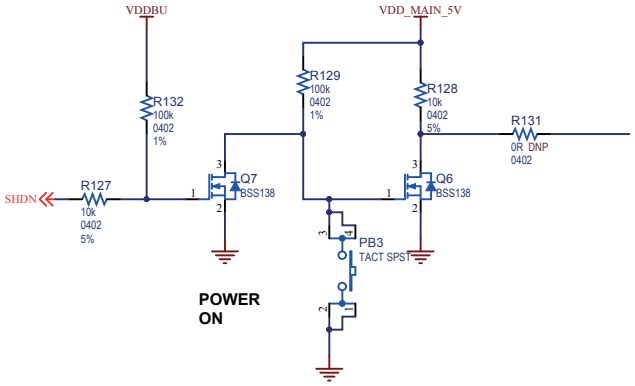
3.2.3 Shutdown Circuitry

On the baseboard, this circuitry is implemented but inhibited by default (R131 is not populated).

The SHDN signal, output of the shutdown controller, signals the shutdown request to the power supply. This output signal is supplied by VDDBU that is present in Backup mode.

The shutdown controller manages the main power supply and is connected to the ENABLE input pin of the DC/DC converter providing the main power supplies of the system.

Figure 3-9. Shutdown Controller

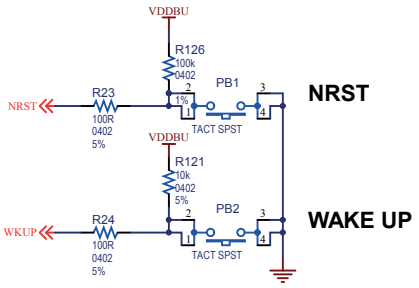


3.2.4 Push Button Switches

The baseboard features four push buttons:

- One reset push button (PB1). When pressed and released, the baseboard is reset.
- One wake-up push button (PB2) connected to the SAMA5D27 WKUP pin, used to exit the processor from Backup mode.
- One power-on button (PB3).

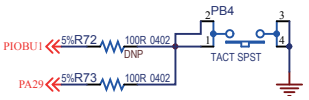
Figure 3-10. System Push Buttons



- One user momentary push button (PB4) connected to PIO PA29, and optionally to PIOBU1.

The wake-up is available only if the shutdown controller is used (see figure Shutdown Controller).

Figure 3-11. User Push Button



3.2.5 Additional Memories

One additional memory, QSPI device U9, can be soldered on the baseboard. This QSPI Flash memory uses the same PIOs as the SOM QSPI. Such configuration makes it possible to choose between two bootable memories.

The figure below illustrates the QSPI memory implementation.

Figure 3-12. Optional QSPI Serial Data Flash on Baseboard

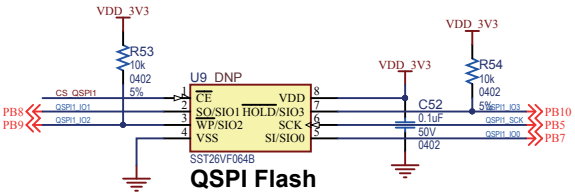


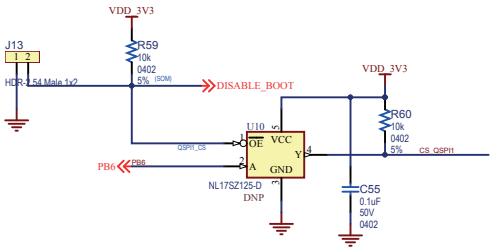
Table 3-4. QSPI Signal Descriptions

PIO	Mnemonic	Shared PIO	Signal Description
PB5	QSPI1_SCK	QSPI on SOM	Clock
PB6	QSPI1_CS	QSPI on SOM	Chip select
PB7	QSPI0_IO0	QSPI on SOM	Data0
PB8	QSPI0_IO1	QSPI on SOM	Data1
PB9	QSPI0_IO2	QSPI on SOM	Data2
PB10	QSPI0_IO3	QSPI on SOM	Data3

3.2.5.1 CS Disable Boot

One jumper (J13) controls the selection (CS#) of the bootable memory components (QSPI) using a non-inverting 3-state buffer.

Figure 3-13. CS Disable Boot



The rule of operation is:

- PB1 (RESET) pressed and J13 open = booting from QSPI on SOM
- PB1 (RESET) pressed and J13 closed = booting from QSPI on baseboard if fitted. The QSPI on SOM is disabled.

Refer to the SAMA5D2 Series datasheet for more information on standard boot strategies and sequencing.

3.2.6 Secure Digital Multimedia Card (SDMMC) Interface

The SD (Secure Digital) Card is a non-volatile memory card format used as a mass storage memory in mobile devices.

3.2.6.1 Secure Digital Multimedia Card (SDMMC) Controller

The baseboard features two Secure Digital Multimedia Card (SDMMC) interfaces that support the MultiMedia Card (e.MMC) Specification V4.41, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 Specification.

- The SDMMC0 interface is connected to a standard SD card interface.
- The SDMMC1 interface is connected to a microSD card interface.

3.2.6.2 SDMMC0 Card Connector (J12)

A standard MMC/SD card connector, connected to SDMMC0, is mounted on the top side of the baseboard. The SDMMC0 communication is based on a 12-pin interface (clock, command, write protect, power switch and data (8)). A card detection switch is included.

The figure below illustrates the SDMMC0 interface implementation.

Figure 3-14. SDMMC0

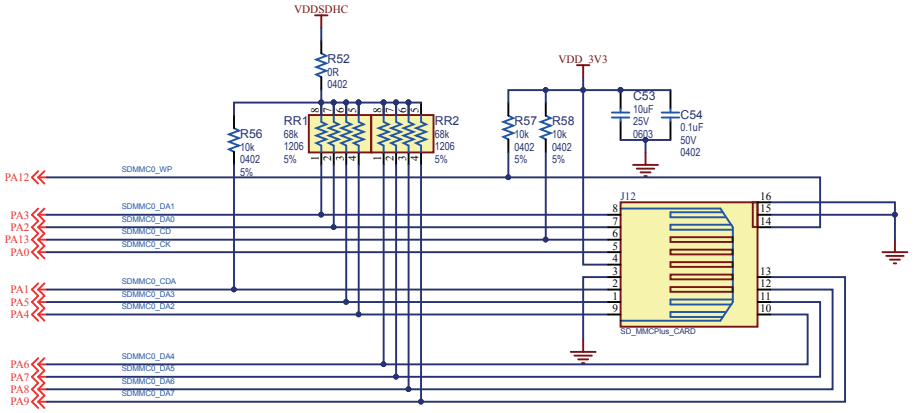
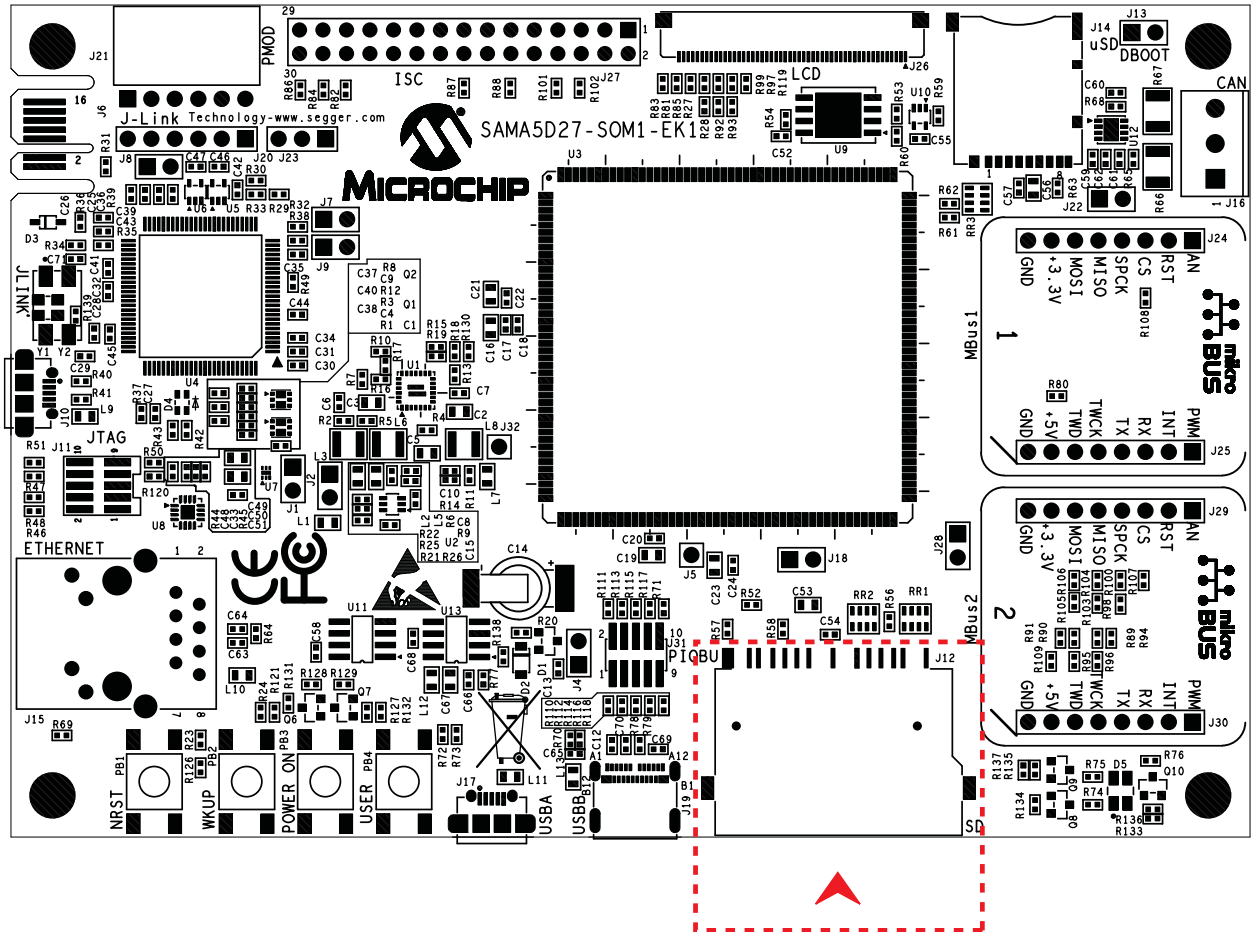


Figure 3-15. Standard SD Socket J12 Location



The table below describes the pin assignment of SDMMC connector J12.

Table 3-5. Standard SD Socket J12 Pin Assignment

Pin No	Mnemonic	PIO	Signal Description
1	SDMMC0_DAT3_PA5	PA5	Data line
2	SDMMC0_CMD_PA1	PA1	Command/response line
3	GND	–	GND
4	VDDSDHC (3.3V or 1.8V)	–	Power line
5	SDMMC0_CK_PA0	PA0	Clock line
6	SDMMC0_CD_PA13	PA13	Card detect
7	SDMMC0_DAT0_PA2	PA2	Data line
8	SDMMC0_DAT1_PA3	PA3	Data line
9	SDMMC0_DAT2_PA4	PA4	Data line
10	SDMMC0_DAT4_PA6	PA6	Data line
11	SDMMC0_DAT5_PA7	PA7	Data line
12	SDMMC0_DAT6_PA8	PA8	Data line
13	SDMMC0_DAT7_PA9	PA9	Data line
14	SDMMC0_WP_PA12	PA12	Write protect signal
15	GND	–	GND
16	GND	–	GND

Table 3-6. SDMMC1 Power Command

PIO	Mnemonic	Signal Description
PA11	SDMMC0_VDDSEL	Select 3.3V or 1.8V

3.2.6.3 SDMMC1 Card Connector (J14)

A microSD card connector, connected to SDMMC1, is mounted on the top side of the baseboard. The SDMMC1 communication is based on a 6-pin interface (clock, command and four data). A card detection switch is included. The microSD connector can be used to connect any microSD card for mass storage.

Figure 3-16. SDMMC1 microSD

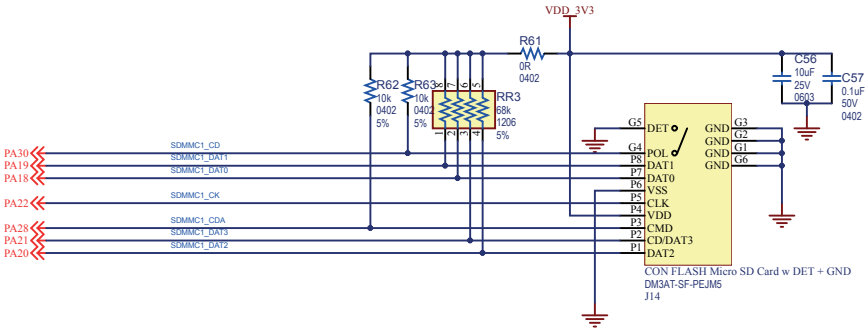
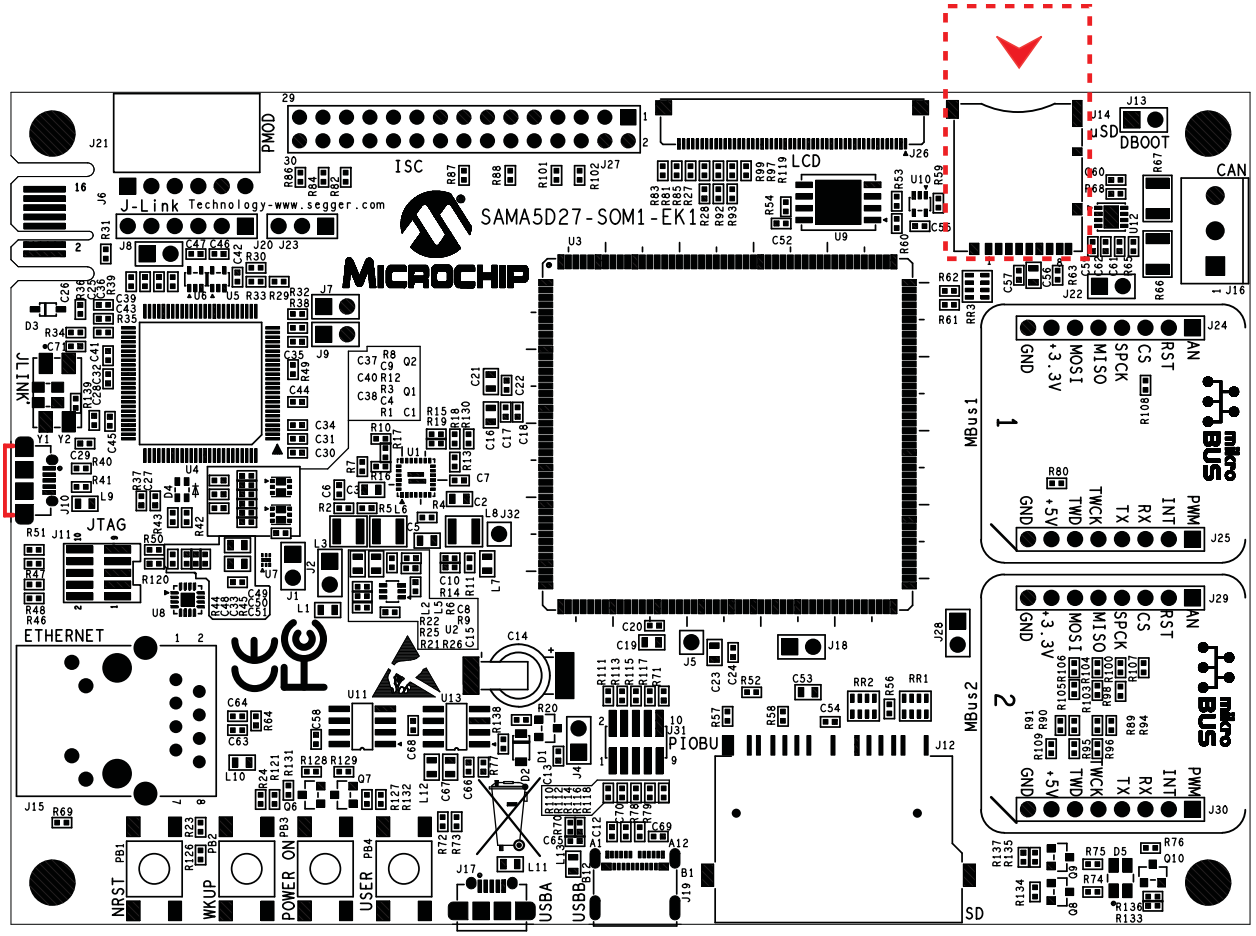


Figure 3-17. microSD Socket J14 Location



The table below describes the pin assignment of microSD connector J14.

Table 3-7. microSD Socket J14 Pin Assignment

Pin No	Mnemonic	PIO	Signal Description
1	SDMMC1_DAT2	PA20	Data bit 2
2	SDMMC1_DAT3	PA21	Data bit 3
3	SDMMC1_CDA	PA28	Command
4	VCC	–	3.3V supply voltage
5	SDMMC1_CK	PA22	Clock
6	GND	–	Common ground
7	SDMMC1_DAT0	PA18	Data bit 0
8	SDMMC1_DAT1	PA19	Data bit 1
9	SW1	GND	Ground
10	SDMMC1_CD	PA30	Card detection switch
11	GND	–	Common ground
12	GND	–	Common ground
13	GND	–	Common ground
14	GND	–	Common ground

3.2.6.4 CryptoAuthentication™

ATECC608A is a member of the CryptoAuthentication family of crypto engine authentication devices with highly secure hardware-based key storage.

The ATECC608A features a flexible command set enabling use in many applications, including network/IoT node protection, anti-counterfeiting, firmware or media protection, secure data storage and user password checking.

The device (U11) is mounted in an 8-lead UDFN package.

For more information, refer to the ATECC608A datasheet on www.microchip.com.

Figure 3-18. CryptoAuthentication ATECC608

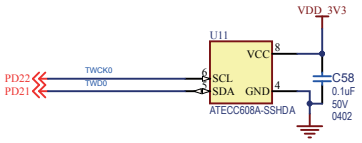


Table 3-8. ATECC608 PIO Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PD21	TWD0	SOM E^2PROM 24AA02E48	TWI data
PD22	TWCK0	SOM E^2PROM 24AA02E48	TWI clock

3.2.7 Communication Interfaces

This section describes the signals and connectors related to the ETH, USB and CAN communication interfaces.

3.2.7.1 Ethernet 10/100 (GMAC) Port

The on-board SOM integrates a 10/100 Mbps Ethernet controller (KSZ8081RNA) allowing direct connection to any 10/100 Mbps Ethernet-based Local Area Network, for full interaction with local servers and wide area networks such as the Internet.

ETH signals from the SOM are connected to a RJ45 MagJack. Additionally, for monitoring and control purposes, a LED functionality is carried on the RJ45 connector to indicate link status.

Figure 3-19. Ethernet PHY

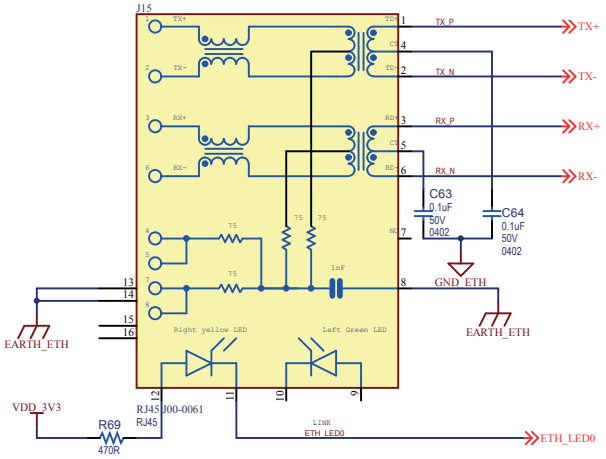
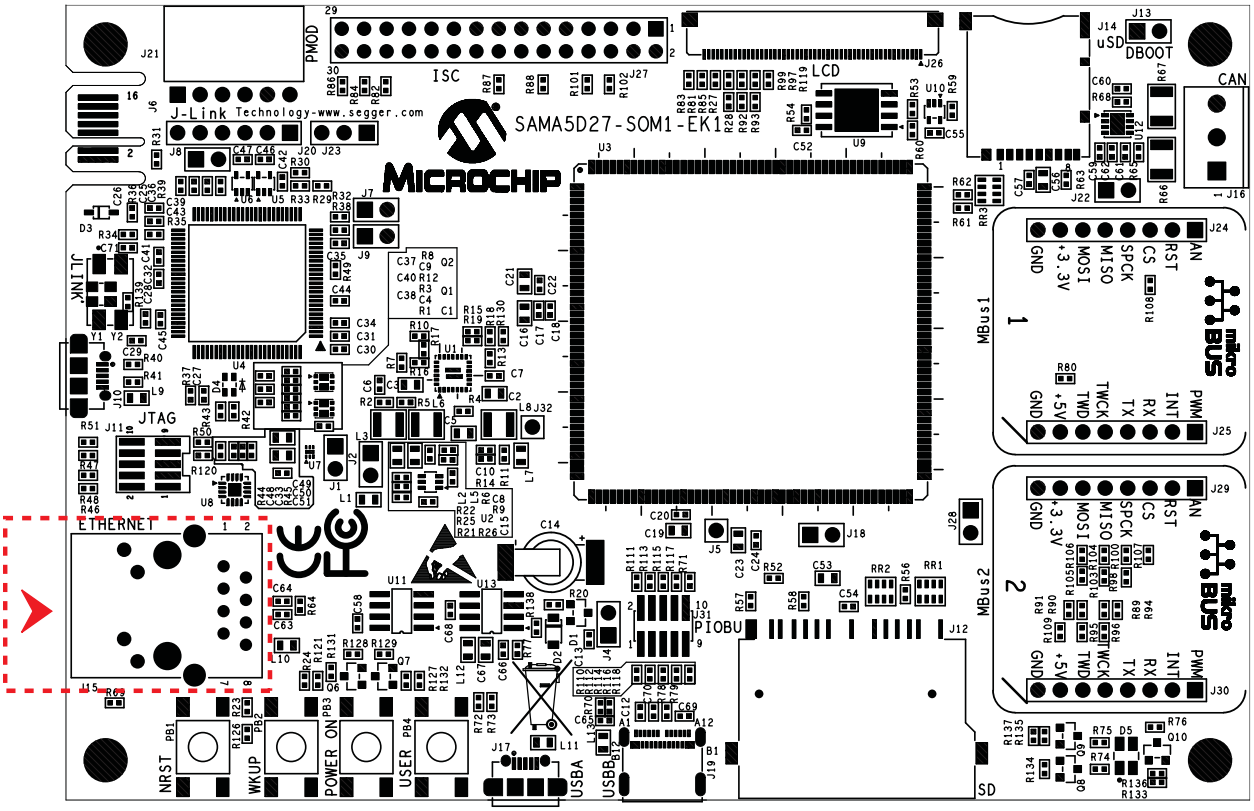


Figure 3-20. Ethernet RJ45 Connector J15 Location



The table below describes the pin assignment of Ethernet connector J15.

Table 3-9. Ethernet RJ45 Connector J15 Pin Assignment

Pin No	Mnemonic	Signal Description
1	TX+	Transmit positive differential pair
2	TX-	Transmit negative differential pair
3	RX+	Receive positive differential pair
4	Decoupling capacitor	–

.....continued		
Pin No	Mnemonic	Signal Description
5	Decoupling capacitor	–
6	RX-	Receive negative differential pair
7	NC	–
8	EARTH / GND	Common ground
9	ACT LED (A)	LED activity (not used)
10	ACT LED (K)	LED activity (not used)
11	LINK LED (K)	LED link connection
12	LINK LED (A)	LED link connection
13	EARTH / GND	Common ground
14	EARTH / GND	Common ground
15	NC	–
16	NC	–

3.2.7.2 USB Interfaces

The USB (Universal Serial Bus) is a hot-pluggable general-purpose high-speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High Speed USB). A USB host bus connector uses 4 pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin.

The baseboard features three USB communication ports named USB-A to USB-C:

- USB-A device interface
  - One USB device standard micro-AB connector.
  - This port offers a VBUS detection function through the R81-R83 resistor ladder.
  - The USB-A port is used as a secondary power source and as a communication link for the baseboard, and derives power from the PC over the USB cable. In most cases, this port is limited to 500 mA.
- USB-B (host port B high- and full-speed interface)
  - One USB host type C connector.
  - The USB-B host port is equipped with a 500 mA high-side power switch.
- USB-C (High-Speed Inter-Chip/HSIC port)
  - One USB high-speed host port with an HSIC interface.
  - The port is connected to a single 2-pin header (not populated).

3.2.7.3 USB-A Interface

The figure below shows the USB implementation on the USB-A port terminated on a micro USB type microAB connector.

The USB-A port (J17) features a VBUS insert detection function through ladder-type resistors R70 and R71.

Figure 3-21. USB-A Type microAB Connector

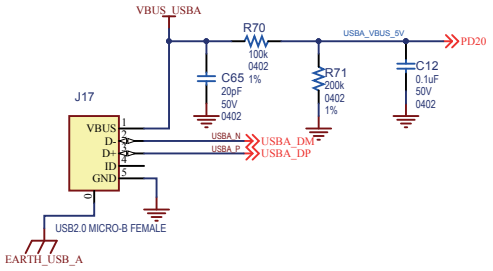
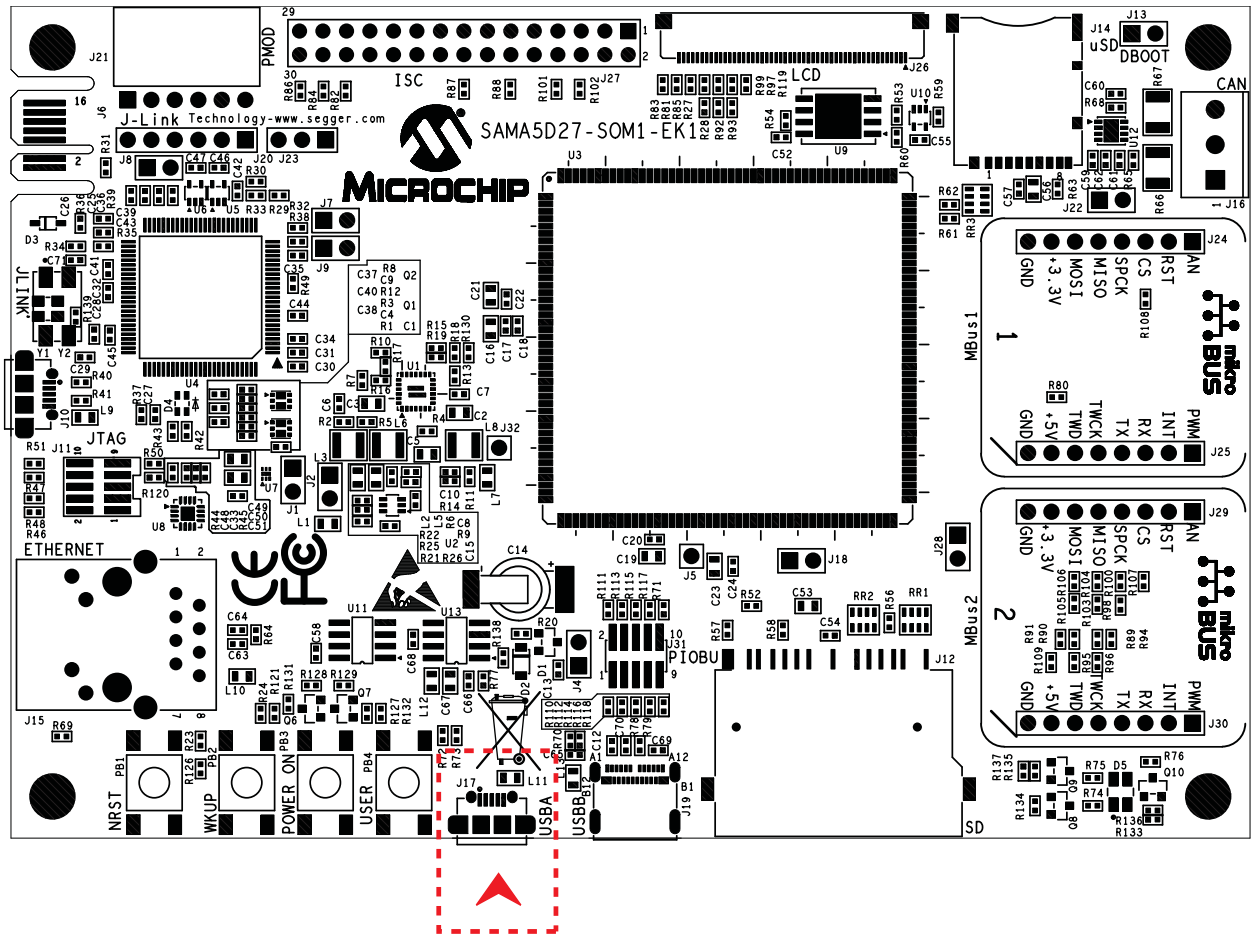


Table 3-10. USB-A PIO Signal Description

PIO	Mnemonc	Shared	Signal Description
PD20	USBA_VBUS_5V	–	VBUS insertion detection

Figure 3-22. USB-A Type microAB Connector J17 Location



The table below describes the pin assignment of USB-A connector J17.

Table 3-11. USB-A Connector J17 Pin Assignment

Pin No	Mnemonic	Signal Description
1	VBUS	5V power
2	DM	Data minus
3	DP	Data plus

.....continued		
Pin No	**Mnemonic**	**Signal Description**
4	ID	On-the-go identification
5	GND	Common ground

3.2.7.4 USB-B Interface

The figure below shows the USB implementation on the USB-B port terminated on USB Type C connector J19.

Figure 3-23. USB-B Type C Connector

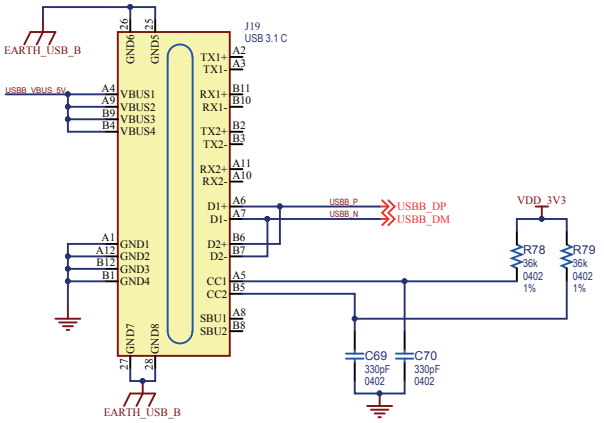
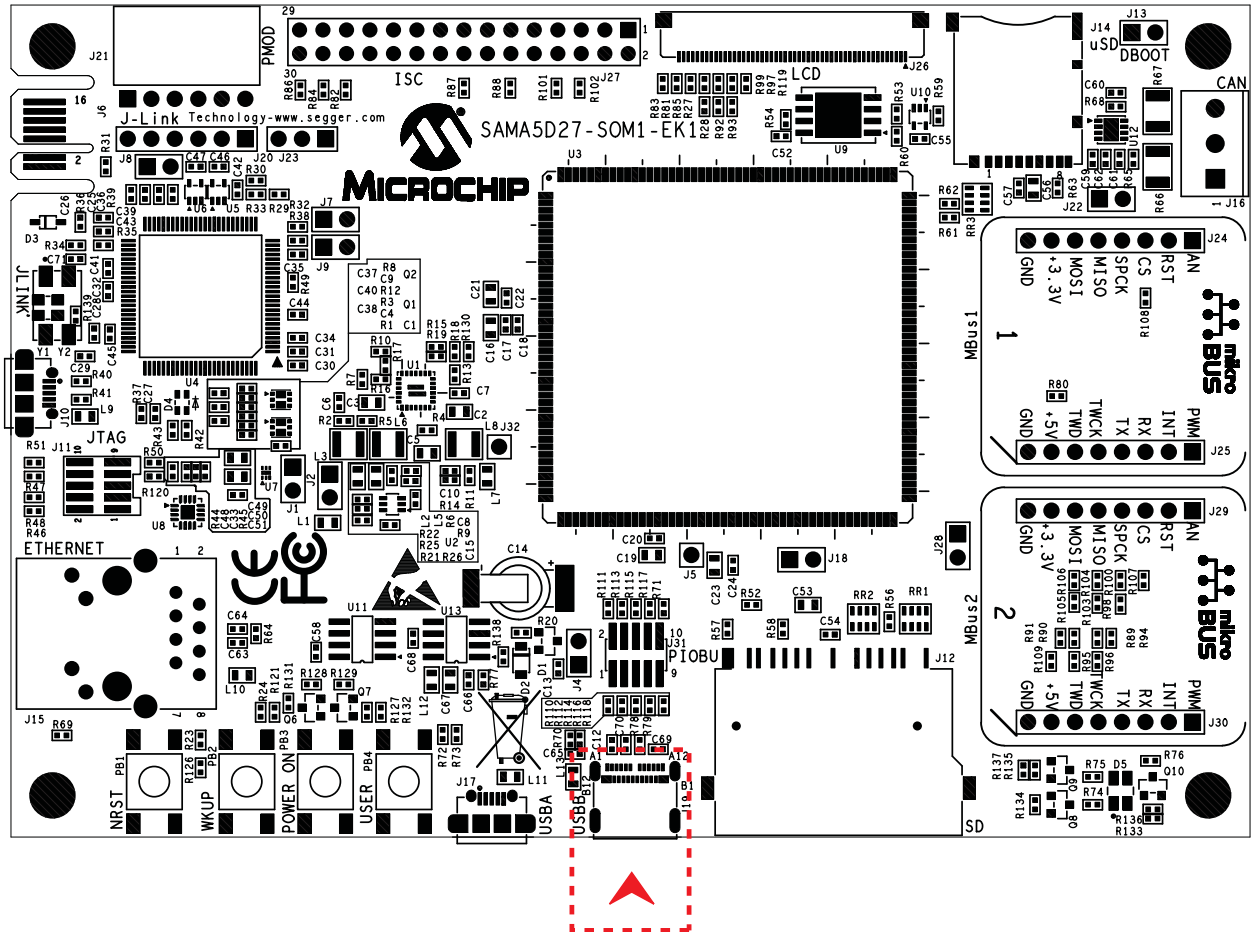


Figure 3-24. USB-B Type C Connector J19 Location



The table below describes the pin assignment of USB-B connector J19.

Table 3-12. USB-B Connector J19 Pin Assignment

Pin No	Mnemonic	Signal Description
A1	GND	Ground return
A2	SSTXp1	SuperSpeed differential pair #1, TX, positive (NOT USED)
A3	SSTXn1	SuperSpeed differential pair #1, TX, negative (NOT USED)
A4	VBUS	Bus power
A5	CC1	Configuration channel
A6	DP1	USB 2.0 differential pair, position 1, positive
A7	DN1	USB 2.0 differential pair, position 1, negative
A8	SBU1	Sideband use (SBU)
A9	VBUS	Bus power
A10	SSRXn2	SuperSpeed differential pair #2, RX, negative (NOT USED)
A11	SSRXp2	SuperSpeed differential pair #2, RX, positive (NOT USED)
A12	GND	Ground return
B12	GND	Ground return
B11	SSRXp1	SuperSpeed differential pair #1, RX, positive (NOT USED)
B10	SSRXn1	SuperSpeed differential pair #1, RX, negative (NOT USED)
B9	VBUS	Bus power

.....continued		
Pin No	**Mnemonic**	**Signal Description**
B8	SBU2	Sideband use (SBU)
B7	DN2	USB 2.0 differential pair, position 2, negative
B6	DP2	USB 2.0 differential pair, position 2, positive
B5	CC2	Configuration Channel
B4	VBUS	Bus power
B3	SSTXn2	SuperSpeed differential pair #2, TX, negative (NOT USED)
B2	SSTXp2	SuperSpeed differential pair #2, TX, positive (NOT USED)
B1	GND	Ground return

3.2.7.4.1 USB-B Power Switch

The USB-B Host port is equipped with a 500 mA high-side power switch for self-powered and bus-powered applications. If the client device is bus-powered, the carrier can supply a 5V, 500mA power to the client device. The USBB_EN_5V_PA27 signal controls the power switch and current limiter, the Microchip MIC2025, which in turn supplies power to a bus-powered client device. Per the USB specification, bus-powered USB 2.0 devices are limited to a maximum of 500 mA. The MIC2025 limits the current and indicates an overcurrent with the USBB_OVCUR_PD19 signal.

Figure 3-25. USB-B Power Switch

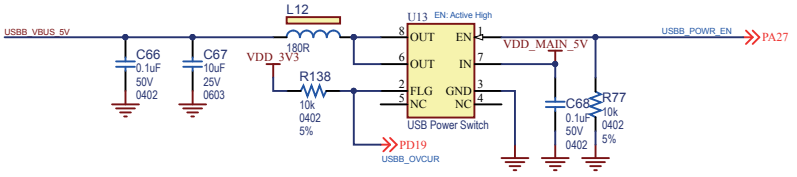


Table 3-13. Power Switch PIO Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PA27 USBB_POWR_EN	USBB_EN_5V	–	Power switch enable (active high)
PD19	USBB_OVCUR	–	Indicates overcurrent (open drain)

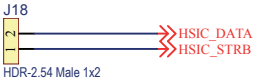
3.2.7.5 HSIC Interface

High-Speed Inter-Chip (HSIC) is a standard for USB chip-to-chip interconnect with a 2-signal (strobe, data) source synchronous serial interface using 240 MHz DDR signaling to provide only high-speed 480 Mbps data rate.

The interface operates at high speed, 480 Mbps, and is fully compatible with existing USB software stacks. It meets all data transfer needs through a single unified USB software stack.

The HSIC interface is connected to two-point header J18. This connector is not mounted.

Figure 3-26. HSIC Interface J18



3.2.7.6 CAN Interface

This section lists the signals related to the Controller Area Network (CAN) interface.

The CAN interface transmits and receives signals from the SOM. CAN PIOs PC26 and PC27 are connected to the CAN transceiver (ATA6561) and the output signals from the transceiver are connected to the screw connector (J16) physically located on top of the baseboard.

Figure 3-27. CAN Interface

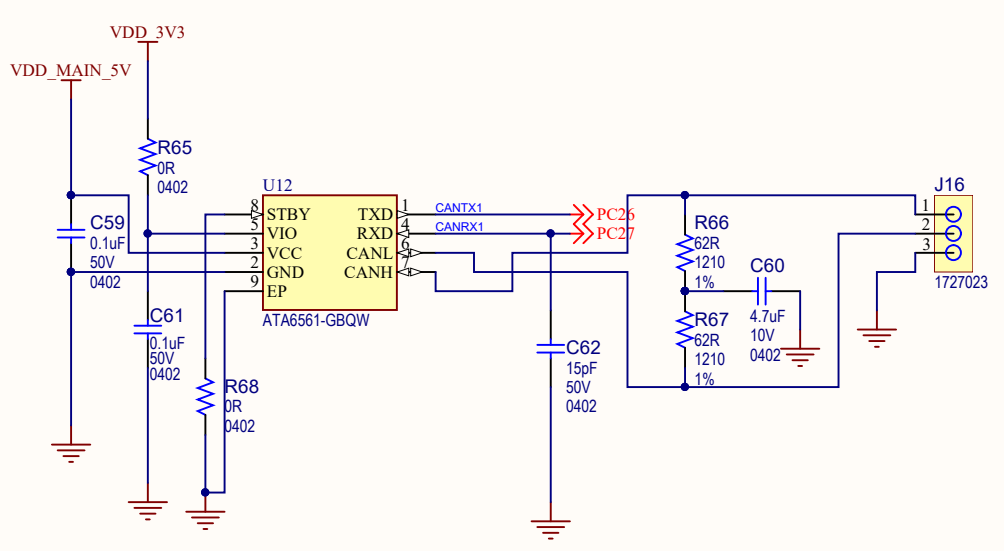


Figure 3-28. CAN Connector J16 Location

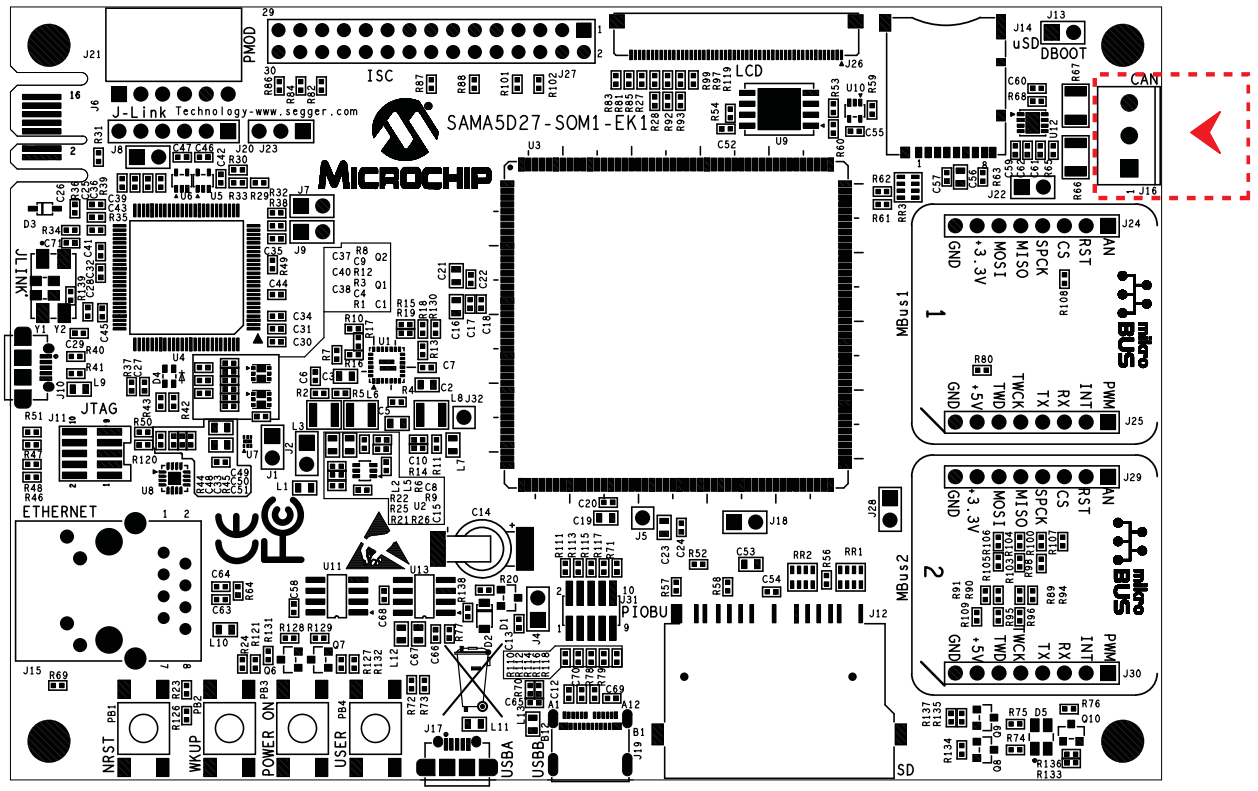


Table 3-14. CAN Connector J16 Pin Assignment

Pin	Mnemonic	Signal Description
1	CANH	Differential positive

.....continued		
Pin	Mnemonic	Signal Description
2	CANL	Differential negative
3	GND	Ground

3.3 External Interfaces

3.3.1 LCD TFT Interface

The baseboard provides a FPC connector with 24 bits of data and control signals to the LCD interface. Other signals are used to control the LCD and are available on connector J26: TWI, SPI, two GPIOs for interrupt, 1-wire and power supply lines.

This connector is used to connect LCD display type TM43xx series, TM5000 series or TM7000 series from PDA Inc. (www.pdaatl.com).

A 50-pin FPC (J26) header is provided on the baseboard to interface the LCD module with 24-bit parallel RGB.

The connector provides two PIOs as interrupts, one SPI and a TWI port to interface the MaXTouch® touch controller or QTouch® button controller embedded on the LCD module.

In order to operate correctly out of the processor with various LCD modules, two voltage lines are available: 3.3V and 5VCC (default). Both are selected by 0R resistors R81 and R83.

Figure 3-29. LCD Expansion Header Interface

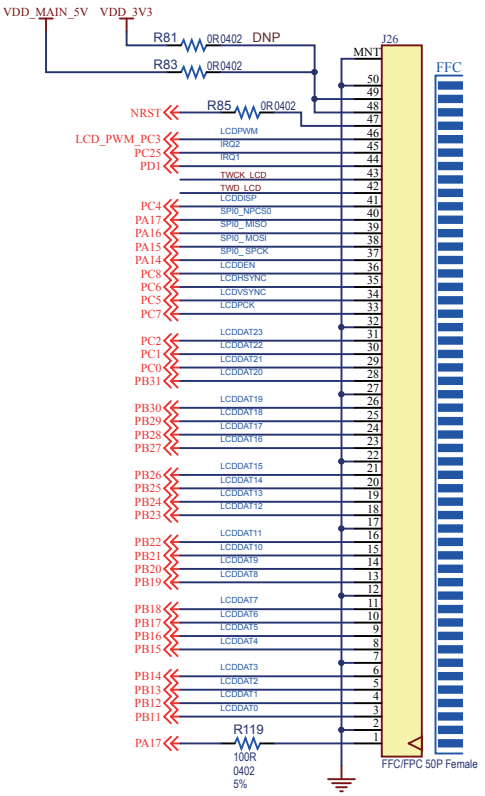
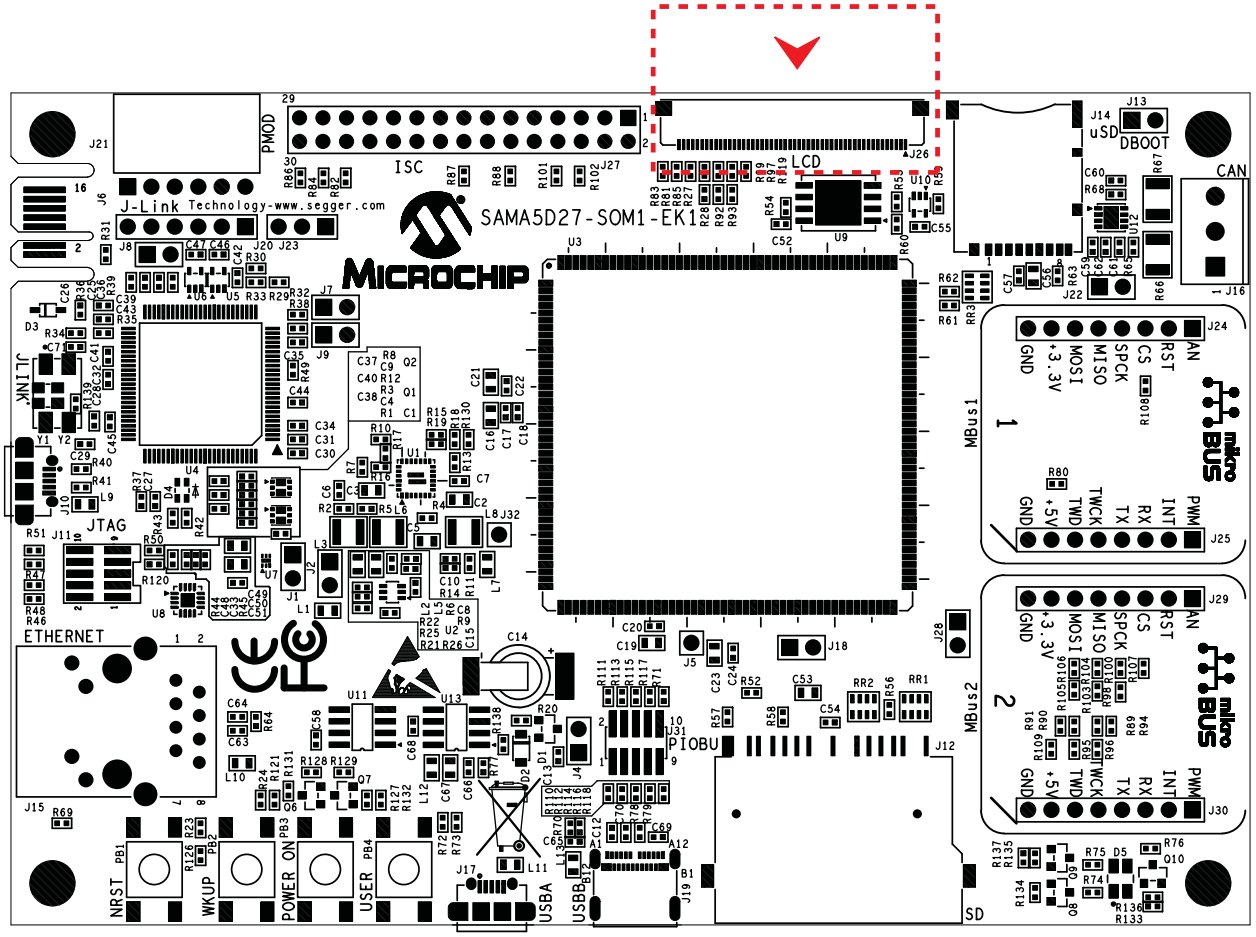


Figure 3-30. LCD Connector J26 Location



The table below describes the pin assignment of LCD connector J26.

Table 3-15. LCD Connector J26 Pin Assignment

Pin No	Signal	PIO	Signal	RGB Interface Function
1	ID	PA17	ID	Shared with SPI_NPCS0 pin 40
2	GND	GND	GND	GND
3	LCDDAT0	PB11	D0	Data line (BLUE0)
4	LCDDAT1	PB12	D1	Data line (BLUE1)
5	LCDDAT2	PB13	D2	Data line (BLUE2)
6	LCDDAT3	PB14	D3	Data line (BLUE3)
7	–	–	GND	GND
8	LCDDAT4	PB15	D4	Data line (BLUE4)
9	LCDDAT5	PB16	D5	Data line (BLUE5)
10	LCDDAT6	PB17	D6	Data line (BLUE6)
11	LCDDAT7	PB18	D7	Data line (BLUE7)
12	–	GND	GND	GND
13	LCDDAT8	PB19	D8	Data line (GREEN0)
14	LCDDAT9	PB20	D9	Data line (GREEN1)
15	LCDDAT10	PB21	D10	Data line (GREEN2)
16	LCDDAT11	PB22	D11	Data line (GREEN3)

.....continued				
Pin No	Signal	PIO	Signal	RGB Interface Function
17	–	–	GND	GND
18	LCDDAT12	PB23	D12	Data line (GREEN4)
19	LCDDAT13	PB24	D13	Data line (GREEN5)
20	LCDDAT14	PB25	D14	Data line (GREEN6)
21	LCDDAT15	PB26	D15	Data line (GREEN7)
22	–	GND	GND	GND
23	LCDDAT16	PB27	D16	Data line (RED0)
24	LCDDAT17	PB28	D17	Data line (RED1)
25	LCDDAT18	PB29	D18	Data line (RED2)
26	LCDDAT19	PB30	D19	Data line (RED3)
27	–	–	GND	GND
28	LCDDAT20	PB31	D20	Data line (RED4)
29	LCDDAT21	PC0	D21	Data line (RED5)
30	LCDDAT22	PC1	D22	Data line (RED6)
31	LCDDAT23	PC2	D23	Data line (RED7)
32	–	GND	GND	GND
33	LCDPCK	PC7	PCLK	Pixel clock
34	LCDVSYNC	PC5	VSYNC/CS	Vertical sync
35	LCDHSYNC	PC6	HSYNC/WE	Horizontal sync
36	LCDDEN	PC8	DATA_ENABLE	Data enable
37	SPI_SPCK	PA14	SPI_SCK	SPI clock
38	SPI_MOSI	PA15	SPI_MOSI	SPI Master OUT Slave IN
39	SPI_MISO	PA16	SPI_MISO	SPI Master IN Slave OUT
40	SPI_NPCS0	PA17	SPI_CS	SPI chip select
41	LCDDISP	PC4	ENABLE	Display enable signal
42	TWD	PD4	TWI_SDA	I2C data line (maXTouch)
43	TWCK	PD5	TWI_SCL	I2C clock line (maXTouch)
44	GPIO	PD1	IRQ1	maXTouch interrupt line
45	GPIO	PC25	IRQ2	Interrupt line for other I2C devices
46	LCDPWM	PC3	PWM	Backlight control
47	RESET	nRST	RESET	Reset for both display and maXTouch
48	Main_5V/3V3	VCC	VCC	3.3V or 5V supply (R81/R83 selected)
49	Main_5V/3V3	VCC	VCC	3.3V or 5V supply (R81/R83 selected)
50	GND	GND	GND	GND

3.3.2 Image Sensor (ISC) Interface

This section describes the signals and connectors related to the ISC interface.

The Image Sensor Controller (ISC) system manages incoming data from a parallel or serial CSI-2 based CMOS/CCD sensor. The system supports a single active interface, as well as the ITU-R BT 656/1120 422 protocol with an 8-bit or 10-bit data width and raw Bayer format. The internal image processor includes adjustable white balance, color filter array interpolation, color correction, gamma correction, 12-bit to 10-bit compression, programmable color space conversion, as well as horizontal and vertical chrominance subsampling module.

Figure 3-31. ISC Interface

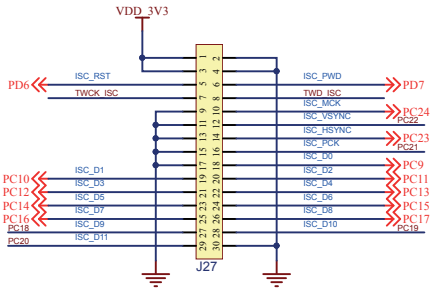
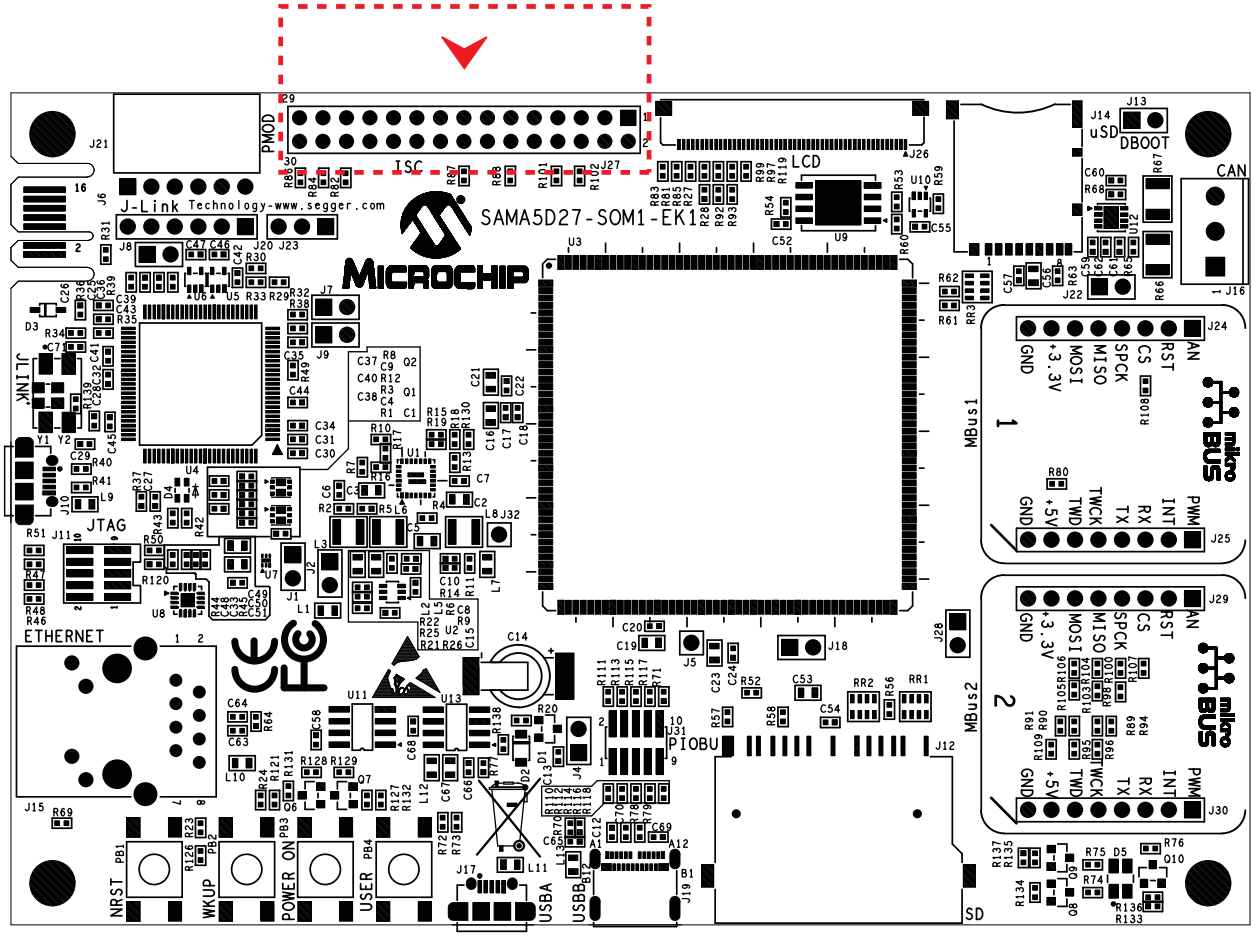


Figure 3-32. ISC Connector J27 Location



The table below describes the pin assignment of ISC connector J27.

Table 3-16. ISC Connector J27 Pin Assignment

SAMA5D27		Signal	Pin No		Signal	SAMA5D27	
Function	PIO					PIO	Function
3.3V power	–	VDD_3V3	1	2	GND	–	Ground
3.3V power	–	VDD_3V3	3	4	GND	–	Ground
Reset	PD6	ISC_RST	5	6	ISC_PWD	PD7	Power down
TWI clock	PD5	TWCK_ISC	7	8	TWD_ISC	PD4	TWI data
Ground	–	GND	9	10	ISC_MCK	PC24	Master clock

.....continued

SAMA5D27		Signal	Pin No		Signal	SAMA5D27	
Function	PIO					PIO	Function
Ground	–	GND	11	12	ISC_VSYNC	PC22	Vertical sync
Ground	–	GND	13	14	ISC_HSYNC	PC23	Horizontal sync
Ground	–	GND	15	16	ISC_PCK	PC21	Clock
Ground	–	GND	17	18	ISC_D0	PC9	Data0
Data1	PC10	ISC_D1	19	20	ISC_D2	PC11	Data2
Data3	PC12	ISC_D3	21	22	ISC_D4	PC13	Data4
Data5	PC14	ISC_D5	23	24	ISC_D6	PC15	Data6
Data7	PC16	ISC_D7	25	26	ISC_D8	PC17	Data8
Data9	PC18	ISC_D9	27	28	ISC_D10	PC19	Data10
Data11	PC20	ISC_D11	29	30	GND	–	Ground

Note: ISC and LCD share the same TWI interface.

3.3.3 RGB LED

The baseboard features one RGB LED which can be controlled by the user. The three LED cathodes are controlled via GPIO PWM or timer/counter pins.

Figure 3-33. RGB LED Indicators

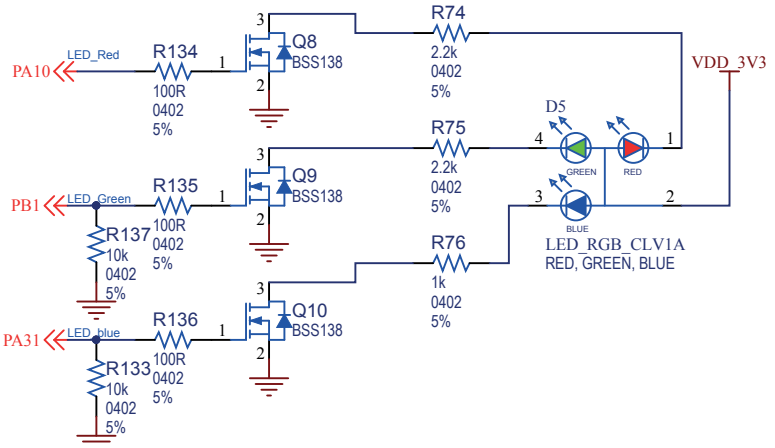


Table 3-17. RGB LED PIOs

Signal	Shared	PIO	Function
LED_RED	–	PA10	TIOA1
LED_GREEN	PWM MBUS1	PB1	PWML1
LED_BLUE	PWM MBUS2	PA31	PWML0

3.4 Debugging Capabilities

The baseboard includes two main debugging interfaces to provide debug-level access to the SAMA5D2:

- One UART through USB J-Link-CDC
- Two JTAG interfaces, one connected from the MPU using connector J11 and one through the J-Link-OB interface USB port J10

3.4.1 Debug JTAG

This section describes the signals and connectors related to the JTAG interface.

A 10-pin JTAG header is provided on the baseboard to facilitate software development and debugging using various JTAG emulators. The interface signals have a voltage level of 3.3V.

Figure 3-34. JTAG Interface

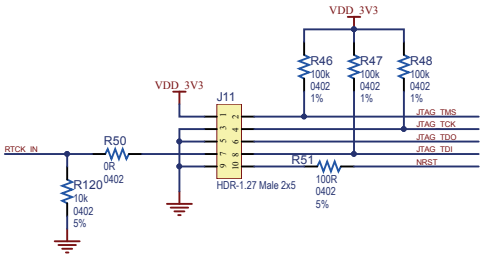
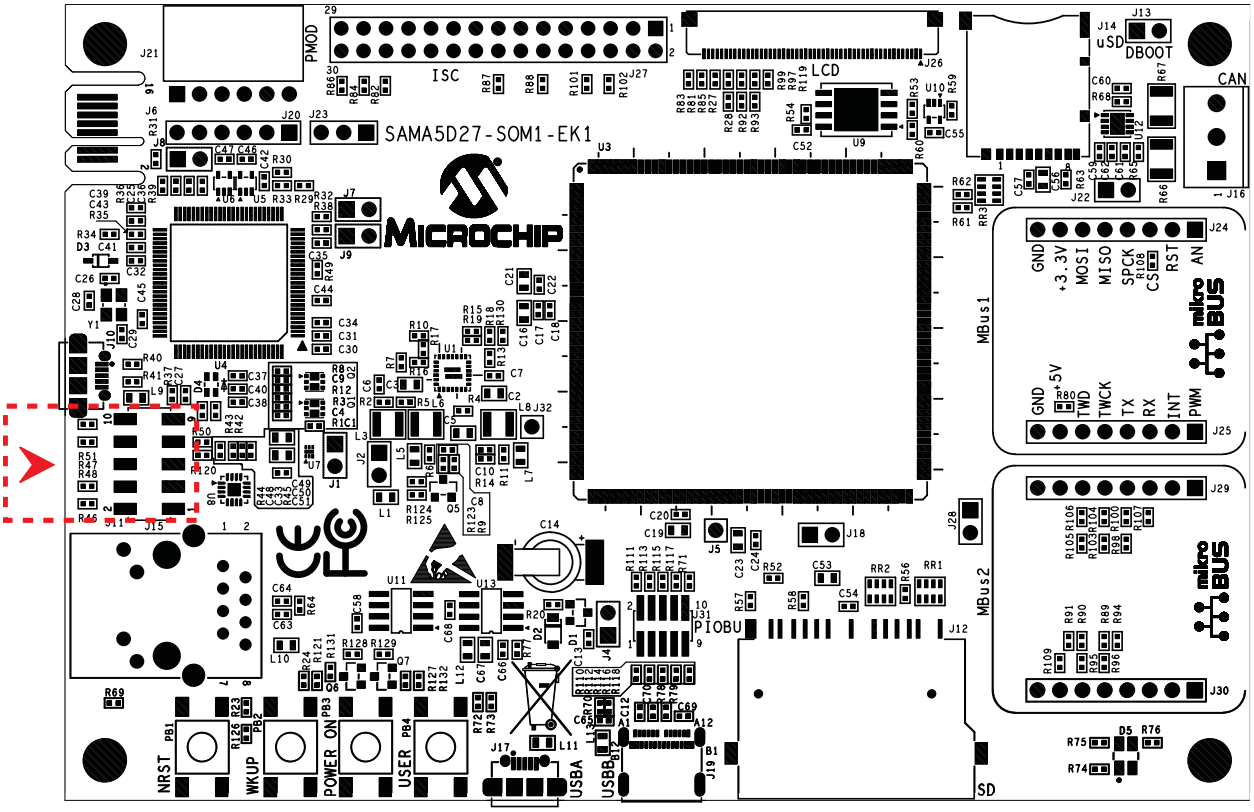


Figure 3-35. JTAG Connector J11 Location



The table below describes the pin assignment of JTAG connector J11.

Table 3-18. JTAG/ICE Connector J11 Pin Assignment

Pin No	Mnemonic	Signal Description
1	VTref. 3.3V power	This is the target reference voltage (main 3.3V).
2	TMS TEST MODE SELECT	JTAG mode set input into target processor
3	GND	Common ground
4	TCK TEST CLOCK - Output timing signal, for synchronizing test logic and control register access	JTAG clock signal into target processor
5	GND	Common ground

.....continued		
Pin No	**Mnemonic**	**Signal Description**
6	TDO JTAG TEST DATA OUTPUT - Serial data input from the target	JTAG data output from target processor
7	RTCK - Input return test clock signal from the target	Some targets with a slow system clock must synchronize the JTAG inputs to internal clocks. In the present case, such synchronization is unneeded and TCK is merely looped back into RTCK.
8	TDI TEST DATA INPUT - Serial data output line, sampled on the rising edge of the TCK signal	JTAG data input into target processor
9	GND	Common ground
10	nRST RESET	Active-low reset signal. Target processor reset signal.

3.4.2 Embedded Debugger (J-Link-OB) Interface

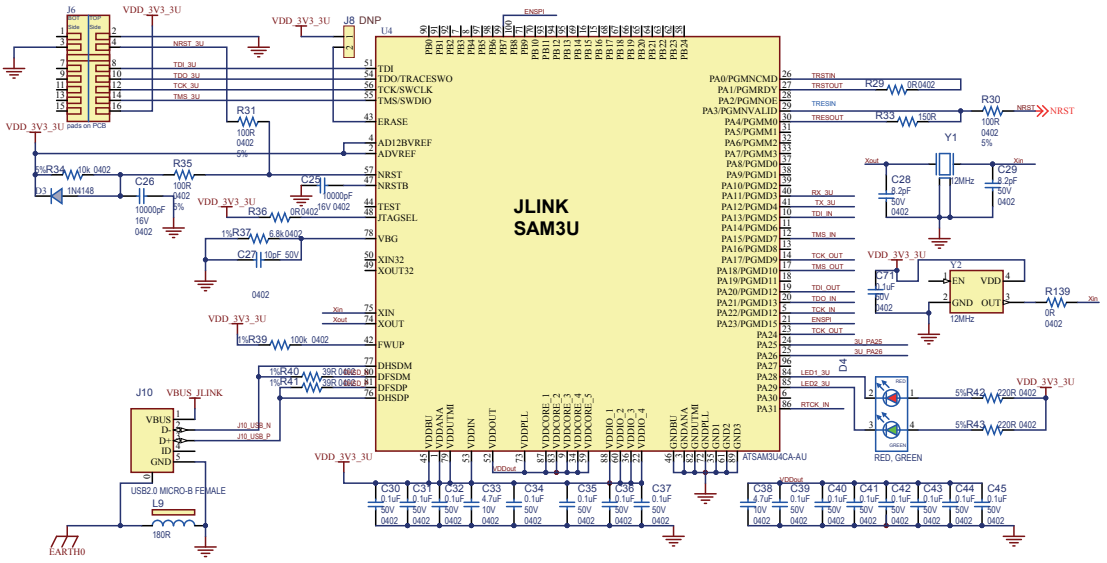
The baseboard includes a built-in SEGGER J-Link-On-Board device. The functionality is implemented with an ATSAM3U4C microcontroller in an LQFP100 package. The ATSAM3U4C provides JTAG functions and a bridge USB/Serial debug port (CDC). One dual LED D4 mounted on the baseboard shows the status of the J-Link-On-Board device.

J-Link-OB-ATSAM3U4C was designed in order to provide an efficient, low-cost, on-board alternative to the standard J-Link.

The internal J-Link-OB connects to the target only after it receives a first command; otherwise, it remains disabled.

The USB J-Link-OB port is used as a secondary power source and as a communication link for the baseboard, and derives power from the PC over the USB cable. This port is limited in most cases to 500 mA. A single PC USB port is sufficient to power the baseboard.

Figure 3-36. J-Link-OB Interface



3.4.2.1 Disabling J-Link-OB (ATSAM3U4C)

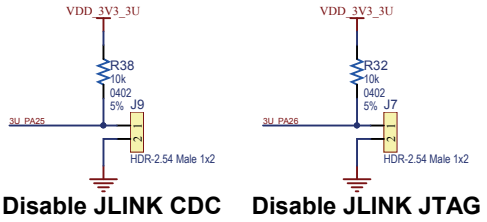
Jumper J7 disables the J-Link-OB-ATSAM3U4C JTAG functionality. When the jumper is installed, it grounds pin 25 (PA26) of the ATSAM3U4C that is normally pulled high.

- Jumper J7 not installed: J-Link-OB-ATSAM3U4C is enabled and fully functional.

- Jumper J7 installed: J-Link-OB-ATSAM3U4C is disabled and an external JTAG controller can be used through the 10-pin JTAG port J11.

Jumper JP9 disables only the J-Link functionality. The debug serial com port that is emulated through a Communication Device class (CDC) of the same USB connector remains operational (if J9 is open).

Figure 3-37. Enabling/Disabling J-Link-OB and J-Link-CDC



Jumper J7 disables the JTAG functionality only. The debug serial com port that is emulated through a CDC of the same USB connector remains operational.

When J7 is on and the J-Link-OB-ATSAM3U4C JTAG disabled, the JTAG function is available through connector J11. A quad analog switch (NLAS3899B) is used to select and isolate the JTAG interface.

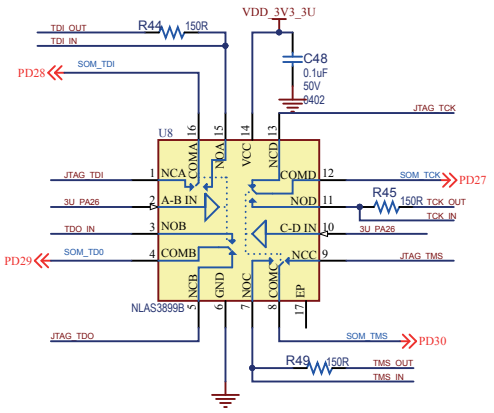
Table 3-19. J-Link-OB and J-Link-CDC Jumper J7 Settings

Jumper J7	J-Link-OB	JTAG MPU
Open	Active	Inactive
Closed	Inactive	Active

Table 3-20. J-Link-OB and J-Link-CDC Jumper J9 Settings

Jumper J9	J-Link-CDC
Open	Active
Closed	Inactive

Figure 3-38. JTAG Switch



3.4.3 Hardware UART via J-Link-CDC

In addition to the J-Link-OB functionality, the ATSAM3U4C microcontroller provides a bridge to a debug serial port (UART DBGU) of the processor on a SOM board. The port is made accessible over the same USB connection used by JTAG by implementing Communication Device Class (CDC), which allows terminal communication with the target device.

This feature is enabled only if microcontroller pin 24 (PIO PA25) is not grounded. The pin is normally pulled high and controlled by jumper J9.

- Jumper J9 not installed: the J-Link-CDC is enabled and fully functional.
- Jumper J9 installed: the J-Link-CDC device is disabled.

The USB Communications Device Class (CDC) enables conversion of the USB device into a serial communication device. The target device running USB-Device CDC is recognized by the host as a serial interface (USB2COM, virtual COM port) without the need to install a special host driver (since the CDC is standard). All PC software using a COM port work without modifications with this virtual COM port. Under Windows®, the device shows up as a COM port; under Linux, as a /dev/ACMx device. This enables the user to use host software which was not designed to be used with USB, such as a terminal program.

Figure 3-39. Debug COM Port Isolation

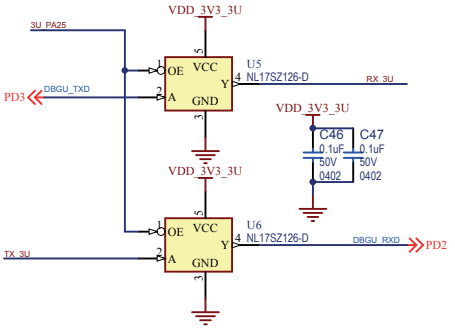
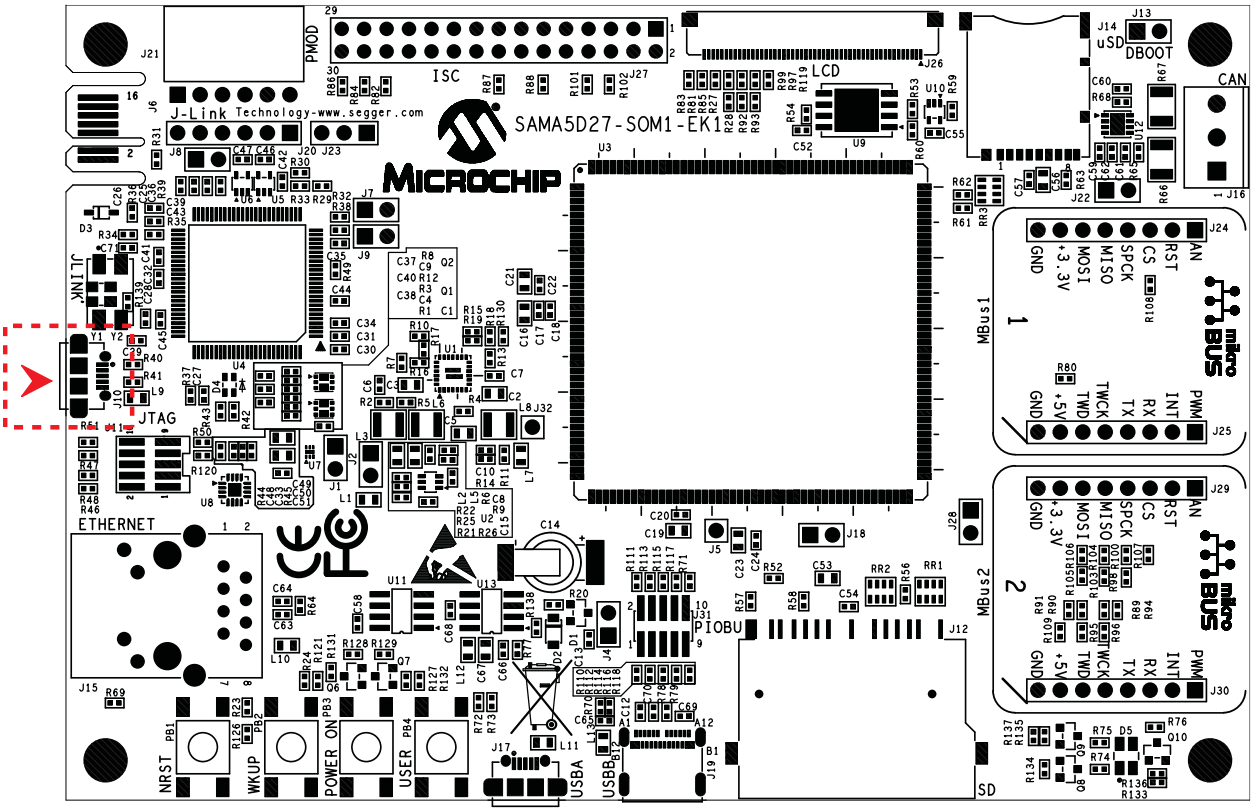


Table 3-21. Debug COM Port PIOs Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PD2	DBGU_RXD	-	Receive data
PD3	DBGU_TXD	-	Transmit data

Figure 3-40. J-Link-OB and CDC USB Connector J10 Location



The table below describes the pin assignment of USB connector J14.

Table 3-22. USB Connector J14 Pin Assignment

Pin No	Mnemonic	Signal Description
1	VBUS	5V power
2	DM	Data minus
3	DP	Data plus
4	ID	Not used
5	GND	Common ground

3.4.3.1 Baseboard Edge Connector

This connector (J6) is used to upgrade or download code to the ATSAM3U4C microcontroller JLINK-OB. The J-Link-OB software is factory-programmed.

3.5 PIO Usage on Expansion Connectors

This section describes the signals and connectors related to the PIO usage on expansion connectors.

The baseboard includes numerous peripherals. Many of these are connected to the GPIO block so that the I/O pins can be configured to carry out many alternative functions. This provides great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Note that most pins are configured as GPIO inputs, with a 100 Kohm pull-up resistor, after reset.

3.5.1 PIOBU Interface

The baseboard features eight tamper pins for static or dynamic intrusion detection, UART reception, and two analog pins for comparison.

For a description of intrusion detection, refer to the SAMA5D2 datasheet, chapter "Security Module (SECUMOD)".

Figure 3-41. PIOBU Connector

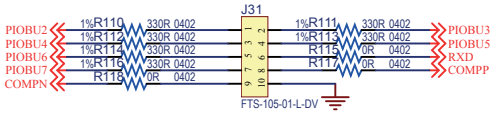
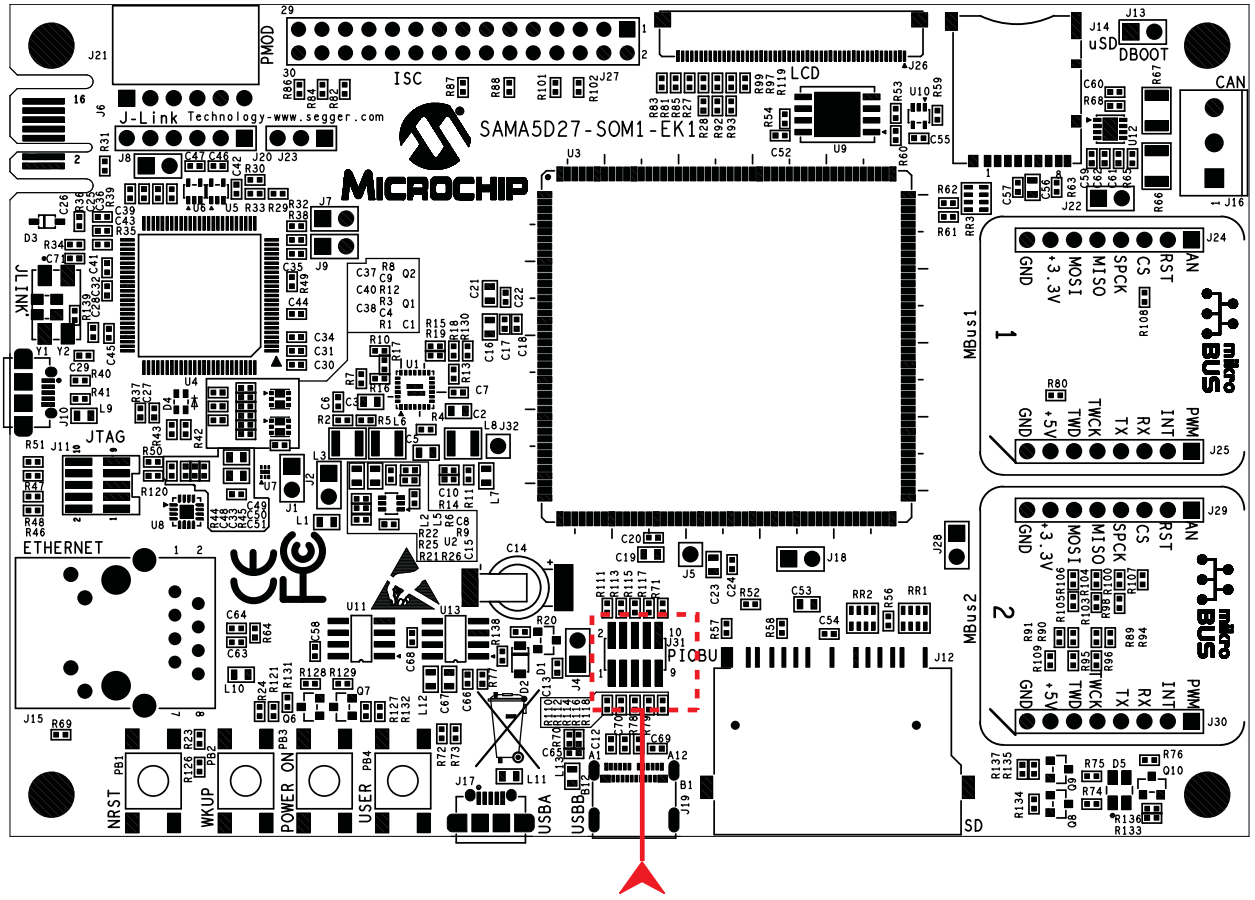


Figure 3-42. PIOBU Connector J31 Location



The table below describes the pin assignment of PIOBU connector J31.

Table 3-23. PIOBU Connector J31 Pin Assignment

Signal	Pin No.		Signal
PIOBU2	1	2	PIOBU3
PIOBU4	3	4	PIOBU5
PIOBU6	5	6	RXD
PIOBU7	7	8	COMPP
COMPN	9	10	GND

3.5.2 mikroBUS Interfaces

The SAMA5D27 SOM1 Kit1 hosts two pairs of 8-pin female headers acting as mikroBus interfaces. The mikroBUS standard defines the main board sockets and add-on boards (a.k.a. "click boards")

used for interfacing microprocessors with integrated modules with proprietary pin configuration and silkscreen markings. The pinout consists of three groups of communication pins (SPI, UART and TWI), four additional pins (PWM, interrupt, analog input and reset) and two power groups (+3.3V and GND on the left, and 5V and GND on the right 1x8 header).

Figure 3-43. mikroBUS1 Interface Connectors

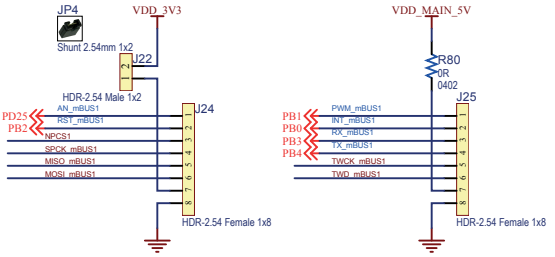
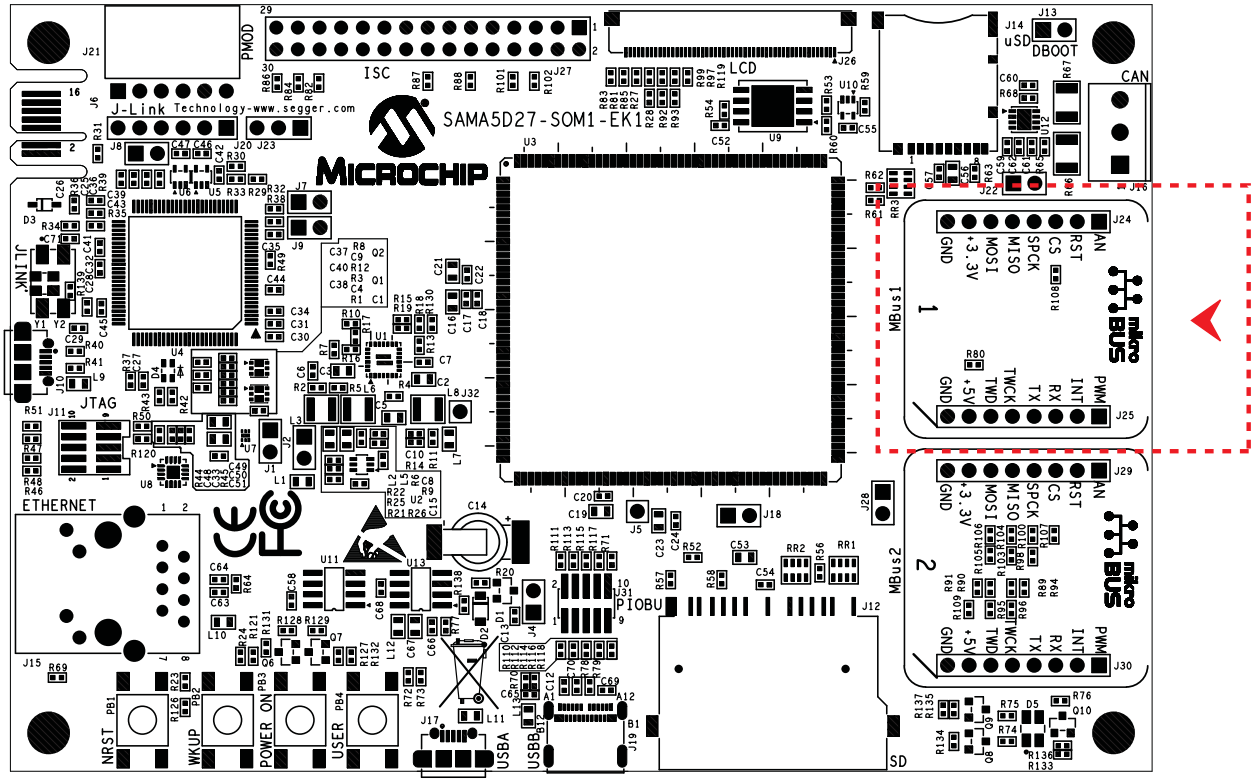


Figure 3-44. mikroBUS1 Connectors J24 and J25 Location



The table below describes the pin assignment of mikroBUS1 connectors J24 and J25.

Table 3-24. mikroBUS1 Connectors J24 and J25 Pin Assignment

SAMA5D27						SAMA5D27	
Function	PIO	J24 Signal	Pin No.		J25 Signal	PIO	Function
Analog input	PD25	AN	1	1	PWM	PB1	PWM
Reset	PB2	RST	2	2	RST	PB0	Interrupt
SPI chip select	PD0	NPCS	3	3	RX	PB3	UART receive
SPI clock	PC30	SPCK	4	4	TX	PB4	UART transmit
SPI MISO	PC29	MISO	5	5	TWCK	PA23	TWI clock

.....continued

SAMA5D27						SAMA5D27	
Function	PIO	J24 Signal	Pin No.		J25 Signal	PIO	Function
SPI MOSI	PC28	MOSI	6	6	TWD	PA24	TWI data
3.3VCC	–	3.3V	7	7	+5V	NC	5V supply
GROUND	–	GND	8	8	GND	_	GROUND

Figure 3-45. mikroBUS2 Interface Connectors

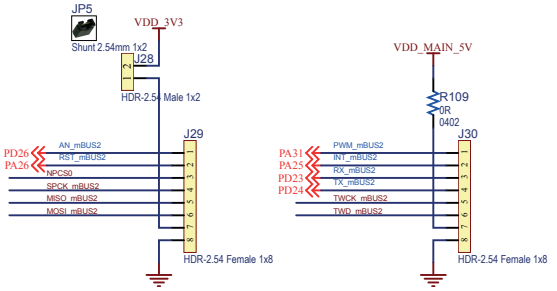
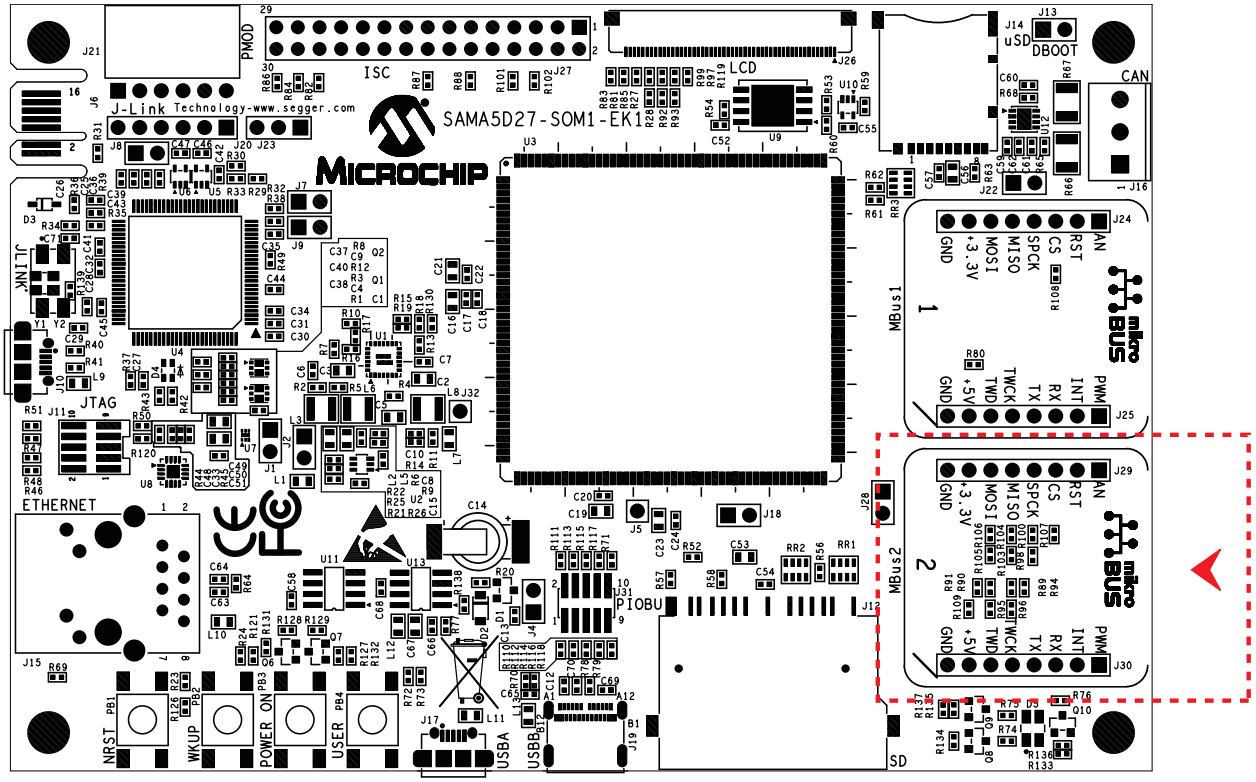


Figure 3-46. mikroBUS2 Interface Connectors J29 and J30 Location



The table below describes the pin assignment of mikroBUS2 connectors J29 and J30.

Table 3-25. mikroBUS2 Connectors J29 and J30 Pin Assignment

SAMA5D27						SAMA5D27	
Function	PIO	J29 Signal	Pin No.		J30 Signal	PIO	Function
Analog input	PD26	AN	1	1	PWM	PA31	PWM
Reset	PA26	RST	2	2	RST	PA25	Interrupt
SPI chip select	PC31	NPCS	3	3	RX	PD23	UART receive

.....continued

SAMA5D27						SAMA5D27	
Function	PIO	J29 Signal	Pin No.		J30 Signal	PIO	Function
SPI clock	PC30	SPCK	4	4	TX	PD24	UART transmit
SPI MISO	PC29	MISO	5	5	TWCK	PA23	TWI clock
SPI MOSI	PC28	MOSI	6	6	TWD	PA24	TWI data
3.3VCC	–	3.3V	7	7	+5V	NC	5V supply
GROUND	–	GND	8	8	GND	_	GROUND

3.5.3 Pmod Interface

Pmod devices are Digilent's line of small I/O interface boards that offer an ideal way to extend the capabilities of programmable logic and embedded control boards. They allow sensitive signal conditioning circuits and high-power drive circuits to be placed where they are most effective - near sensors and actuators.

The Pmod interface on the baseboard is a 6-pin connector. The 6-pin version provides four digital I/O signal pins, one power pin and one ground pin.

Note: The Pmod interface is shared with the ISC interface. Thus, the ISC and Pmod interfaces cannot be used at the same time.

Figure 3-47. Pmod Interface Connector

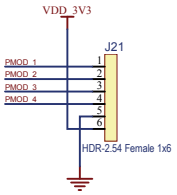
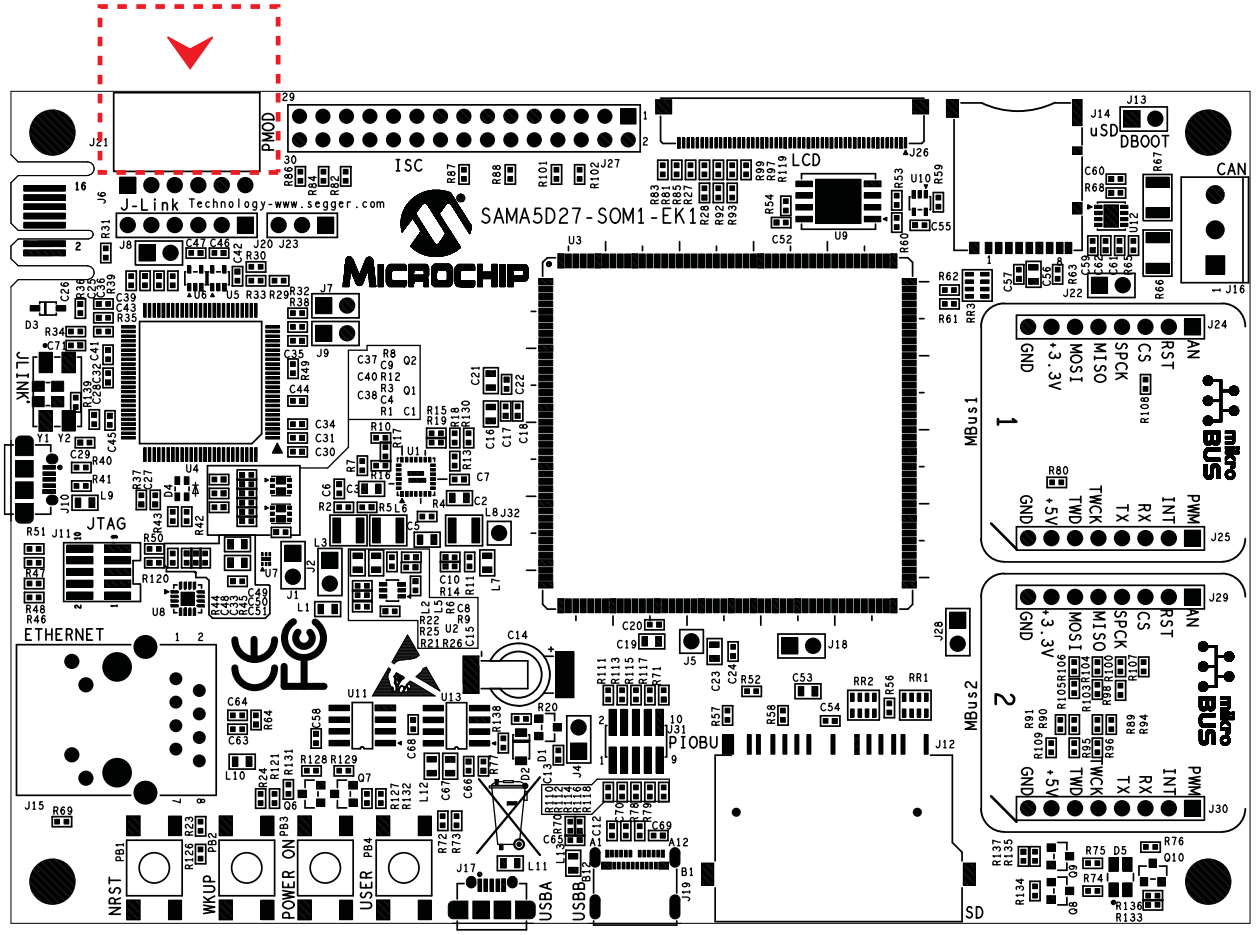


Figure 3-48. Pmod Connector J21 Location



3.5.3.1 Pmod Configuration

A set of jumpers, J20 and J23, is used to configure this type of interface. The table below describes the jumper configuration to select one of the Pmod functions (SPI, TWI or USART).

Figure 3-49. Pmod Jumper Configuration

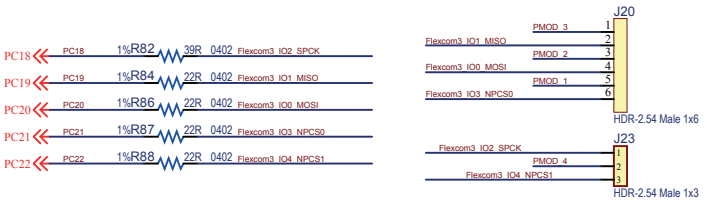


Figure 3-50. Pmod Jumpers J20 and J23 Location

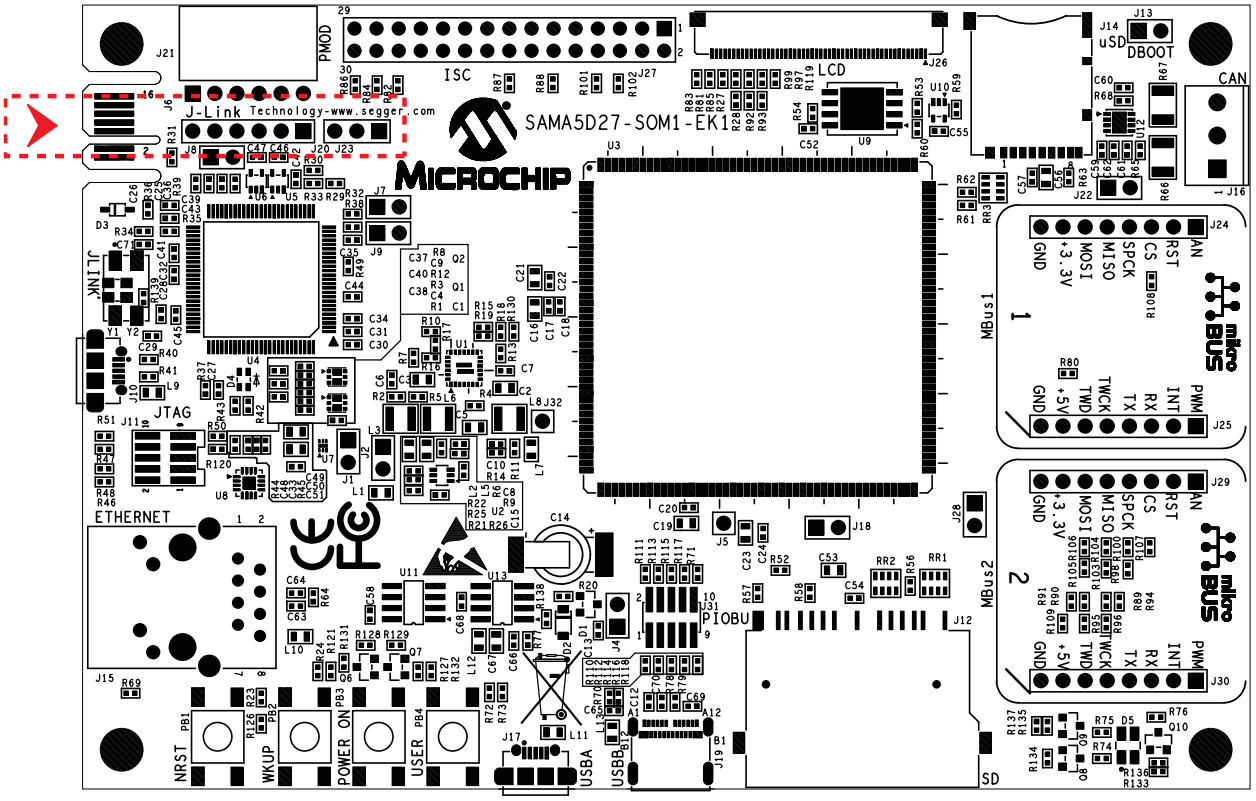


Table 3-26. Pmod Configuration Mode

Jumper J20	Jumper J23	Selected Function
1-2, 3-4, 5-6	1-2	SPI
2-3, 4-5	–	TWI
1-2, 3-4, 5-6	2-3	USART

4. Installation and Operation

4.1 System and Configuration Requirements

The SAMA5D27 SOM1 Kit1 requires the following:

- Personal Computer
- USB cable (included in the kit box)

4.2 Baseboard Setup

Follow these steps to verify proper operation of the kit:

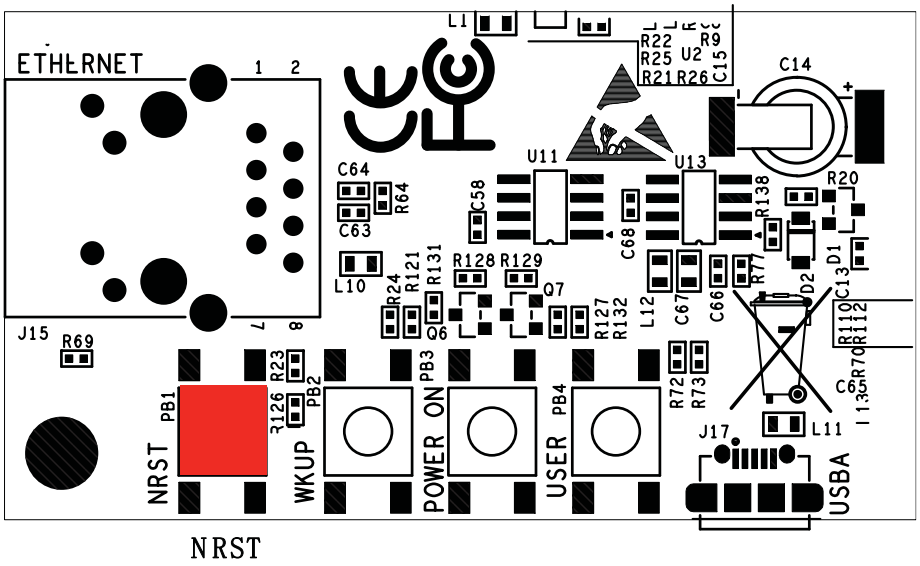
1. Unpack the baseboard, taking care to avoid electrostatic discharge.
2. Check the default jumper settings.
3. Connect the USB Micro-AB cable to connector J10 (JLINK-OB).
4. Connect the other end of the cable to a free port of your PC.
5. Open a terminal (console 115200, N, 8, 1) on your Personal Computer.
6. Reset the baseboard. A startup message appears on the console.

5. Errata

5.1 Incorrect NRST and WKUP Push Button Markings

The PCB silkscreen markings for push buttons PB1 (NRST) and PB2 (WKUP) were inverted. PB1/NRST is actually located to the left of PB2/WKUP, as shown in the figure below. However, the produced baseboards have been patched with stickers, which currently convey correct information to the user. This information is given in case the stickers get removed and/or to clarify the actual baseboards' appearance versus the design files printouts.

Figure 5-1. NRST Push Button Location

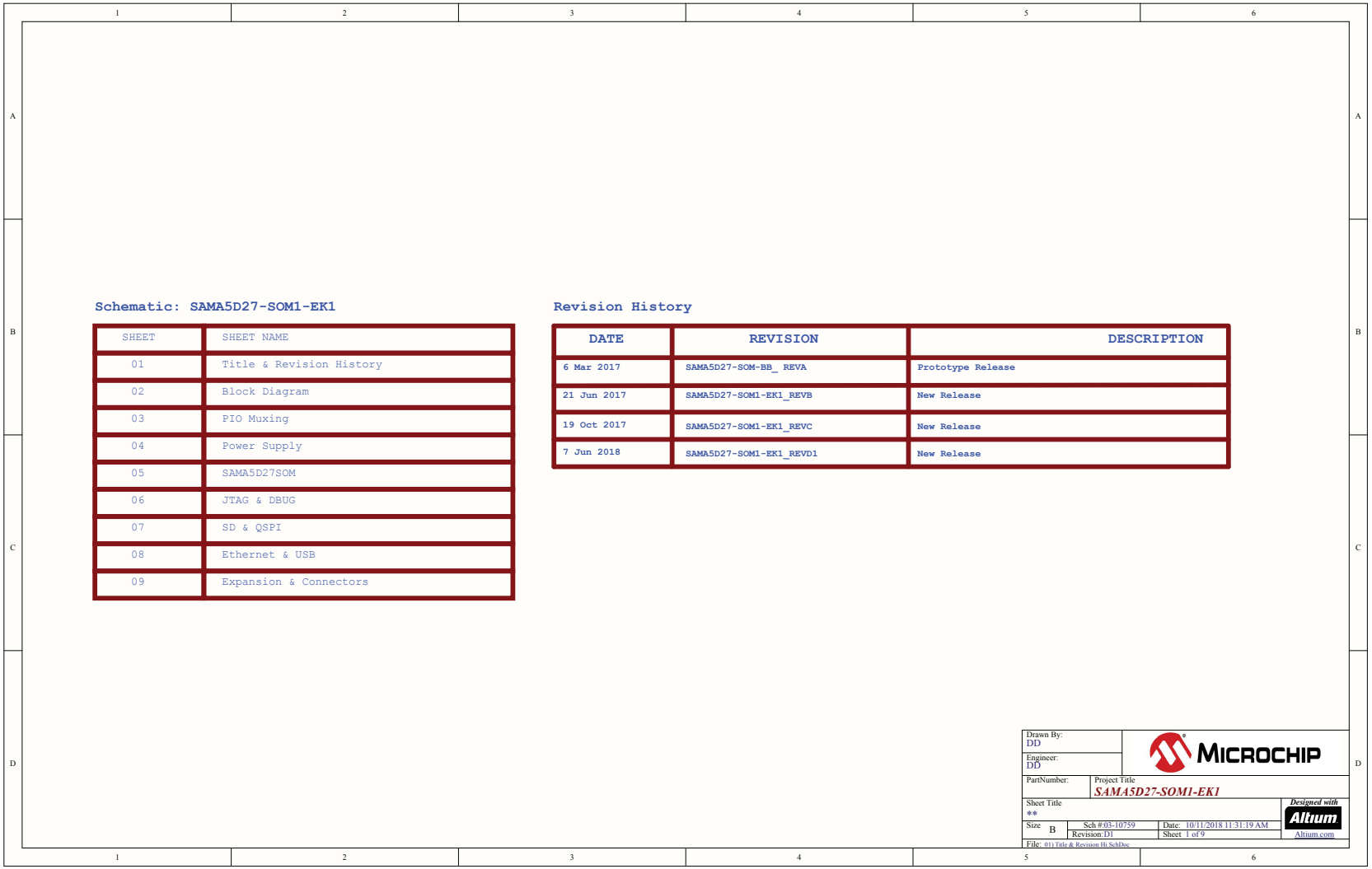


6. Appendix: Schematics and Layouts

This appendix contains the following schematics and layouts:

- Title and Revision History
- Block Diagram
- PIO Muxing Table
- Power Supply
- SAMA5D27 - SOM
- JTAG and DBGU
- SD and QSPI
- Ethernet and USB
- Expansion and Connectors

Figure 6-1. Title and Revision History



Schematic: SAMA5D27-SOM1-EK1

SHEET	SHEET NAME
01	Title & Revision History
02	Block Diagram
03	PIO Muxing
04	Power Supply
05	SAMA5D27SOM
06	JTAG & DBUG
07	SD & QSPI
08	Ethernet & USB
09	Expansion & Connectors

Revision History

DATE	REVISION	DESCRIPTION
6 Mar 2017	SAMA5D27-SOM-BB_ REVA	Prototype Release
21 Jun 2017	SAMA5D27-SOM1-EK1_REVB	New Release
19 Oct 2017	SAMA5D27-SOM1-EK1_REVC	New Release
7 Jun 2018	SAMA5D27-SOM1-EK1_REVD1	New Release

Drawn By: DD
Engineer: DD
PartNumber:
Project Title: SAMA5D27-SOM1-EK1
Sheet Title: **
Size: B | Sch #:03-10759 | Revision:D1 | Date: 10/11/2018 11:31:19 AM | Sheet 1 of 9
File: 01) Title & Revision Hi.SchDoc
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Figure 6-2. Block Diagram

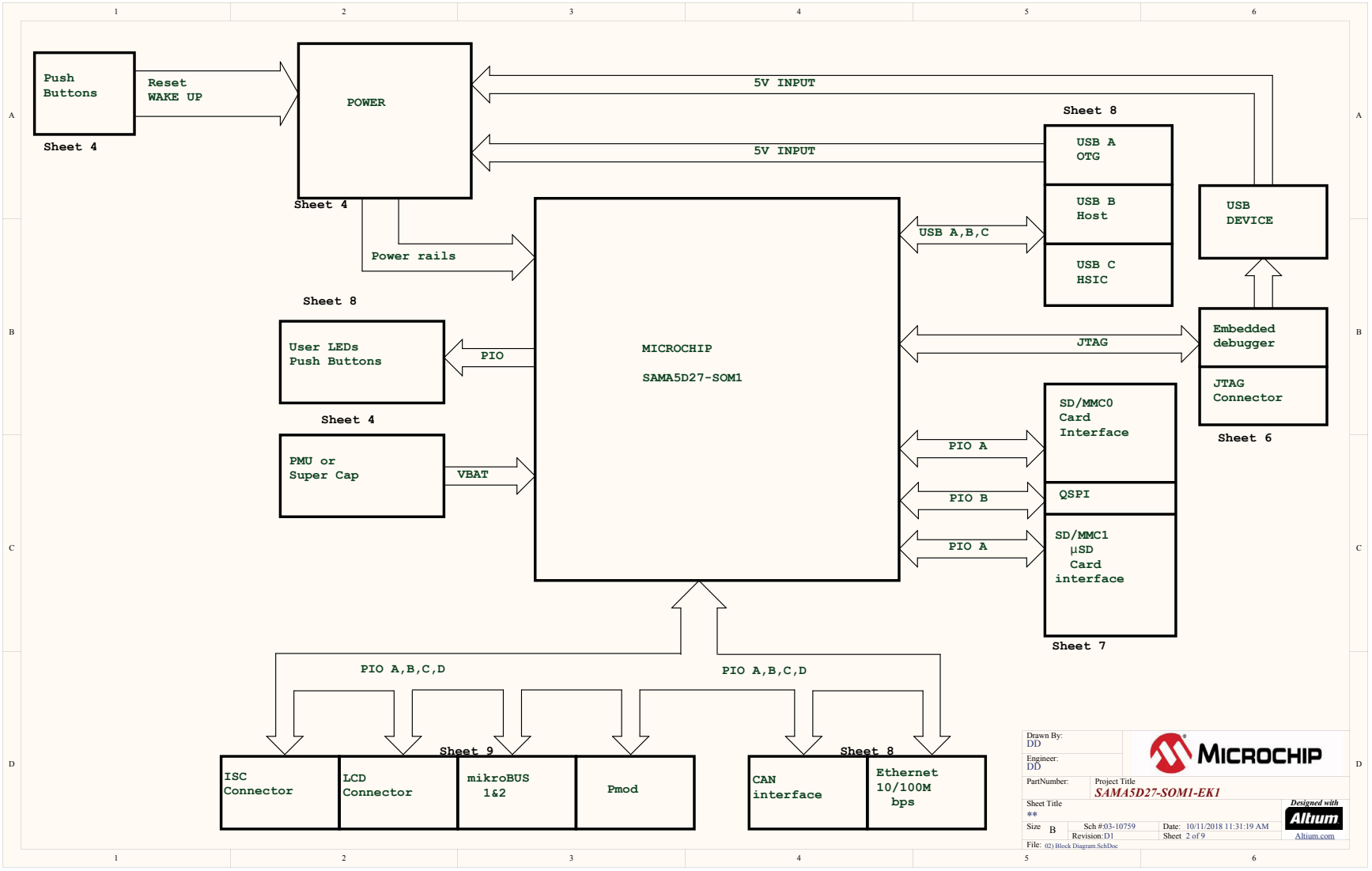

Figure 6-3. PIO Muxing Table

PIO Muxing & Jumper setting

LCD			
NC	1	LCDDAT19	26
GND	2	GND	27
LCDDAT0	3	LCDDAT20	28
LCDDAT1	4	LCDDAT21	29
LCDDAT2	5	LCDDAT22	30
LCDDAT3	6	LCDDAT23	31
GND	7	GND	32
LCDDAT4	8	LCDPCK	33
LCDDAT5	9	LCDVSYNC	34
LCDDAT6	10	LCDHSYNC	35
LCDDAT7	11	LCDDEN	36
GND	12	SPI0_ SPCK	37
LCDDAT8	13	SPI0_ MOSI	38
LCDDAT9	14	SPI0_ MISO	39
LCDDAT10	15	SPI0_NPCS0	40
LCDDAT11	16	LCDDISP	41
GND	17	TWD1	42
LCDDAT12	18	TWCK1	43
LCDDAT13	19	IRQ1	44
LCDDAT14	20	IRQ2	45
LCDDAT15	21	LCDPWM	46
GND	22	NRST	47
LCDDAT16	23	VCC	48
LCDDAT17	24	VCC	49
LCDDAT18	25	GND	50

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE
PA0	SDMMC0_CK	PA16	SPI0_ MISO	PB0	INT_mBUS1	PB16	LCDDAT5	PC0	LCDDAT21
PA1	SDMMC0_CDA	PA17	SPI0_NPCS0	PB1	LED_Green/PWM_mBUS1	PB17	LCDDAT6	PC1	LCDDAT22
PA2	SDMMC0_DA0	PA18	SDMMC1_DAT0	PB2	RST_mBUS1	PB18	LCDDAT7	PC2	LCDDAT23
PA3	SDMMC0_DA1	PA19	SDMMC1_DAT1	PB3	RX_mBUS1	PB19	LCDDAT8	PC3	LCDPWM
PA4	SDMMC0_DA2	PA20	SDMMC1_DAT2	PB4	TX_mBUS1	PB20	LCDDAT9	PC4	LCDDISP
PA5	SDMMC0_DA3	PA21	SDMMC1_DAT3	PB5	QSPI1_SCK	PB21	LCDDAT10	PC5	LCDVSYNC
PA6	SDMMC0_DA4	PA22	SDMMC1_CK	PB6	QSPI1_CS	PB22	LCDDAT11	PC6	LCDHSYNC
PA7	SDMMC0_DA5	PA23	TWCK_mBUS1&2	PB7	QSPI1_IO0	PB23	LCDDAT12	PC7	LCDPCK
PA8	SDMMC0_DA6	PA24	TWD_mBUS1&2	PB8	QSPI1_IO1	PB24	LCDDAT13	PC8	LCDDEN
PA9	SDMMC0_DA7	PA25	INT_mBUS2	PB9	QSPI1_IO2	PB25	LCDDAT14	PC9	ISC_D0
PA10	LED_Red	PA26	RST_mBUS2	PB10	QSPI1_IO3	PB26	LCDDAT15	PC10	ISC_D1
PA11	SDMMC0_VDDSEL	PA27	USBB_POWR_EN	PB11	LCDDAT0	PB27	LCDDAT16	PC11	ISC_D2
PA12	SDMMC0_WP	PA28	SDMMC1_CDA	PB12	LCDDAT1	PB28	LCDDAT17	PC12	ISC_D3
PA13	SDMMC0_CD	PA29	User Button	PB13	LCDDAT2	PB29	LCDDAT18	PC13	ISC_D4
PA14	SPI0_ SPCK	PA30	SDMMC1_CD	PB14	LCDDAT3	PB30	LCDDAT19	PC14	ISC_D5
PA15	SPI0_ MOSI	PA31	LED_blue/PWM_mBUS2	PB15	LCDDAT4	PB31	LCDDAT20	PC15	ISC_D6

PIOC	USAGE	PIOD	USAGE	PIOD	USAGE
PC16	ISC_D7	PD0	NPCS1_mBUS2	PD16	NA
PC17	ISC_D8	PD1	IRQ1	PD17	NA
PC18	ISC_D9	PD2	DBGU_RXD	PD18	NA
PC19	ISC_D10	PD3	DBGU_TXD	PD19	USBB_OVCUR
PC20	ISC_D11	PD4	TWD_LCD_ISC	PD20	USBA_VBUS_5V
PC21	ISC_PCK	PD5	TWCK_LCD_ISC	PD21	TWD0
PC22	ISC_VSYNC	PD6	ISC_RST	PD22	TWCK0
PC23	ISC_HSYNC	PD7	ISC_PWD	PD23	RX_mBUS2
PC24	ISC_MCK	PD8	BB_PWR_GOOD	PD24	TX_mBUS2
PC25	IRQ2	PD9	NA	PD25	AN_mBUS1
PC26	CANTX1	PD10	NA	PD26	AN_mBUS2
PC27	CANRX1	PD11	NA	PD27	SOM_TCK
PC28	MOSI_mBUS1&2	PD12	NA	PD28	SOM_TDI
PC29	MISO_mBUS1&2	PD13	NA	PD29	SOM_TD0
PC30	SPCK_mBUS1&2	PD14	NA	PD30	SOM_TMS
PC31	NPCS0_mBUS1	PD15	NA	PD31	NA

JUMPER DESCRIPTION		
PART	DEFAULT	FUNCTION
J1	CLOSE	I VDD_MAIN_5V Measurement
J2	CLOSE	I VDD_3V3 Measurement
J4	CLOSE	I VDDBU Measurement
J7	OPEN	Disable JLINK JTAG
J8	OPEN	ERASE SAM3U
J9	OPEN	Disable JLINK CDC
J13	OPEN	Disable boot
J22	CLOSE	POWER SELECT
J28	CLOSE	POWER SELECT

Drawn By: DD
Engineer: DD
PartNumber:
Project Title: *SAMA5D27-SOM1-EK1*
Sheet Title: **
Size: B | Sch #:03-10759 | Revision:D1 | Date: 10/11/2018 11:31:19 AM | Sheet 3 of 9
File: 03) PIO Muxing.SchDoc
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Figure 6-4. Power Supply

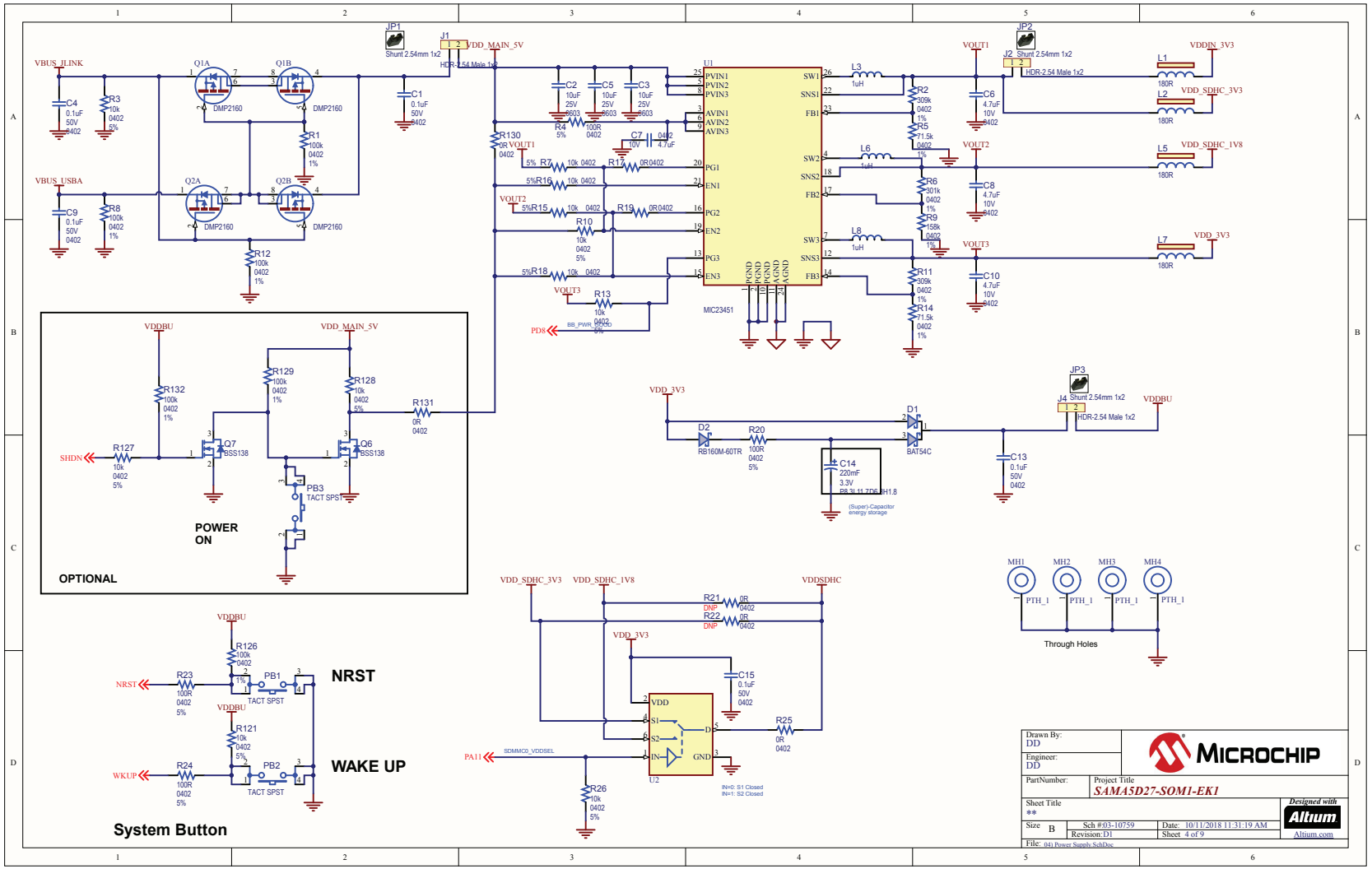


Figure 6-5. SAMA5D27 - SOM

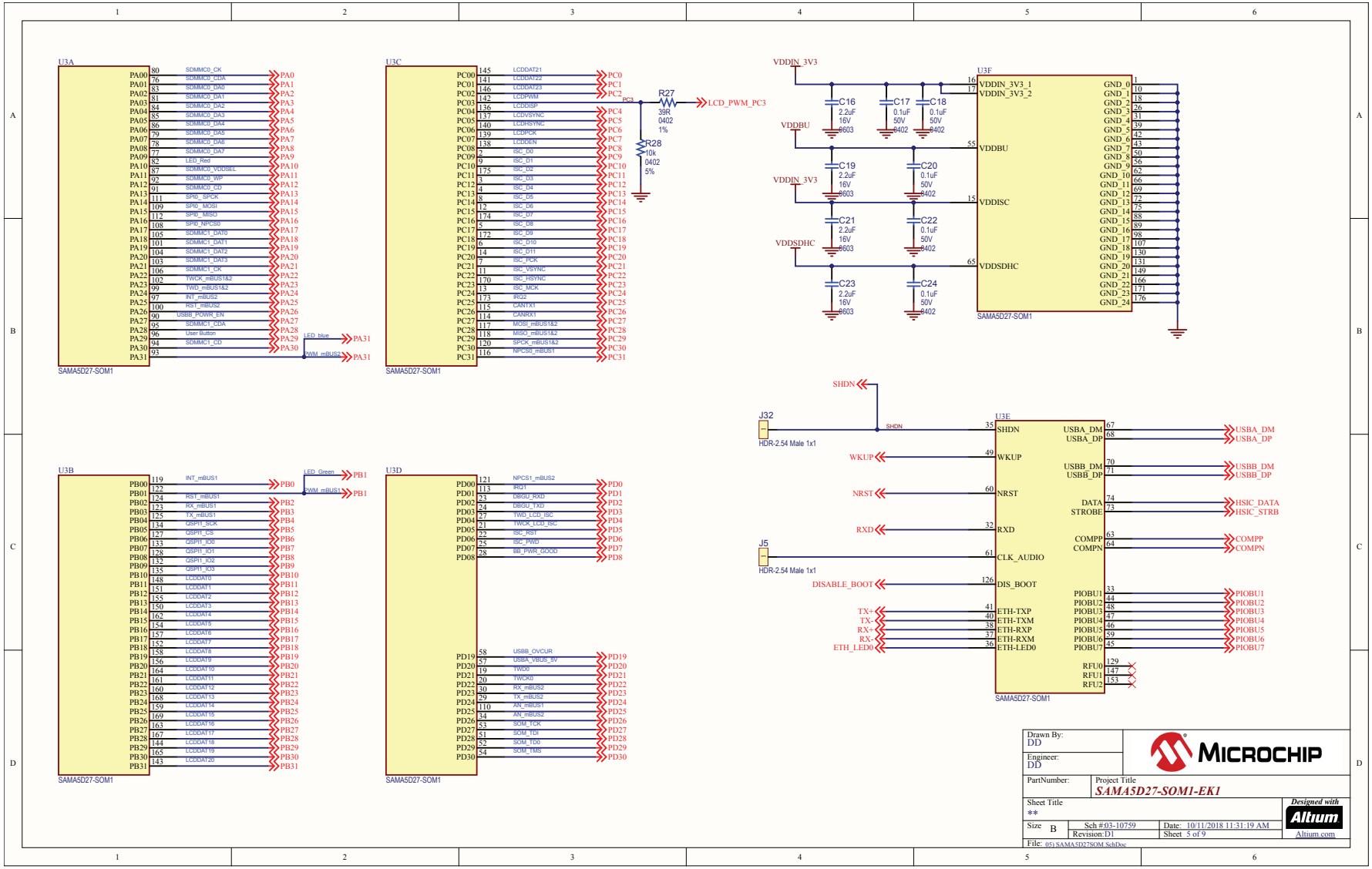


Figure 6-6. JTAG and DBGU

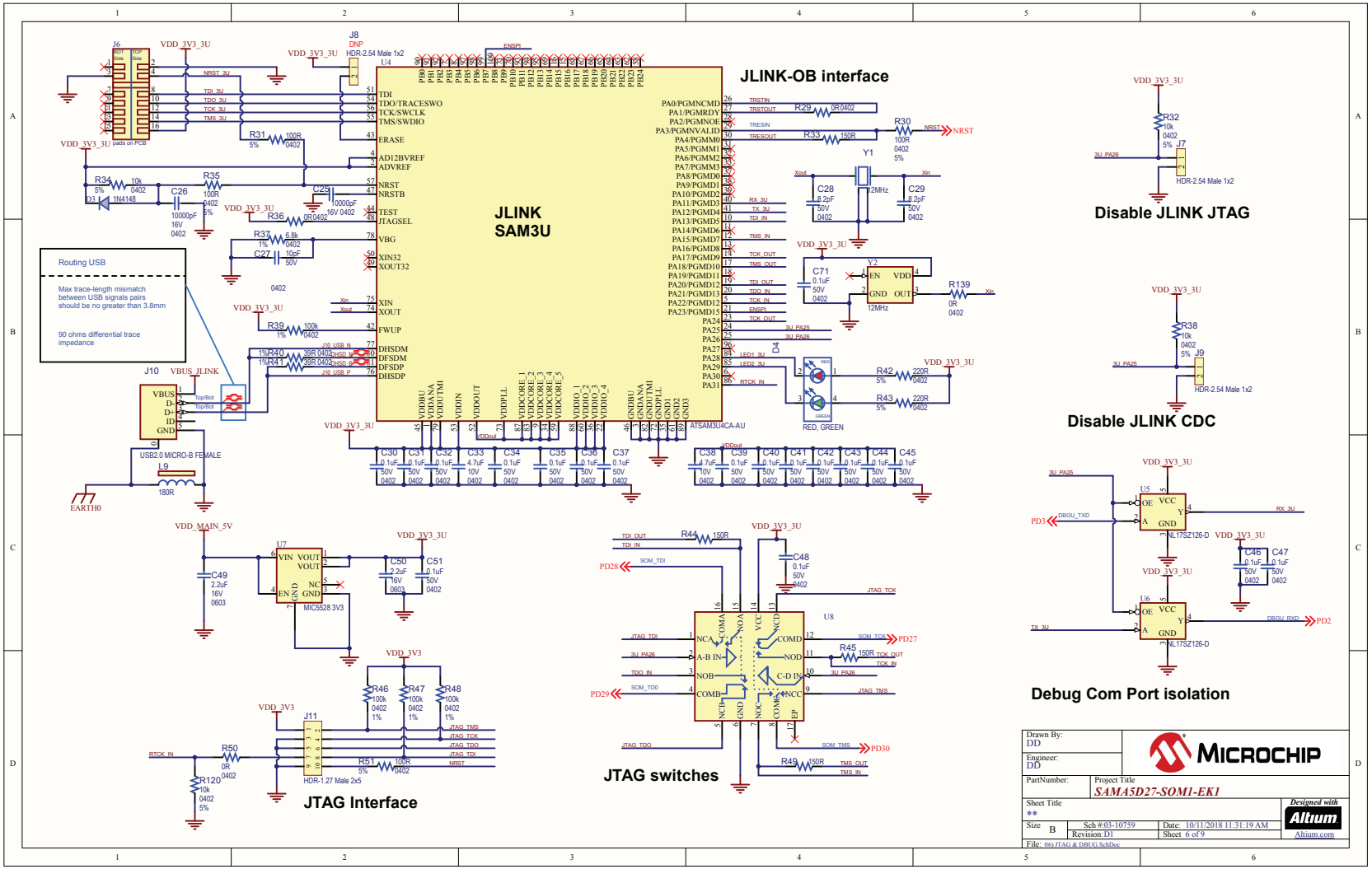


Figure 6-7. SD and QSPI

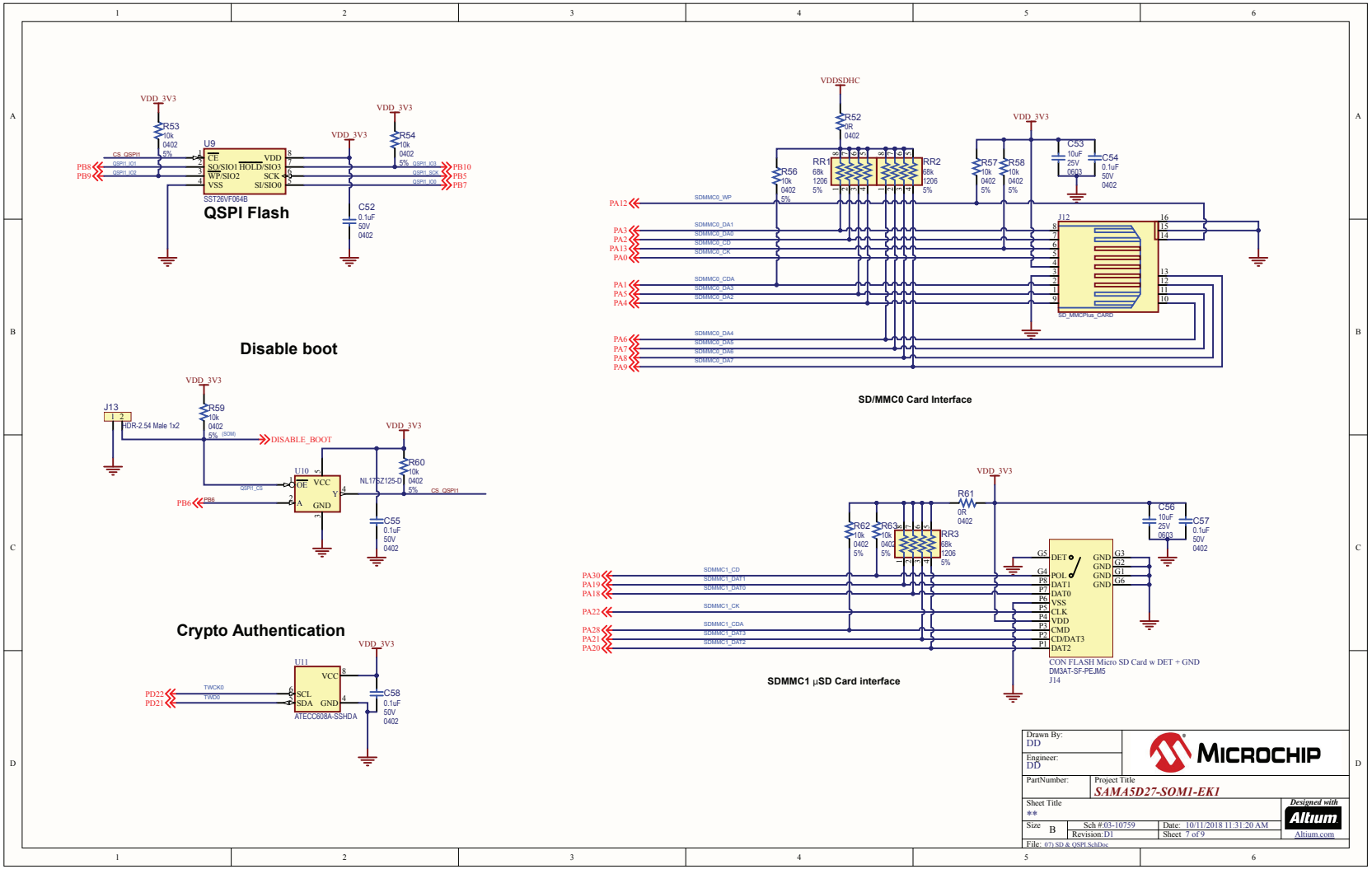


Figure 6-8. Ethernet and USB

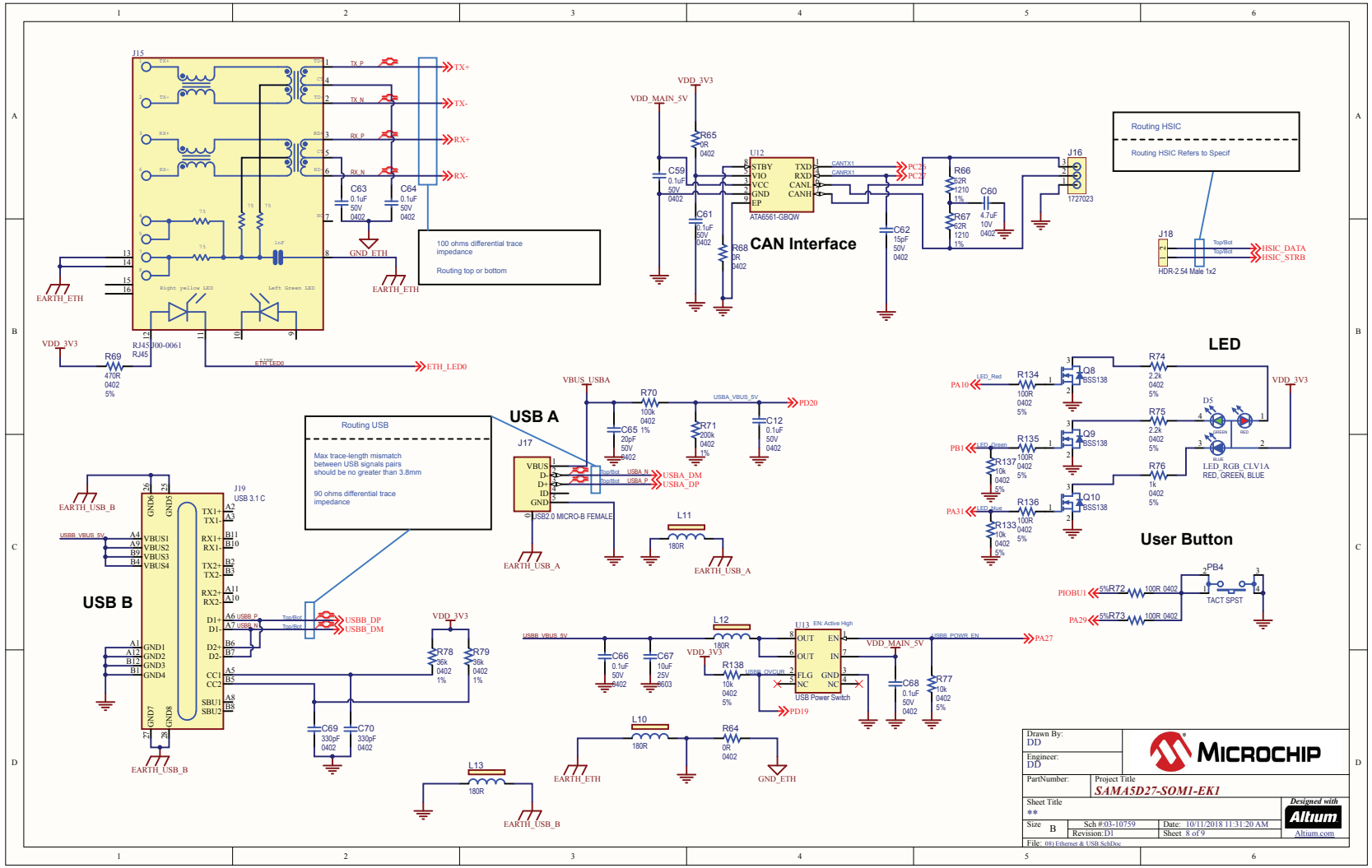
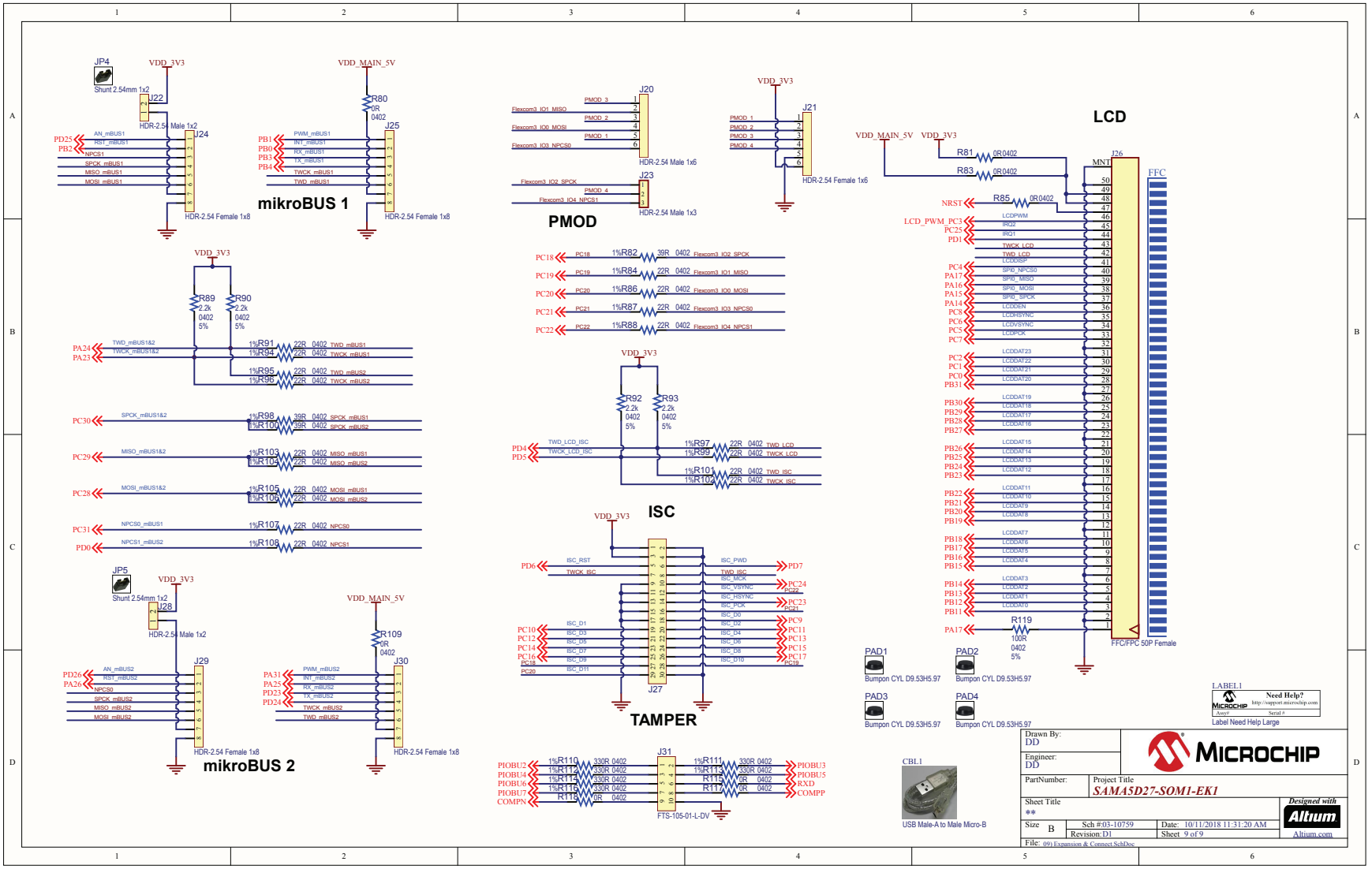


Figure 6-9. Expansion and Connectors



7. Revision History

Doc. Rev.	Changes
D – 09/2023	Updated CAN Interface.
C – 10/2018	Crypto memory U11 changed from ECC508 to ECC608. Schematics regenerated.
B – 06/2018	3.3.1. LCD TFT Interface: added TM5000 series to list of supported LCD display types. 3.5.2. mikroBUS Interfaces: updated J24 and J29 signal assignments.
A – 10/2017	First release

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