SAMA7G54-EK User's Guide

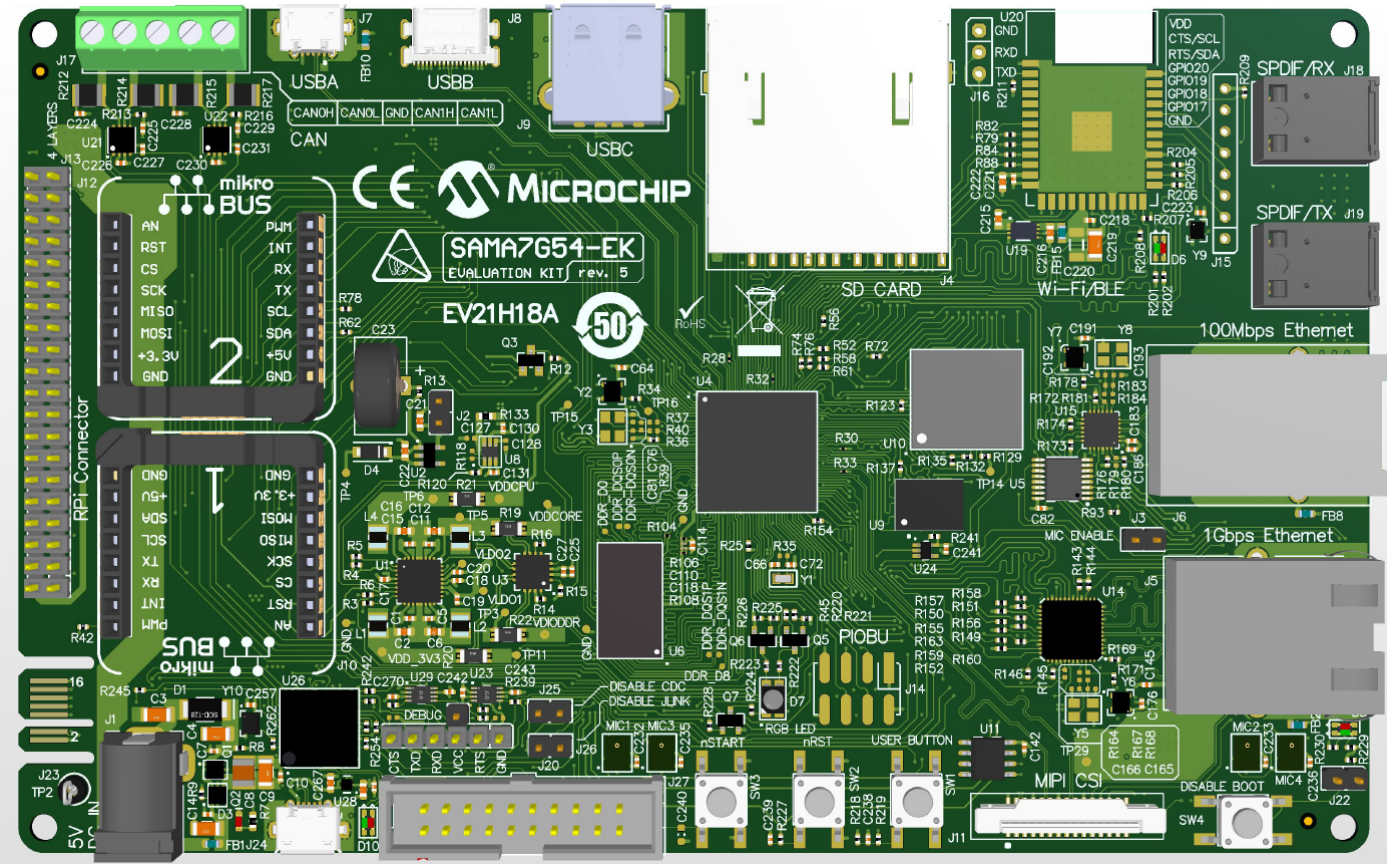
EV21H18A

Scope

This user's guide provides detailed information on the overall design of the SAMA7G54 Evaluation Kit (EV21H18A) and describes how to use the kit.

The kit is the evaluation platform for the SAMA7G5 Series devices.

Figure 1. SAMA7G54-EK Overview



1. Introduction

1.1 Document Layout

The document is organized as follows:

- Introduction
- Product Overview—Important information about the evaluation kit
- Function Blocks—Evaluation kit specification and high-level description of the major components and interfaces
- Installation and Operation—How to get started with the evaluation kit
- Appendix A: Schematics and Layout—Evaluation kit schematics and layout diagrams
- Appendix B: Unmounted Elements—List of unmounted components, description of their use in the system and guidance for manually assembling the Wi-Fi®/Bluetooth® module

1.2 Reference Documents

The following Microchip document are available and recommended as supplemental reference resources.

Table 1-1. Reference Documents

Document Title	Document Type	Literature No.
SAMA7G5 Series	Data sheet	DS60001765
MCP16502	Data sheet	DS20006275
24AA025E48	Data sheet	DS20002124
KSZ8081RNA/RND	Data sheet	DS00002199
KSZ9131RNX	Data sheet	DS00002841
MCP2542FD	Data sheet	DS20005514
ATWILC3000-MR110xA	Data sheet	DS70005327
ATECC608B	Data sheet	DS40002239
PAC1934	Data sheet	DS20005850
How to Manually Solder the ATWILC3000 Module on an MPU Board	Application note	AN3227

2. Product Overview

The SAMA7G54 Evaluation Kit (EV21H18A) provides a versatile Total System Solution platform that highlights Microchip MPU and connectivity ICs.

The board features on-board memories, two Ethernet interfaces, three USB ports, two CAN interfaces, one SD card connector, two mikroBUS™ click interface headers to support over 450 MikroElektronika Click boards™, an RPi CSI camera to support a camera module, an RPi extension connector to support several extension boards, and provision to solder a Microchip ATWILC3000-MR110xA Wi-Fi/Bluetooth module.

Note: RPi stands for “Raspberry Pi”. Raspberry Pi is a trademark of Raspberry Pi Trading.

2.1 SAMA7G54-EK Features

Table 2-1. SAMA7G54-EK Features

Characteristic	Specifications	Components
Processor	14x14 mm, 0.65 mm pitch, 343-ball TFBGA	Microchip SAMA7G54-V/4HB
External clock	MPU: 24 MHz MPU: 32.768 kHz Crystal Ethernet: 25 MHz	Microchip DSC1001DI5-024.0000 NDK NX2012SA-32.768-STD-MUB-1 2 * Microchip DSC1001DI5-025.0000
Memory	One 16-bit, 4-Gbit DDR3L One 32-Gbit e.MMC One 1-Gbit Octal SPI Flash Two EEPROMs with EUI-48™ MAC ID	Alliance Memory AS4C256M16D3LC-12BCNTR SkyHigh Memory S40FC004C1B1C00000 Micron MX66LM1G45GXDI00 2 * Microchip 24AA02E48
SD/MMC	One standard 4-bit SD Card interface with power control	Microchip MIC9085
USB	One Micro-AB host/device with power switch One Type-A host with power switch One Type-C™ host with power switch	3 * Microchip MIC2025
CAN	Two CAN interfaces	Microchip MCP2542FD
Ethernet	One Ethernet 10/100 port One Gigabit Ethernet port	Microchip KSZ8081 Microchip KSZ9131
Wi-Fi/BT	One optional Wi-Fi/BT interface	Slot for Microchip ATWILC3000
Audio	One SPDIF RX port One SPDIF TX port Four digital microphones	– – SPK0641HT4H-1
Camera	One RPi CSI camera interface	–
Debug port	One J-Link-OB + CDC One JTAG interface	Embedded J-Link-OB through the CDC (Communication Device Class) interface (ATSAM3U4C TFBGA100)
Board monitor	One RGB (red, green, blue) LED Four push button switches	– –
Expansion	One RPi Expansion connector Two mikroBUS connectors	– Hundreds of possible click extensions featuring Microchip functions
Power management	One power management IC One power consumption measurement device	Microchip MCP16502 Microchip PAC1934
Board supply	From USBA or from wall adapter	–

.....continued		
Characteristic	Specifications	Components
Backup battery	SuperCap	–

2.2 SAMA7G54-EK Content

The SAMA7G54 evaluation kit includes the following:

- The SAMA7G54-EK board
- Two USB-A to USB Micro-AB cables

2.3 Evaluation Kit Specifications

Table 2-2. Evaluation Kit Specifications

Characteristic	Specifications
Board	SAMA7G54-EK
Board supply voltage	External or USB-powered
Temperature	Operating: 0°C to +70°C Storage: -20°C to +70°C
Relative humidity	0 to 85% (non-condensing)
Board dimensions	160 x 100 mm
RoHS status	Compliant

2.4 Power Sources

Two options are available to power up the SAMA7G54-EK board:

- Through an external AC to DC +5V wall adapter connector (J1)
- Through the USB Micro-AB connector on the USBA port (J7)

Table 2-3. Electrical Characteristics

Electrical Parameter	Value
Input voltage	5 VDC
Maximum input voltage	6 VDC
Maximum 3.3 VDC current	300 mA

⚠ CAUTION The SAMA7G54-EK board runs at a 3.3V voltage level logic. The maximum voltage that the I/O pins can tolerate is 3.3V. Providing higher voltages (e.g. 5V) to an I/O pin could damage the board.

2.5 On-Board Connectors

The fully-featured SAMA7G54 Evaluation Kit integrates multiple peripherals and interface connectors, as shown in the following figure.

Figure 2-1. SAMA7G54-EK Connectors

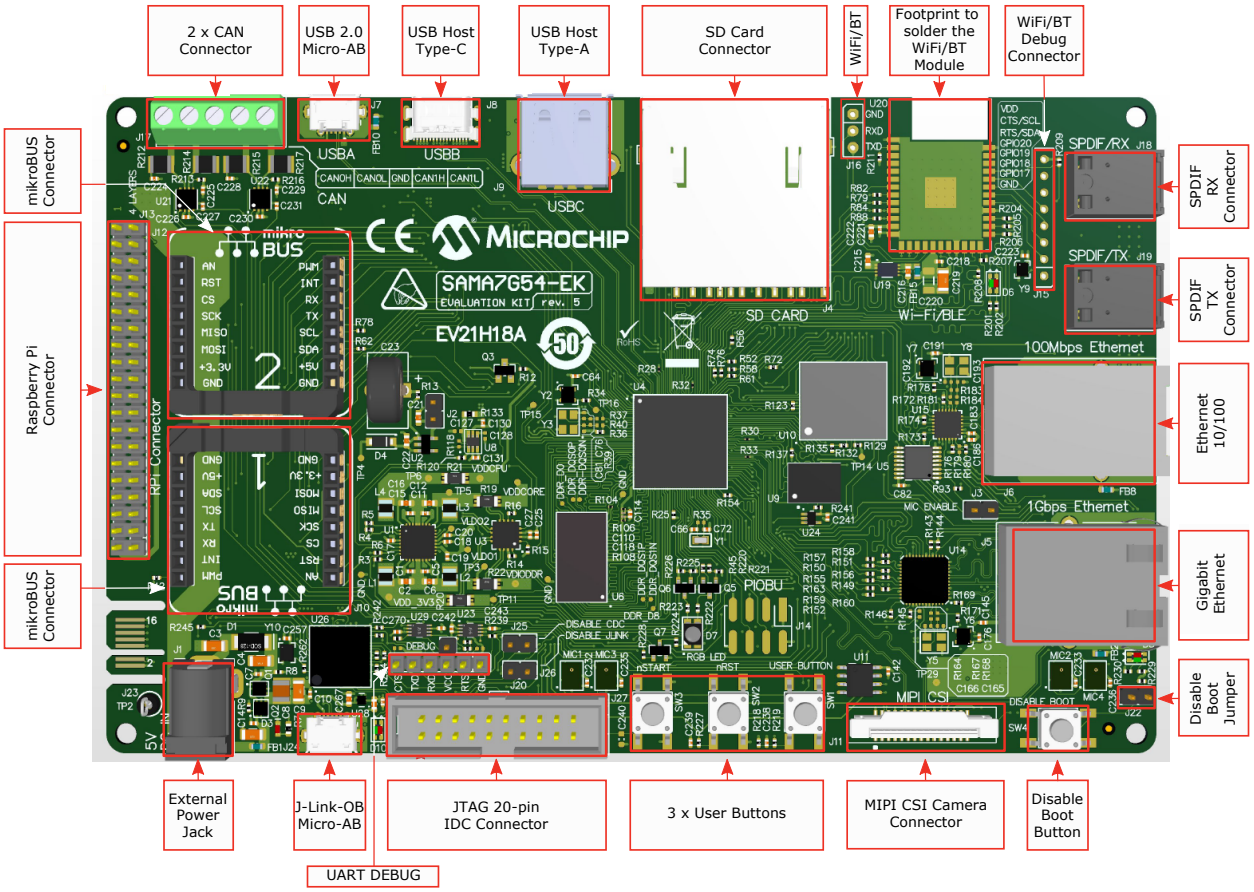


Table 2-4. SAMA7G54-EK Board Interface Connectors

Connector	Interfaces To
J1	External power jack
J4	Standard SDMMC connector
J5	Gigabit Ethernet RJ45
J6	Ethernet 10/100 RJ45
J7	USB 2.0 Micro-AB (USB-A)
J8	USB 2.0 Type-C (USB-B)
J9	USB 2.0 Type-A (USB-C)
J10	mikroBUS socket (mBUS1)
J11	MIPI CSI camera connector
J12	mikroBUS socket (mBUS2)
J13	40-pin Raspberry Pi connector
J14	Tamper pins connector
J15	ATWILC3000 debug connector
J16	ATWILC3000 UART debug connector
J17	Dual CAN connector
J18	SPDIF RX connector
J19	SPDIF TX connector
J20	UART debug connector (FTDI connector)
J22	Disable boot jumper

.....continued	
Connector	**Interfaces To**
J23	PCB connector for factory-programming the SAM3U/J-Link-OB (not to be used by end user)
J24	J-Link-OB USB connection
J27	JTAG, 20-pin IDC

2.6 Default Jumper Settings

The following picture shows the default jumper settings. Jumpers in blue are in open position, jumpers in red are in closed position.

Boards are delivered in a factory configuration that may not correspond to a customer-specific use case. Before using the board, double check the jumpers settings against the view and table given below.

Figure 2-2. SAMA7G54-EK Default Jumper Settings

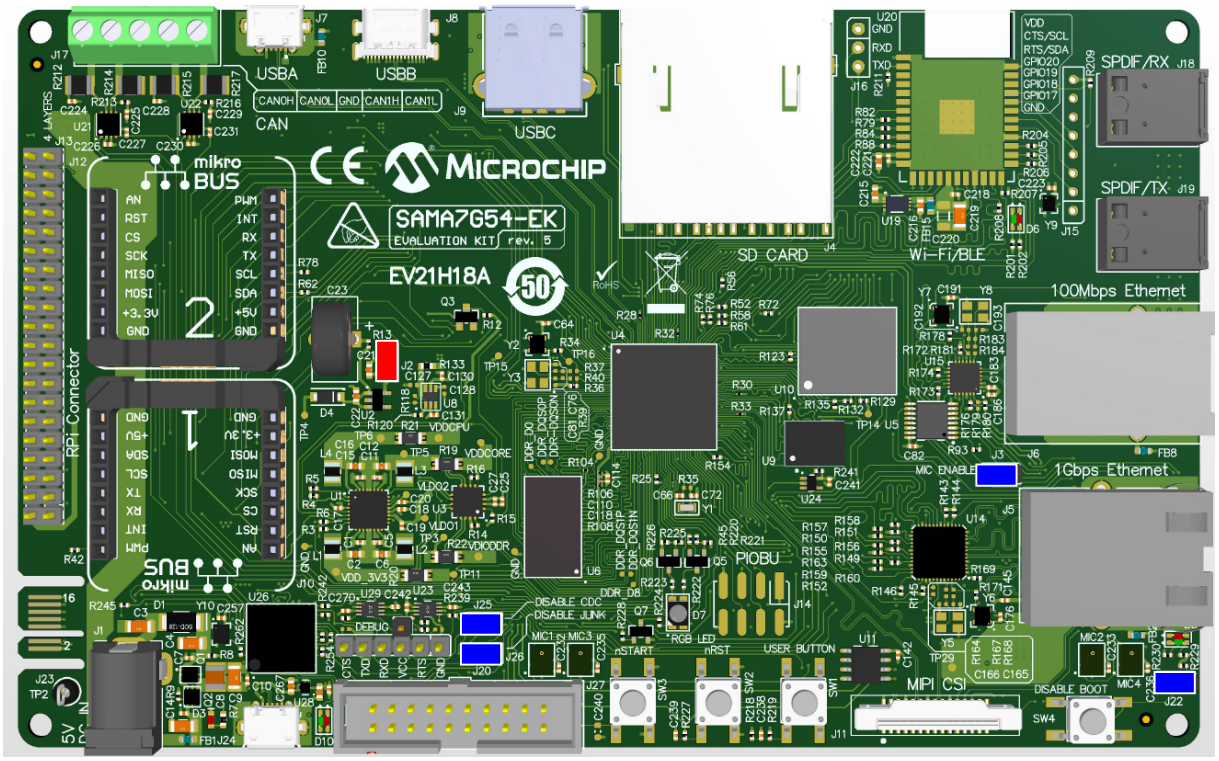


Table 2-5. SAMA7G54-EK Jumper Settings

Jumper	State	Function
J2	Closed	VDDBU current measurement
J3	Open (default)	RMII Ethernet interface is selected.
	Closed	The 4-microphone PDMIC interface is selected.
J22	Open (default)	Booting from on-board memory is permanently allowed and only disabled during SW4 pressure.
	Closed	Booting from on-board memory is permanently disabled.
J25	Open (default)	Enables UART communication (CDC) between MPU and SAM3U.
	Closed	Disables UART communication (CDC) between MPU and SAM3U.

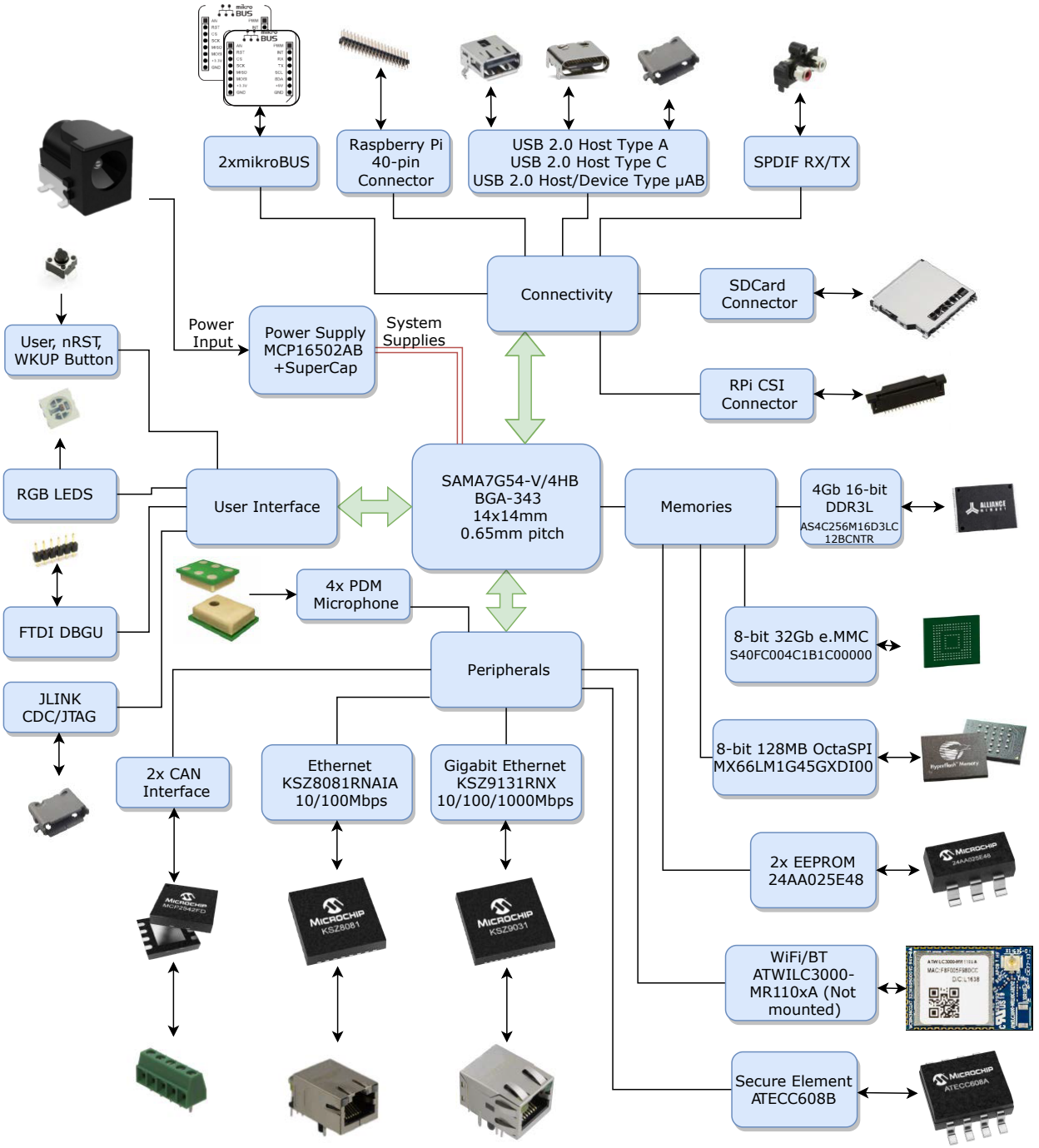
.....continued		
Jumper	**State**	**Function**
J26	Open (default)	The on-board J-Link interface is enabled and used for MPU debugging.
	Closed	The on-board J-Link interface is disabled. MPU debugging is done through the JTAG connector (J27).

3. Function Blocks

This section covers the SAMA7G45-EK specifications and provides a high-level description of the board's major components and interfaces.

This document is not intended to provide detailed information about the processor or about any other components used on the board. Refer to the components documentation for further details.

Figure 3-1. SAMA7G54-EK Block Diagram



3.1 Power Supply Topology and Power Distribution

This section describes the implementation and circuitry that ensure adequate voltage stability for all the devices on the board and a correct power-up sequence for the MPU. The power-up and power-down sequences indicated in the SAMA7G5 Series data sheet must be respected for a reliable operation of the device.

3.1.1 Input Power Options

The SAMA7G54-EK board can be powered through:

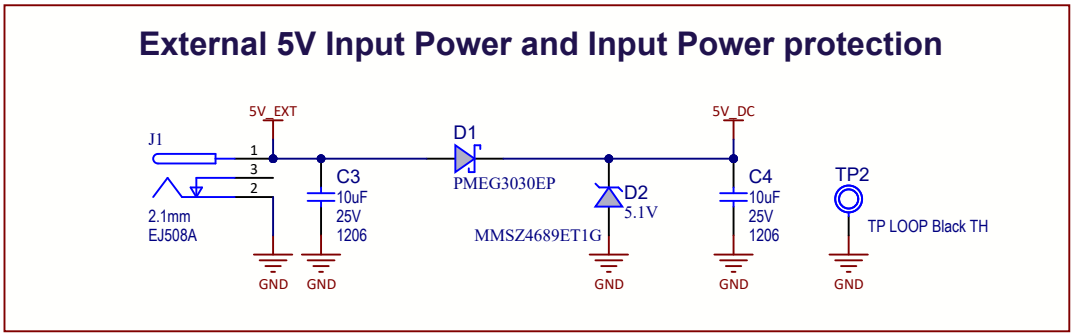
- An external AC to DC +5V wall adapter connected via a 2.1 mm center-positive plug into the power jack of the board (J1); the recommended output capacity of the power adapter is 2A
- USB port A (J7)

3.1.1.1 Wall Adapter Input

The 5V_EXT from the wall adapter is protected through a pair of Schottky/Zener diodes (D1 and D2) that limit the input voltage to 5.1V.

The following figure shows the wall adapter input power supply topology.

Figure 3-2. Wall Adapter Input Power Schematic

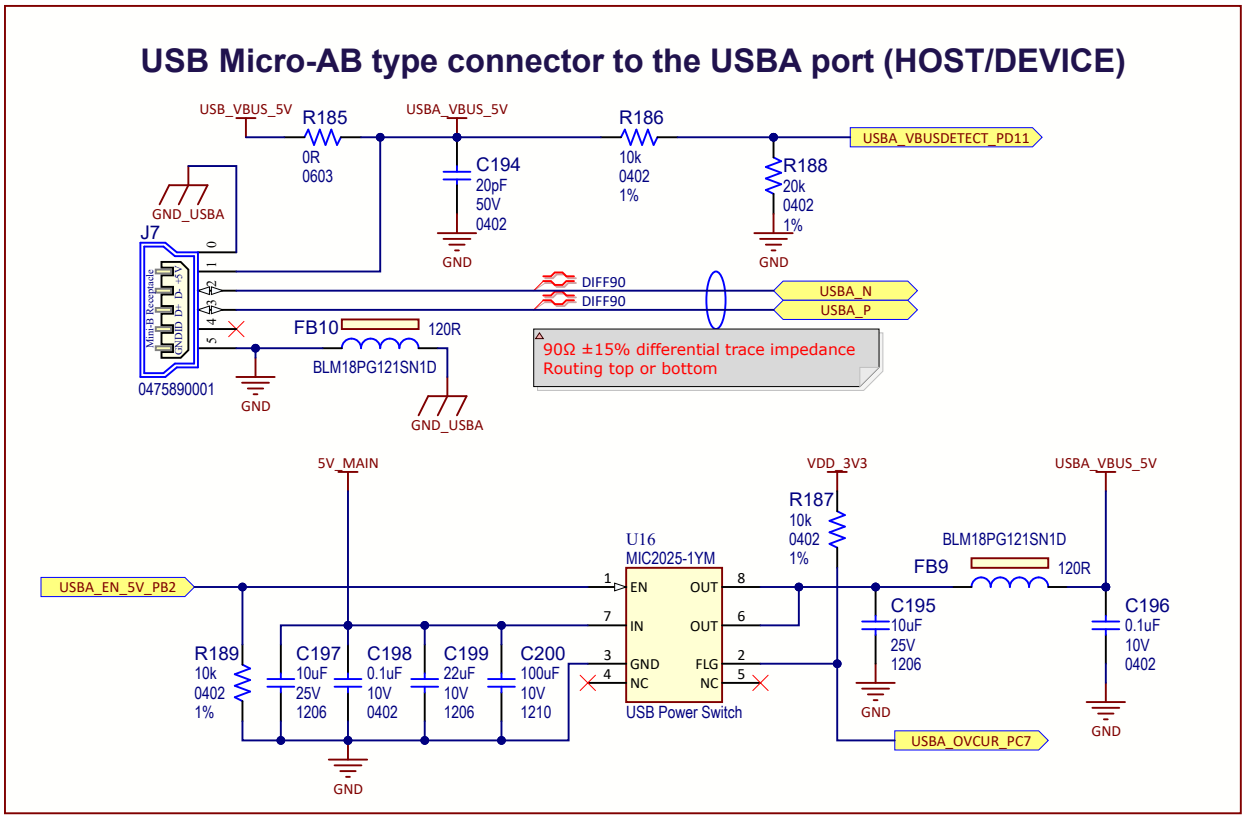


3.1.1.2 USB Supply Input

The USB-powered operation comes from the USB device port connected to a PC or a 5 VDC supply. The USB supply is enough to power the board in most applications. It is important to note that when the USB supply is used, the USB port has limited power. If a USB host port is required for the application, it is recommended to use the external DC supply or a more capable micro USB external power supply.

The following figure shows the USB input power supply topology.

Figure 3-3. USB Input Power Schematic



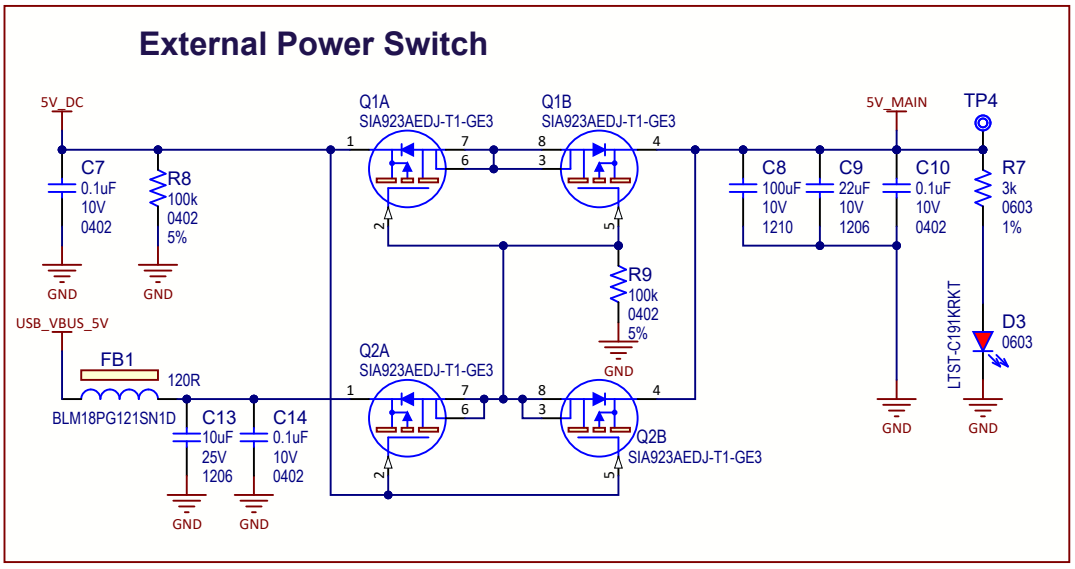
Note: USB-powered operation eliminates the need for additional wires and batteries. It is the preferred mode of operation for any project that requires only a 5V source at up to 500 mA.

3.1.1.3 Automatic Power Switch

The switch between the two powering options is made by four transistors that ensure the separation between the two when both are plugged. The switch prioritizes powering from the wall adapter to maximize power transfer.

The following figure shows the automatic power switch topology.

Figure 3-4. Automatic Power Switch Schematic



3.1.2 Power Management Integrated Circuit

The MCP16502 is a fully-featured PMIC optimized for Microchip MPU devices.

The MCP16502 integrates four DC-DC buck regulators and two auxiliary LDOs, and provides a comprehensive interface to the MPU, which includes an interrupt flag and an I^2C interface.

All buck channels can support loads up to 1A. All bucks are 100% duty cycle capable.

Two 300 mA LDOs are provided so that sensitive analog loads can be supported.

The default power channel sequencing is built-in, according to the requirements of the Microchip MPU device.

The MCP16502 features a low no-load operational quiescent current, and draws less than 10 µA in full shutdown.

Active discharge resistors are provided on each output. All buck channels support safe start-up into pre-biased outputs.

The MCP16502 is available in a 32-pin 5 mm x 5 mm VQFN package with an operating junction temperature range from –40°C to +125°C. It is AEC-Q100 Grade 2 (T_{AMB}=105°C) qualified. For more information on the MCP16502, refer to the product web page.

The MCP16502AB comes preset to supply all the voltage rails required by the system:

- 3.3V DC/DC supplies SAMA7G5 I/O pads and devices.
- 1.35V DC/DC supplies SAMA7G5 DDR3 pads (VDDIODDR) and devices.
- 1.1V DC/DC supplies SAMA7G5 core (VDDCORE).
- 1.275V DC/DC supplies SAMA7G5 CPU (VDDCPU).
- 1.8V LDO supplies the SD Card interface and the e.MMC.

The figure below shows the power management scheme.

Figure 3-5. Power Management Unit Schematic

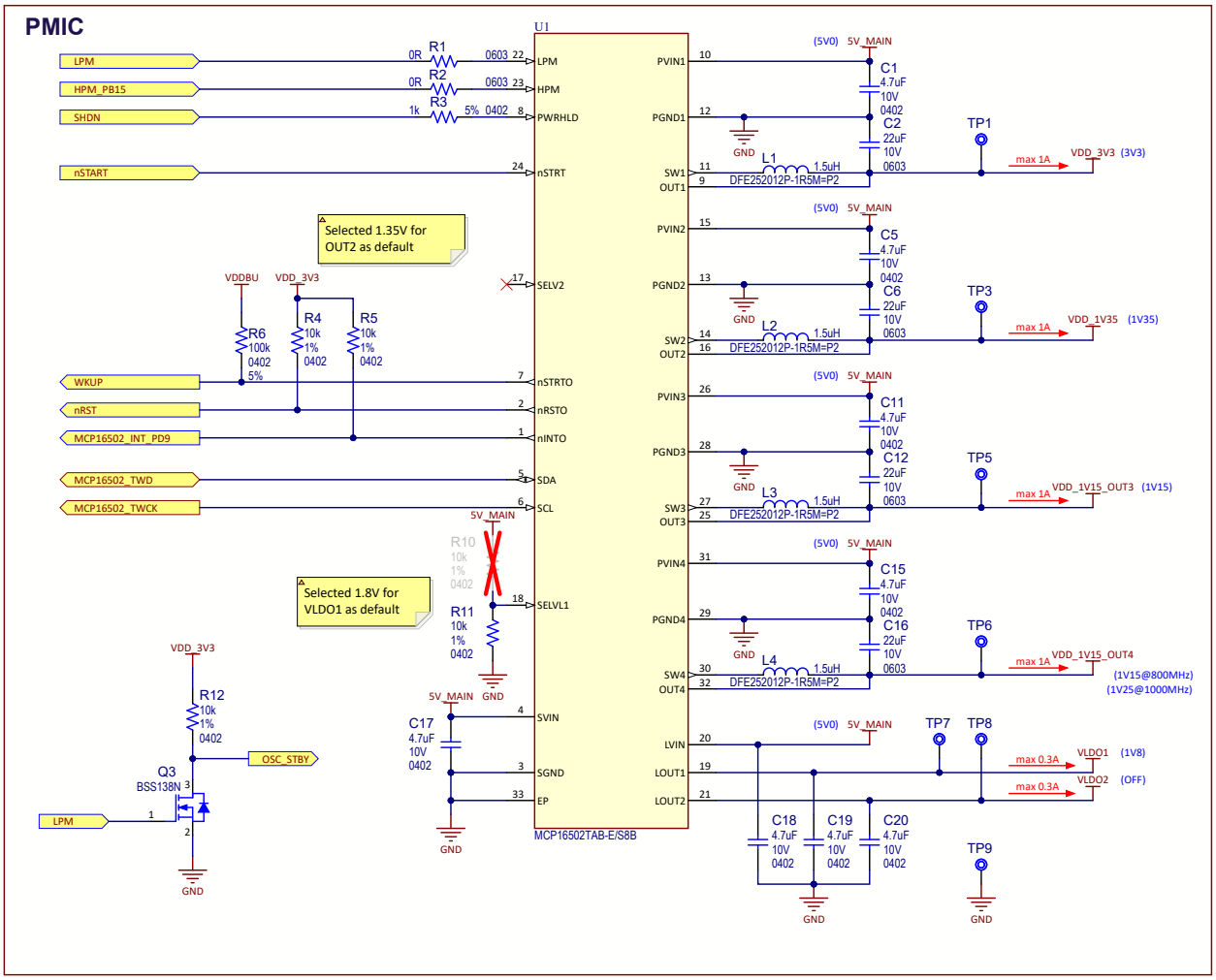


Table 3-1. MCP16502 TWI Address

Device	7-bit client address	Full Address with RD/WR#
MCP16502 TWI Read	1011_011	0xB7
MPC16502 TWI Write		0xB6

3.1.3 Shutdown and Reset Circuitry

The processor controls the Auto-Maintain state and power-down by asserting the SHDN pin. At power-up, the SHDN signal is asserted at high level, sending the instruction to maintain power to the PMIC device. At power-down, SHDN is asserted at low level, PMIC shuts down all the supplies and enters Power-down mode.

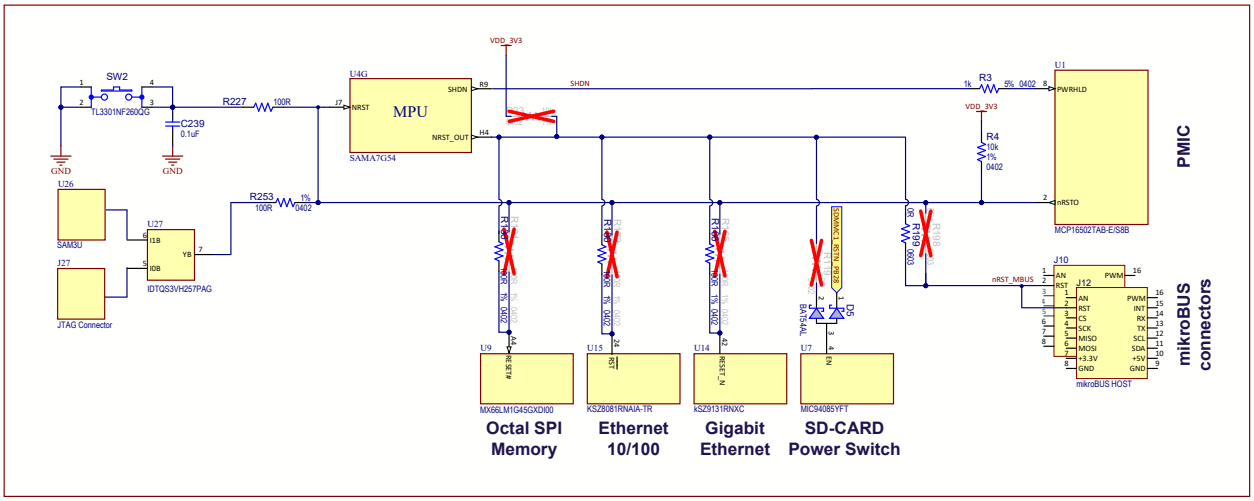
The board includes three reset sources for the SAMA7G5 MPU:

- Power-on reset from the MCP16502 power management unit
- User push button reset (SW2)
- External JTAG or J-Link-OB reset from an in-circuit emulator

Some elements on the board (such as Ethernet PHYs, octal SPI memory and mikroBUS sockets) can be reset by the MPU independently from the general reset. They are connected by default to the NRST_OUT signal of the SAMA7G5 device and each of them can be controlled by the general reset line. A resistor swap must be performed for this configuration.

The figure below shows the shutdown connection and the reset circuitry.

Figure 3-6. SAMA7G54-EK Shutdown and Reset Schematic



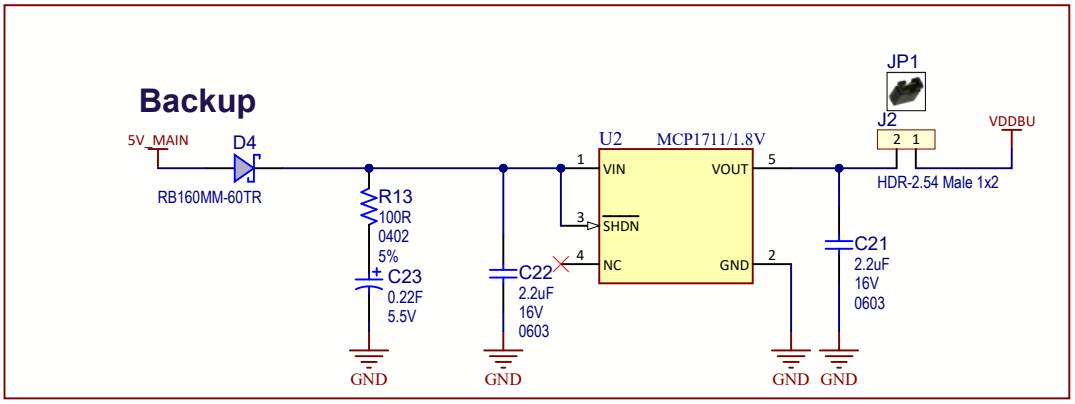
3.1.4 Battery Unit

A 5.0V battery (supercapacitor C23) is implemented to permanently maintain the VDDBU voltage. An LDO (U2 - MCP1711) is assigned to this supercap to decrease the VDDBU voltage down to 1.8V. That allows the VDDBU domain power consumption to be decreased. This LDO has an ultra-low quiescent current and can drive a very low load. For more information on the device, refer to the product webpage.

This function allows the user to shut down the MPU and the system, thus entering a low-power mode, and still keep the custom configuration that was previously set in the MPU backup area.

Jumper JP1/J2 must be in place for proper operation of the MPU, and can be removed if the user wants to bring the MPU back to the initial configuration, by resetting the General Purpose Backup Registers (GPBR).

Figure 3-7. SAMA7G54-EK Backup Circuitry



WARNING Make sure the board is powered off before removing the JP1/J2 jumper.

3.1.5 Power Measurement

One Microchip DC power/energy monitor is embedded on the SAMA7G54-EK board and provides a four-channel current sense monitoring ensured by the PAC1934 device.

The device communicates with the MPU via a Two-Wire Interface (TWI) and an alert output signal.

The PAC1934 is a four-channel power/energy monitor with current sensor amplifier and bus voltage monitors that feed high resolution ADCs. A digital circuitry performs power calculations and energy accumulation. The PAC1934 enables energy monitoring with integration periods ranging from 1 ms to 36 hours. Bus voltage, sense resistor voltage, and accumulated proportional power are stored in registers for retrieval by the system host or embedded controller. For more information about the PAC1934, refer to the product web page.

Four current sense resistors are populated on board for measuring voltage and current consumption on the power rails:

- 10 mΩ on VDD_3V3 node—3.3V power rail power consumtion on SAMA7G5
- 10 mΩ on VDDIODDR node—1.35V power rail power consumption on SAMA7G5 DDR I/Os and on DDR3L memory
- 10 mΩ on VDDCORE node—1.1V power rail power consumption on SAMA7G5 core
- 10 mΩ on VDDCPU node—1.275V power rail power consumption on SAMA7G5 CPU

Figure 3-8. PAC1934 Power Measurement Schematic

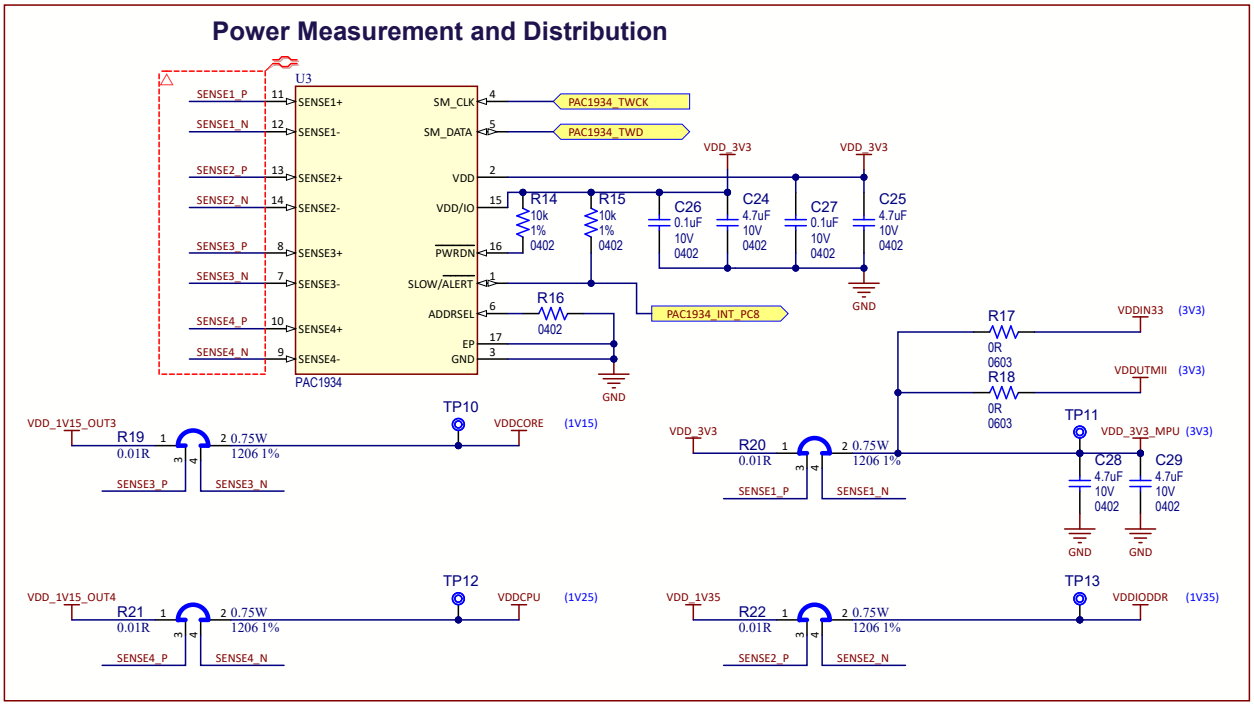


Table 3-2. PAC1934 Signal Descriptions

PIO	Signal Name	Shared PIO	Signal Description
PC10	PAC1934_TWCK	PMIC	TWI clock signal
PC9	PAC1934_TWD	PMIC	TWI data signal
PC8	PAC1935_INT_PC8	–	PAC1934 interrupt

Table 3-3. PAC1934 TWI Address

Device	7-bit Client Address	Full Address with RD/WR#
PAC1934 TWI Read	0010_000	0x21
PAC1934 TWI Write		0x20

3.2 Processor

The SAMA7G5 is a high-performance, ultra-low power Arm® Cortex®-A7 CPU-based embedded microprocessor (MPU) running up to 1 GHz, with support for multiple memories such as 16-bit DDR2, DDR3, DDR3L, LPDDR2, LPDDR3, octal/quad SPI and e.MMC Flash.

The SAMA7G5 integrates complete imaging and audio subsystems with 12-bit parallel and/or MIPI-CSI2 camera interfaces up to 8 Mpixels at 30 fps, up to four I^2S data I/Os, one SPDIF transmitter and receiver and a 4-stereo channel audio sample rate converter.

The device also features a large number of connectivity options with Dual Ethernet (one Gigabit Ethernet and one 10/100 Ethernet), six CAN-FD and three high-speed USB and offers advanced security functions (secure boot, secure key storage, high-performance crypto accelerators for AES, SHA, RSA and ECC).

Refer to the SAMA7G5 Series data sheet for more information (see Reference Documents).

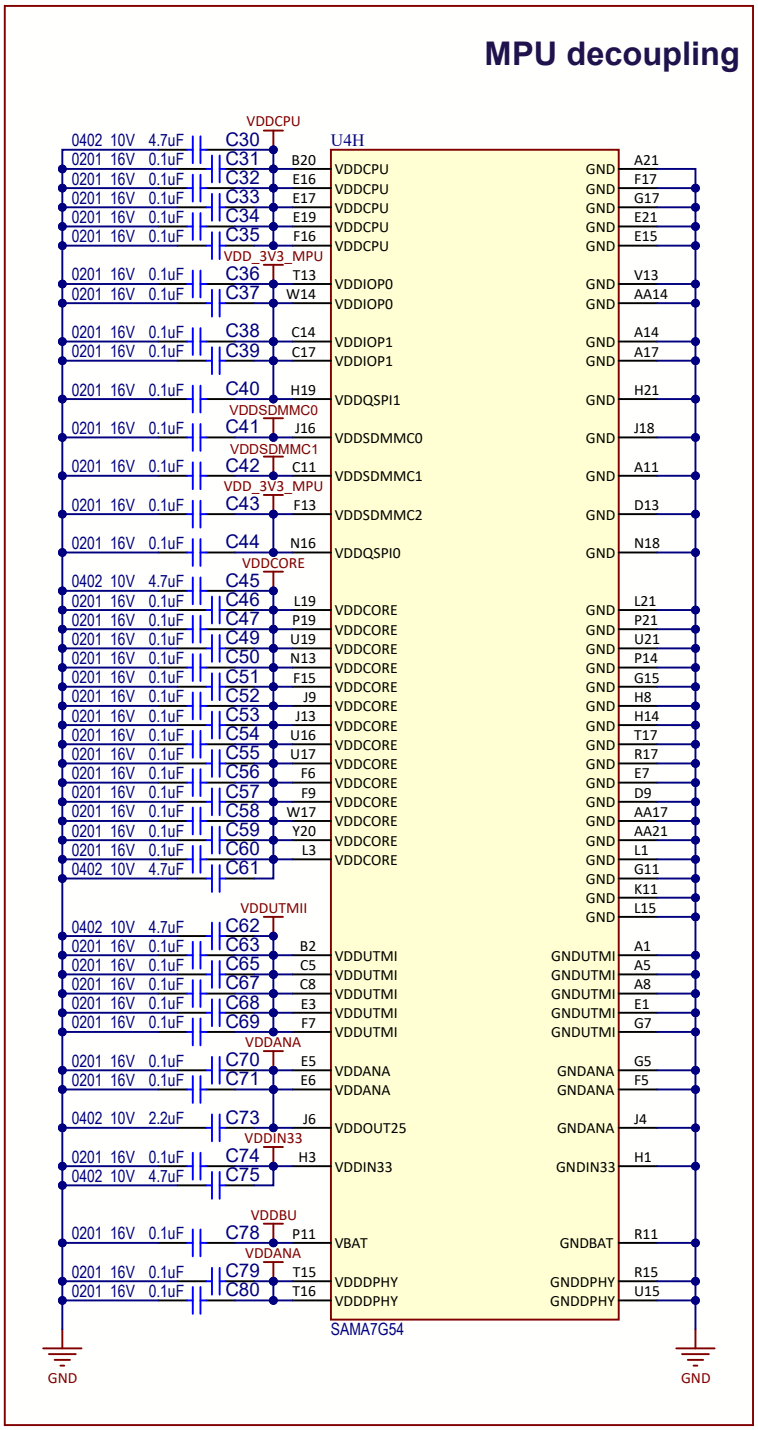
3.2.1 Processor Power Supplies

The power management unit IC (MCP16502) provides all power supplies required by the SAMA7G5 MPU:

- 1.1V for the core power rail (VDDCORE)
- 1.275V for the CPU power rail (VDDCPU)
- 1.35V for the memory power rail (VDDIODDR)
- 3.3V for I/Os, oscillators and digital power rails (VDDIN33, VDDUTMII, VDDIOP0, VDDIOP1, VDDQSPI1, VDDSDMMC2, etc.)

Decoupling capacitors are placed close to the MPU power pins to stabilize the voltage rails.

Figure 3-9. SAMA7G5 Power Decoupling



3.2.2 Configuration and Control

This figure shows the main block for processor configuration and control.

Figure 3-10. Processor Main Configuration and Control

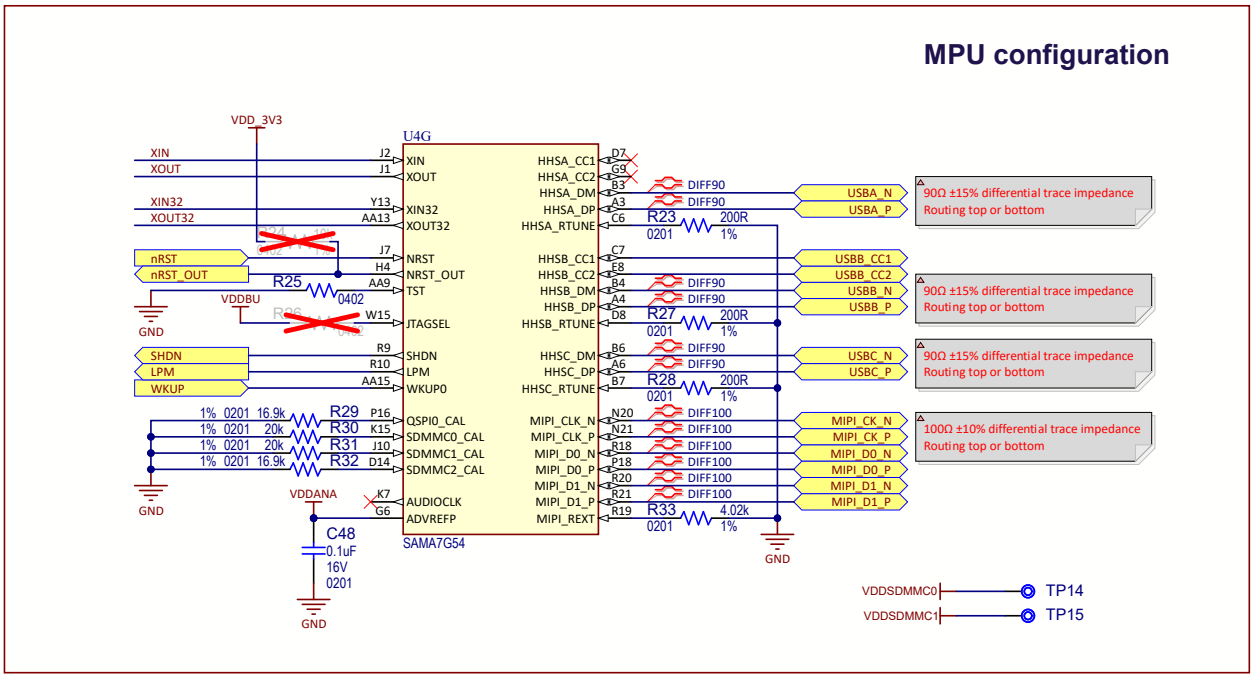


Table 3-4. Processor Main Configuration and Control Pins

Pin Name	Type	Used for
XIN	Input	Main clock oscillator input
XOUT	Output	Main clock oscillator output
XIN32	Input	Slow clock oscillator input
XOUT32	Output	Slow clock oscillator output
NRST	Input	Processor main reset input
NRST_OUT	Output	Processor reset output
TST	Input	Reserved for processor manufacturing tests
JTAGSEL	Input	When pulled high enables the JTAG boundary scan
SHDN	Output	Signal used to enable and disable an external power supply circuit
LPM	Output	Signal used to enable and disable the PMIC Low-Power mode
WKUP0	Input	Event detection input pin used to wake up the processor from Shutdown state
QSPI0_CAL	Input	QSPI calibration
SDMMC0_CAL	Input	SDMMC0 calibration
SDMMC1_CAL	Input	SDMMC1 calibration
SDMMC2_CAL	Input	SDMMC2 calibration
AUDIOCLK	Output	Audio clock output
ADVREFP	Input	Voltage reference for the embedded analog comparator
HHSx_Dx	I/O	Three USB ports embedded inside the MPU
HHSx_RTUNE	Input	USB external tuning
MIPI_CLK_[P-N]	Input	MIPI differential input clock lanes
MIPI_DP[0-1]	Input	MIPI differential input data lanes
MIPI_REXT	Input	MIPI calibration

3.2.3 Clock Circuitry

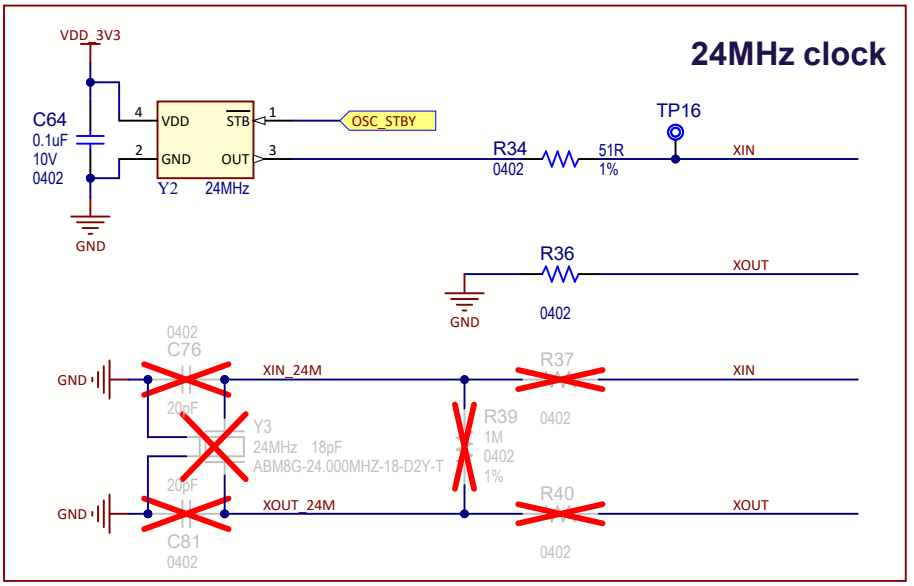
The embedded MPU generates the required clocks based on two oscillators: one slow clock (SLCK) oscillator running at 32.768 kHz and one main clock oscillator running at 24 MHz.

3.2.3.1 Main Clock Circuitry

The main clock oscillator is implemented with a MEMS (Micro Electro-Mechanical System) device DSC1001.

For evaluation purposes, the user can mount a crystal instead of the MEMS, using the PCB footprint reservation (Y3). In that case, remove resistors R34 and R36, populate resistors R37 and R40 and populate capacitors C76 and C81 with the appropriate load capacitance for the selected crystal.

Figure 3-11. Processor Main Clock Schematic

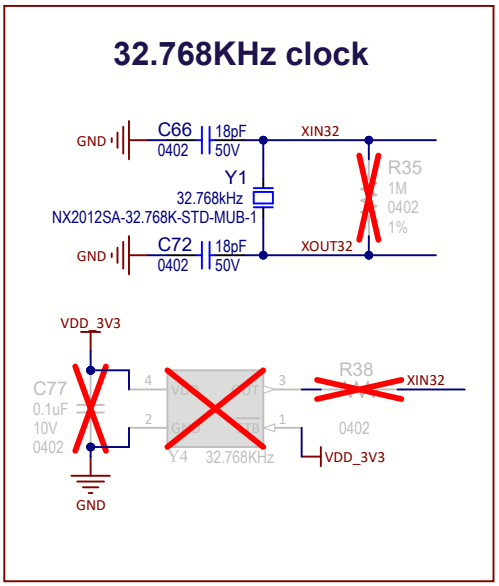


3.2.3.2 Slow Clock Circuitry

The slow clock oscillator is implemented with a NX2012SA-32.768K crystal device.

For evaluation purposes, the user can mount instead a MEMS (Micro Electro-Mechanical System DSC6003MA3B-032K768), using the PCB footprint reservation (Y4). In that case, remove crystal Y1 and capacitors C66 and C72, and populate resistor R38 and capacitor C77 with the appropriate MEMS (Y4).

Figure 3-12. Processor Slow Clock Schematic

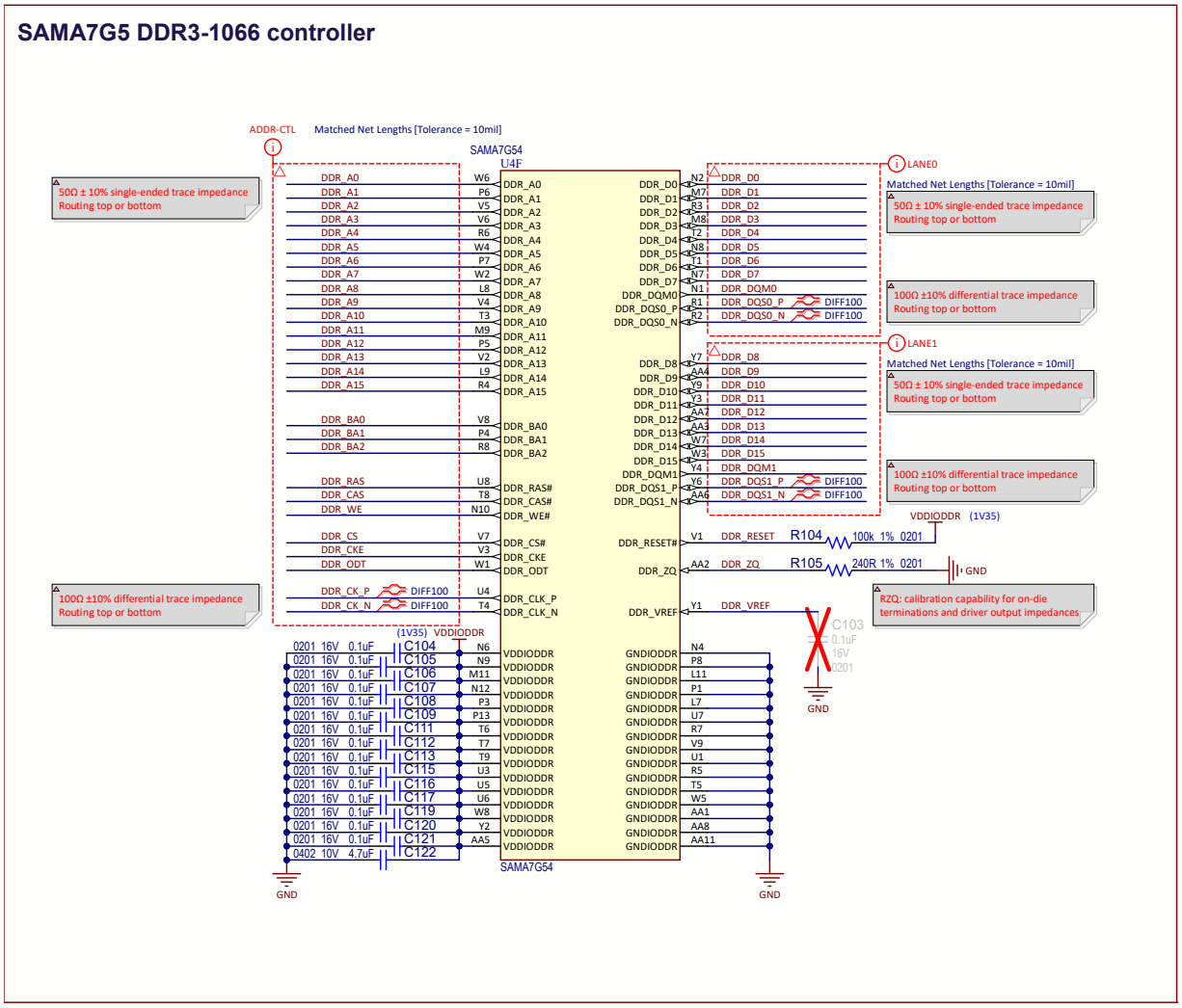


3.2.4 DDR Controller

The SAMA7G5 MPU embeds a Universal DDR Memory Controller (UDDRC) to drive the DDR2, DDR3, LPDDR2 and LPDDR3 memories.

The following figure shows the UDDRC controller schematic and controller layout recommendations.

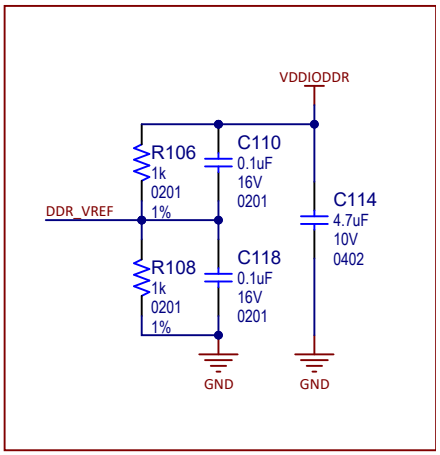
Figure 3-13. Processor UDDRC Controller



The UDDRC I/Os embed an automatic impedance matching control to avoid overshoots and to reach the best performance levels depending on the bus load and external memories. A serial termination connection scheme, where the driver has an output impedance matched to the characteristic impedance of the line, is used to improve signal quality and reduce EMI. This is done using the ZQ calibration procedure to calibrate the SAMA7G5 DDR I/O drive strength. The pin name where the ZQ resistor must be connected is DDR_ZQ, and as indicated in the SAMA7G5 Series data sheet for the DDR3L case, the resistor value is 240 Ohms.

The DDR_VREF pin serves as a voltage reference input for the DDR I/Os when DDR or LPDDR external SDRAM memories are used.

Figure 3-14. DDR_VREF Voltage Reference



3.2.5 Processor PIOs

This section describes all the signals connected to the SAMA7G5 MPU ports.

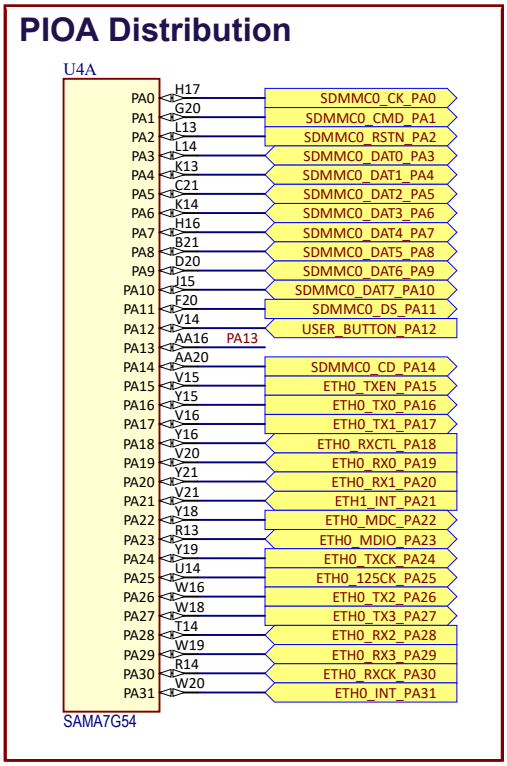
Some of the ports are multiplexed to accommodate more devices on the evaluation kit and to showcase all the functions the SAMA7G5 MPU can address off a single PIO wire. Most of the ports that share multiple functions are split through passive resistors placed on the board as close to the MPU as possible, therefore no other hardware change must be made. In most cases, the user can use only one of their functions at a time, or develop a composite driver enabling the use of multiple functions at the same time.

3.2.5.1 PIOA Bank

The PIOA bank is mainly used for the e.MMC memory and Gigabit Ethernet over power rails VDDSDMMC0 and VDDIOP0, respectively.

The following schematic shows the PIOA bank distribution.

Figure 3-15. SAMA7G5 PIOA Bank Distribution



The following table describes each PIOA bank function.

Table 3-5. SAMA7G5 PIOs Pin Assignment and Signal Description

PIO	Power Rail	Function	Signal Description
PA0	VDDSDMMC0	SDMMC0_CK	e.MMC clock Signal
PA1	VDDSDMMC0	SDMMC0_CMD	e.MMC command line
PA2	VDDSDMMC0	SDMMC0_RSTN	e.MMC reset signal
PA3	VDDSDMMC0	SDMMC0_DAT0	e.MMC data line 0
PA4	VDDSDMMC0	SDMMC0_DAT1	e.MMC data line 1
PA5	VDDSDMMC0	SDMMC0_DAT2	e.MMC data line 2
PA6	VDDSDMMC0	SDMMC0_DAT3	e.MMC data line 3
PA7	VDDSDMMC0	SDMMC0_DAT4	e.MMC data line 4
PA8	VDDSDMMC0	SDMMC0_DAT5	e.MMC data line 5
PA9	VDDSDMMC0	SDMMC0_DAT6	e.MMC data line 6
PA10	VDDSDMMC0	SDMMC0_DAT7	e.MMC data line 7
PA11	VDDSDMMC0	SDMMC0_DS	e.MMC data strobe
PA12	VDDIOP0	PA12	User button
PA13	VDDIOP0	PWMH2	Green LED control or mikroBUS 1 PWM control
PA14	VDDIOP0	SDMMC0_CD	e.MMC card detect
PA15	VDDIOP0	G0_TXEN	Transmit enable
PA16	VDDIOP0	G0_TX0	Transmit data line 0
PA17	VDDIOP0	G0_TX1	Transmit data line 1
PA18	VDDIOP0	G0_RXCTL	Receive data valid and receive error

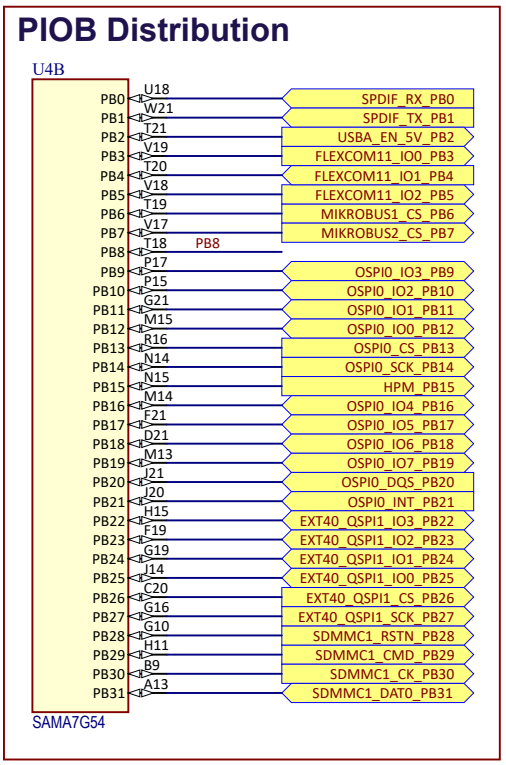
.....continued			
PIO	Power Rail	Function	Signal Description
PA19	VDDIOP0	G0_RX0	Receive data line 0
PA20	VDDIOP0	G0_RX1	Receive data line 1
PA21	VDDIOP0	PA21	Ethernet 1 interrupt (10/100 Ethernet)
PA22	VDDIOP0	G0_MDC	Management data clock
PA23	VDDIOP0	G0_MDIO	Management data input/output
PA24	VDDIOP0	G0_TXCK	Transmit clock
PA25	VDDIOP0	G0_125CK	125 MHz clock
PA26	VDDIOP0	G0_TX2	Transmit data line 2
PA27	VDDIOP0	G0_TX3	Transmit data line 3
PA28	VDDIOP0	G0_RX2	Receive data line 2
PA29	VDDIOP0	G0_RX3	Receive data line 3
PA30	VDDIOP0	G0_RXCK	Receive clock
PA31	VDDIOP0	PA31	Ethernet 0 interrupt (Gigabit Ethernet)

3.2.5.2 PIOB Bank

The PIOB bank is mainly used for the SPI interface, QSPI and SD Card over power rails VDDIOP0, VDDQSPI1/0 and VDDSDMMC1, respectively.

The following schematic shows the PIOB bank distribution.

Figure 3-16. SAMA7G5 PIOB Bank Distribution



The following table describes each PIOB bank function.

Table 3-6. SAMA7G5 PIOs Pin Assignment and Signal Description

PIO	Power Rail	Function	Signal Description
PB0	VDDIOP0	SPDIF_RX	SPDIF receive data

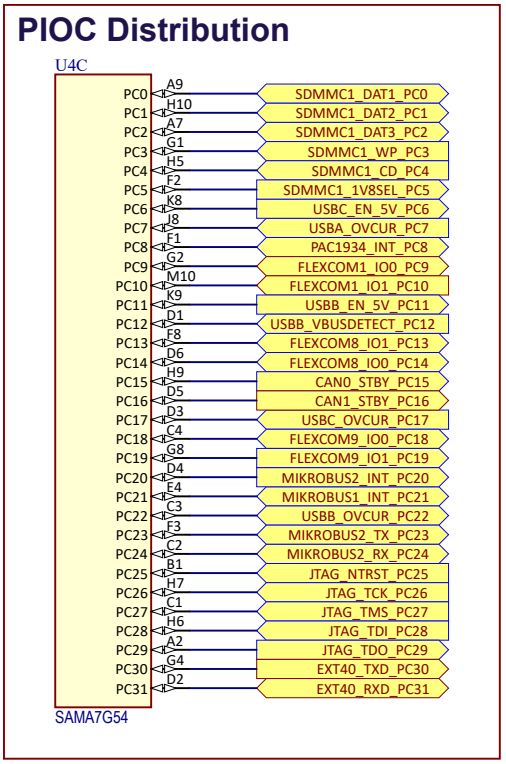
.....continued			
PIO	Power Rail	Function	Signal Description
PB1	VDDIOP0	SPDIF_TX	SPDIF transmit data
PB2	VDDIOP0	PB2	Power enable USB host port A
PB3	VDDIOP0	FLEXCOM11_IO0	mikroBUS 1 or mikroBUS 2 SPI MOSI line
PB4	VDDIOP0	FLEXCOM11_IO1	mikroBUS 1 or mikroBUS 2 SPI MISO line
PB5	VDDIOP0	FLEXCOM11_IO2	mikroBUS 1 or mikroBUS 2 SPI CLOCK line
PB6	VDDIOP0	FLEXCOM11_IO3	mikroBUS 1 SPI Chip Select line
PB7	VDDIOP0	FLEXCOM11_IO4	mikroBUS 2 SPI Chip Select line
PB8	VDDIOP0	PB8	Red LED control or RPi connector GPIO
PB9	VDDQSPI0	QSPI0_IO3	Octal SPI0 I/O line 3
PB10	VDDQSPI0	QSPI0_IO2	Octal SPI0 I/O line 2
PB11	VDDQSPI0	QSPI0_IO1	Octal SPI0 I/O line 1
PB12	VDDQSPI0	QSPI0_IO0	Octal SPI0 I/O line 0
PB13	VDDQSPI0	QSPI0_CS	Octal SPI0 Chip Select
PB14	VDDQSPI0	QSPI0_SCK	Octal SPI0 serial clock
PB15	VDDQSPI0	PB15	MCP16502 HPM control
PB16	VDDQSPI0	QSPI0_IO4	Octal SPI0 I/O line 4
PB17	VDDQSPI0	QSPI0_IO5	Octal SPI0 I/O line 5
PB18	VDDQSPI0	QSPI0_IO6	Octal SPI0 I/O line 6
PB19	VDDQSPI0	QSPI0_IO7	Octal SPI0 I/O line 7
PB20	VDDQSPI0	QSPI0_DQS	Octal SPI0 data strobe
PB21	VDDQSPI0	QSPI0_INT	Octal SPI0 interrupt
PB22	VDDQSPI1	QSPI1_IO3	RPi connector QSPI1 I/O line 3
PB23	VDDQSPI1	QSPI1_IO2	RPi connector QSPI1 I/O line 2
PB24	VDDQSPI1	QSPI1_IO1	RPi connector QSPI1 I/O line 1
PB25	VDDQSPI1	QSPI1_IO0	RPi connector QSPI1 I/O line 0
PB26	VDDQSPI1	QSPI1_CS	RPi connector QSPI1 Chip Select
PB27	VDDQSPI1	QSPI1_SCK	RPi connector QSPI1 serial clock
PB28	VDDSDMMC1	SDMMC1_RSTN	SD Card reset signal
PB29	VDDSDMMC1	SDMMC1_CMD	SD Card command line
PB30	VDDSDMMC1	SDMMC1_CK	SD Card clock signal
PB31	VDDSDMMC1	SDMMC1_DAT0	SD Card data line 0

3.2.5.3 PIOC Bank

The PIOC bank is mainly used for the UART and TWI interfaces, over power rail VDDIN33.

The following schematic shows the PIOC bank distribution.

Figure 3-17. SAMA7G5 PIOC Bank Distribution



The following table describes each PIOC bank function.

Table 3-7. SAMA7G5 PIOs Pin Assignment and Signal Description

PIO	Power Rail	Function	Signal Description
PC0	VDDSDMMC1	SDMMC1_DAT1	SD Card data line 1
PC1	VDDSDMMC1	SDMMC1_DAT2	SD Card data line 2
PC2	VDDSDMMC1	SDMMC1_DAT3	SD Card data line 3
PC3	VDDIN33	SDMMC1_WP	SD Card connector write protect signal
PC4	VDDIN33	SDMMC1_CD	SD Card card detect
PC5	VDDIN33	SDMMC1_1V8SEL	SD Card signal voltage selection
PC6	VDDIN33	PC6	Power enable USB host port C
PC7	VDDIN33	PC7	USB over-current interrupt port A
PC8	VDDIN33	PC8	Power measurement interrupt
PC9	VDDIN33	FLEXCOM1_IO0	TWI data line for MCP16502, PAC1934 devices
PC10	VDDIN33	FLEXCOM1_IO1	TWI clock line for MCP16502, PAC1934 devices
PC11	VDDIN33	PC11	Power enable USB host port B
PC12	VDDIN33	PC12	USB over-current interrupt port B
PC13	VDDIN33	FLEXCOM8_IO1	TWI clock line for ECC608, RPi CSI camera, EEPROM1 or EEPROM2 devices
PC14	VDDIN33	FLEXCOM8_IO0	TWI data line for ECC608, RPi CSI camera, EEPROM1 or EEPROM2 devices
PC15	VDDIN33	PC15	Standby control CAN 0
PC16	VDDIN33	PC16	Standby control CAN 1
PC17	VDDIN33	PC17	USB over-current interrupt port C
PC18	VDDIN33	FLEXCOM9_IO0	TWI data line for mikroBUS 1, mikroBUS 2 or RPi connector devices
PC19	VDDIN33	FLEXCOM9_IO1	TWI clock line for mikroBUS 1, mikroBUS 2 or RPi connector devices
PC20	VDDIN33	PC20	mikroBUS 2 interrupt

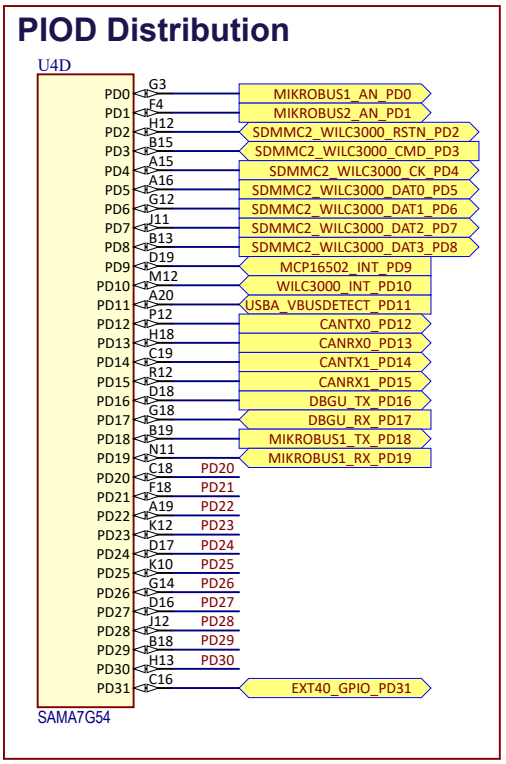
.....continued			
PIO	Power Rail	Function	Signal Description
PC21	VDDIN33	PC21	mikroBUS 1 interrupt
PC22	VDDIN33	PC22	USB over-current interrupt port B
PC23	VDDIN33	FLEXCOM7_IO0	mikroBUS 2 UART TX line
PC24	VDDIN33	FLEXCOM7_IO1	mikroBUS 2 UART RX line
PC25	VDDIN33	NTRST	JTAG - Test reset signal
PC26	VDDIN33	TCK_SWCLK	JTAG - Test clock/serial wire clock
PC27	VDDIN33	TMS_SWDIO	JTAG - Test mode select/serial wire input/output
PC28	VDDIN33	TDI	JTAG - Test data in
PC29	VDDIN33	TDO	JTAG - Test data out
PC30	VDDIN33	FLEXCOM10_IO0	RPi connector UART TX line
PC31	VDDIN33	FLEXCOM10_IO1	RPi connector UART RX line

3.2.5.4 PIOD Bank

The PIOD bank is mainly used for the WILC3000 radio module and Ethernet 10/100, over power rails VDDSDMMC2 and VDDIOP1, respectively.

The following schematic shows the PIOD bank distribution.

Figure 3-18. SAMA7G5 PIOD Bank Distribution



The following table describes each PIOD bank function.

Table 3-8. SAMA7G5 PIOs Pin Assignment and Signal Description

PIO	Power Rail	Function	Signal Description
PD0	VDDIN33	AD14	mikroBUS 1 analog input
PD1	VDDIN33	AD15	mikroBUS 2 analog input
PD2	VDDSDMMC2	SDMMC2_RSTN	WILC3000 SDIO reset line

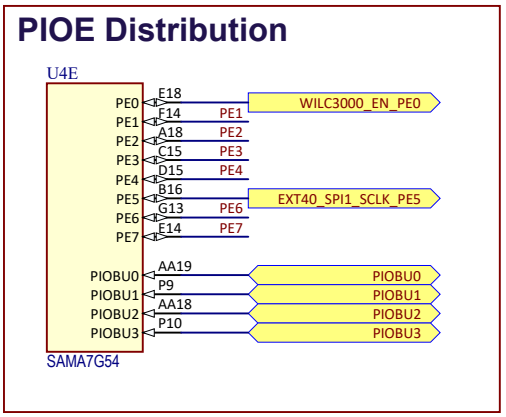
.....continued			
PIO	Power Rail	Function	Signal Description
PD3	VDDSDMMC2	SDMMC2_CMD	WILC3000 SDIO command line
PD4	VDDSDMMC2	SDMMC2_CK	WILC3000 SDIO clock line
PD5	VDDSDMMC2	SDMMC2_DAT0	WILC3000 SDIO data line 0
PD6	VDDSDMMC2	SDMMC2_DAT1	WILC3000 SDIO data line 1
PD7	VDDSDMMC2	SDMMC2_DAT2	WILC3000 SDIO data line 2
PD8	VDDSDMMC2	SDMMC2_DAT3	WILC3000 SDIO data line 3
PD9	VDDIOP1	PD9	MCP16502 interrupt
PD10	VDDIOP1	PD10	WILC3000 interrupt
PD11	VDDIOP1	PD11	Power detect USB port A
PD12	VDDIOP1	CANTX0	CAN transmit line 0
PD13	VDDIOP1	CANRX0	CAN receive line 0
PD14	VDDIOP1	CANTX1	CAN transmit line 1
PD15	VDDIOP1	CANRX1	CAN receive line 1
PD16	VDDIOP1	FLEXCOM3_IO0	Debug UART TX line
PD17	VDDIOP1	FLEXCOM3_IO1	Debug UART RX line
PD18	VDDIOP1	FLEXCOM4_IO0	mikroBUS 1 UART TX line
PD19	VDDIOP1	FLEXCOM4_IO1	mikroBUS 1 UART RX line
PD20	VDDIOP1	PWMH3	LED blue control or mikroBUS 2 PWM control
PD21	VDDIOP1	G1_TXEN/PD21	Transmit enable or RPi connector GPIO
PD22	VDDIOP1	G1_TX0/PDMC0_CLK	Transmit data line 0 or PDM clock line
PD23	VDDIOP1	G1_TX1/PDMC0_DS0	Transmit data line 1 or PDM data line 0
PD24	VDDIOP1	G1_CRSDV/PDMC0_DS1	Carrier sense and data valid or PDM data line 1
PD25	VDDIOP1	G1_RX0/PD25	Receive data line 0 or RPi connector GPIO
PD26	VDDIOP1	G1_RX1/PD26	Receive data line 1 or RPi connector GPIO
PD27	VDDIOP1	G1_RXER/PD27	Receive Error or RPi connector GPIO
PD28	VDDIOP1	G1_MDC/PWML3	Management data clock or RPi connector GPIO
PD29	VDDIOP1	G1_MDIO/PD29	Management data input/output or RPi connector GPIO
PD30	VDDIOP1	G1_TXCK/PD30	Transmit clock or RPi connector GPIO
PD31	VDDIOP1	PD31	RPi connector GPIO

3.2.5.5 PIOE Bank

The PIOE bank is mainly used for the WILC3000 radio module over power rail VDDIOP1.

The following schematic shows the PIOE bank and PIOBUx distributions.

Figure 3-19. SAMA7G5 PIOE Bank Distribution



The following table describes each PIOE bank function.

Table 3-9. SAMA7G5 PIOs Pin Assignment and Signal Description

PIO	Power Rail	Function	Signal Description
PE0	VDDIOP1	PE0	ATWILC3000 enable control signal
PE1	VDDIOP1	PE1	RPi connector SPI chip enable 2 or RPi CSI camera GPIO
PE2	VDDIOP1	PWML0/PE2	RPi connector PWM signal or RPi CSI camera GPIO
PE3	VDDIOP1	FLEXCOM0_IO0	RPi connector SPI MOSI line or WILC3000 USART RX line
PE4	VDDIOP1	FLEXCOM0_IO1	RPi connector SPI MISO line or WILC3000 USART TX line
PE5	VDDIOP1	FLEXCOM0_IO2	RPi connector SPI clock line
PE6	VDDIOP1	FLEXCOM0_IO3	RPi connector SPI chip enable 0 or WILC3000 USART RTS line
PE7	VDDIOP1	FLEXCOM0_IO4	RPi connector SPI chip enable 1 or WILC3000 USART CTS line
PIOBU0	VDDBU	PIOBU0	Tamper 0 - Tamper connector
PIOBU1	VDDBU	PIOBU1	Tamper 1 - Tamper connector
PIOBU2	VDDBU	PIOBU2	Tamper 2 - Tamper connector
PIOBU3	VDDBU	PIOBU3	Tamper 3 - Tamper connector

3.2.5.6 Interfaces Distribution

3.2.5.6.1 TWI Bus Distribution

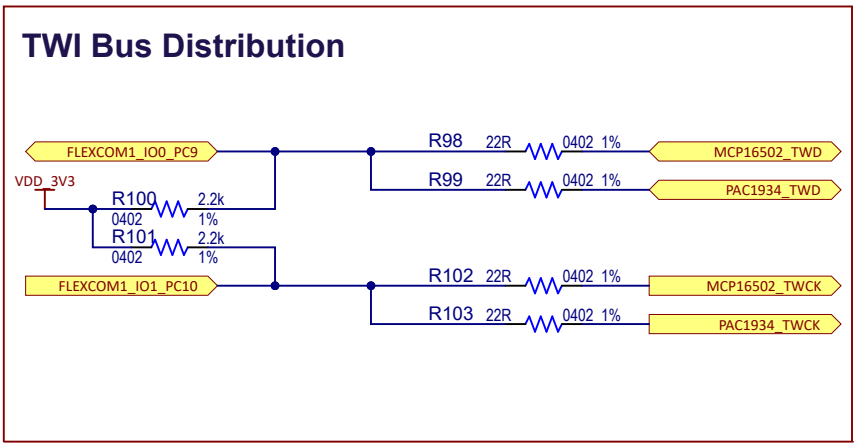
The SAMA7G54-EK features three dedicated TWIs to access the on-board devices.

The TWI interface uses only two lines, namely serial data (TWD) and serial clock (TWCK). According to the standard, the TWI clock rate is limited to 400 kHz in Fast mode and 100 kHz in Normal mode, but a configurable baud rate generator enables adapting the output data rate to a wide range of core clock frequencies. The TWI supports both Host and Client modes.

The first interface is used to access the following devices:

- MCP16502 power management unit (address: 1011_011[R/W])
- PAC1934 voltage monitor (address: 0010_000[R/W])

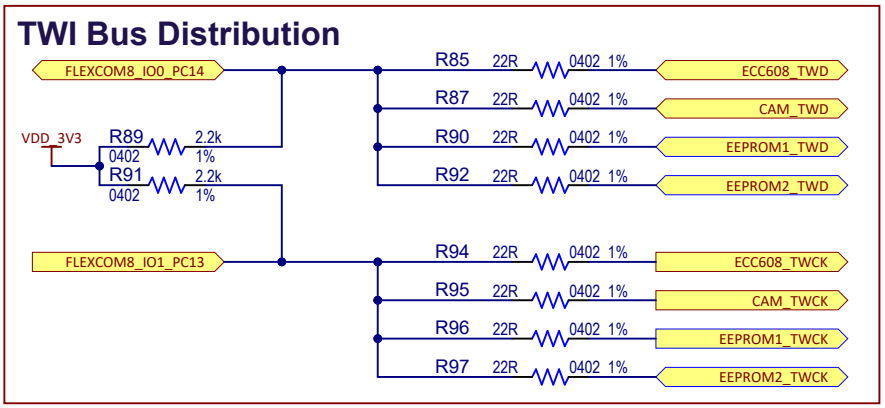
Figure 3-20. First TWI Interface



The second interface is used to access the following devices:

- ATECC608A secure element (address: 1100_000[R/W])
- Any camera module placed on the RPi CSI MIPI connector
- First 24AA025E48 serial EEPROM (address: 1010_010[R/W])
- Second 24AA025E48 serial EEPROM (address: 1010_011[R/W])

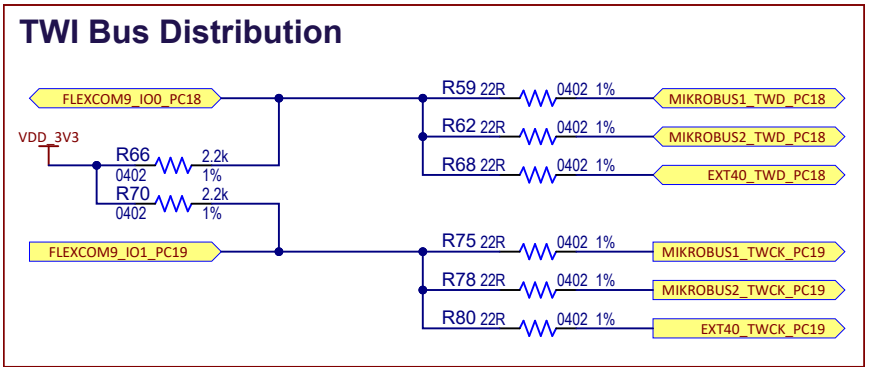
Figure 3-21. Second TWI Interface



The third interface is used to access any device placed on one of the following:

- mikroBUS 1 connector
- mikroBUS 2 connector
- RPi 40-pin connector

Figure 3-22. Third TWI Interface



3.2.5.6.2 SPI Bus Distribution

The SAMA7G54-EK features two dedicated SPIs to access the on-board devices.

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Host or Client mode. It also enables communication between processors if an external processor is connected to the system.

The SPI system consists of two data lines and two control lines:

- Host Out Client In (MOSI)—This data line supplies the output data from the host shifted into the input(s) of the client(s).
- Host In Client Out (MISO)—This data line supplies the output data from a client to the input of the host. There may be no more than one client transmitting data during any particular transfer.
- Serial Clock (SPCK)—This control line is driven by the host and regulates the flow of the data bits. The host can transmit data at a variety of baud rates; there is one SPCK pulse for each bit that is transmitted.
- Client Select (NSS)—This control line allows clients to be turned on and off by hardware.

The first interface is used to access the following devices:

- Any device placed on the mikroBUS 1 connector. Flexcom11 in SPI mode is used to address this interface. Chip Select 0 is used to select the device available in this interface.
- Any device placed on the mikroBUS 2 connector. Flexcom11 in SPI mode is used to address this interface. Chip Select 1 is used to select the device available in this interface.

Figure 3-23. First SPI Distribution Schematic

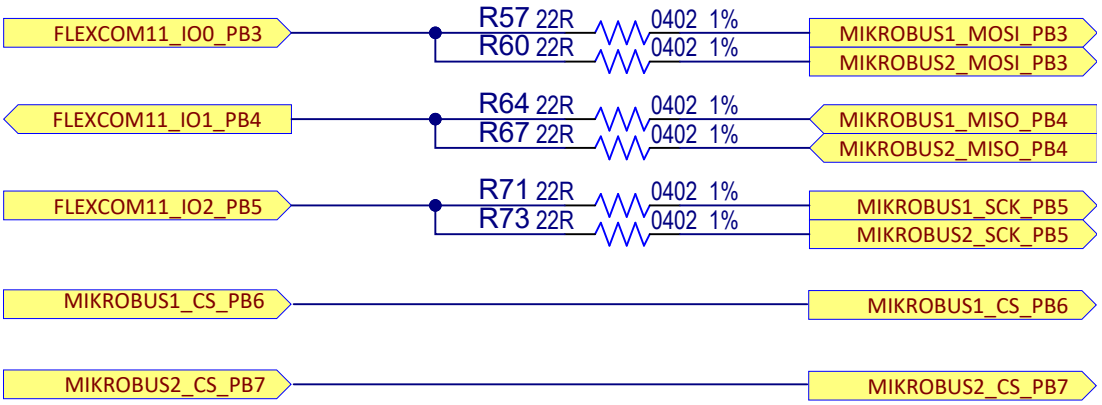


Table 3-10. First SPI PIO Assignments

PIO	MPU Net Name	Device Net Name	Function
PB3	FLEXCOM11_IO0_PB3	MIKROBUS1_MOSI_PB3	SPI MOSI line mikroBUS 1
		MIKROBUS2_MOSI_PB3	SPI MOSI line mikroBUS 2
PB4	FLEXCOM11_IO1_PB4	MIKROBUS1_MISO_PB4	SPI MISO line mikroBUS 1
		MIKROBUS2_MISO_PB4	SPI MISO line mikroBUS 2
PB5	FLEXCOM11_IO2_PB5	MIKROBUS1_SCK_PB5	SPI clock line mikroBUS 1
		MIKROBUS2_SCK_PB5	SPI clock line mikroBUS 2
PB6	MIKROBUS1_CS_PB6	MIKROBUS1_CS_PB6	SPI Chip Select 0 mikroBUS 1
PB7	MIKROBUS2_CS_PB7	MIKROBUS2_CS_PB7	SPI Chip Select 1 mikroBUS 2

The second interface is used to access the following devices either in SPI mode or in USART mode:

- Any device placed on the RPi 40-pin connector. Flexcom0 in SPI mode is used to address this interface. Chip Select 0 and Chip Select 1 are used to select the device(s) available in this interface.
- WILC3000 USART interface. Flexcom0 is used in USART mode.
- **Note:** Only IO0, IO1, IO3 and IO4 are shared between these two interfaces. IO2 (clock) is reserved to SPI mode only.

Figure 3-24. Second SPI Distribution Schematic

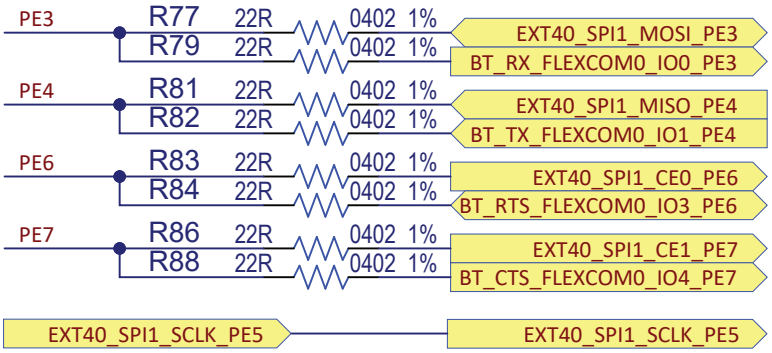


Table 3-11. Second SPI PIO Assignment

PIO	MPU Net Name	Device Net Name	Function
PE3	PE3	EXT40_SPI1_MOSI_PE3	SPI MOSI line RPi 40-pin connector
		BT_RX_FLEXCOM0_IO0_PE3	WILC3000 USART RX line
PE4	PE4	EXT40_SPI1_MISO_PE4	SPI MISO line RPi 40-pin connector
		BT_TX_FLEXCOM0_IO1_PE4	WILC3000 USART TX line
PE6	PE6	EXT40_SPI1_CE0_PE6	SPI Chip Select 0 RPi 40-pin connector
		BT_RTS_FLEXCOM0_IO3_PE6	WILC3000 USART RTS line
PE7	PE7	EXT40_SPI1_CE1_PE7	SPI Chip Select 1 RPi 40-pin connector
		BT_CTS_FLEXCOM0_IO4_PE7	WILC3000 USART CTS line
PE5	EXT40_SPI1_SCLK_PE5	EXT40_SPI1_SCLK_PE5	SPI clock line RPi 40-pin connector

3.2.5.6.3 GPIO Distribution

The SAMA7G54-EK features one QuickSwitch 2:1 multiplexer to distribute the MPU PIOs.

The multiplexer distributes the PIOs according to the J3 status:

- J3 is open (default mode): the Ethernet 10/100 interface is distributed.
- J3 is closed: the PDMC0 interface is distributed.

Figure 3-25. GPIO Distribution Schematic

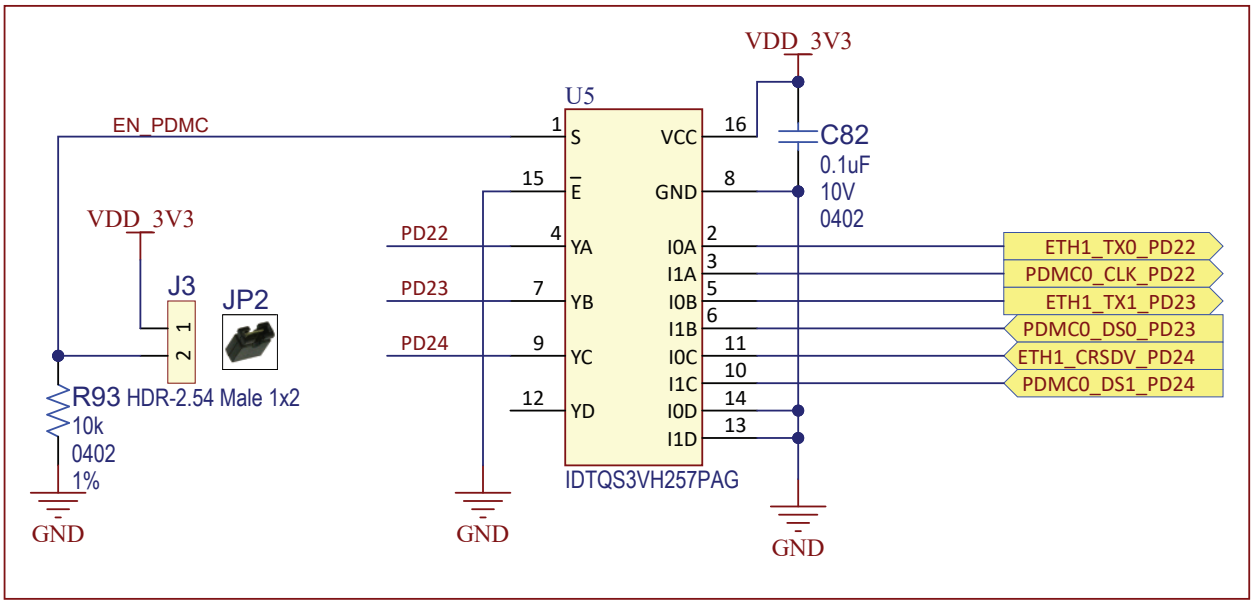


Table 3-12. GPIO Assignments

PIO	MPU Net Name	Device Net Name	Function
PD22	PD22	ETH1_TX0_PD22	Transmit data line 0
		PDMC0_CLK_PD22	PDM clock line
PD23	PD23	ETH1_TX1_PD23	Transmit data line 1
		PDMC0_DS0_PD23	PDM data line 0
PD24	PD24	ETH1_CRSDV_PD24	Receive data valid or carrier sense and data valid
		PDMC0_DS1_PD24	PDM data line 1

3.2.5.6.4 Shared GPIO Resources

The SAMA7G54-EK embeds several GPIOs shared between two devices/interfaces.

The schematic below describes the sharing information.

Figure 3-26. GPIO Sharing Schematic

Table 3-13. GPIO Assignements

PIO	MPU Net Name	Device Net Name	Function
PA13	PA13	LED_GREEN_PA13	Green LED control in PWM mode
		MIKROBUS1_PWM_PA13	mikroBUS 1 PWM control
PB8	PB8	LED_RED_PB8	Red LED control in GPIO mode
		EXT40_GPIO_PB8	RPi 40-pin connector GPIO
PD20	PD20	LED_BLUE_PD20	Blue LED control in PWM mode
		MIKROBUS2_PWM_PD20	mikroBUS 2 PWM control
PD21	PD21	ETH1_TXEN_PD21	Ethernet 10/100 transmit enable
		EXT40_GPIO_PD21	RPi 40-pin connector GPIO
PD25	PD25	ETH1_RX0_PD25	Ethernet 10/100 receive data line 0
		EXT40_GPIO_PD25	RPi 40-pin connector GPIO
PD26	PD26	ETH1_RX1_PD26	Ethernet 10/100 receive data line 1
		EXT40_GPIO_PD26	RPi 40-pin connector GPIO
PD27	PD27	ETH1_RXER_PD27	Ethernet 10/100 receive error
		EXT40_GPIO_PD27	RPi 40-pin connector GPIO
PD28	PD28	ETH1_MDC_PD28	Ethernet 10/100 management data clock
		EXT40_PWM1_PD28	RPi 40-pin connector GPIO

.....continued			
PIO	MPU Net Name	Device Net Name	Function
PD29	PD29	ETH1_MDIO_PD29	Ethernet 10/100 management data input/output
		EXT40_GPIO_PD29	RPi 40-pin connector GPIO
PD30	PD30	ETH1_TXCK_PD30	Ethernet 10/100 transmit clock or 50 MHz reference clock
		EXT40_GPIO_PD30	RPi 40-pin connector GPIO
PE1	PE1	EXT40_SPI1_CE2_PE1	RPi 40-pin connector SPI chip enable 2
		CAM_GPIO0_PE1	RPi CSI camera GPIO
PE2	PE2	EXT40_PWM0_PE2	RPi 40-pin connector PWM signal in PWM mode
		CAM_GPIO1_PE2	RPi CSI camera GPIO

3.3 On-Board Memories

The SAMA7G5 MPU features a Universal DDR Memory Controller (UDDRC), a Quad Serial Peripheral Interface (QSPI) and a Secure Digital MultiMedia Card Controller (SDMMC) to enable interfacing to a wide range of external memories.

This section describes the memory devices mounted on the SAMA7G54-EK board:

- One 16-bit, 4-Gbit DDR3L SDRAM
- One 32-Gbit e.MMC NAND Flash
- One 1-Gbit Serial multi I/O Flash
- Two 2-Kb I^2C serial EEPROMs with pre-programmed EUI-48 MAC ID

Additional memory can be added to the board by:

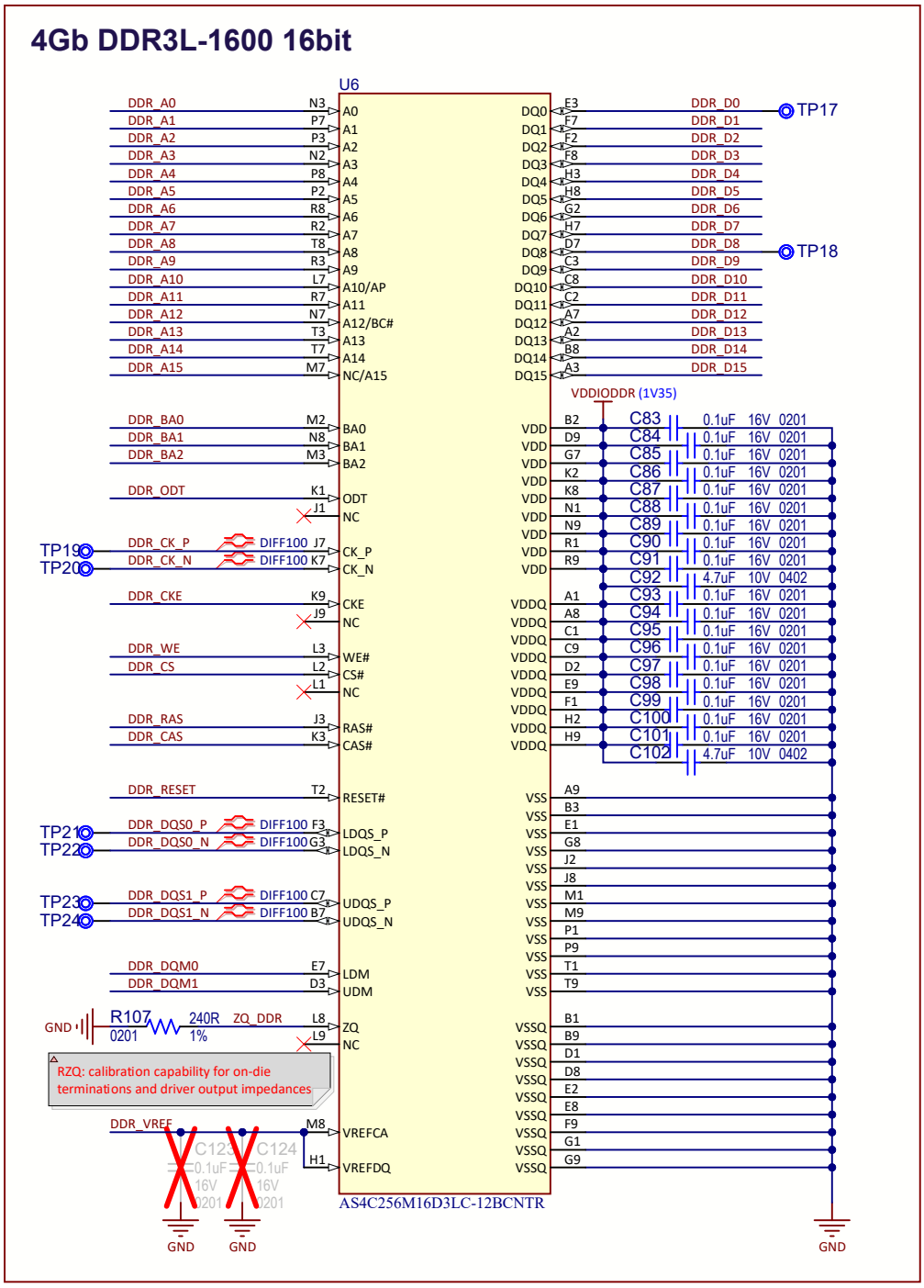
- installing an SD Card in the SD Card slot,
- using the USB ports.

Support depends on the OS driver support.

3.3.1 DDR3L Memory

One DDR3L memory (4-Gbit AS4C256M16D3LC-12BCNTR = 32 Mwords x 16 bits x 8 banks) is used as main system memory, totaling 512 MBytes of SDRAM on the board. The memory bus is 16 bits wide and operates with a frequency of up to 533 MHz.

Figure 3-27. DDR3L Memory Schematic



3.3.2 e.MMC Memory

The SAMA7G54-EK supports e.MMC NAND Flash memory through its Secure Digital Multimedia Controller (SDMMC), and the board implements an S40FC004C1B1C00000, 32-Gb e.MMC NAND Flash to provide a 4-Gbyte memory space.

Figure 3-28. e.MMC Memory Schematic

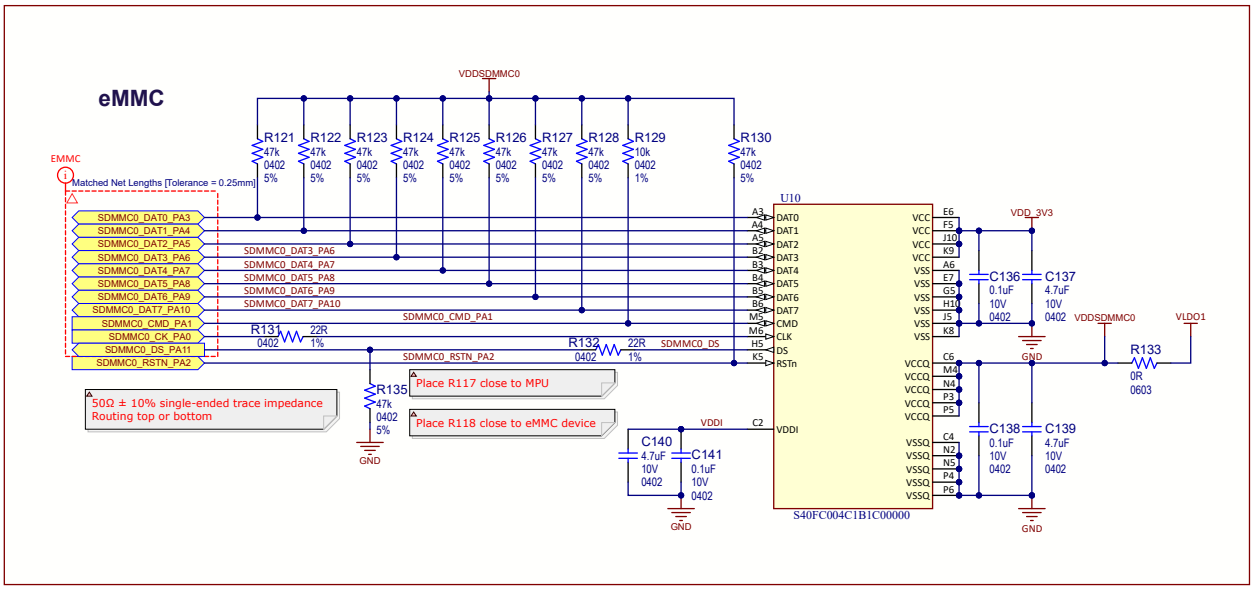


Table 3-14. e.MMC NAND Flash Signal Descriptions

PIO	Signal Name	Shared PIO	Signal Description
PA0	SDMMC0_CK_PA0	–	e.MMC clock signal
PA1	SDMMC0_CMD_PA1	–	e.MMC command line
PA2	SDMMC0_RSTN_PA2	–	e.MMC reset signal
PA3	SDMMC0_DAT0_PA3	–	e.MMC data line 0
PA4	SDMMC0_DAT1_PA4	–	e.MMC data line 1
PA5	SDMMC0_DAT2_PA5	–	e.MMC data line 2
PA6	SDMMC0_DAT3_PA6	–	e.MMC data line 3
PA7	SDMMC0_DAT4_PA7	–	e.MMC data line 4
PA8	SDMMC0_DAT5_PA8	–	e.MMC data line 5
PA9	SDMMC0_DAT6_PA9	–	e.MMC data line 6
PA10	SDMMC0_DAT7_PA10	–	e.MMC data line 7
PA11	SDMMC0_DS_PA11	–	e.MMC data strobe

To enable booting on e.MMC, the PA14 I/O must be grounded. A circuitry is available on the SAMA7G54-EK board to enable/disable boot from e.MMC. See Disable Boot for more details.

3.3.3 Octal Serial Flash

The SAMA7G54-EK board features one Quad Serial Peripheral Interface (QSPI) memory MX66LM1G45GXDI00.

The QSPI is a synchronous serial data link that provides communication with external devices in Host mode.

The QSPI can be used in SPI mode to interface to serial peripherals (such as ADCs, DACs, LCD controllers, CAN controllers and sensors), or in Serial Memory mode to interface to serial Flash memories. Octal SPI mode is then used.

Using the QSPI, the system executes code directly from a serial Flash memory (XIP) without code shadowing to RAM. The serial Flash memory mapping is seen in the system as other memories such as ROM, SRAM, DRAM, embedded Flash memory, etc.

With the support of the Quad SPI protocol, the system can use high-performance serial Flash memories which are small and inexpensive compared to parallel Flash memories.

Figure 3-29. Octal SPI Flash Schematic

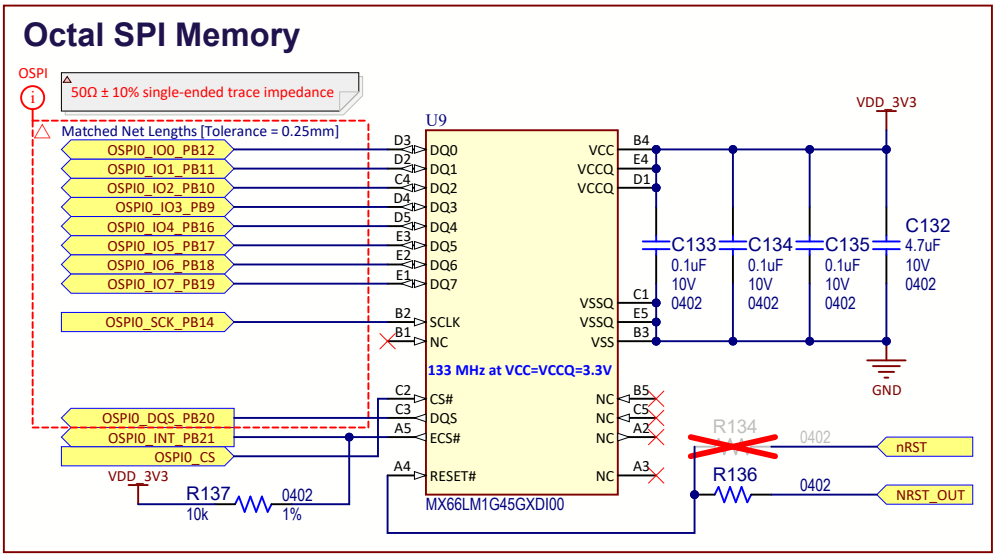


Table 3-15. Octal SPI Flash Signal Description

PIO	Signal Name	Shared PIO	Signal Description
PB9	QSPI0_IO3_PB9	–	QSPI0 I/O line 3
PB10	QSPI0_IO2_PB10	–	QSPI0 I/O line 2
PB11	QSPI0_IO1_PB11	–	QSPI0 I/O line 1
PB12	QSPI0_IO0_PB12	–	QSPI0 I/O line 0
PB13	QSPI0_CS	–	QSPI0 Chip Select
PB14	QSPI0_DDR_CK_P	–	QSPI0 serial clock
PB16	QSPI0_IO4_PB16	–	QSPI0 I/O line 4
PB17	QSPI0_IO5_PB17	–	QSPI0 I/O line 5
PB18	QSPI0_IO6_PB18	–	QSPI0 I/O line 6
PB19	QSPI0_IO7_PB19	–	QSPI0 I/O line 7
PB20	QSPI0_DQS_PB20	–	QSPI00 data strobe
PB21	QSPI0_INT_PB21	–	QSPI0 interrupt
nRST/NRST_OUT	RESET#	–	Reset line from processor or from general reset

3.3.4 Dual Serial EEPROM

The SAMA7G54-EK board embeds two Microchip 24AA025E48 serial Electrically-Erasable Programmable Read-Only Memories (EEPROMs).

The 24AA025E48 features 2048 bits of serial EEPROMs organized as 256 words of eight bits each and is accessed via an I^2C-compatible (2-wire) serial interface. In addition, the 24AA025E48 incorporates an easy and inexpensive method to obtain a globally unique MAC or EUI address (EUI-48). For more information about the 24AA025E48, refer to the product web page.

An EUI-48 address can be assigned as the actual physical address of a system hardware device or node, or it can be assigned to a software instance. Such addresses are factory-programmed by Microchip and unique. They are permanently write-protected in an extended memory block located outside the standard 2-Kbit memory array.

Each EEPROM has a specific I^2C address and is connected to the same TWI bus interface.

- EEPROM1 (U12) I²C address: 1010_010[R/W]
- EEPROM2 (U13) I²C address: 1010_011[R/W]

Figure 3-30. Dual Serial EEPROM Schematic

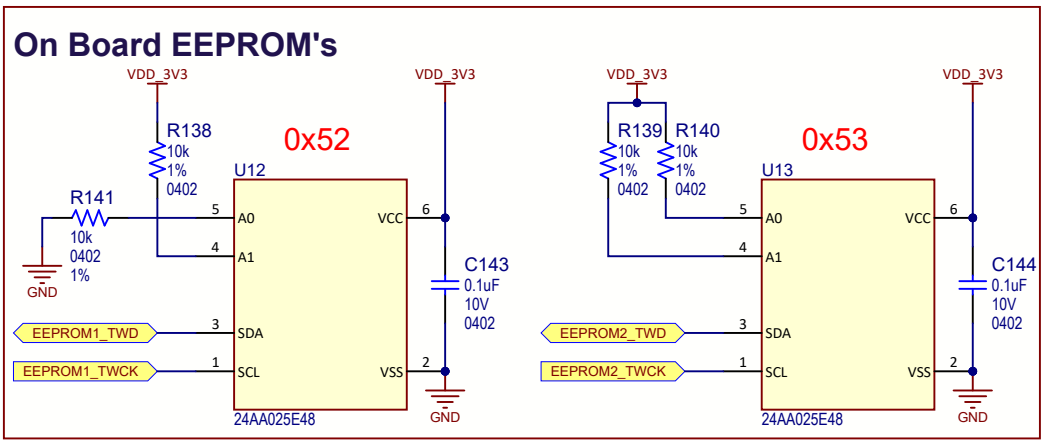


Table 3-16. EEPROM Signal Descriptions

PIO	Signal Name	Shared With	Device Signal Name	Signal Description
PC14	FLEXCOM8_IO0_PC14	ECC608	ECC608_TWD	TWI data line
		CAM	CAM_TWD	
		EEPROM1	EEPROM1_TWD	
		EEPROM2	EEPROM2_TWD	
PC13	FLEXCOM8_IO1_PC13	ECC608	ECC608_TWCK	TWI clock line
		CAM	CAM_TWCK	
		EEPROM1	EEPROM1_TWCK	
		EEPROM2	EEPROM2_TWCK	

Table 3-17. 24AA025E48 TWI Addresses

Device	7-bit Client Address	Full Address with RD/WR#
24AA025E48 TWI Read (U12)	1010_010	0xA5
24AA025E48 TWI Write (U12)		0xA4
24AA025E48 TWI Read (U13)	1010_011	0xA7
24AA025E48 TWI Write (U13)		0xA6

3.4 Peripheral Interfaces

Several interfaces and connectors are implemented in the SAMA7G54-EK to enable the user to test all the features offered by the MPU and to facilitate a reference design for future customer applications.

This section describes the following peripherals mounted on the SAMA7G54-EK board:

- Ethernet 10/100 interface
- Gigabit Ethernet interface
- USBA host/device
- USBB host interface
- USBC host interface
- Dual mikroBUS Click interfaces
- Dual CAN interfaces

- RPi connector Interface
- RPi CSI camera interface
- S/PDIF RX/TX interfaces
- Quad MEMS microphones
- Wi-Fi/Bluetooth module (optional)
- Secure Digital Multimedia Card (SDMMC)
- Secure element
- Tamper pins connector

3.4.1 Ethernet Interfaces

3.4.1.1 Ethernet 10/100 Interface

The KSZ8081 is a single-supply 10Base-T/100Base-TX Ethernet physical-layer transceiver for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable. The KSZ8081 is a highly-integrated PHY solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low-noise regulator to supply the 1.2V core, and by offering 1.8/2.5/3.3V digital I/O interface support.

The KSZ8081RNA is connected over the Reduced Media Independent Interface (RMII) directly to the RMII-compliant MAC inside the SAMA7G5 MPU. As the power-up default, the KSZ8081RNA uses a 25 MHz MEMS oscillator to generate all required clocks, including the 50-MHz RMII reference clock output for the MAC.

For more information about the KSZ8081RNx, refer to the product web page.

An indiviual unique 48-bit MAC address (Ethernet hardware address) is allocated to this product and is stored in one of the Microchip 24AA025E48 TWI serial EEPROMs described in Dual Serial EEPROM.

Additionally, for monitoring and control purposes, the RJ45 connectors feature a LED functionality to indicate activity, link, and speed status.

Figure 3-31. RMII Ethernet Interface Schematic

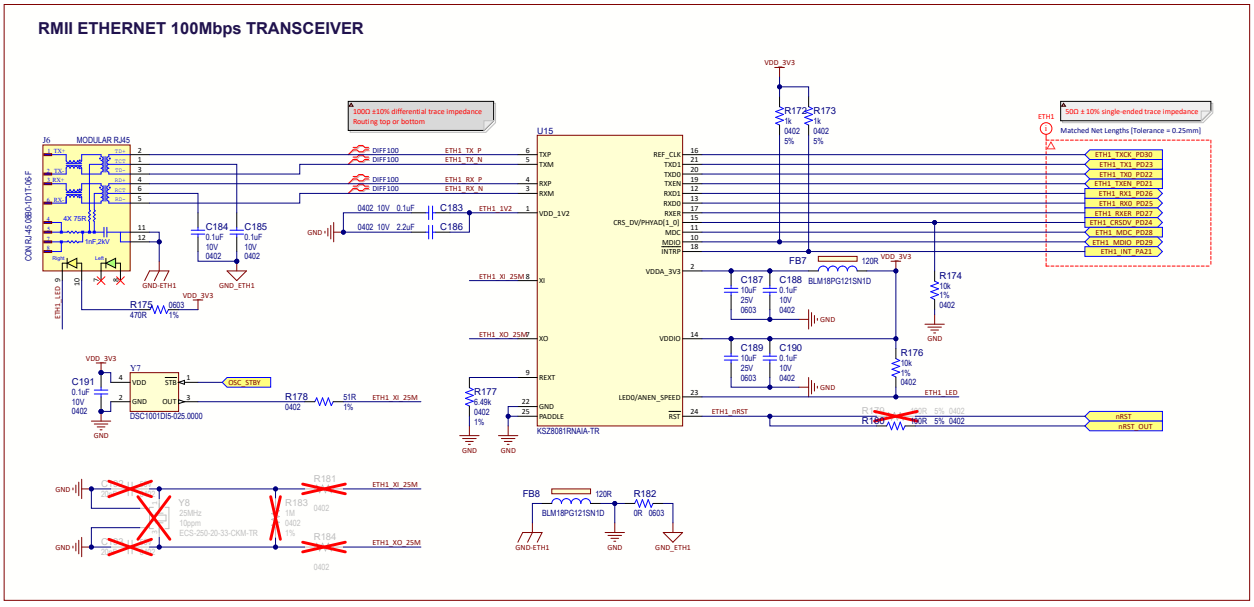


Table 3-18. Ethernet PHY 10/100 Signal Descriptions

PIO	Signal Name	Shared With	Signal Description
PD21	ETH1_TXEN_PD21	RPi 40-pin connector	Transmit enable or RPi connector GPIO
PD22	ETH1_TW1_TW0_PD22	PDM microphone	Transmit data line 0 or PDM clock line
PD23	ETH1_TX1_PD23	PDM microphone	Transmit data line 1 or PDM data line 0
PD24	ETH1_CRSDV_PD24	PDM microphone	Receive data valid or carrier sense and data valid or PDM data line 1
PD25	ETH1_RX0_PD25	RPi 40-pin connector	Receive data line 0 or RPi connector GPIO
PD26	ETH1_RX1_PD26	RPi 40-pin connector	Receive data line 1 or RPi connector GPIO
PD27	ETH1_RXER_PD27	RPi 40-pin connector	Receive error or RPi connector GPIO
PD28	ETH1_MDC_PD28	RPi 40-pin connector	Management data clock or RPi connector GPIO
PD29	ETH1_MDIO_PD29	RPi 40-pin connector	Management data input/output or RPi connector GPIO
PD30	ETH1_TXCK_PD30	RPi 40-pin connector	Transmit clock or 50 MHz reference clock or RPi connector GPIO
PA21	ETH1_INT_PA21	--	Ethernet 1 interrupt

Table 3-19. Ethernet RJ45 Connector J6 Pin Assignment

Pin No.	Signal Name	Signal Description
1	TCT	Decoupling capacitor
2	ETH1_TX_P	Physical transmit or receive signal (+ differential)
3	ETH1_TX_N	Physical transmit or receive signal (- differential)
4	ETH1_RX_P	Physical receive or transmit signal (+ differential)
5	RCT	Decoupling capacitor
6	ETH1_RX_N	Physical receive or transmit signal (- differential)
7	NC	Green LED cathode
8	NC	Green LED anode
9	ETH1_LED	Yellow LED cathode
10	–	Yellow LED anode
11	Earth	Earth ground
12	Earth	Earth ground

3.4.1.2 Gigabit Ethernet Interface

The KSZ9131RNX is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical layer transceiver for transmission and reception of data on standard CAT-5 as well as CAT-5e and CAT-6 unshielded twisted pair (UTP) cables.

The KSZ9131RNX provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet processors and switches for data transfers at 10/100/1000 Mbps.

The KSZ9131RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

The KSZ9131RNX offers diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment.

An individual unique 48-bit MAC address (Ethernet hardware address) is allocated to this product and is stored in one of the Microchip 24AA025E48 TWI serial EEPROMs described in Dual Serial EEPROM.

Additionally, for monitoring and control purposes, the RJ45 connectors feature a LED functionality to indicate activity, link, and speed status.

Figure 3-32. Gigabit Ethernet Interface Schematic

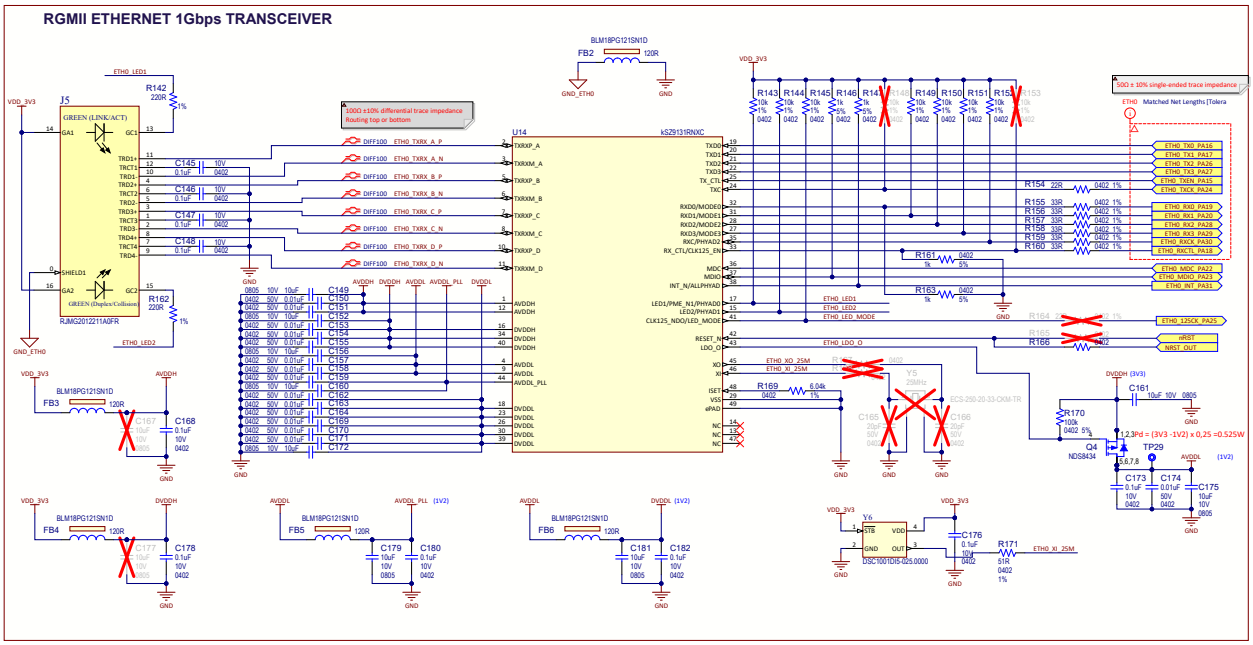


Table 3-20. Gigabit Ethernet Interface Schematic

PIO	Signal Name	Shared With	Signal Description
PA15	ETH0_TXEN_PA15	–	Transmit enable
PA16	ETH0_TX0_PA16	–	Transmit data line 0
PA17	ETH0_TX1_PA17	–	Transmit data line 1
PA18	ETH0_RXCTL_PA18	–	Receive data valid or carrier sense and data valid
PA19	ETH0_RX0_PA19	–	Receive data line 0
PA20	ETH0_RX1_PA20	–	Receive data line 1
PA22	ETH0_MDC_PA22	–	Management data clock
PA23	ETH0_MDIO_PA23	–	Management data input/output
PA24	ETH0_TXCK_PA24	–	Transmit clock or 50 MHz reference clock
PA25	ETH0_125CK_PA25	–	125 MHz clock
PA26	ETH0_TX2_PA26	–	Transmit data line 2
PA27	ETH0_TX3_PA27	–	Transmit data line 3
PA28	ETH0_RX2_PA28	–	Receive data line 2
PA29	ETH0_RX3_PA29	–	Receive data line 3
PA30	ETH0_RXCK_PA30	–	Receive clock
PA31	ETH0_INT_PA31	–	Ethernet 0 interrupt

Table 3-21. Ethernet RJ45 Connector J7 Pin Assignment

Pin No.	Signal Name	Signal Description
0	–	Earth ground
1	–	Digital ground
2	ETH0_TXRX_D_N	Media Dependent Interface[3], negative signal of differential pair
3	ETH0_TXRX_D_P	Media Dependent Interface[3], positive signal of differential pair
4	ETH0_TXRX_C_N	Media Dependent Interface[2], negative signal of differential pair
5	ETH0_TXRX_C_P	Media Dependent Interface[2], positive signal of differential pair
6	ETH0_TXRX_B_N	Media Dependent Interface[1], negative signal of differential pair

.....continued		
Pin No.	**Signal Name**	**Signal Description**
7	ETH0_TXRX_B_P	Media Dependent Interface[1], positive signal of differential pair
8	ETH0_TXRX_A_N	Media Dependent Interface[0], negative signal of differential pair
9	ETH0_TXRX_A_P	Media Dependent Interface[0], positive signal of differential pair
10	–	–
11	–	Green LED anode
12	–	Green LED cathode
13	–	Yellow LED anode
14	–	Yellow LED cathode

3.4.2 USB Interfaces

The USB (Universal Serial Bus) is a hot-pluggable general-purpose high-speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 specification defines data transfer rates as high as 480 Mbps ("high-speed USB"). A USB host bus connector uses four pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin.

The SAMA7G54-EK board features three USB communication ports named USBA, USBB and USBC.

3.4.2.1 USBA Host/Device

The USBA port can act as a USB device or USB host interface and can be accessed via the USB micro-B connector (J7).

Two resistors (R186 and R188) are placed on its power rail to form a voltage divider, converting 5V into 3.3V voltage that is then used to indicate the presence of a USB host to the MPU (USBA_VBUSDETECT_PD11).

In the case of board bring-up, USBA is the default port used to connect to the MPU over SAM-BA (SAM Boot Assistance). For more information, refer to the product web page.

The USBA port is also used as a secondary power source, as described in Power Supply Topology and Power Distribution. In most cases, this port is limited to 500 mA.

Figure 3-33. USBA Port Schematic

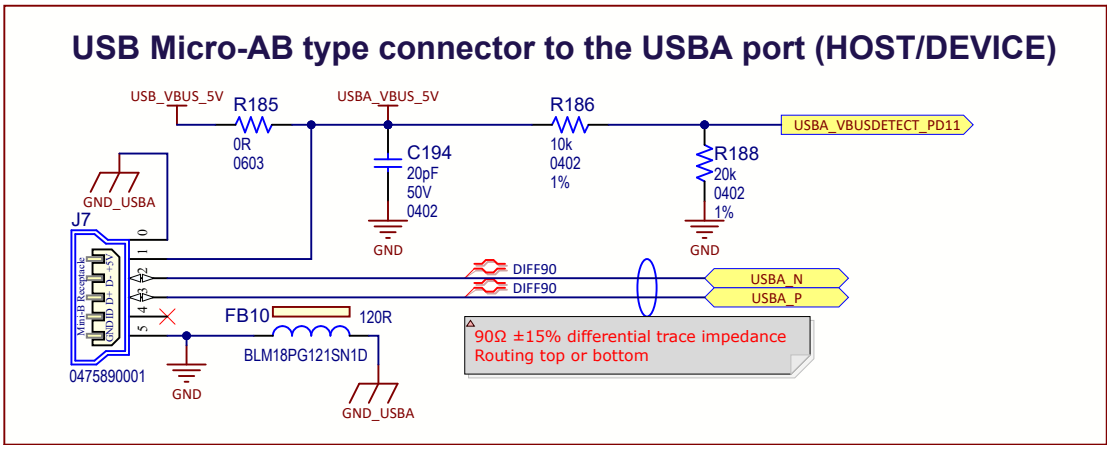


Table 3-22. USBA J7 Connector Signal Descriptions

Pin No.	Signal Name	Signal Description
1	USBA_VBUS_5V	First port 5V power
2	USBA_N	First port data minus

.....continued		
Pin No.	**Signal Name**	**Signal Description**
3	USBA_P	First port data plus
4	ID	– (not used)
5	GND	First port ground

Table 3-23. USBA PIO Signal Description

PIO	Signal Name	Shared	Signal Description
PD11	USBA_VBUSDETECT_PD11	–	VBUS detection

In Host mode, the USB host port A is equipped with 500-mA high-side power switches to enable self-powered and bus-powered applications. The USBA_EN_5V_PB2 signal controls the current limiting power switch MIC2025, which in turn supplies power to a client device. As per the USB specification, bus-powered USB 2.0 devices are limited to a maximum of 500 mA, therefore the MIC2025 limits the current and reports an overcurrent with the USBA_OVCUR_PC7 signal. For more information about the MIC2025, refer to the product web page.

Figure 3-34. USBA Port Power Switch Schematic

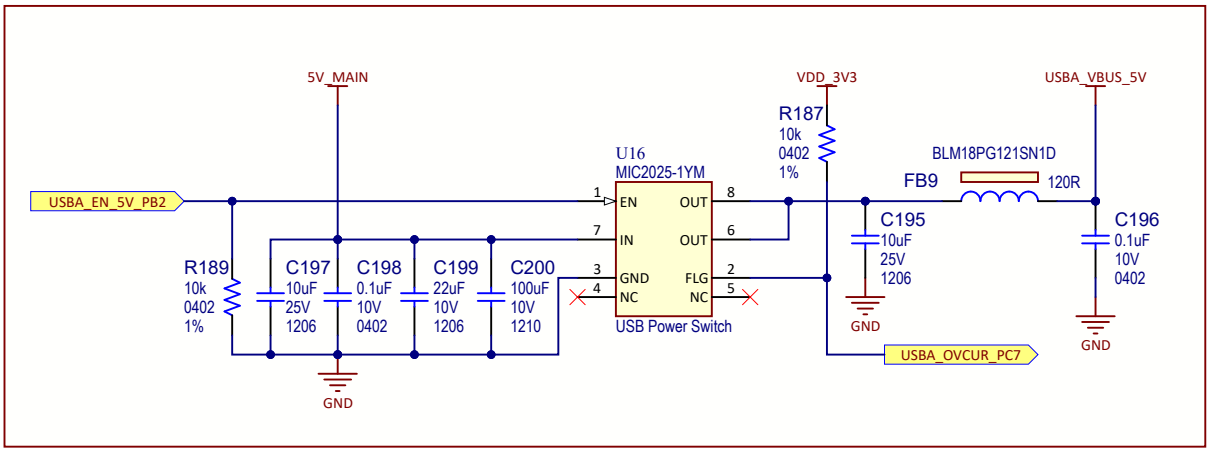


Table 3-24. USBA Power Switch PIO Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PB2	USBA_EN_5V_PB2	–	Power switch enable (active high)
PC7	USBA_OVCUR_PC7	–	Indicates overcurrent (open drain)

3.4.2.2 USBB Host Interface

The USBB port can act as a USB device or USB host interface and can be accessed via the USB Type-C connector (J8).

Two resistors (R192 and R193) are placed on its power rail to form a voltage divider, converting 5V into 3.3V voltage that is then used to indicate the presence of a USB host to the MPU (USBB_VBUSDETECT_PC12).

Figure 3-35. USB-B Port Schematic

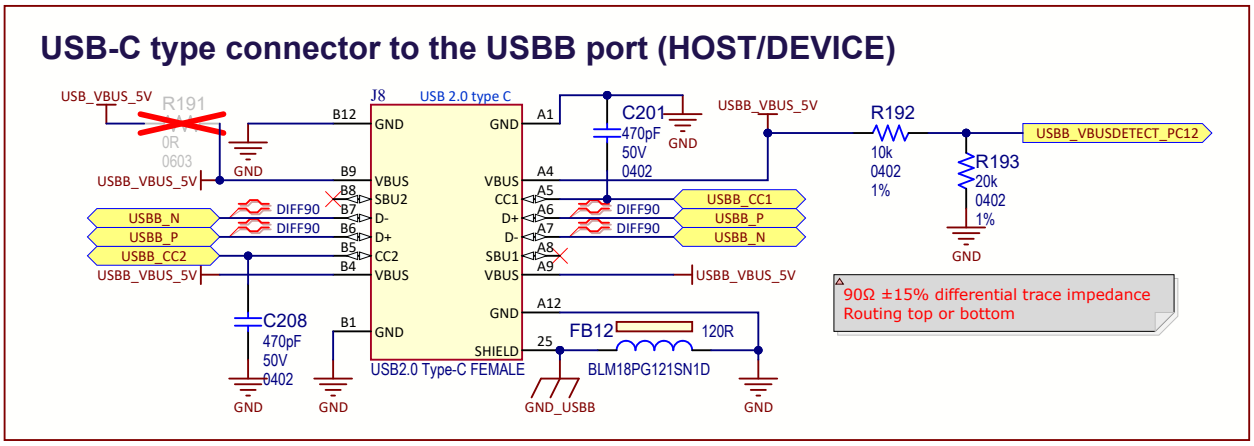


Table 3-25. USB-B J8 Connector Signal Descriptions

Signal Description	Signal Name	Pad Name	Pin No.	Pin No.	Pad Name	Signal Name	Signal Description
Ground	GND	GND	A1	B1	GND	GND	Ground
Not used	Not connected	TX1+	A2	B2	TX2+	Not connected	Not used
Not used	Not connected	TX1-	A3	B3	TX2-	Not connected	Not used
Port-B 5V power	USBB_VBUS_5V	VBUS	A4	B4	VBUS	USBB_VBUS_5V	Port-B 5V power
Sideband use	USBB_CC1	CC1	A5	B5	CC2	USBB_CC2	Configuration channel
Port-B data plus	USBB_P	D+	A6	B6	D+	USBB_P	Port-B data plus
Port-B data minus	USBB_N	D-	A7	B7	D-	USBB_N	Port-B data minus
Not used	SBU1	SBU1	A8	B8	SBU2	SBU2	Not used
Port-B 5V power	USBB_VBUS_5V	VBUS	A9	B9	VBUS	USBB_VBUS_5V	Port-B 5V power
Not used	Not connected	RX2-	A10	B10	RX1-	Not connected	Not used
Not used	Not connected	RX2+	A11	B11	RX1+	Not connected	Not used
Ground	GND	GND	A12	B12	GND	GND	Ground

Table 3-26. USB-B PIO Signal Description

PIO	Signal Name	Shared	Signal Description
PC12	USBB_VBUSDETECT_PC12	–	VBUS detection

In Host mode, the USB Host port B is equipped with 500-mA high-side power switches to enable self-powered and bus-powered applications. The USBB_EN_5V_PC11 signal controls the current limiting power switch MIC2025, which in turn supplies power to a client device. As per the USB specification, bus-powered USB 2.0 devices are limited to a maximum of 500 mA, therefore the MIC2025 limits the current and indicates an overcurrent with the USBB_OVCUR_PC22 signal.

Figure 3-36. USB-B Port Power Switch Schematic

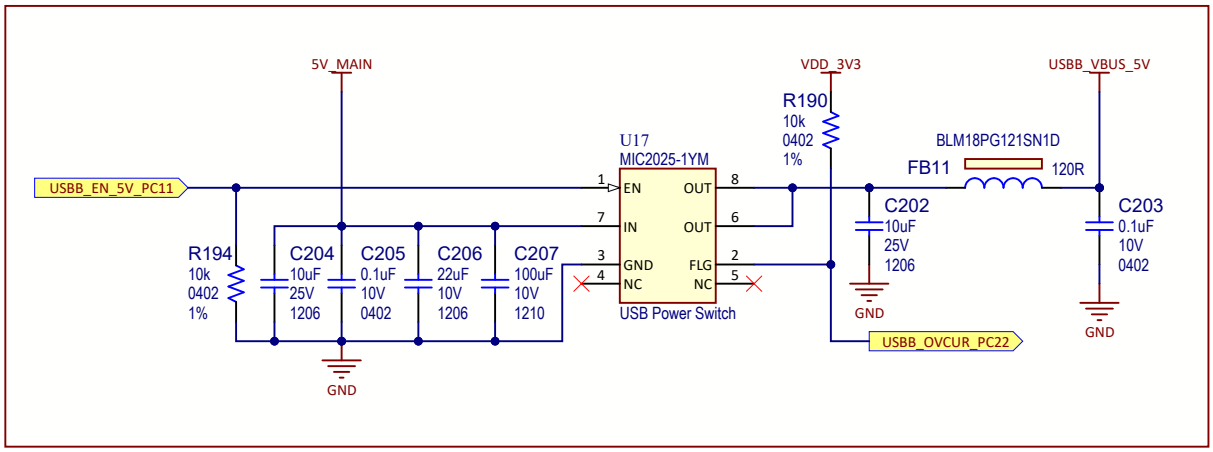


Table 3-27. USB-B Power Switch PIO Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PC11	USBB_EN_5V_PC11	–	Power switch enable (active high)
PC22	USBB_OVCUR_PC22	–	Indicates overcurrent (open drain)

3.4.2.3 USBC Host Interface

The USBC port can act as a USB device only and can be accessed via the USB Type-A connector (J9).

Figure 3-37. USBC Port Schematic

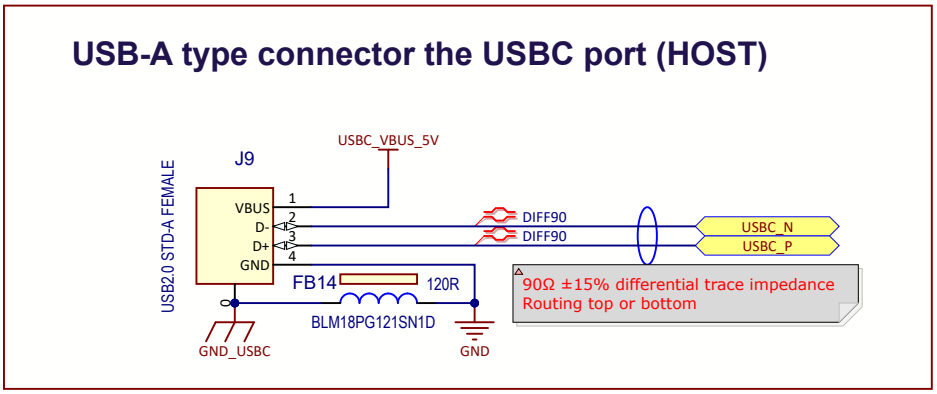


Table 3-28. USBC J9 Connector Signal Descriptions

Pin No.	Signal Name	Signal Description
1	USBA_VBUS_5V	First port 5V power
2	USBA_N	First port data minus
3	USBA_P	First port data plus
4	GND	First port ground

In Host mode, the USB host port C is equipped with 500-mA high-side power switches to enable self-powered and bus-powered applications. The USBC_EN_5V_PC6 signal controls the current limiting power switch MIC2025, which in turn supplies power to a client device. As per the USB specification, bus-powered USB 2.0 devices are limited to a maximum of 500 mA, therefore the MIC2025 limits the current and indicates an overcurrent with the USBC_OVCUR_PC17 signal.

Figure 3-38. USBC Port Power Switch Schematic

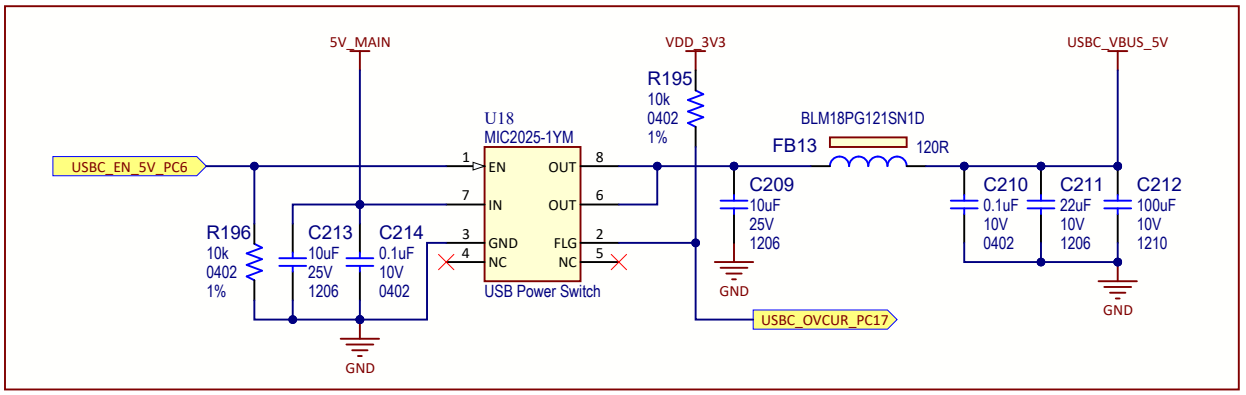


Table 3-29. USBC Power Switch PIO Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PC6	USBC_EN_5V_PC6	–	Power switch enable (active high)
PC17	USBC_OVCUR_PC17	–	Indicates overcurrent (open drain)

3.4.3 Dual mikroBUS Click Interfaces

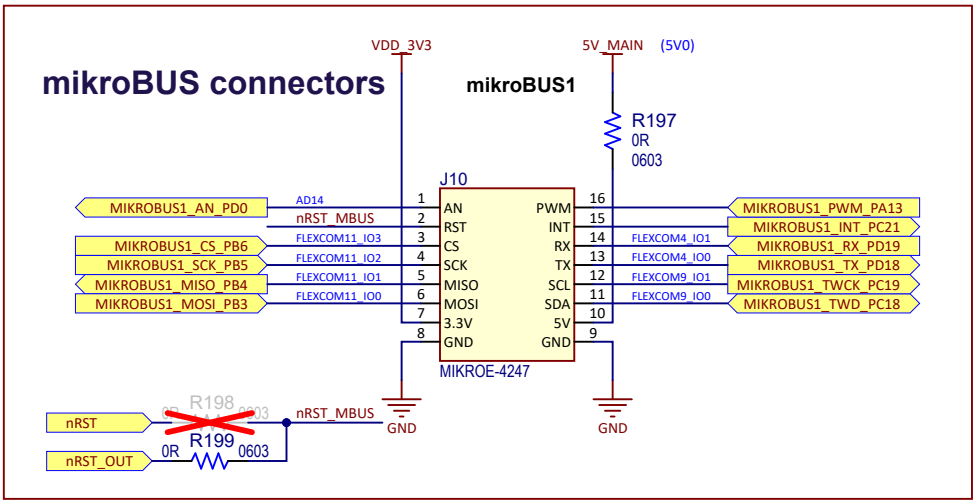
The SAMA7G54-EK hosts two pairs of 8-pin female headers (J10 and J12) implementing the official mikroBUS socket. For details, refer to the mikroBUS documentation on www.mikroe.com/mikrobus.

3.4.3.1 mikroBUS 1 Connector

The first mikroBUS 8-pin female header (J10) implements all mikroBUS features as described in the schematic below.

The reset feature is ensured (by default) by the processor reset line and can be controlled by the general reset line by swapping R198 and R199.

Figure 3-39. mikroBUS 1 Interface



The first mikroBUS interface features an SPI bus shared with the second mikroBUS interface. Each interface has its own Chip Select line to its SPI interface (PB6 for the mikroBUS1 interface). I/Os in common are PB3, PB4 and PB5. That means that the SPI interface cannot be used at the same time on the two mikroBUS interfaces.

The first mikroBUS interface features a two-wire interface (PC18 and PC19) shared with the second mikroBUS interface and with the 40-pin RPi connector. The end user must pay attention to the I²C addresses used on these nodes.

The PWM feature of the first mikroBUS interface (PA13) is shared with the green LED control.

Table 3-30. mikroBUS 1 Connector J10 Pin Assignment

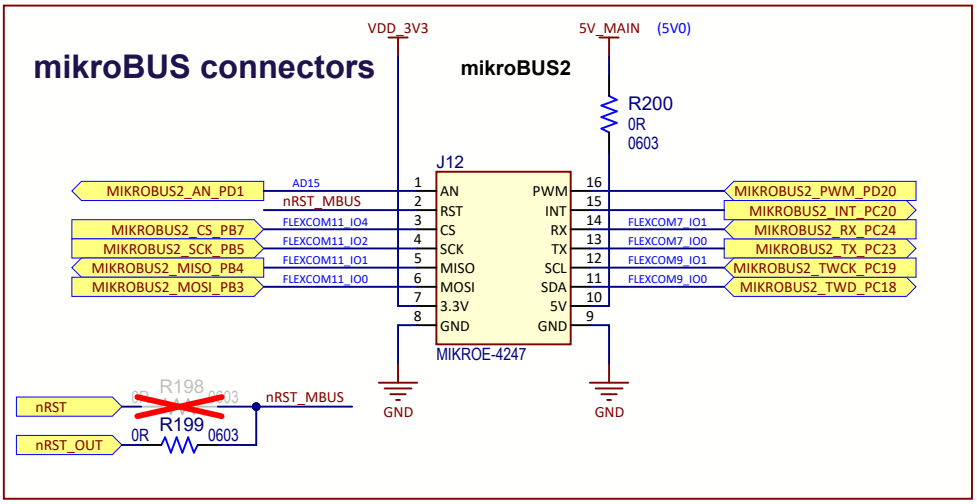
Function	PIO	Mbus Signal	Pin No.	Pin No.	Mbus Signal	PIO	Function
Analog input	PD0	AN	1	16	PWM	PA13	PWM
Reset	nRST_MBUS	RST	2	15	INT	PC21	Interrupt
SPI Chip Select	PB6	SPI_NPCS	3	14	UART_RX	PD19	UART receive (mBUS output to SAM)
SPI Clock	PB5	SPI_SPCK	4	13	UART_TX	PD18	UART transmit (mBUS input from SAM)
SPI MOSI	PB4	SPI_PISO	5	12	TWI_SCL	PC19	TWI clock
SPI MISO	PB3	SPI_MOSI	6	11	TWI_SDA	PC18	TWI data
VCC	–	3.3V supply	7	10	5V supply	–	VDD
GROUND	–	GND	8	9	GND	–	Ground

3.4.3.2 mikroBUS 2 Connector

The second mikroBUS 8-pin female header (J12) implements all mikroBUS features as described in the schematic below.

The reset feature is ensured (by default) by the processor reset line and can be controlled by the general reset line by swapping R198 and R199.

Figure 3-40. mikroBUS 2 Interface



The second mikroBUS interface features an SPI bus shared with the first mikroBUS interface. Each interface has its own Chip Select line to its SPI interface (PB7 for the mikroBUS 2 interface). I/Os in common are PB3, PB4 and PB5. That means that the SPI interface cannot be used at the same time on the two mikroBUS interfaces.

The second mikroBUS interface features a two-wire interface (PC18 and PC19) shared with the first mikroBUS interface and with a 40-pin RPi connector. The end user must take care of the I²C addresses used on this nodes.

The PWM feature of the first mikroBUS interface (PD20) is shared with the blue LED control.

Table 3-31. mikroBUS 2 Connector J12 Pin Assignment

Function	PIO	Mbus Signal	Pin No.	Pin No.	Mbus Signal	PIO	Function
Analog input	PD1	AN	1	16	PWM	PD20	PWM
Reset	nRST_MBUS	RST	2	15	INT	PC20	Interrupt
SPI Chip Select	PB7	SPI_NPCS	3	14	UART_RX	PC24	UART receive (Mbus output to SAM)
SPI clock	PB5	SPI_SPCK	4	13	UART_TX	PC23	UART transmit (Mbus input from SAM)
SPI MOSI	PB4	SPI_PISO	5	12	TWI_SCL	PC19	TWI clock
SPI MISO	PB3	SPI_MOSI	6	11	TWI_SDA	PC18	TWI data
VCC	--	3.3V supply	7	10	5V supply	–	VDD
GROUND	--	GND	8	9	GND	–	Ground

3.4.4 Dual CAN Interfaces

The SAMA7G54-EK features two MCP2542FD transceivers.

The MCP2542FD is a high-speed CAN transceiver that provides the interface between the Controller Area Network (CAN) protocol controller and the physical two-wire bus. For more information about the MCP2542FD, refer to the product web page.

Figure 3-41. Dual CAN Interfaces

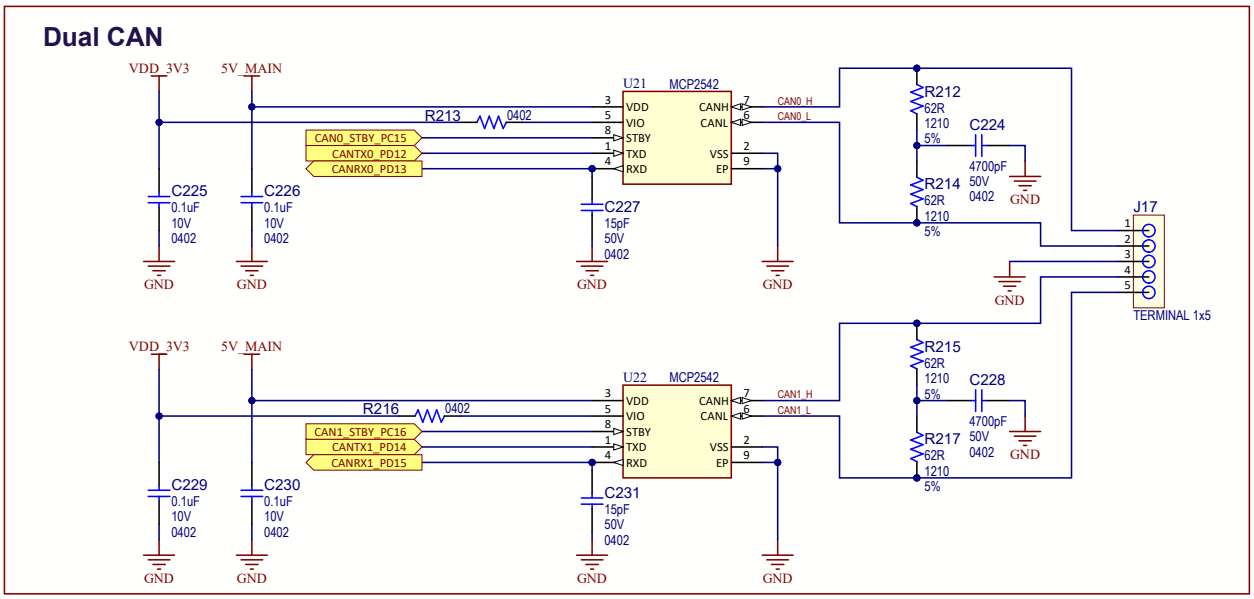


Table 3-32. CAN Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PD12	CANTX0_PD12	–	CAN transmit port 0
PD13	CANRX_PD13	–	CAN receive port 0
PC15	CAN0_STBY_PC15	–	CAN standby port 0
PD14	CANTX1_PD14	–	CAN transmit port 1
PD15	CANRX1_PD15	–	CAN receive port 1
PC16	CAN1_STBY_PC16	–	CAN standby port 1

Table 3-33. CAN Connector J17 Signal Descriptions

Pin No.	Signal Name	Signal Description
1	CAN0_H	Differential positive port 0
2	CAN0_L	Differential negative port 0

.....continued		
Pin No.	**Signal Name**	**Signal Description**
3	GND	Common ground
4	CAN1_H	Differential positive port 1
5	CAN1_L	Differential negative port 1

3.4.5 RPi Connector Interface

The SAMA7G54-EK board features a 40-pin connector (Raspberry Pi compatible) for free use.

Figure 3-42. RPi 40-Pin Connector Schematic

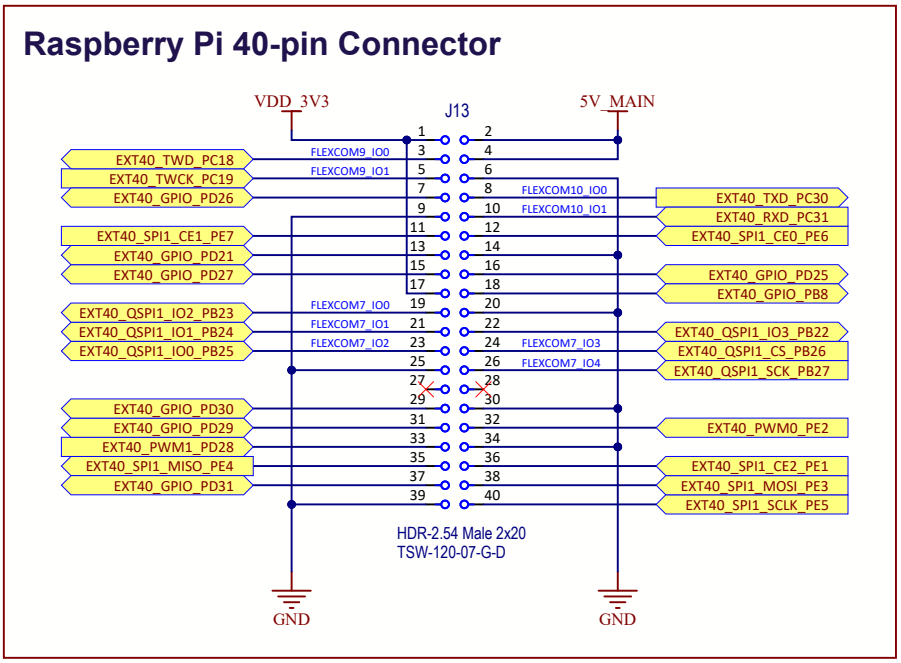


Table 3-34. RPi Connector Pin Assignment

Pin No.	RPi Signal	Signal Name	Shared With	PIO	Function
1	3.3V power	VDD_3V3	–	–	3.3V power supply
2	5V power	5V_MAIN	–	–	5.0V power supply
3	GPIO 2 (SDA)	EXT40_TWD_PC18	mBUS1, mBUS2	PC18[3]	I²C data line
4	5V power	5V_MAIN	–	–	5.0V power supply
5	GPIO 3 (SCL)	EXT40_TWCK_PC19	mBUS1, mBUS2	PC19[3]	I²C clock line
6	Ground	GND	–	–	Ground
7	GPIO 4 (GPCLK0)	EXT_GPIO_PD26	10/100 Ethernet	PD26[2]	GPIO clock
8	GPIO 14 (TXD)	EXT40_TXD_PC30	–	PC30	UART TXD
9	Ground	GND	–	–	Ground
10	GPIO 15 (RXD)	EXT40_RXD_PC31	–	PC31	UART RXD
11	GPIO 17	EXT40_SPI1_CE1_PE7	USART WILC3000	PE7[1]	GPIO standard
12	GPIO 18 (PCM_CLK)	EXT_SPI1_CE0_PE6	USART WILC3000	PE6[1]	GPIO standard PWM
13	GPIO 27	EXT_GPIO_PD21	10/100 Ethernet	PD21[2]	GPIO standard
14	Ground	GND	–	–	Ground
15	GPIO 22	EXT_GPIO_PD27	10/100 Ethernet	PD27[2]	GPIO standard
16	GPIO 23	EXT40_GPIO_PD25	10/100 Ethernet	PD25[2]	GPIO standard
17	3.3V power	VDD_3V3	–	–	3.3V power supply

.....continued					
Pin No.	RPi Signal	Signal Name	Shared With	PIO	Function
18	GPIO 24	EXT_GPIO_PB8	Red LED	PB8	GPIO standard
19	GPIO 10 (MOSI)	EXT40_QSPI1_IO2_PB23	–	PB23	SPI MOSI
20	Ground	GND	–	–	Ground
21	GPIO 9 (MISO)	EXT40_QSPI1_IO1_PB24	–	PB24	SPI MISO
22	GPIO 25	EXT40_QSPI1_IO3_PB22	–	PB22	GPIO standard
23	GPIO 11 (SCLK)	EXT40_QSPI1_IO0_PB25	–	PB25	SPI clock
24	GPIO 8 (CE0)	EXT40_QSPI1_CS_PB26	–	PB26	SPI Chip Select 0
25	Ground	GND	–	–	Ground
26	GPIO 7 (CE1)	EXT40_QSPI1_SCK_PB27	–	PB27	SPI Chip Select 1
27	GPIO 0 (ID_SD)	–	–	NC	I²C ID EEPROM data line
28	GPIO 1 (ID_SC)	–	–	NC	I²C ID EEPROM clock line
29	GPIO 5	EXT40_GPIO_PD30	10/100 Ethernet	PD30[2]	GPIO standard "clock"
30	Ground	GND	–	–	Ground
31	GPIO 6	EXT40_GPIO_PD29	10/100 Ethernet	PD29[2]	GPIO standard "clock"
32	GPIO 12 (PWM0)	EXT40_PWM0_PE2	MIPI CSI camera	PE2	GPIO standard PWM
33	GPIO 13 (PWM1)	EXT40_PWM1_PD28	10/100 Ethernet	PD28[2]	GPIO standard PWM
34	Ground	GND	–	–	Ground
35	GPIO 19 (PCM_FS)	EXT40_SPI1_MISO_PE4	USART WILC3000	PE4[1]	GPIO standard SPI MISO
36	GPIO 16	EXT40_SPI1_CE2_PE1	MIPI CSI camera	PE1	GPIO standard
37	GPIO 26	EXT40_GPIO_PD31	–	PD31	GPIO standard
38	GPIO 20 (PCM_DIN)	EXT40_SPI1_MOSI_PE3	USART WILC3000	PE3[1]	GPIO standard SPI MOSI
39	Ground	GND	–	–	Ground
40	GPIO 21 (PCM_DOUT)	EXT40_SPI1_SCLK_PE5	–	PE5	GPIO standard SPI CLK

Notes:

1. These I/Os are shared with the USART of the (optional) WILC3000 module for its Bluetooth functionality. The two interfaces cannot work together and the user should pay particular attention to impedance adaptation on each node. The series resistor can be removed to improve behavior.
2. These I/Os are shared with the GMAC interface of the KSZ8081 (Ethernet 10/100) interface. The user should pay particular attention to impedance adaptation on each node. The series resistor can be removed to improve behavior.
3. This interface is shared with the mikroBUS1 and mikroBUS2 interfaces. The end user must pay attention to the I²C addresses used on these nodes.

3.4.6 RPi CSI Camera Interface

The SAMA7G54-EK board features a MIPI CSI camera connector (Raspberry Pi compatible).

Figure 3-43. RPi MIPI CSI Connector Schematic

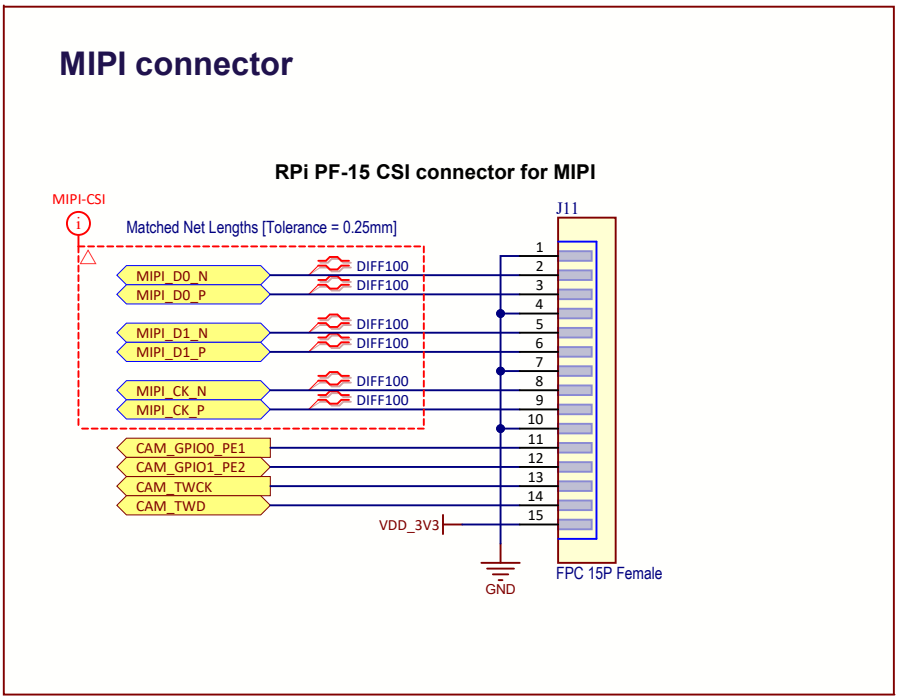


Table 3-35. RPi CSI Connector Pin Assignment

Pin No.	RPi Signal	Signal Name	Shared With	PIO	Function
1	GND	GND	–	–	Ground
2	CAM_DO_N	MIPI_D0_N	–	MIPI_DN0	MIPI DPHY negative differential input data lane 0
3	CAM_DO_P	MIPI_D0_P	–	MIPI_DP0	MIPI DPHY positive differential input data lane 0
4	GND	GND	–	–	Ground
5	CAM_D1_N	MIPI_D1_N	–	MIPI_DN1	MIPI DPHY negative differential input data lane 1
6	CAM_D1_P	MIPI_D1_P	–	MIPI_DP1	MIPI DPHY positive differential input data lane 1
7	GND	GND	–	–	Ground
8	CAM_CK_N	MIPI_CK_N	–	MIPI_CLKN	MIPI DPHY negative differential input clock lane
9	CAM_CK_P	MIPI_CK_P	–	MIPI_CLKP	MIPI DPHY positive differential input clock lane
10	GND	GND	–	–	Ground
11	CAM_IO0	CAM_GPIO0_PE1	RPi 40-pin connector	PE1	MIPI CSI power enable
12	CAM_IO1	CAM_GPIO1_PE2	RPi 40-pin connector	PE2	MIPI CSI LED indicator
13	CAM_SCL	CAM_TWCK	ECC608B	PC13	TWI clock line
14	CAM_SDA	CAM_TWD	ECC608B	PC14	TWI data line
15	CAM_3V3	VDD_3V3	–	–	3.3V power supply

3.4.7 S/PDIF RX/TX Interfaces

The SAMA7G54-EK board features S/PDIF TX/RX interfaces.

S/PDIF (Sony/Philips Digital Interface) is a type of digital audio interconnect used to output audio. The signal is transmitted over a fiber optic cable with TOSLINK connectors.

The SAMA7G54-EK embeds the following:

- Connector J19 for data transmit
- Connector J18 for data receive

Figure 3-44. SPDIF Interface Schematic

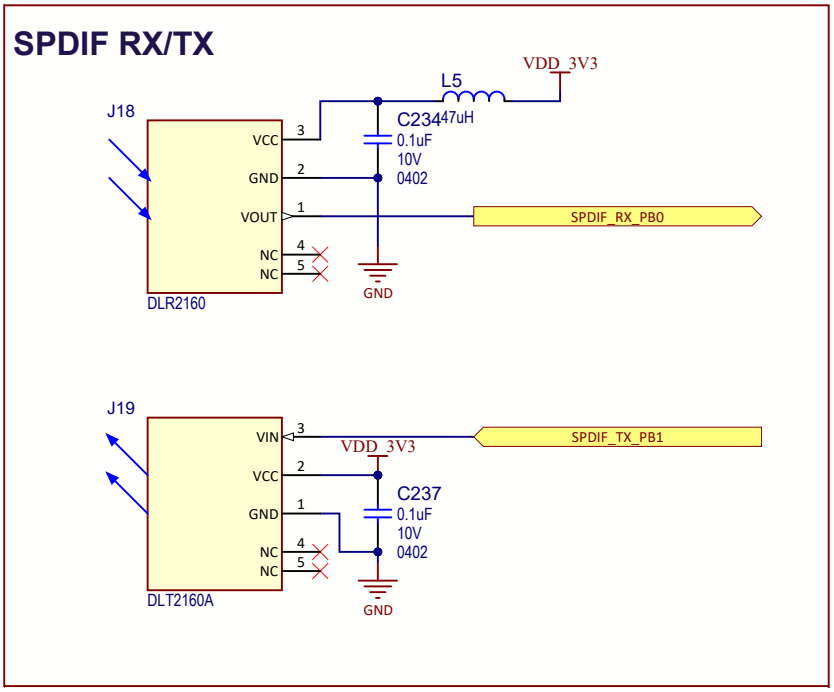


Table 3-36. S/PDIF Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PB0	SPDIF_RX_PB0	–	S/PDIF receive data
PB1	SPDIF_TX_PB1	–	S/PDIF transmit data

3.4.8 Quad MEMS Microphones

The SAMA7G54-EK embeds four digital MEMS microphones SPK0641HT4H-1.

Those microphones convert acoustic pressure waves into a digital signal. This signal is acquired by the SAMA7G5 MPU through a PDMIC interface as shown in the following schematic.

Figure 3-45. QUAD MEMS Microphones Schematic

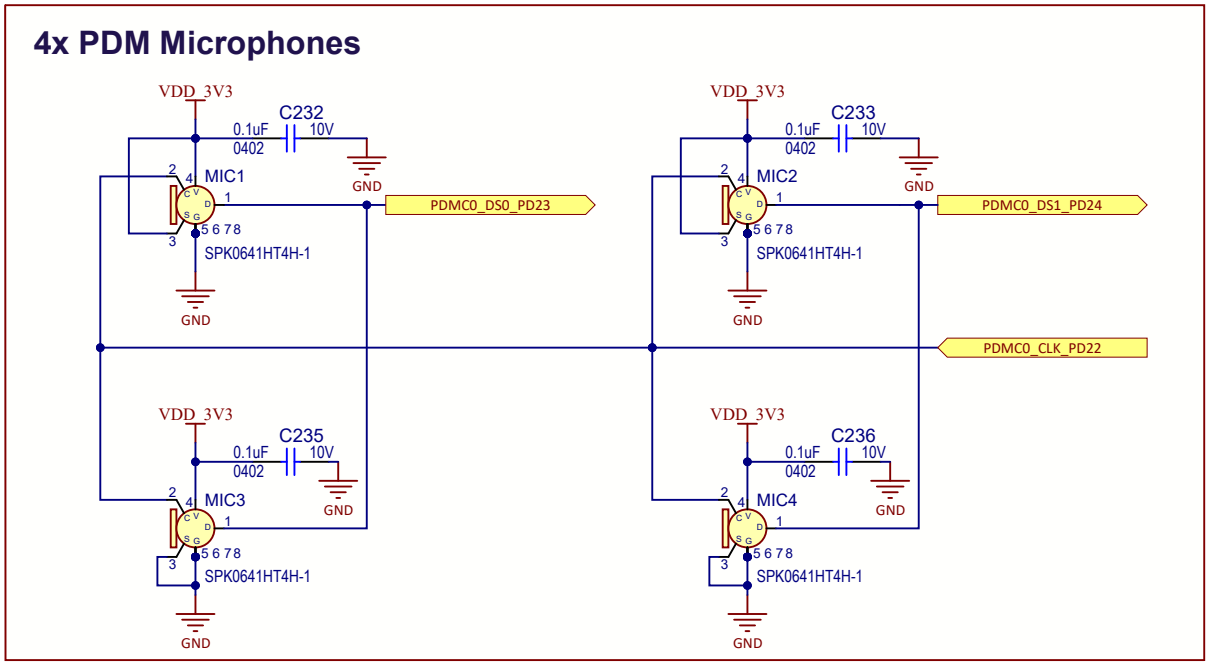


Table 3-37. Digital MEMS Signal Descriptions

PIO	Signal Name	Shared With	Signal Description
PD22	PDMC0_CLK_PD22	Ethernet 10/100	PDM clock line for all microphones
PD23	PDMC0_DS0_PD23	Ethernet 10/100	PDM data line 0 (data from MIC1 and MIC2)
PD24	PDMC0_DS1_PD24	Ethernet 10/100	PDM data line 1 (data from MIC3 and MIC4)

Note: To activate the PDM interface, place the jumper JP2 on the connector J3 as defined in GPIO Distribution. In this mode, the Ethernet 10/100 interface is not accessible.

3.4.9 Wi-Fi/Bluetooth Module (Optional)

The user has the option to solder an ATWILC3000-MR110CA Wi-Fi/BT module with a chip antenna or an ATWILC3000-MR110UA Wi-Fi/BT module with a U.FL connector.

The ATWILC3000-MR110PA WLAN PHY is designed to achieve a reliable and power-efficient physical layer communication as specified by IEEE® 802.11 b/g/n in Single Stream mode with a 20-MHz bandwidth. Advanced algorithms are used to achieve maximum throughput in a real-world communication environment with impairments and interference. The PHY implements all required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as automatic gain control. The module is available in a fully certified, 22.428 x 17.732 mm, 36-pin module package. For more information about the ATWILC3000, refer to the product web page.

Figure 3-46. Wi-Fi/Bluetooth Interface Schematic

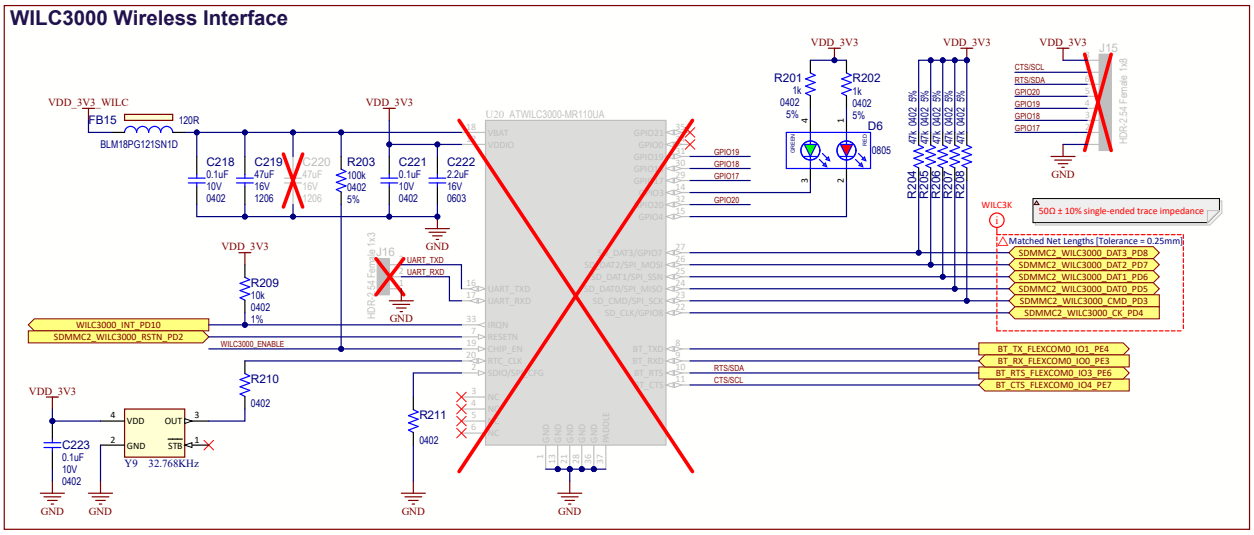


Table 3-38. Wi-Fi/Bluetooth Signal Descriptions

PIO	Signal Name	Shared	Signal Description
PD5	SDMMC2_WILC3000_DAT0_PD5	–	SDIO data
PD6	SDMMC2_WILC3000_DAT1_PD6	–	SDIO data
PD7	SDMMC2_WILC3000_DAT2_PD7	–	SDIO data
PD8	SDMMC2_WILC3000_DAT3_PD8	–	SDIO data
PD3	SDMMC2_WILC3000_CMD_PD3	–	SDIO command
PD4	SDMMC2_WILC3000_CK_PD4	–	SDIO clock
PE4	BT_TX_FLEXCOM0_IO1_PE4	40-pin RPi connector	Bluetooth serial TX (RX into SAMA7G5)
PE3	BT_RX_FLEXCOM0_IO0_PE3	40-pin RPi connector	Bluetooth serial RX (TX from SAMA7G5)
PE6	BT_RTS_FLEXCOM0_IO3_PE6	40-pin RPi connector	Bluetooth serial RTS
PE7	BT_CTS_FLEXCOM0_IO4_PE7	40-pin RPi connector	Bluetooth serial CTS
PD2	SDMMC2_WILC3000_RSTN_PD2	–	Module reset
PD10	WILC3000_INT_PD10	–	Interrupt
PE0	WILC3000_EN_PE0	–	Chip enable

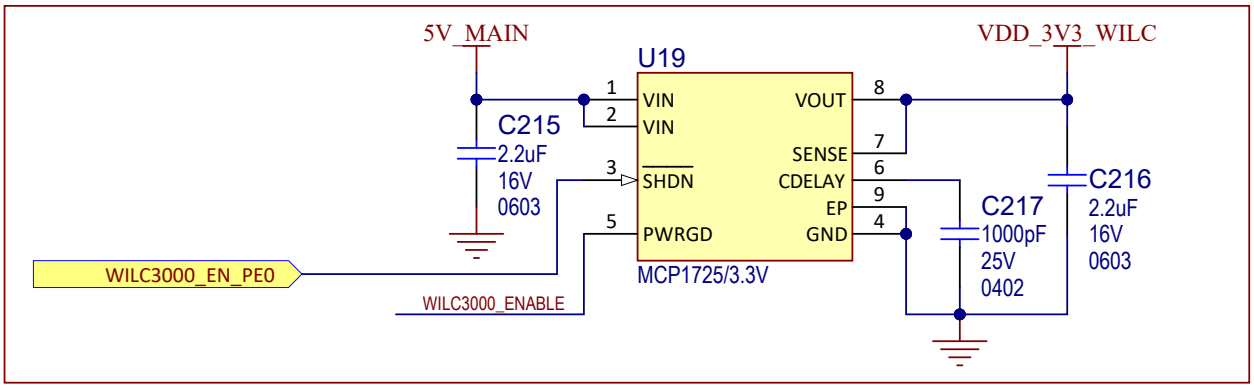
Special care must be taken when powering the ATWILC3000 wireless module. Due to the nature of the wireless transmission, the module draws much current from its supply rail. In the worst-case scenario, the module can draw up to 300 mA.

To address this power consumption, the module is fitted with its own separate power supply, the MCP1725, which is a 500-mA low dropout (LDO) linear regulator that provides high current and low output voltages in a very small package. For more information about the MCP1725, refer to the product web page.

The MCP1725 was chosen because it can supply the current required by the module, and because it features a shutdown input pin (SHDN) and a power good output pin (PWRGD):

- The SHDN input allows to shut down the wireless module when unused, therefore saving power.
- The PWRGD output ensures that the ATWILC3000 wireless module is kept in reset until its power rails are stable.

Figure 3-47. Wi-Fi/Bluetooth Enable Schematic



Note: When the ATWILC3000 module is enabled, the Flexcom SPI cannot be used with the RPi 40-pin connector.

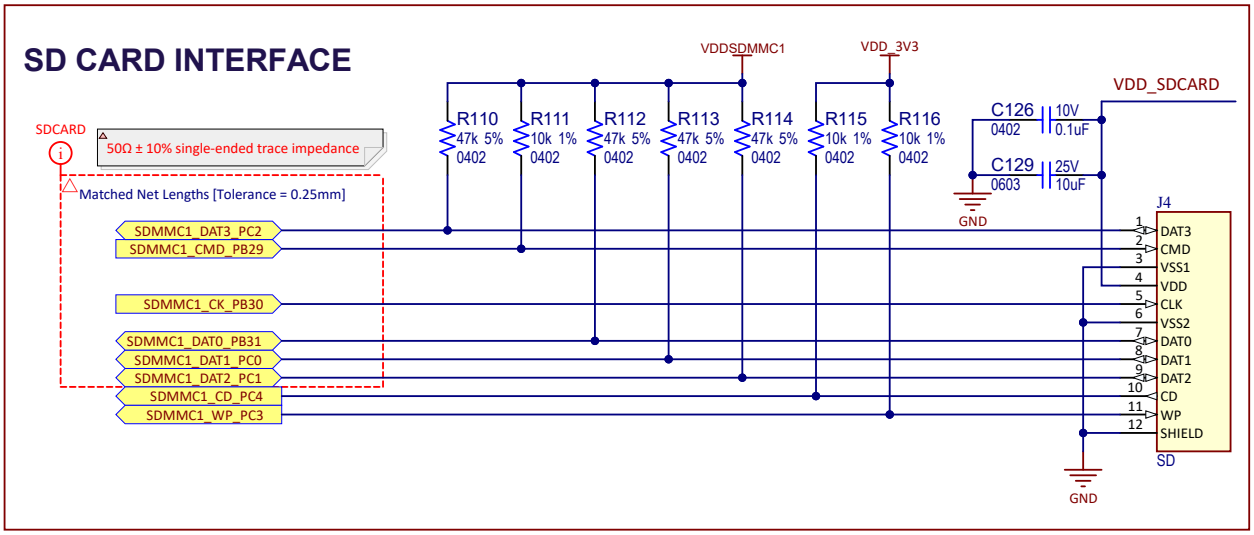
3.4.10 Secure Digital Multimedia Card

The SD (Secure Digital) Card is a non-volatile memory card format used as a mass storage memory in mobile devices.

The SAMA7G54-EK has one Secure Digital Multimedia Card (SDMMC) interface that supports the MultiMedia Card (e.MMC) specification V4.51, the SD Memory Card specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 specification.

A standard MMC/SD Card connector, connected to the SDMMC interface, is mounted on the top side of the board. The SDMMC0 communication is based on an 8-pin interface (clock, command, four data and power lines). It includes a card detection switch.

Figure 3-48. SD Card Interface Schematic



The table below describes the pin assignment of SD/MMC connector J4.

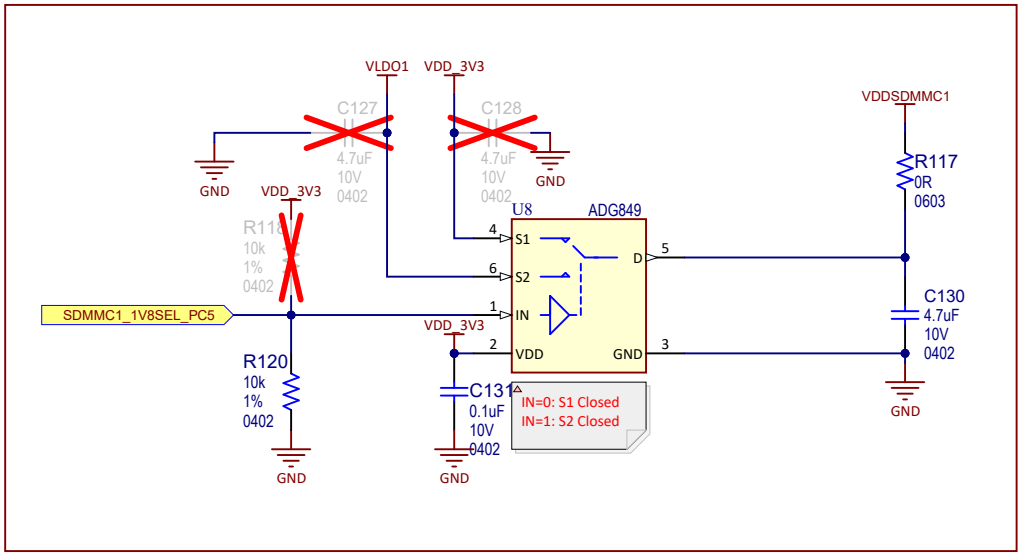
Table 3-39. Standard SD Socket J4 Pin Assignment Signal Descriptions

Function	Pin	PIO	Signal Description
SD Card data line 3	1	PC2	SDMMC1_DAT3_PC2
SD Card command line	2	PB29	SDMMC1_CMD_PB29

.....continued			
Function	**Pin**	**PIO**	**Signal Description**
Ground	3	–	Ground
3.3V SD Card supply	4	–	VDD_SDCARD (3.3V)
SD Card clock line	5	PB30	SDMMC1_CK_PB30
Ground	6	–	Ground
SD Card data line 0	7	PB31	SDMMC1_DAT0_PB31
SD Card data line 1	8	PC0	SDMMC1_DAT1_PC0
SD Card data line 1	9	PC1	SDMMC1_DAT2_PC1
SD Card card detect	10	PC4	SDMMC1_CD_PC4
SD Card write protect	11	PC3	SDMMC1_WP_PC3
Ground	12	–	Ground

SDMMC data and control lines can be 3.3V or 1.8V, depending on the SD Card speed. A power voltage selector is implemented and controlled by pin PC5 of the MPU. The voltage selected by default is 3.3V.

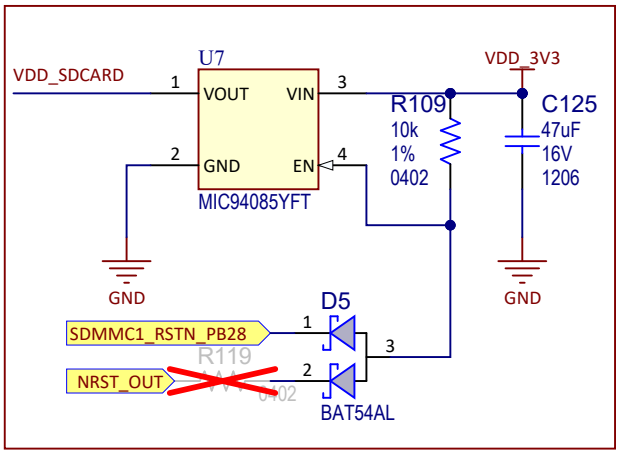
Figure 3-49. SD Card Power Selector Schematic



The user can perform a hard reset of the SD Card by forcing the PB28 PIO of the SAMA7G5 device or by using the processor reset line (R262 must be populated) "NRST_OUT" signal.

This action disables the MIC94085YFT power switch and VDD_SDCARD is forced to ground. For more details about the MIC94085YFT power switch, refer to the product web page.

Figure 3-50. SD Card Reset Schematic



The table below describes the pin assignment of the SD/MMC interface.

Table 3-40. SD/MMC Pin Assignment

PIO	Signal Name	Shared With	Signal Description
PB28	SDMMC1_RSTN_PB28	–	SD Card reset signal
PB29	SDMMC1_CMD_PB29	–	SD Card command line
PB30	SDMMC1_CK_PB30	–	SD Card clock signal
PB31	SDMMC1_DAT0_PB31	–	SD Card data line 0
PC0	SDMMC1_DAT1_PC0	–	SD Card data line 1
PC1	SDMMC1_DAT2_PC1	–	SD Card data line 2
PC2	SDMMC1_DAT3_PC2	–	SD Card data line 3
PC3	SDMMC1_WP_PC3	–	SD Card connector write protect signal
PC4	SDMMC1_CD_PC4	–	SD Card card detect
PC5	SDMMC1_1V8SEL_PC5	–	SD Card signal voltage selection
NRST_OUT	NRST_OUT	–	Microprocessor reset output

3.4.11 Secure Element - CryptoAuthentication™

The ECC608B is a member of the Microchip CryptoAuthentication family of high-security cryptographic devices which combine a world-class hardware-based key storage with hardware cryptographic accelerators to implement various authentication and encryption protocols.

The ECC608B includes an EEPROM array which can be used for storage of up to 16 keys, certificates, miscellaneous read/write, read-only or secret data, consumption logging, and security configurations. Access to the various memory sections can be restricted in a variety of ways and the configuration can be locked to prevent changes.

For more details about ECC608B, refer to the product web page.

Table 3-41. ECC608B PIO Signal Descriptions

PIO	MPU Signal Name	Device Signal Name	Shared With	Signal Description
PC14	FLEXCOM8_IO0_PC14	ECC608_TWD	MIPI CSI camera	TWI data
PC13	FLEXCOM8_IO1_PC13	ECC608_TWCK	MIPI CSI camera	TWI clock

ATECC608B-SSHDA is placed on the same TWI bus as the MIPI CSI camera, as described below.

Figure 3-51. ECC608 Interface Schematic

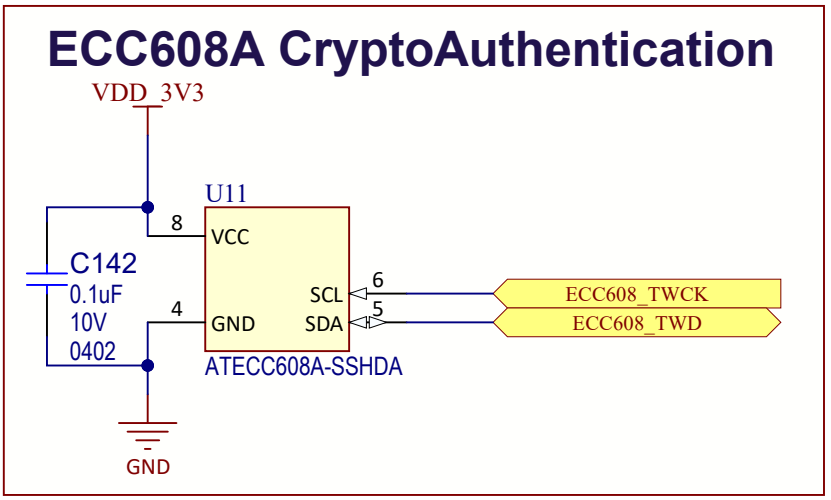


Table 3-42. ECC608B TWI Address

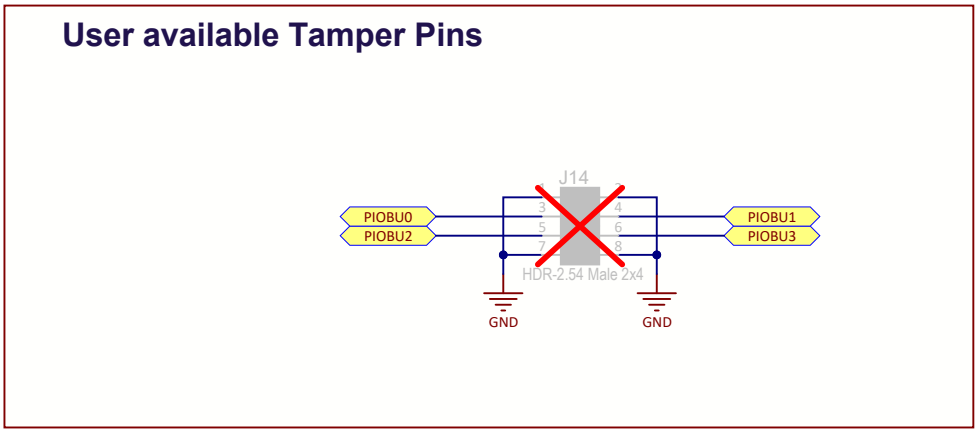
Device	7-bit Client Address	Full Address with RD/WR#
ECC608B TWI Read	1100_000	0xC1
ECC608B TWI Write		0xC0

3.4.12 Tamper Pins Connector

The SAMA7G54-EK board features four tamper pins for static or dynamic intrusion detections.

For a description of intrusion detection, refer to the SAMA7G5 Series data sheet, section “Security Module (SECUMOD)”. See Reference Documents.

Figure 3-52. Tamper Pin Connector Schematic



The table below describes the pin assignment of PIOBU connector J14.

Table 3-43. PIOBU Connector J14 Pin Assignment

Signal Name	Signal Description	Pin No.	Pin No.	Signal Description	Signal Name
GND	Ground	1	2	Ground	GND
PIOBU0	Tamper I/O 0	3	4	Tamper I/O 1	PIOBU1
PIOBU2	Tamper I/O 2	5	6	Tamper I/O 3	PIOBU3
GND	Ground	7	8	Ground	GND

3.5 User Interaction and Debugging

The SAMA7G54-EK includes two main debugging interfaces to provide debug-level access to the SAMA7G5 device:

- Two UART interfaces, one connected directly to the MPU using connector J20 and one through the USB/J-Link-OB CDC feature on USB port J24
- Two JTAG interfaces, one connected directly to the MPU using connector J27 and one through the J-Link-OB interface USB port J24

3.5.1 Serial Debug COM Port

The SAMA7G54-EK board features a dedicated serial port for debugging, accessible through header J20. Various interfaces can be used as a USB/serial DBGU port bridge, such as the FTDI TTL-232R USB-to-TTL serial cable.

Figure 3-53. Debug COM Port Interface Schematic

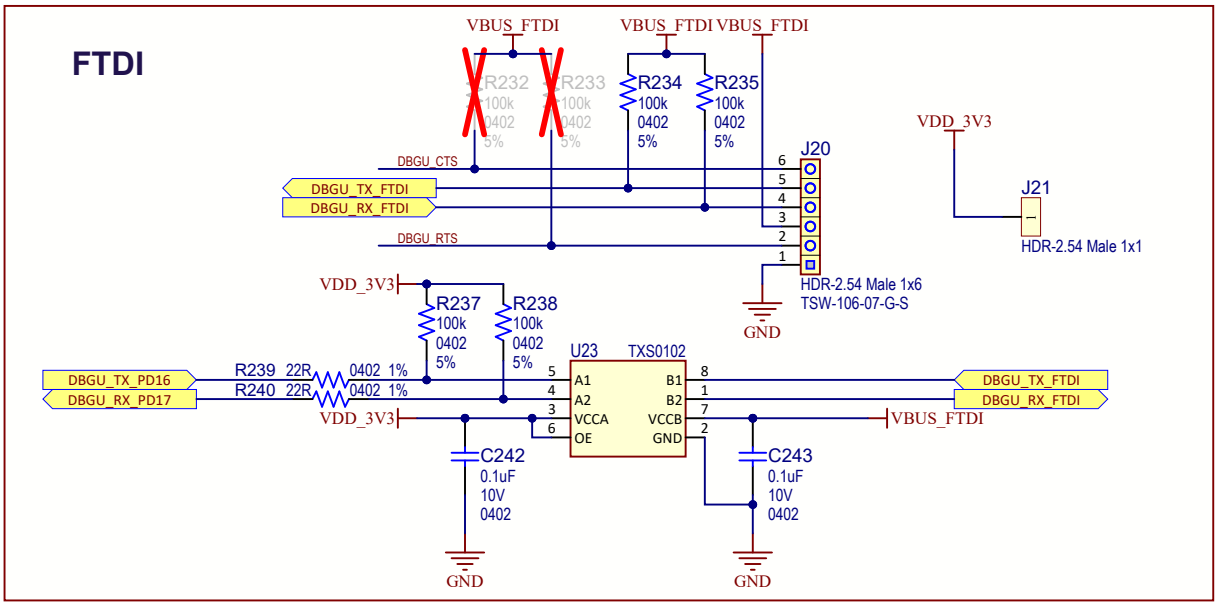


Table 3-44. Debug COM Port Signal Description

PIO	Signal Name	Shared	Signal Description
PD17	DBGU_RX_PD17	DEBUG	Receive data
PD16	DBGU_TX_PD16	DEBUG	Transmit data

Note: The use of a 6-pin header FTDI cable is necessary to supply U23 with 5V in order to polarize the pull-up resistors R234 and R235. If a 3-wire FTDI cable is used, a shortcut between VBUS_FTDI and VDD_3V3 is necessary.

3.5.2 Debug JTAG

A 20-pin JTAG header (J27) is provided on the SAMA7G54-EK board to facilitate software development and debugging using various JTAG emulators. The interface signals have a voltage level of 3.3V.

Figure 3-54. JTAG Interface Schematic

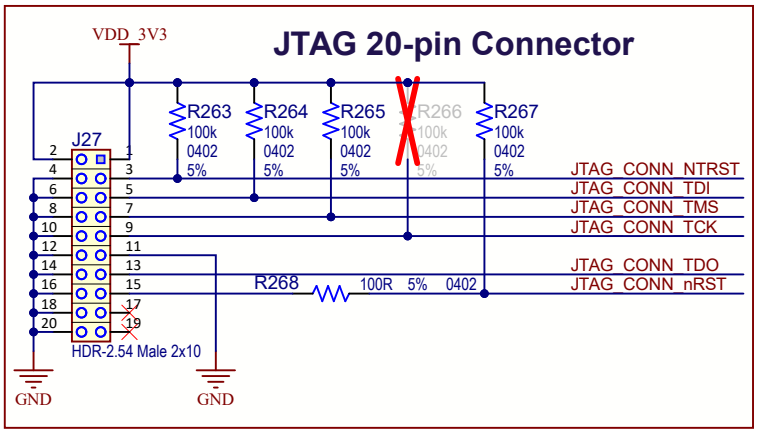


Table 3-45. JTAG/ICE Connector J27 Pin Assignment

Signal	Signal Name	Pin No.	Pin No.	Signal Name	Signal
+3.3V	VDD_3V3	2	1	VDD_3V3	+3.3V
GND	GND	4	3	JTAG_CONN_NTRST	NTRST
GND	GND	5	5	JTAG_CONN_TDI	TDI
GND	GND	8	7	JTAG_CONN_TMS	TMS
GND	GND	10	9	JTAG_CONN_TCK	TCK
GND	GND	12	11	GND	GND
GND	GND	14	13	JTAG_CONN_TDO	TDO
GND	GND	16	15	JTAG_CONN_nRST	nRST
GND	GND	18	17	Not connected	NC
GND	GND	20	19	Not connected	NC

3.5.3 Embedded Debugger (J-Link-OB) Interface

The SAMA7G54-EK includes a built-in SEGGER J-Link-On-Board (J-Link-OB) device. The functionality is implemented with an ATSAM3U4C microcontroller in an LFBGA100 package. The ATSAM3U4C provides the functions of the JTAG interface and a bridge from USB to the serial debug port (CDC, or Communication Device Class). The two-colored LED (D10) shows the status of the J-Link-OB device.

The J-Link-OB device is designed to provide an efficient, low-cost, on-board alternative to the standard J-Link or SAM-ICE.

Its own dedicated USB port acts as a power source for this block (which is separated from the rest of the system) and provides the communication link to program and debug the MPU.

Figure 3-55. J-Link-OB with J-Link-CDC Interface Schematic

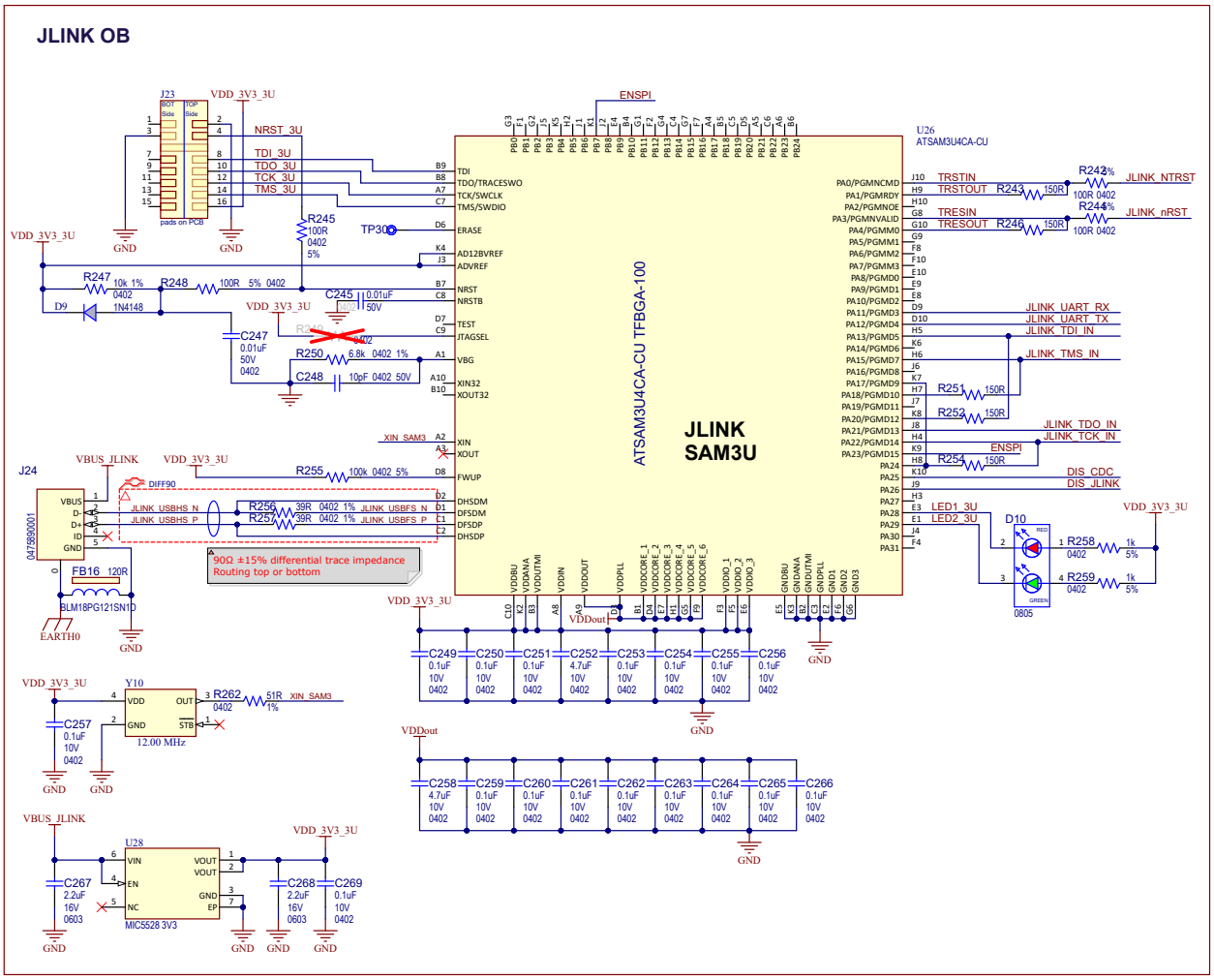


Table 3-46. J-Link-OB and J-Link-CDC LED D10 Status

LED D10	State	Description
Red and green	Off	J-Link (SAM3U device) is not programmed, or J25 and J26 are shorted.
Red	On	J-Link (SAM3U device) is programmed but J-Link is disabled (J26 shorted).
Green	Flashing	J-Link is operational but the USB port is not connected.
Green	On	J-Link-OB is connected and ready.

The ATSAM3U microcontroller (U26) is powered only through the J-Link USB connector. The programmer IC is therefore separated from the rest of the system and the user can have a better reading of the power that the system is drawing when interrogating the on-board power measurement devices.

The MIC5528 (U28) has been selected to convert the 5V coming from the USB connector into the 3.3V rail required by the microcontroller. The MIC5528 is a simple low-power, low dropout regulator designed for optimal performance in a very small footprint. It is capable of sourcing up to 500 mA of output current while only drawing 38 µA of operating current. For more information about the MIC5528, refer to the product web page.

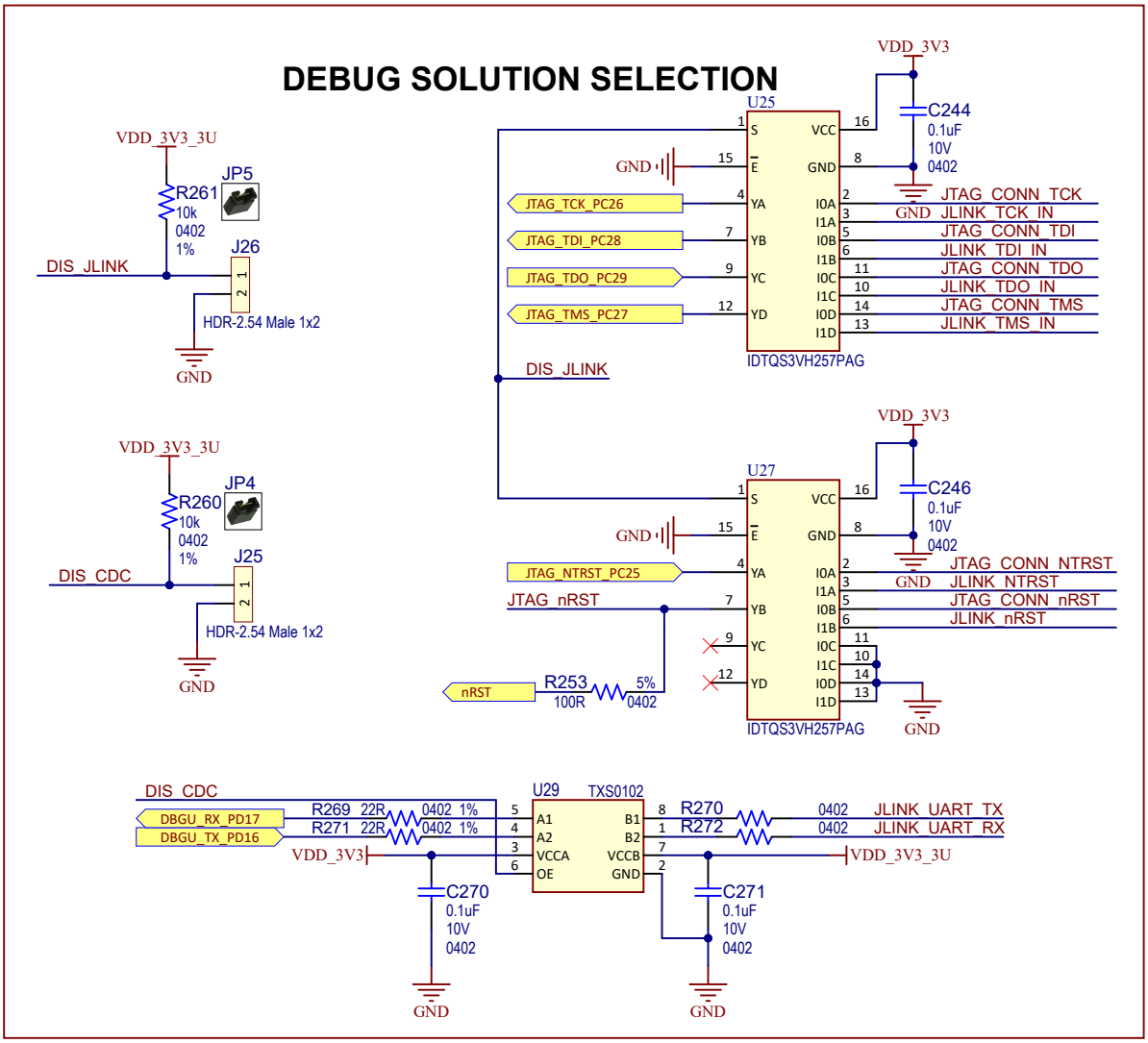
3.5.4 Debug Solution Selection

If the user does not require the on-board programming feature, this section can be left unpowered, with no impact on the rest of the system. A level shifter has been placed on the DEBUG UART line (U29) between the SAMA7G5 MPU and the on-board programmer (U26) to properly separate the two voltage domains.

Jumper JP5/J26 disables the J-Link-OB JTAG functionality. When installed (J26 shorted), a quad analog switch (U25/U27) routes the JTAG interface of the SAMA7G5 to the 20-pin header J27.

- Jumper JP5/J26 not installed: J-Link-OB-ATSAM3U4C is enabled and fully functional.
- Jumper JP5/J26 installed: J-Link-OB-ATSAM3U4C is disabled and an external JTAG controller can be used through the 20-pin JTAG port J27.

Figure 3-56. Debug Solution Selection Schematic



In addition to the J-Link-OB functionality, the ATSAM3U4C microcontroller provides a bridge to a debug serial port (DBGU) of the main board processor. The port is made accessible over the same USB connection used by JTAG by implementing a Communication Device Class (CDC), which allows a terminal communication with the target device.

This feature is enabled/disabled by jumper J25.

- Jumper J25 not shorted: the J-Link-OB CDC function is enabled and fully functional.
- Jumper J25 shorted: the J-Link-OB CDC function is disabled.

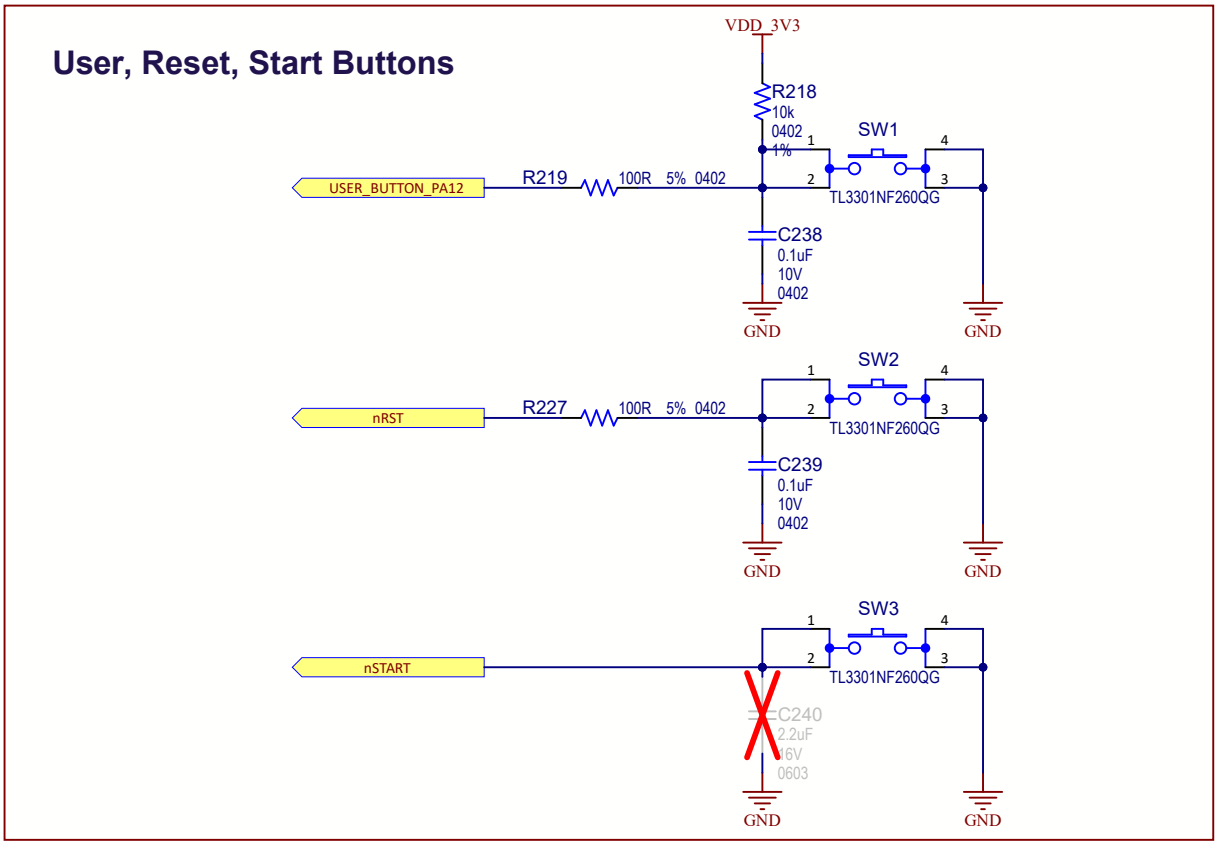
The USB CDC converts the USB device into a serial communication device. The target device running the CDC is recognized by the host as a serial interface (USB2COM, virtual COM port) without the need to install a special host driver (the CDC is standard). All PC software using a COM port work without modifications with this virtual COM port. Under Microsoft® Windows®, the device shows up as a COM port; under Linux®, as a /dev/ACMx device. This enables the user to use host software which was not designed to be used with USB, such as a terminal program.

3.5.5 Push Button Switches

The SAMA7G54-EK features three push buttons:

- One user push button (SW1) connected to PIO_PA12 for free use.
- One board reset push button (SW2). When pressed, the processor is reset.
- One start or wake-up push button (SW3) connected to the nSTRT pin of the PMIC, used to instruct the PMIC to initiate a power-on sequence or to make the processor exit Low-Power mode[1].

Figure 3-57. Push Buttons Schematic



Note:

1. For more details about the SW3 push button behavior, see Startup Conditions.

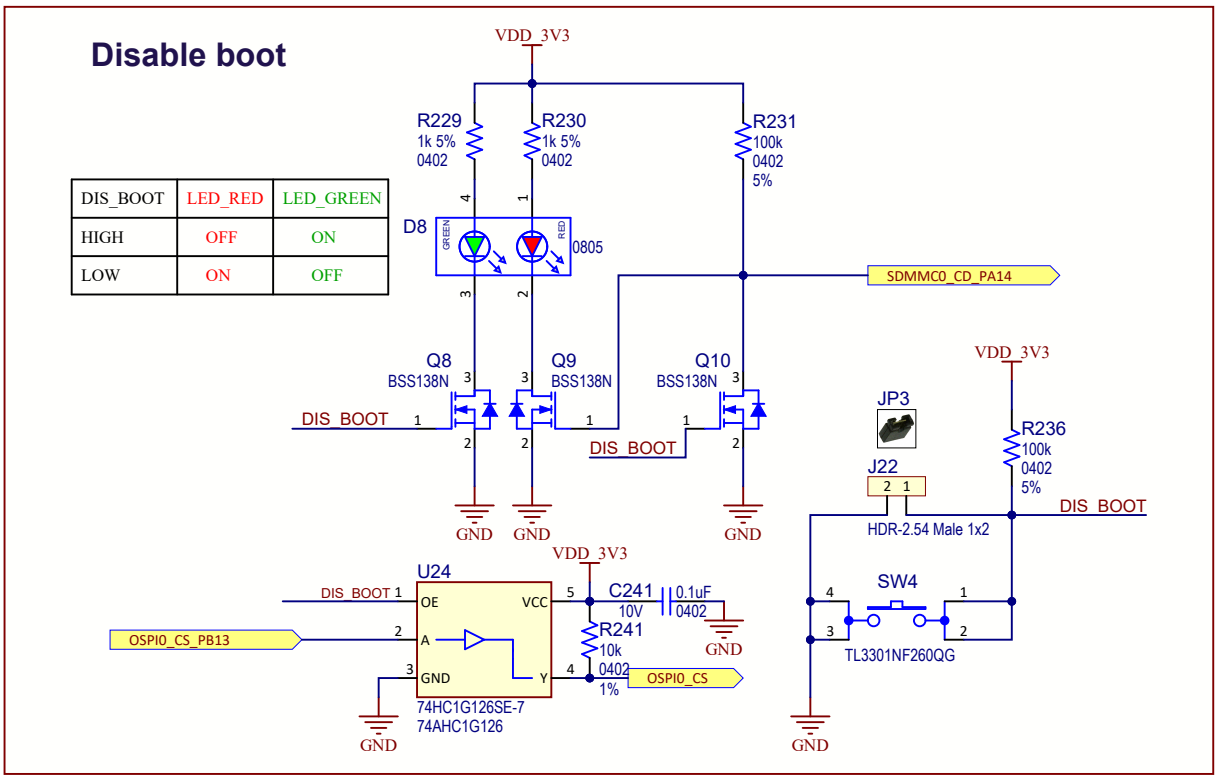
3.5.6 Disable Boot

On-board push button SW4 and/or jumper J22 control the selection (CS#) of the bootable memory components, QSPI and e.MMC NAND Flash, using a non-inverting 3-state buffer for the first memory and a MOSFET for the second one.

The rule of operation is:

- SW4 (DISABLE_BOOT) or J22 shorted: booting from QSPI and e.MMC NAND FLASH is disabled.
- LED D8 indicates the state of the DIS_BOOT signal:
  - Red: the on-board boot memories are disabled.
  - Green: the on-board boot memories are enabled.

Figure 3-58. Disable Boot Schematic



Note: The “Disable Boot” mechanism does not disable booting from SD Card connector J4. The user must remove the SD Card to disable booting from it.

3.5.7 RGB LED

The SAMA7G54-EK board features one RGB (red, green, blue) LED. The three LED cathodes are controlled via one standard GPIO and two GPIOs in PWM mode.

At Reset state, the blue and green LEDs are off; only the red LED is on, representing the "power on" status.

Figure 3-59. User RGB LEDs Schematic

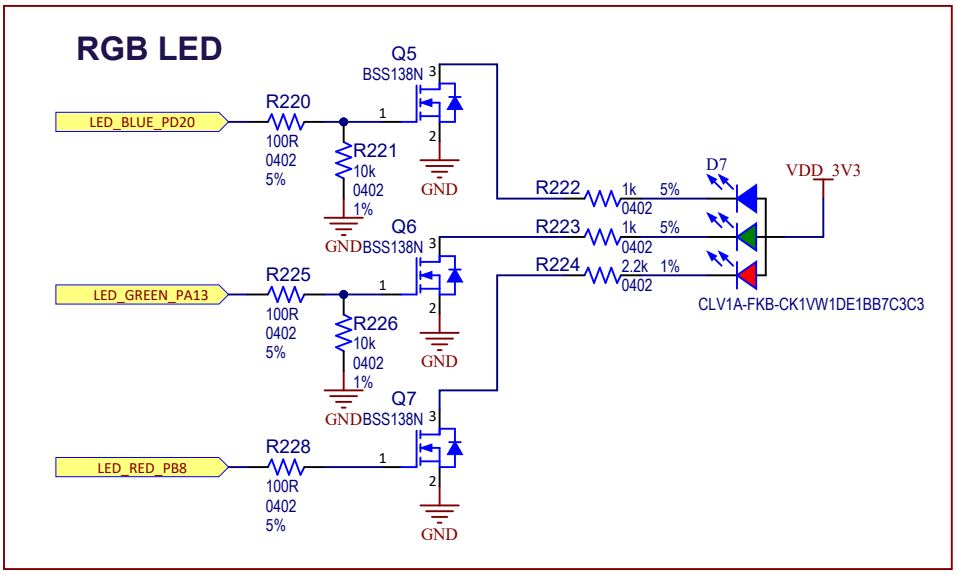


Table 3-47. RGB LED PIOs

Signal	PIO	Shared With	Function
LED_BLUE_PD20	PD20	mikroBUS 2 connector	PWMH3
LED_GREEN_PA13	PA13	mikroBUS 1 connector	PWMH2
LED_RED_PB8	PB8	RPi 40-pin connector	GPIO

4. Installation and Operation

4.1 System and Configuration Requirements

The SAMA7G54-EK requires the following:

- A personal computer
- A USB-A to USB-microAB cable (provided in the kit box)
- An AC/DC wall adapter (not provided in the kit box) in case of high power consumption system

4.2 Board Setup

Follow these steps before using the SAMA7G54-EK:

1. Unpack the board, taking care to avoid electrostatic discharge.
2. Check the Default Jumper Settings.
3. Connect the USB-micro-AB cable to connector J24 (J-Link-OB USB port).
4. Connect the other end of the cable to a free port on the PC.
5. Open a terminal (console 115200, N, 8, 1) on the PC.
6. Supply the board by performing one of the following connections:
   a. USB-micro-AB cable to connector J7 (USB-A port)
   b. AC/DC wall adapter to connector J1 (DC jack connector)
7. Reset the board.
8. A startup message appears on the console as shown in the picture below.

Figure 4-1. Start-Up Message on Console

4.3 Startup Conditions

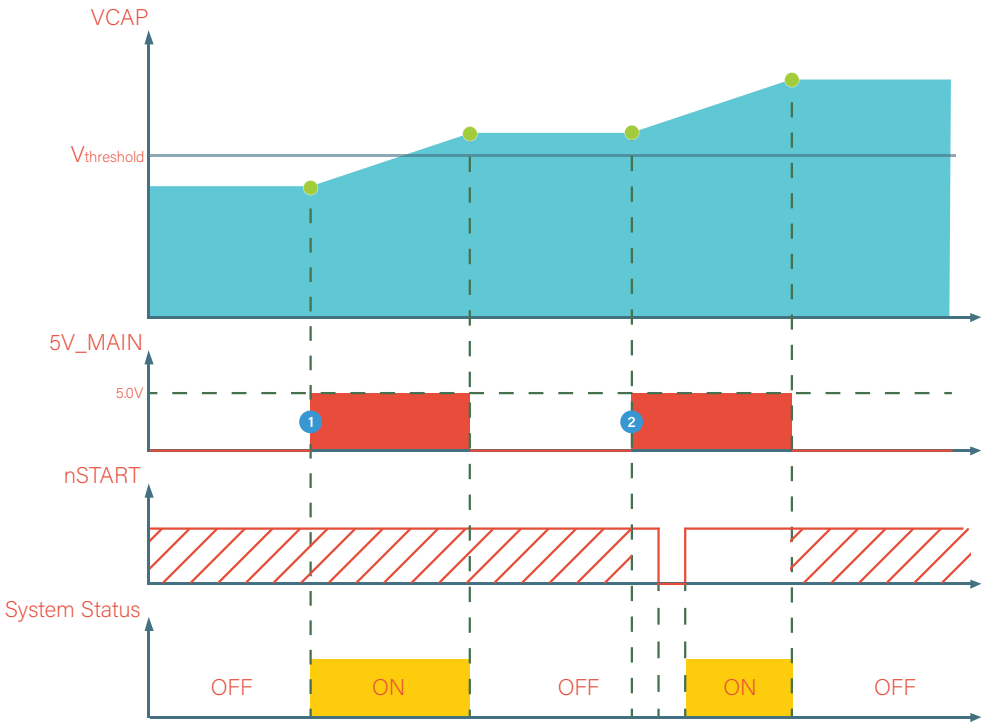
The board startup is managed by the power panagement unit MCP16502. The MCP16502 generates all the power supplies required by the processor and the system. For more details on the power-up conditions, refer to the MCP16502 data sheet. See Reference Documents.

Several startup scenarios are applicable depending on the status of the default board configuration:

- The backup battery is not charged. This is the case for the board first use.
  - The backup battery is empty or below the value of $V_{threshold}$.
  - When inserting the USB cable (J7) or the DC jack (J1), the system starts up on its own without any action on the nSTART button. See event "1" in the diagram below.

- The backup battery is partially or fully charged.
  - The backup battery is charged above the value of $V_{threshold}$.
  - When inserting the USB cable (J7) or DC jack (J1), the system does not start automatically and a short action on the nSTART button is necessary to start the system. See event "2" in the diagram below.

Figure 4-2. Start-Up Behavior Diagram



Notes:

1. The system can be powered off by a long pressure (> 4 seconds) on the nSTART button.
2. It is possible to setup an automatic startup at each power insertion by mounting a C240 capacitor. With this configuration, the system starts automatically when the USB cable (J7) or the DC jack (J1) is connected. This is not the factory configuration.

5. Ordering Information

Table 5-1. Evaluation Kit Ordering Information

Ordering Code	Board Marking
EV21H18A	SAMA7G54-EK EVALUATION KIT

6. Appendix A. Schematics and Layouts

Figure 6-1. SAMA7G54-EK: Schematic Page 1

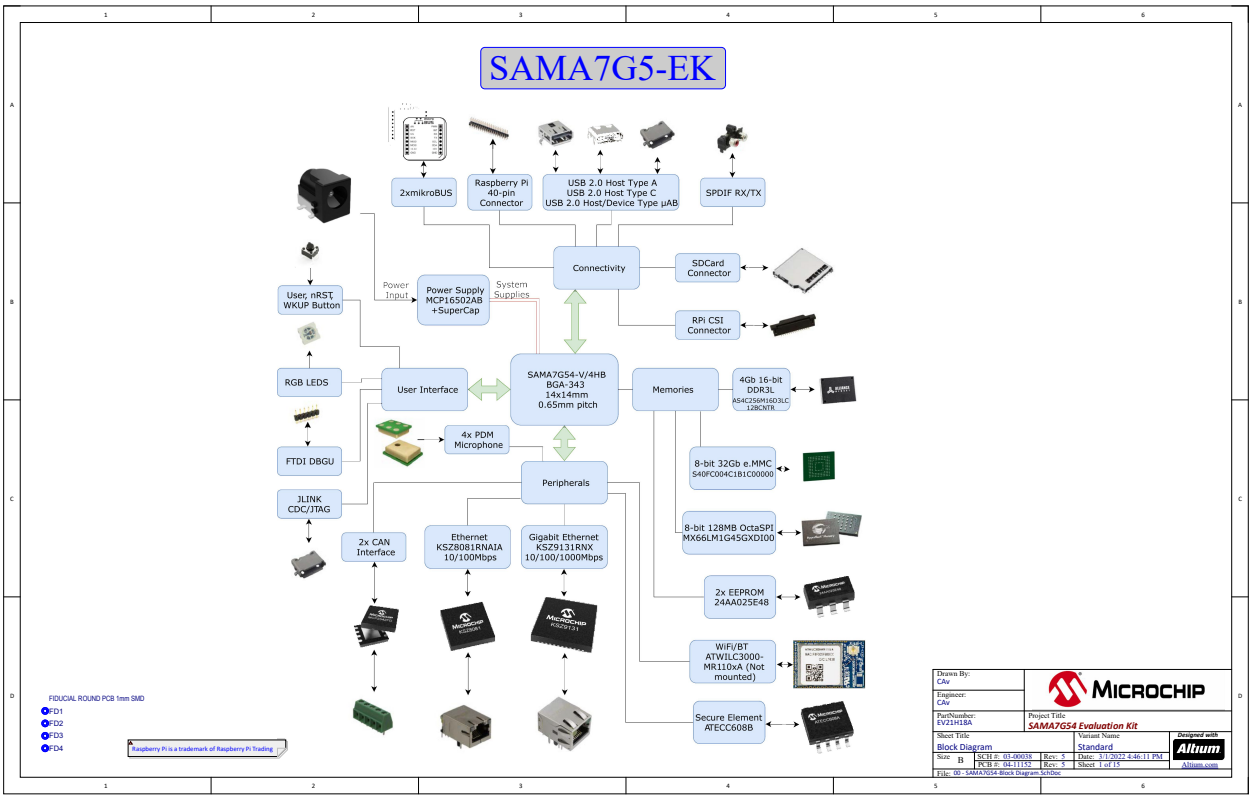


Figure 6-2. SAMA7G54-EK: Schematic Page 2

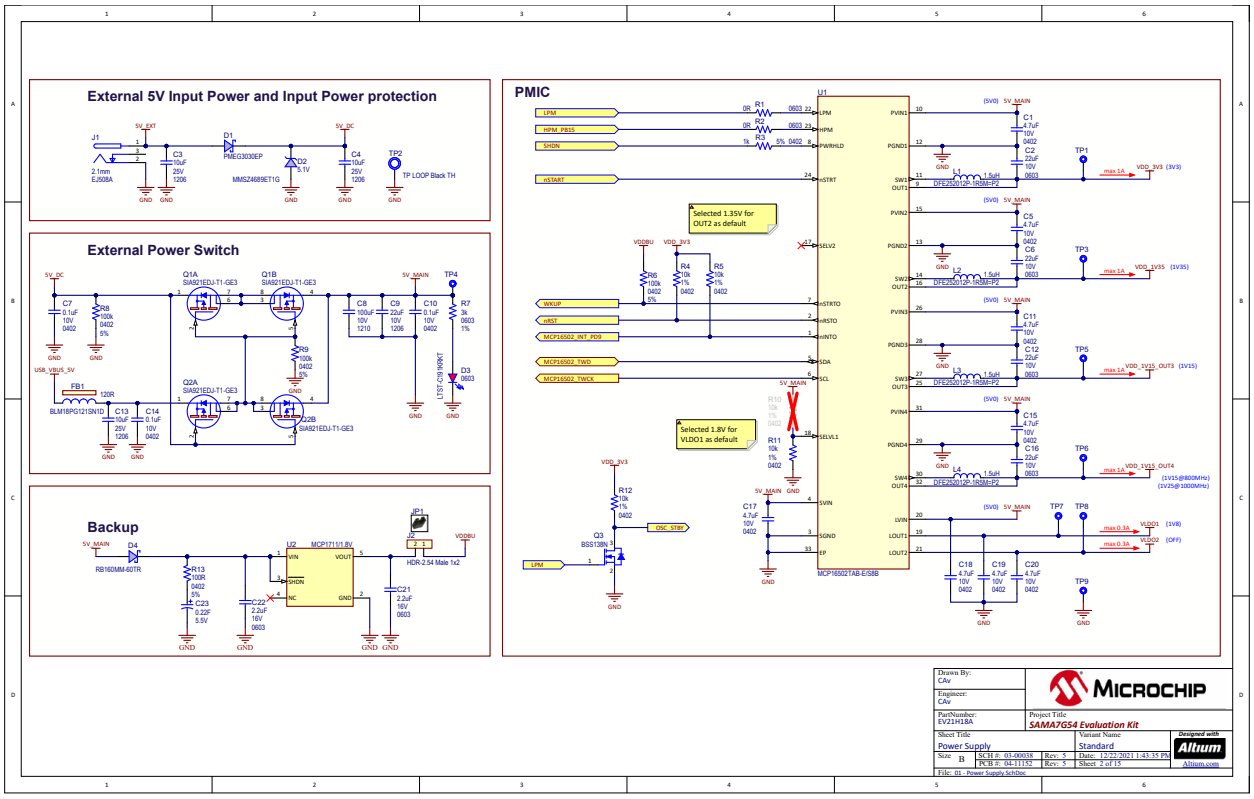


Figure 6-3. SAMA7G54-EK: Schematic Page 3

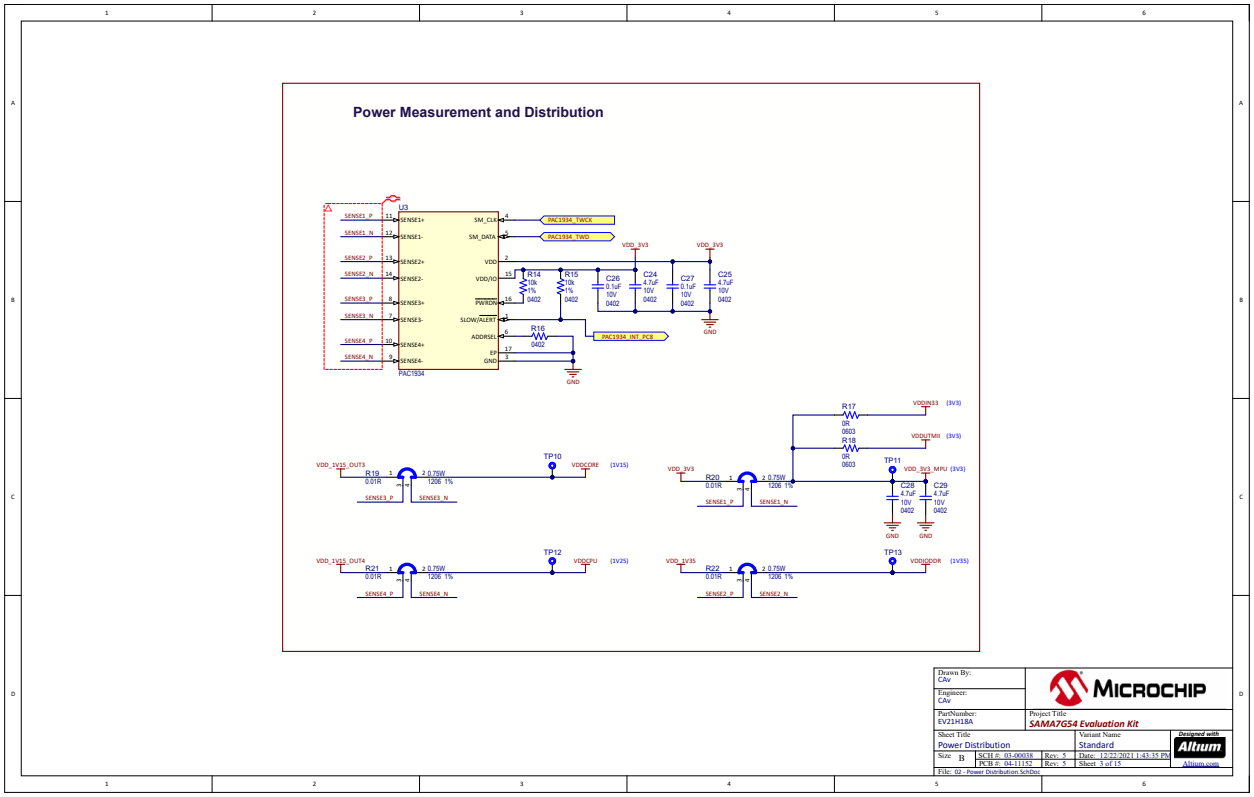


Figure 6-4. SAMA7G54-EK: Schematic Page 4

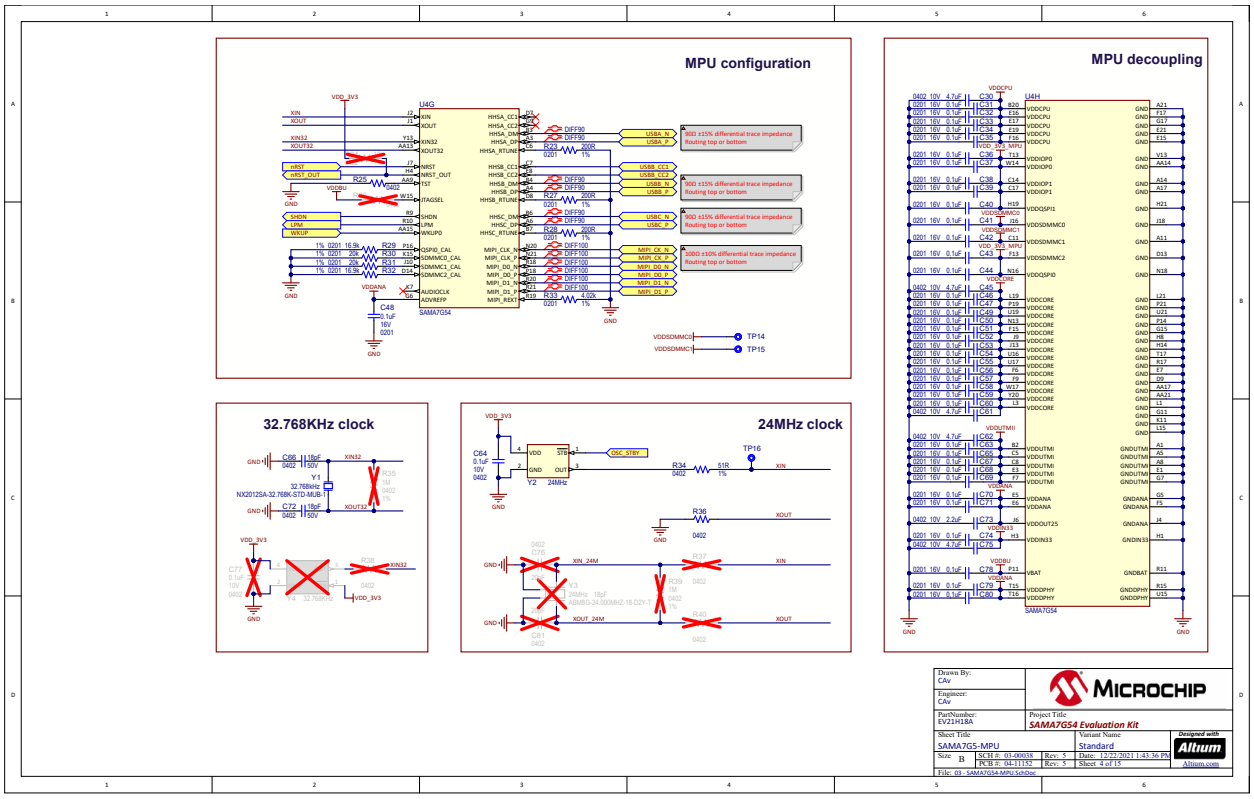


Figure 6-5. SAMA7G54-EK: Schematic Page 5

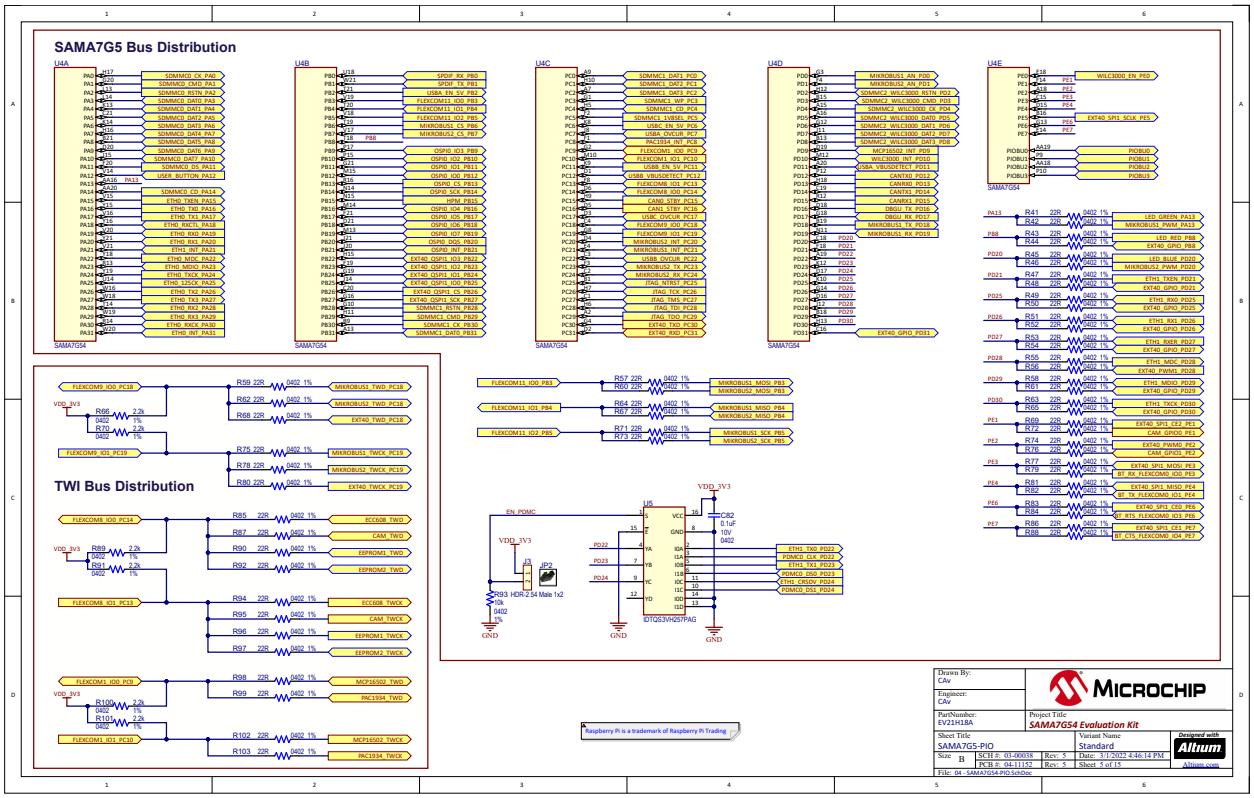


Figure 6-6. SAMA7G54-EK: Schematic Page 6

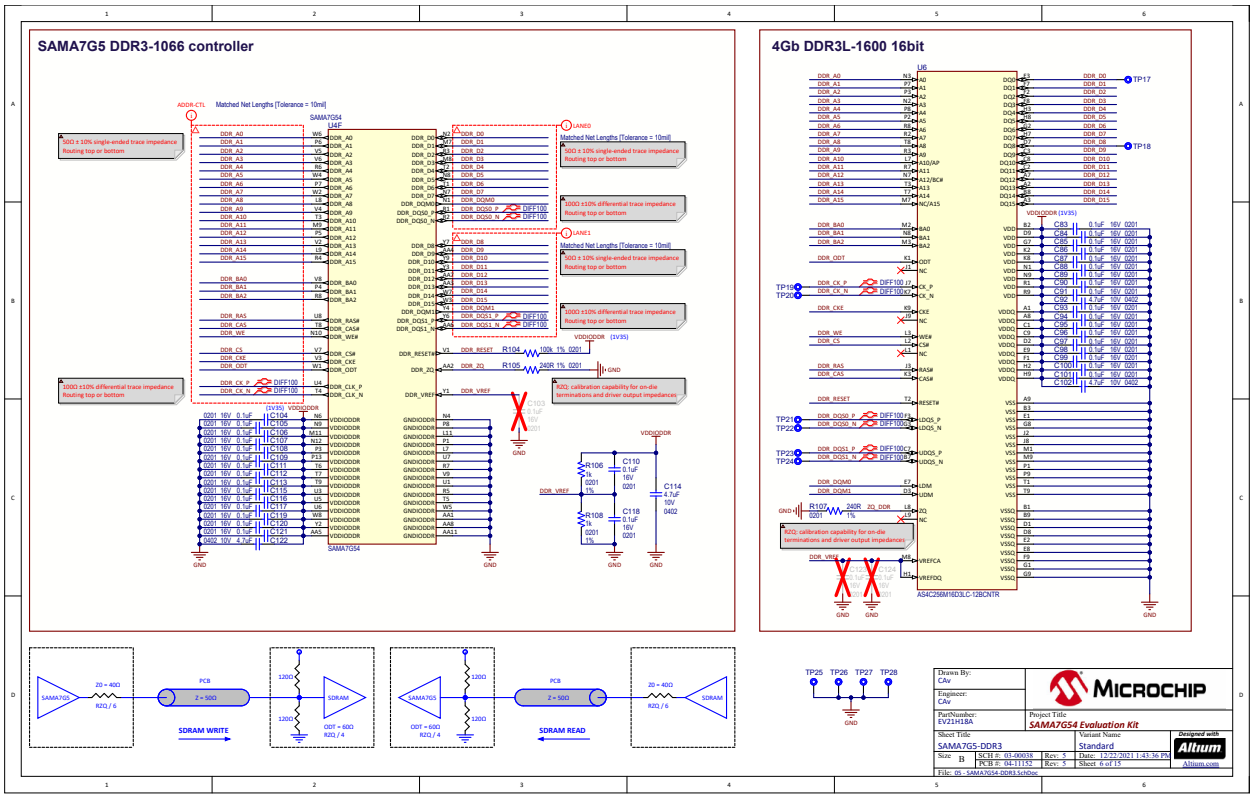


Figure 6-7. SAMA7G54-EK: Schematic Page 7

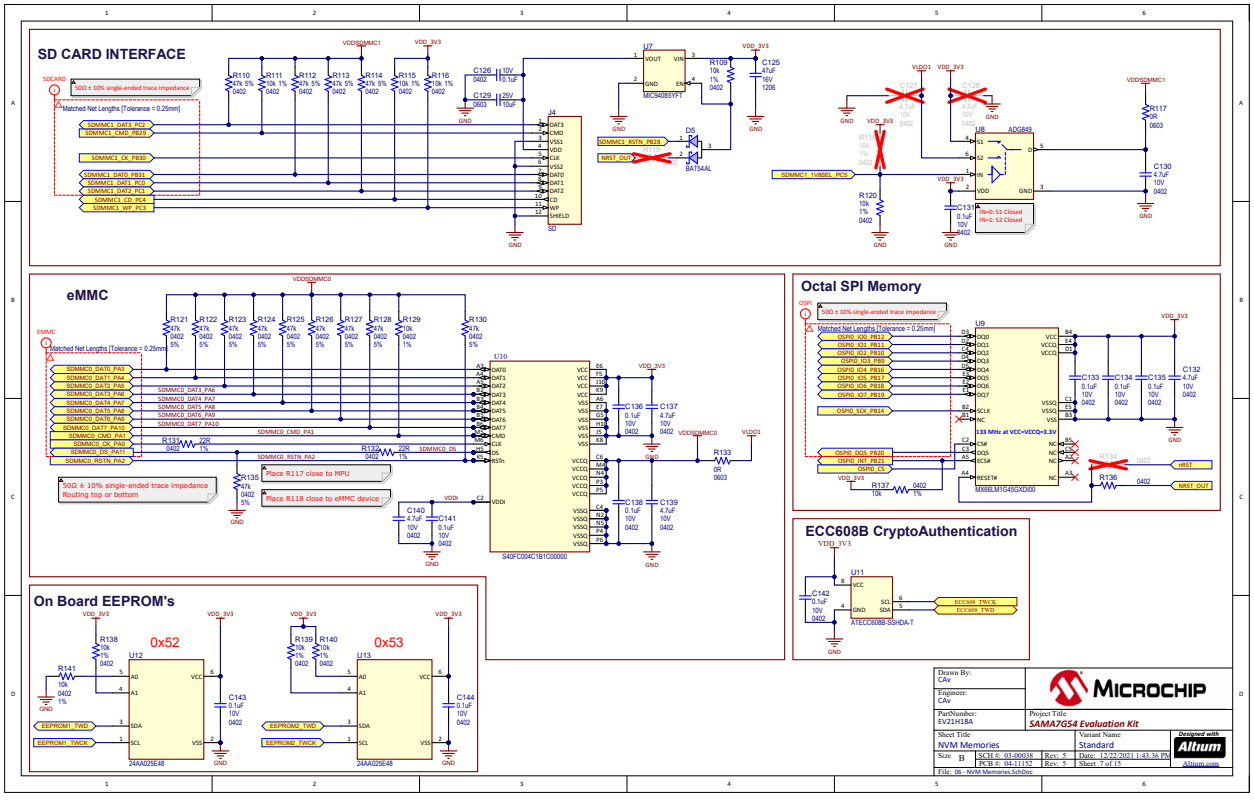


Figure 6-8. SAMA7G54-EK: Schematic Page 8

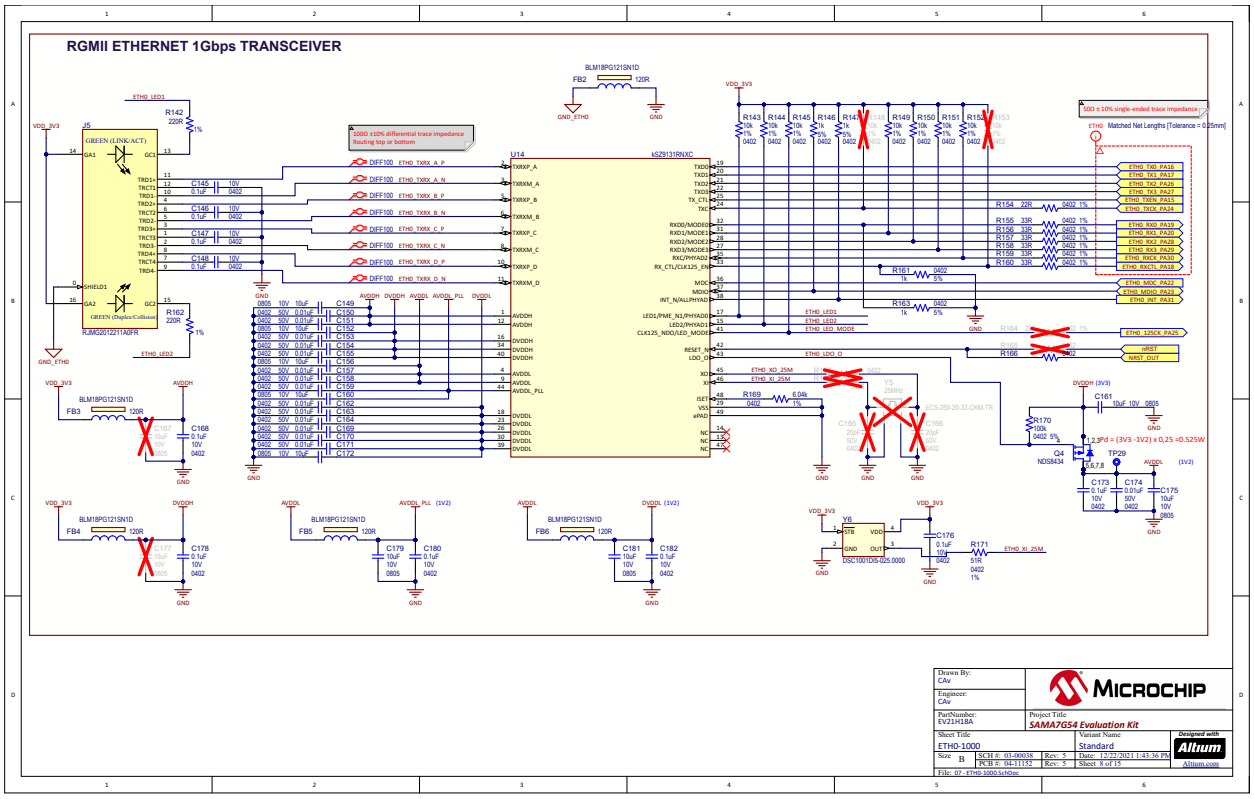


Figure 6-9. SAMA7G54-EK: Schematic Page 9

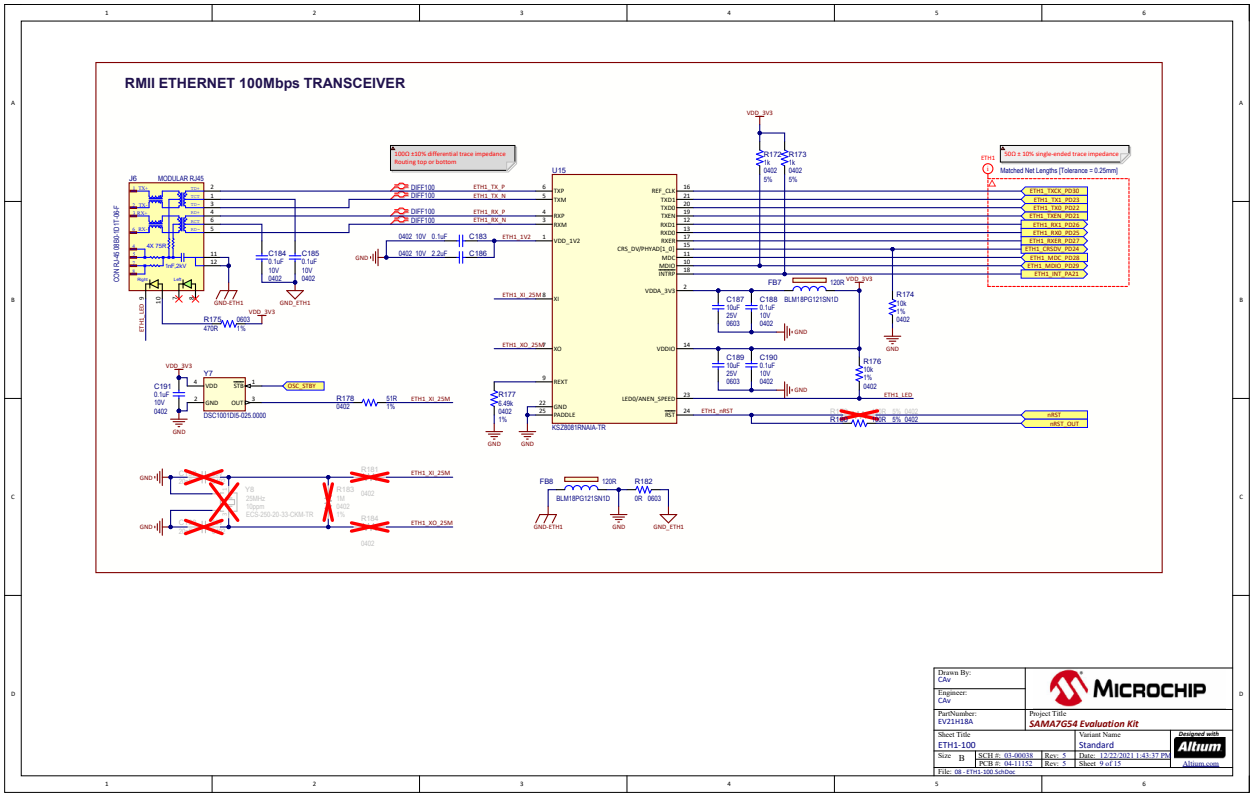


Figure 6-10. SAMA7G54-EK: Schematic Page 10

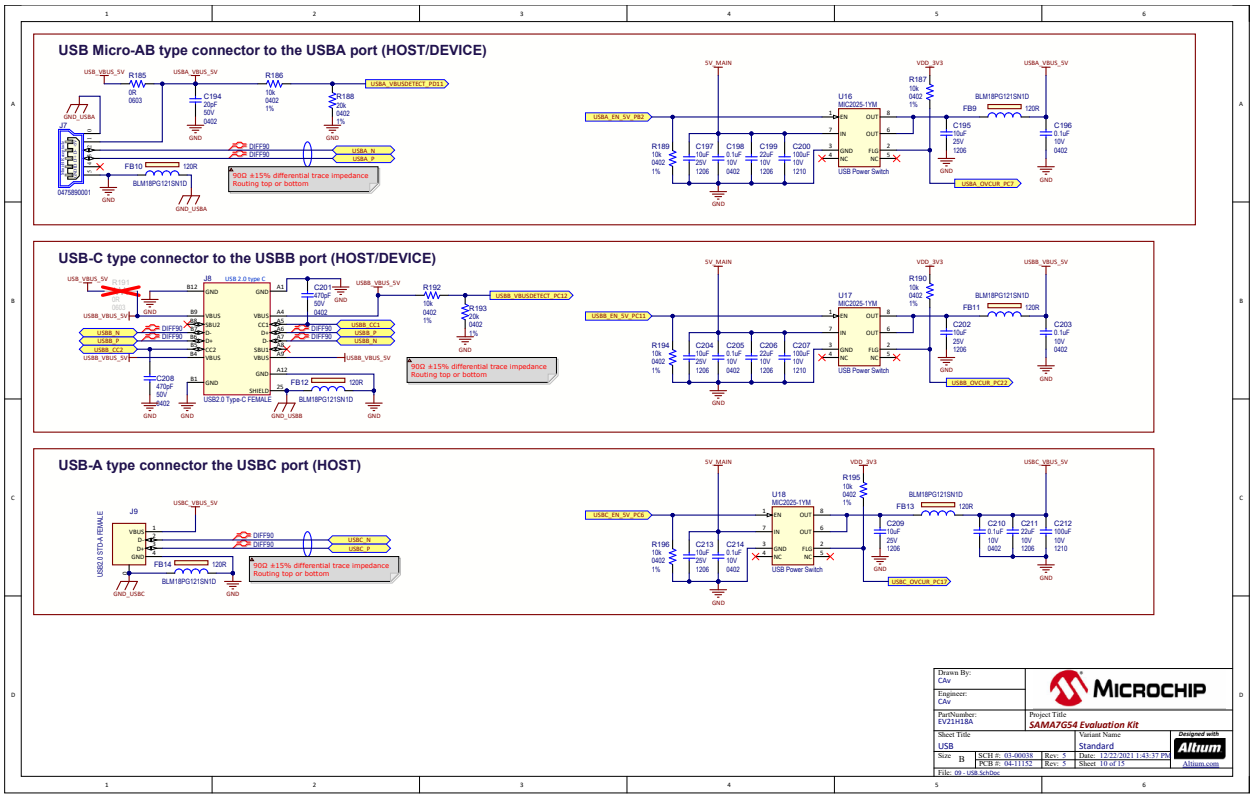


Figure 6-11. SAMA7G54-EK: Schematic Page 11

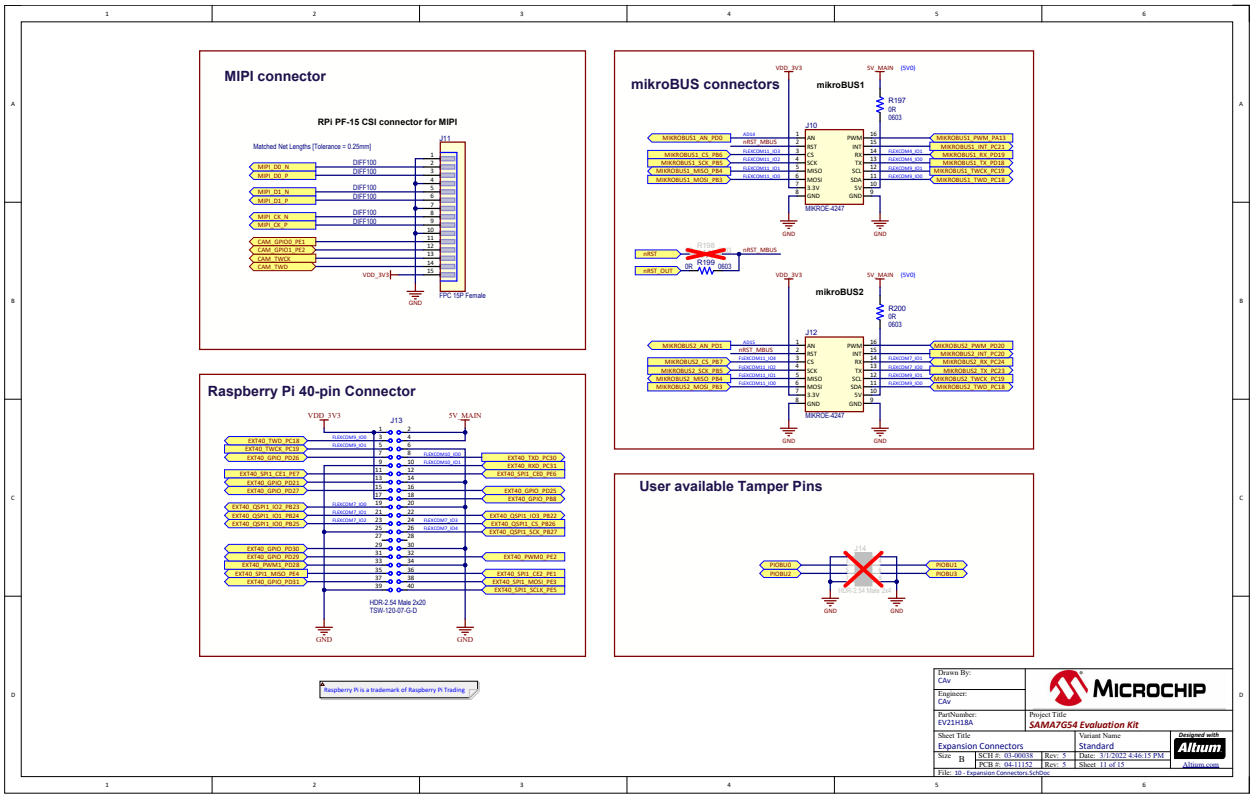


Figure 6-12. SAMA7G54-EK: Schematic Page 12

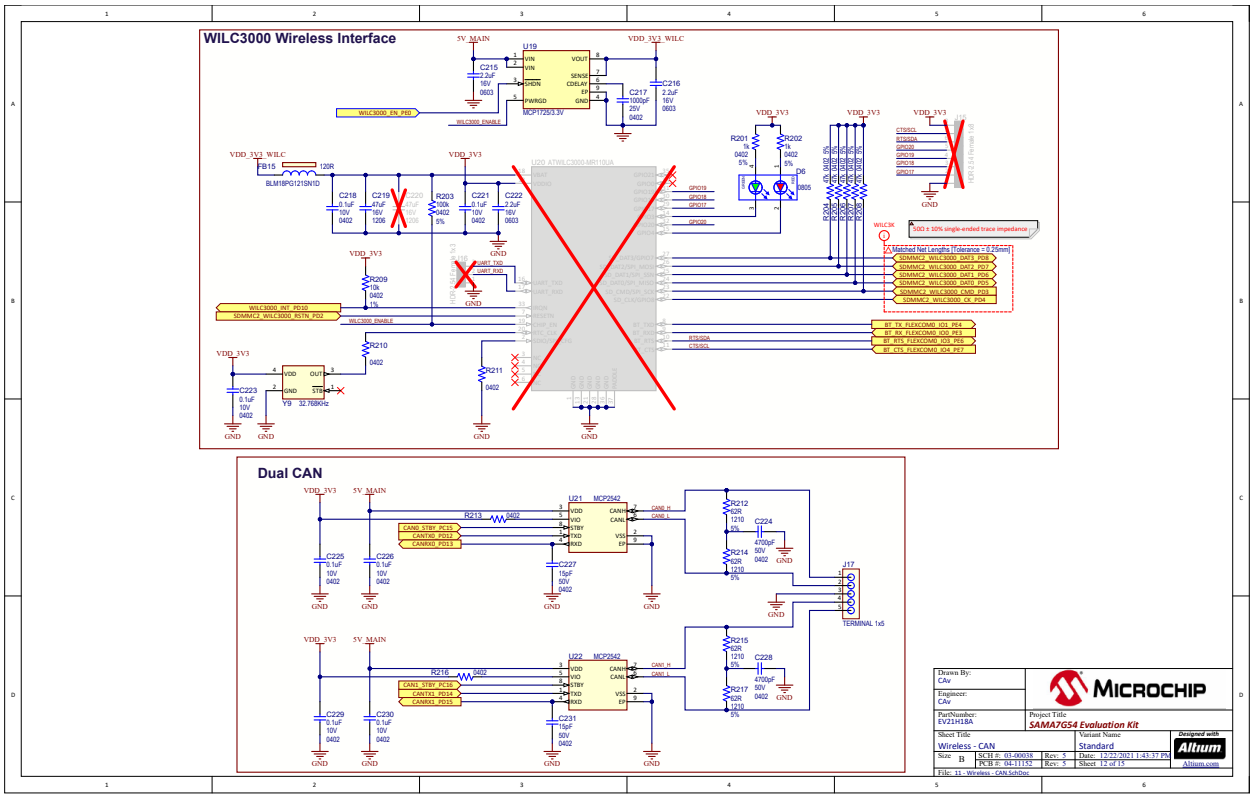


Figure 6-13. SAMA7G54-EK: Schematic Page 13

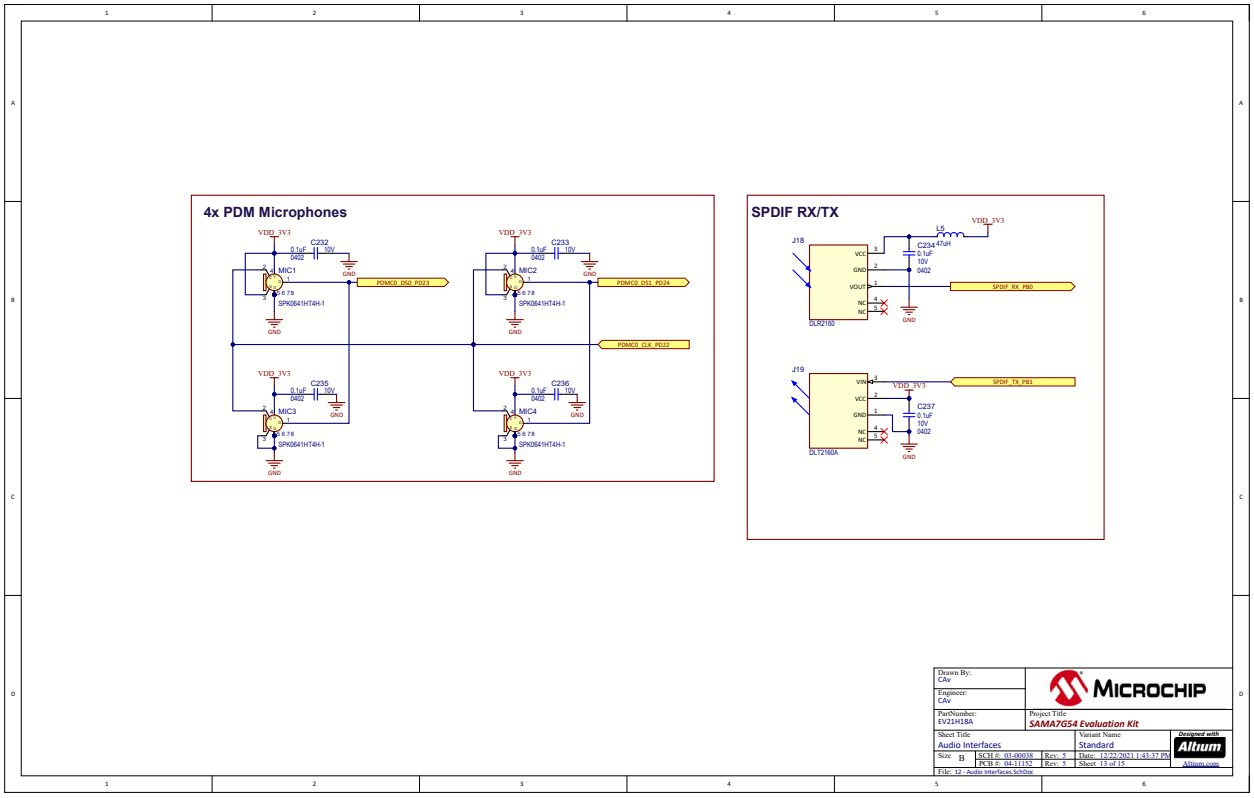


Figure 6-14. SAMA7G54-EK: Schematic Page 14

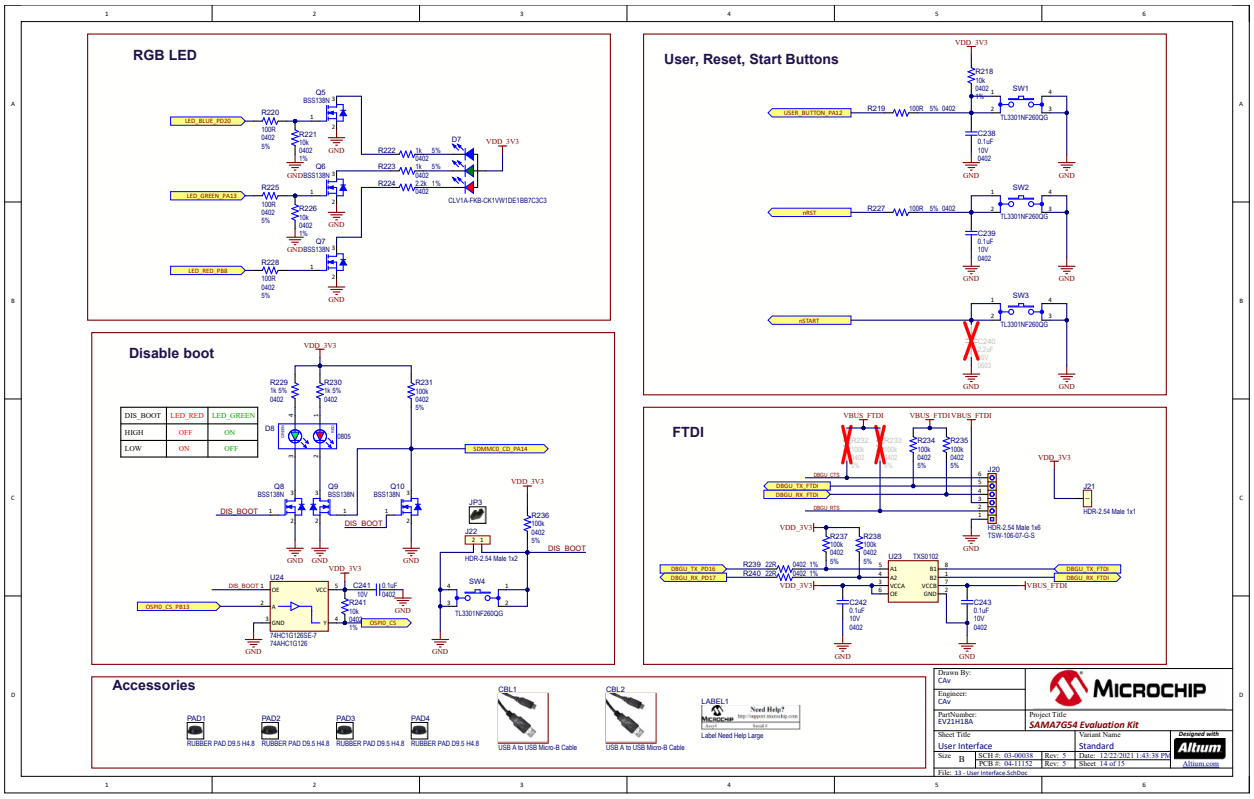


Figure 6-15. SAMA7G54-EK: Schematic Page 15

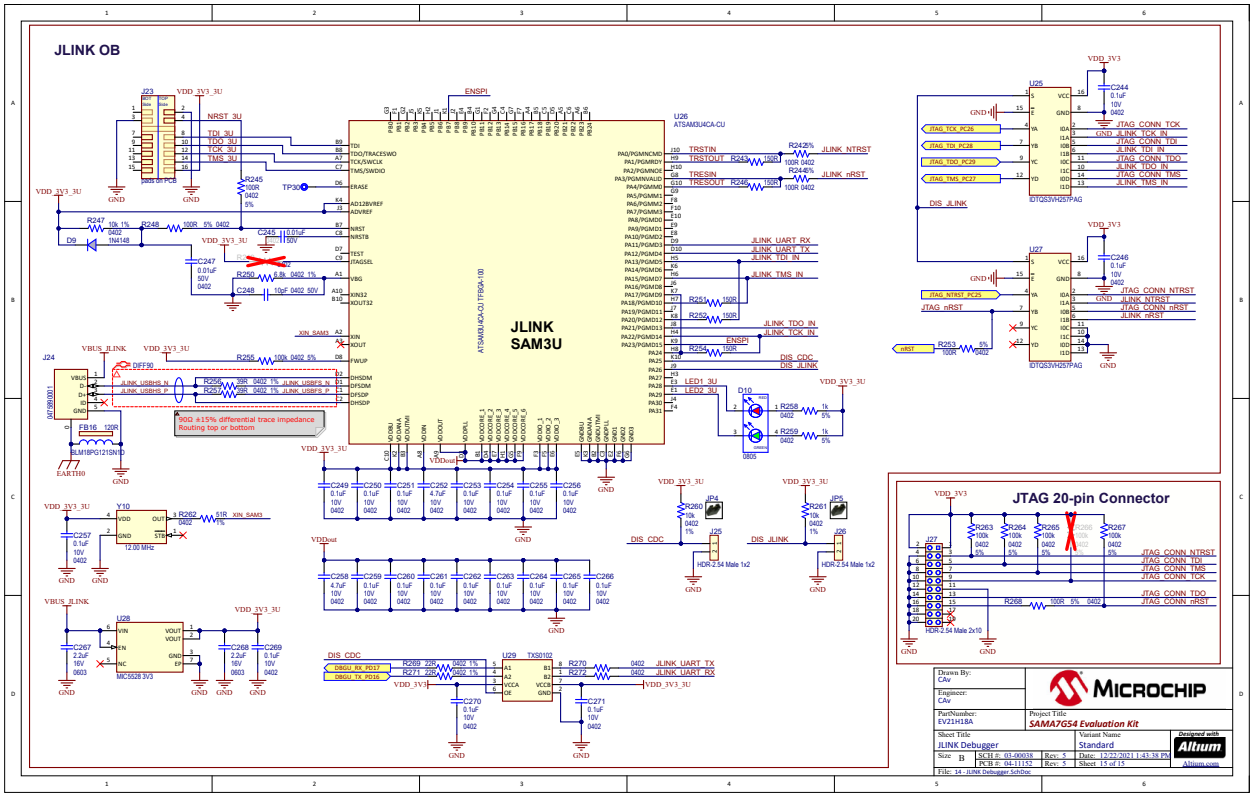


Figure 6-16. SAMA7G54-EK: Layer 1

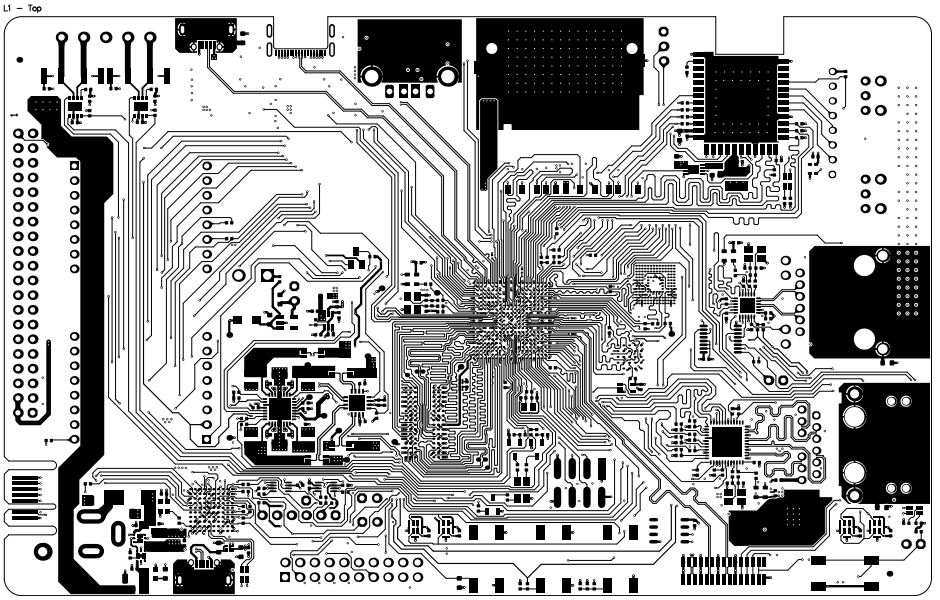


Figure 6-17. SAMA7G54-EK: Layer 2

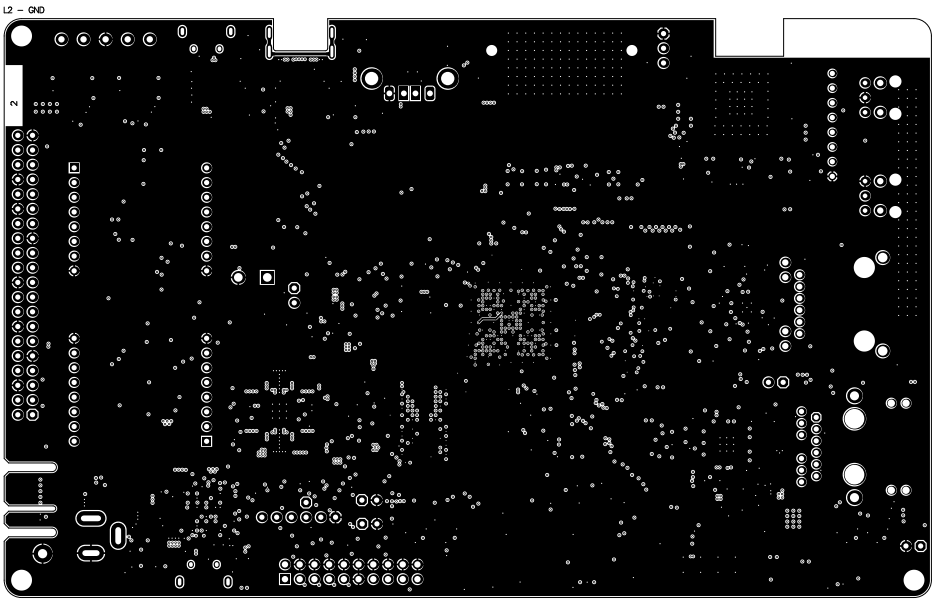


Figure 6-18. SAMA7G54-EK: Layer 3

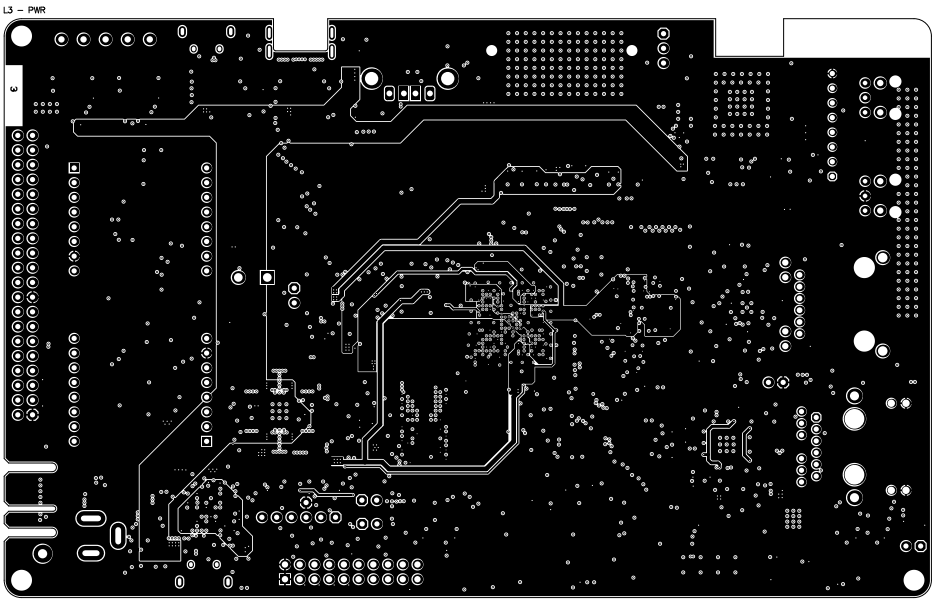
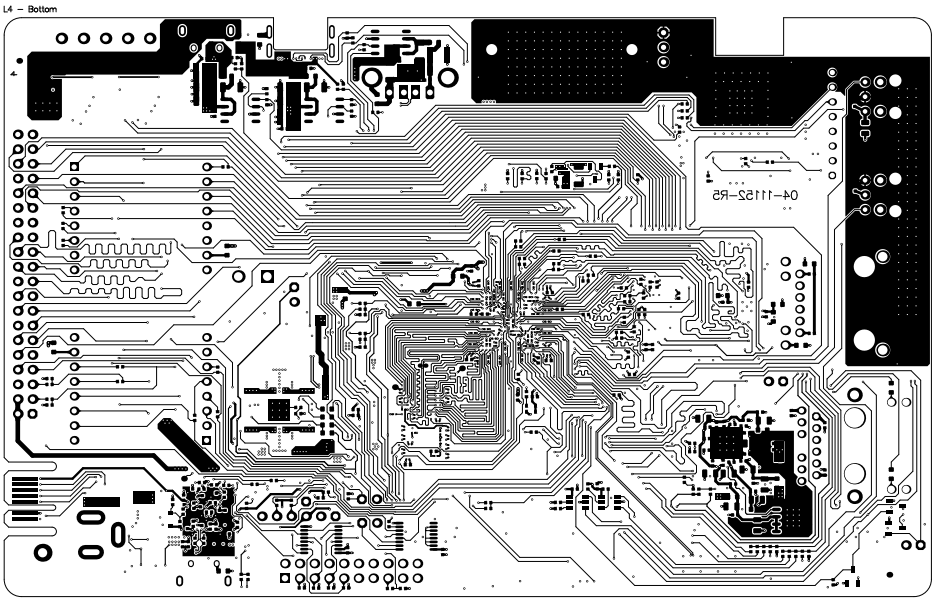


Figure 6-19. SAMA7G54-EK: Layer 4



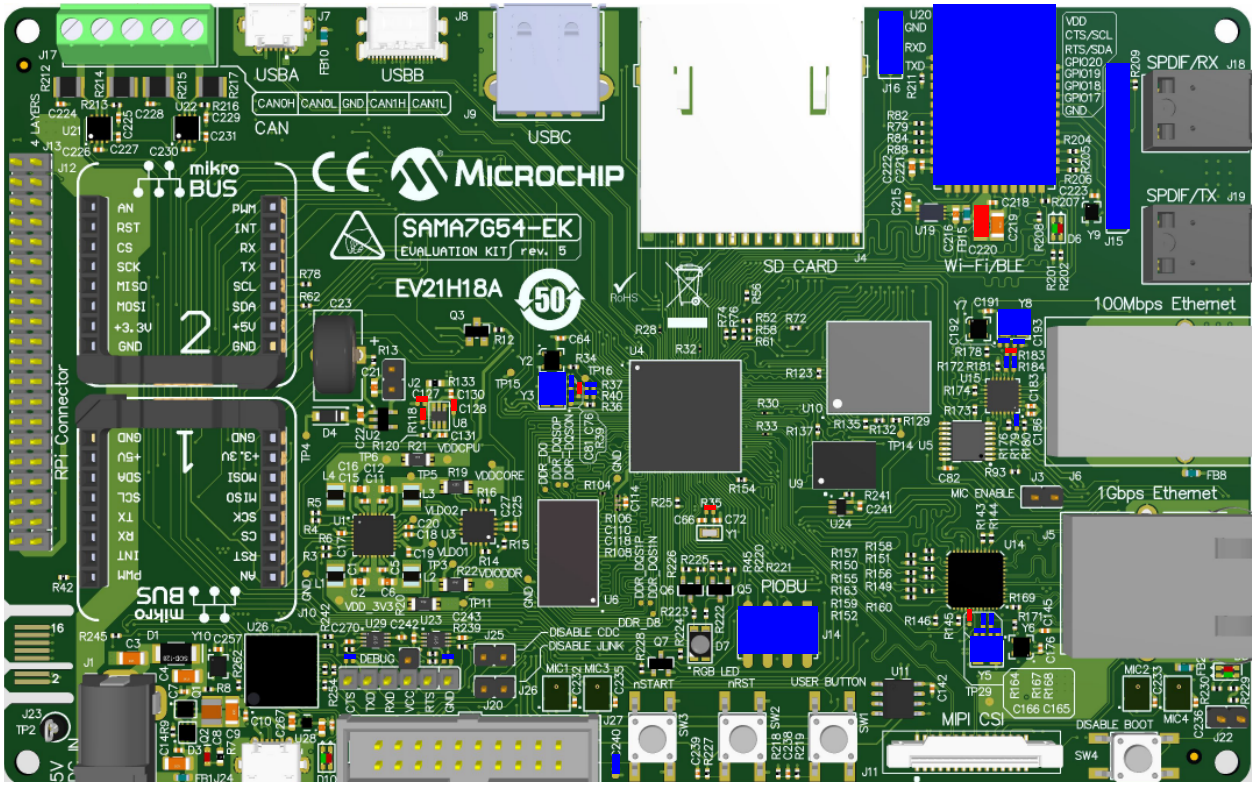
7. Appendix B. Unmounted Elements

7.1 List of Unmounted Elements

Two types of unmounted components are listed in this section:

- In blue, the components that can be mounted, with some board adaptation, without any damage to the system.
- In red, unmounted components used for factory and debug configuration. Those should never be mounted, as such action could result in damage or destruction of the board or system elements.

Figure 7-1. Unmounted Components Overview: Top View



The following table lists the top side unmounted components and their functionalities.

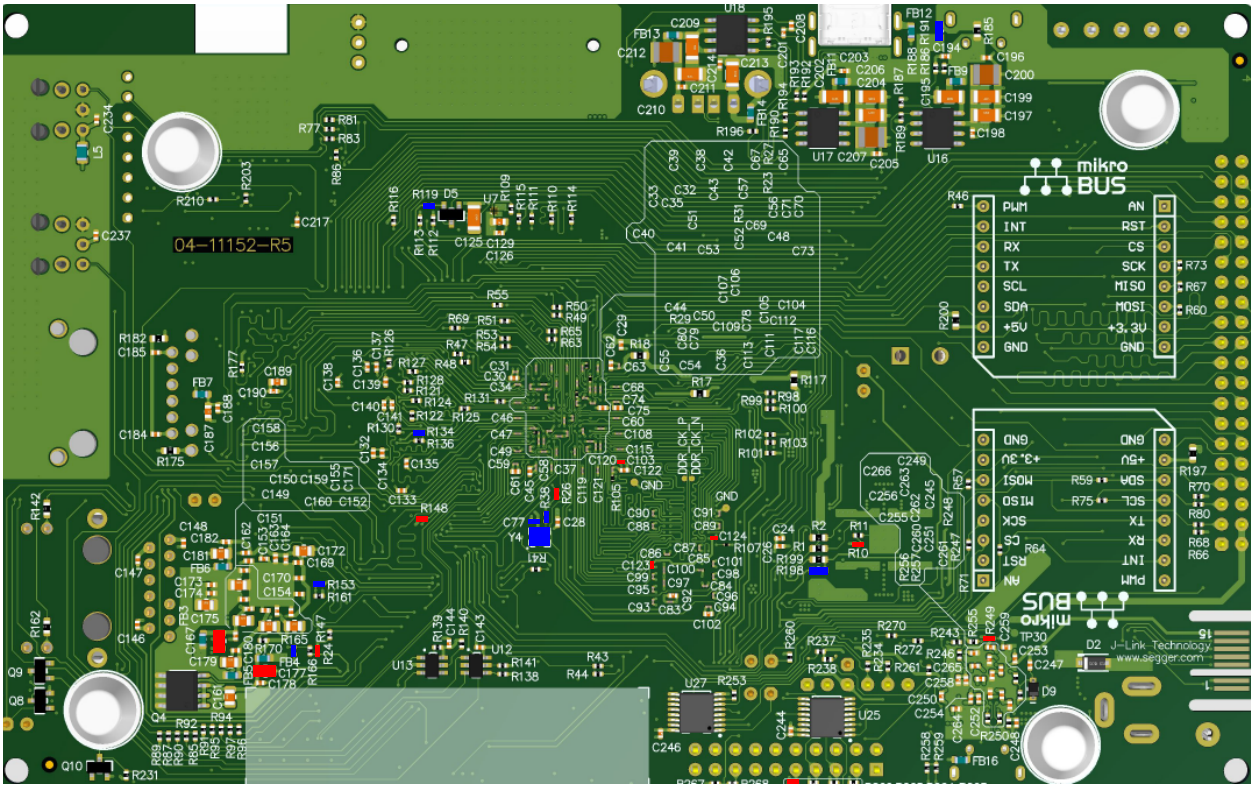
Table 7-1. Top Side Unmounted Elements

Ref.	Type	Feature	Color Status	Used for	What to do if mounted
C76	Capacitor	24 MHz	Blue	Crystal load capacitance	Remove R34 and R36.
C81	Capacitor	24 MHz	Blue	Crystal load capacitance	
R37	Resistor	24 MHz	Blue	Crystal selection	
R40	Resistor	24 MHz	Blue	Crystal selection	
Y3	Crystal	24 MHz	Blue	24 MHz crystal	
R39	Resistor	24 MHz	Red	Crystal measurement	Only use in factory. If mounted, the crystal behavior will be degraded.

.....continued

Ref.	Type	Feature	Color Status	Used for	What to do if mounted
C165	Capacitor	25 MHz RGMII	Blue	Crystal load capacitance	Remove R171.
C166	Capacitor	25 MHz RGMII	Blue	Crystal load capacitance	
R167	Resistor	25 MHz RGMII	Blue	Crystal selection	
R168	Resistor	25 MHz RGMII	Blue	Crystal selection	
Y5	Crystal	25 MHz RGMII	Blue	25 MHz crystal	
C192	Capacitor	25 MHz RMII	Blue	Crystal load capacitance	Remove R178.
C193	Capacitor	25 MHz RMII	Blue	Crystal load capacitance	
R181	Resistor	25 MHz RMII	Blue	Crystal selection	
R184	Resistor	25 MHz RMII	Blue	Crystal selection	
Y8	Crystal	25 MHz RMII	Blue	25 MHz crystal	
R183	Resistor	25 MHz RMII	Red	Crystal measurement	Only use in factory. If mounted, the crystal behavior will be degraded.
R35	Resistor	32 kHz	Red	Crystal measurement	Only use in factory. If mounted, the crystal behavior will be degraded.
U20	Module	ATWILC3000	Blue	ATWILC3000 module	–
J15	Connector	Debug	Blue	WILC3000 debug interface	–
J16	Connector	Debug	Blue	WILC3000 debug interface	–
R232	Resistor	Debug	Blue	Debug CTS pull-up	–
R233	Resistor	Debug	Blue	Debug RTS pull-up	–
R179	Resistor	nRST_OUT	Blue	nRST selection instead of NRST_OUT	Remove R180.
R118	Resistor	SD Card	Red	SDMMC1_1V8_SEL pull-up	–
C127	Capacitor	Supply	Red	VLDO1 decoupling	–
C128	Capacitor	Supply	Red	VDD_3V3 decoupling	Note: Excessive capacitor load on the MCP16502 DCDC or LDO lines can result in output instability and power-on sequence failure.
C220	Capacitor	Supply	Red	VDD_3V3_WILC decoupling	
C240	Capacitor	System	Blue	nSTART decoupling and startup configuration	The product starts automatically.
J14	Connector	Tamper	Blue	Tamper pins use	–
R164	Resistor	Ethernet RGMII	Red	Gigabit Ethernet 125 MHz clock line	–

Figure 7-2. Unmounted Components Overview: Bottom View



The following table lists the bottom side unmounted components and their functionalities.

Table 7-2. Bottom Side Unmounted Elements

Ref.	Type	Feature	Color Status	Used for	What to do if mounted
C77	Capacitor	32 kHz	Blue	MEMS oscillator decoupling	Remove Y1, C66 and C72.
R38	Resistor	32 kHz	Blue	MEMS oscillator selection	
Y4	MEMS oscillator	32 kHz	Blue	32 kHz MEMS generation	
R266	Resistor	Debug	Red	JTAG TCK pull-up	
R249	Resistor	J-Link-OB	Red	Boundary scan selection	If mounted, at boot the device enters in boundary scan. J-Link-OB will never start.
R134	Resistor	nRST_OUT	Blue	nRST selection instead of NRST_OUT	Remove R136.
R165	Resistor	nRST_OUT	Blue	nRST selection instead of NRST_OUT	Remove R166.
R198	Resistor	nRST_OUT	Blue	nRST selection instead of NRST_OUT	Remove R199.
R119	Resistor	nRST_OUT	Blue	NRST_OUT selection instead of SDMMC1_RSTN_PB28	If mounted, the SD Card can also be reset by the processor reset line.
R24	Resistor	nRST_OUT	Red	nRST_OUT pull-up	No impact
R10	Resistor	PMIC	Red	PMIC output voltage selection	Never mount this element. The VLDO1 output voltage is set to 1.8V for SD Card voltage selection. If changed, the SD Card interface might get destroyed.

.....continued					
Ref.	**Type**	**Feature**	**Color Status**	**Used for**	**What to do if mounted**
C103	Capacitor	SAMA7G5	Blue	DDR_VERF decoupling	No impact
C123	Capacitor	SAMA7G5	Red	DDR_VERF decoupling	
C124	Capacitor	SAMA7G5	Red	DDR_VERF decoupling	
R26	Resistor	SAMA7G5	Red	Boundary scan selection	If mounted, at boot the device enters in boundary scan.
R191	Resistor	Supply	Blue	Input supply selection	Remove R185.
C167	Capacitor	Supply	Red	AVDDH decoupling	–
C177	Capacitor	Supply	Red	DVDDH decoupling	Note: Excessive capacitor load on the MCP16502 DCDC or LDO lines can result in output instability and power-on sequence failure.
R148	Resistor	Ethernet RGMII	Red	TXCK pull-up	–
R153	Resistor	Ethernet RGMII	Blue	RXCTL pull-up	–

7.2 Soldering the Wi-Fi/BT Module

Extra care must be taken when assembling the ATWILC3000-MR110xA Wi-Fi/BT module.

Refer to the application note "How to Manually Solder the ATWILC3000 Module on an MPU Board". See Reference Documents.

8. Revision History

8.1 DS50003273B - 09/2023

DDR3L Memory: updated. Default Jumper Settings: updated.

8.2 DS50003273A - 03/2022

First issue.

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
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