MCP14E6/7/8

2.0A Dual High-Speed Power MOSFET Driver With Enable

Features

- High Peak Output Current: 2.0A (typical)
- Independent Enable Function for Each Driver Output
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- Low Shoot-Through/Cross-Conduction Current in Output Stage
- High Capacitive Load Drive Capability:
  - t_R: 12 ns with 1000 pF load (typical)
  - t_F: 15 ns with 1000 pF load (typical)
- Short Delay Times: 45 ns (typical)
- Low Supply Current:
  - With Logic '`1`' Input/Enable – 1 mA (typical)
  - With Logic '`0`' Input/Enable – 300 µA (typical)
- Latch-up Protected: Passed JEDEC JESD78A
- Logic Input will Withstand Negative Swing, up to 5V
- Space-Saving Packages:
  - 8-Lead SOIC, PDIP, 6x5 DFN

Applications

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Motor and Solenoid Drive

General Description

The MCP14E6/7/8 devices are high-speed MOSFET drivers, capable of providing 2.0A of peak current. The dual inverting, dual non-inverting and complementary outputs are directly controlled from either TTL or CMOS (3V to 18V). These devices also feature low shoot-through current, fast rise/fall times and propagation delays, which make them ideal for high switching frequency applications.

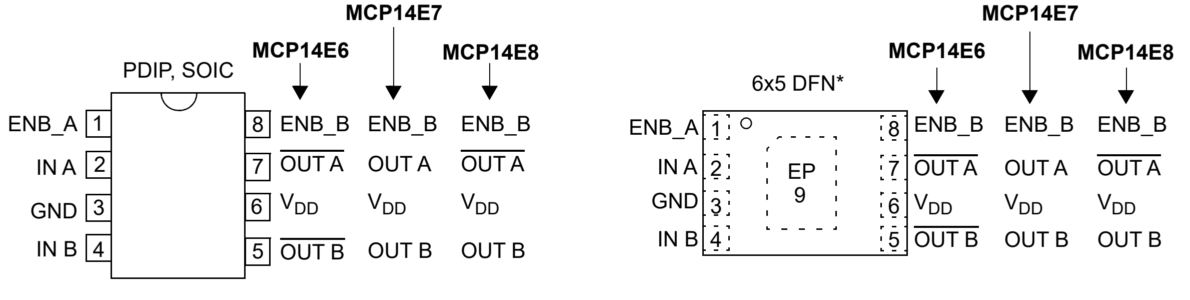
The MCP14E6/7/8 devices operate from a 4.5V to 18V single power supply and can easily charge and discharge 1000 pF of MOSFET gate capacitance. They provide low enough impedances, in both the ON and OFF states, to ensure the MOSFETs' intended state will not be affected, even by large transients.

The additional control of the MCP14E6/7/8 outputs is allowed by the use of separate enable functions. The ENB_A and ENB_B pins are active-high and are internally pulled up to V_{DD}. The pins may be left floating for standard operation.

The MCP14E6/7/8 dual output, 2.0A driver family is offered in both surface-mount and pin-through-hole packages with a -40°C to +125°C temperature rating. The low thermal resistance of the thermally enhanced DFN package allows greater power dissipation capability for driving heavier capacitive or resistive loads.

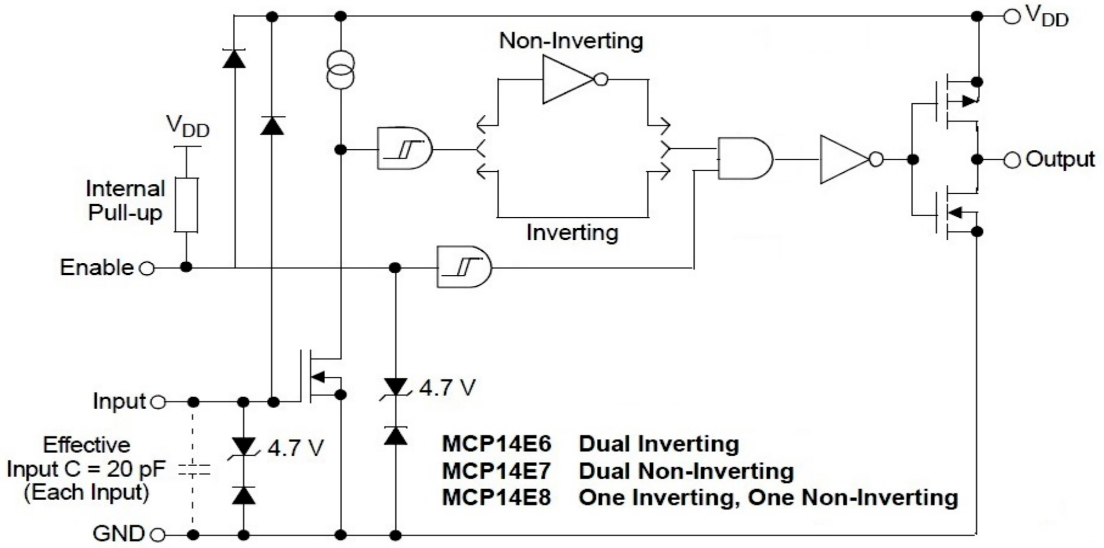
These devices are highly latch-up resistant under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. The devices are fully latch-up protected when tested according to JEDEC JESD78A. All terminals are fully protected against Electrostatic Discharge (ESD), up to 4 kV (HBM) or 400V (MM).

Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram(1)



Note 1: Unused inputs should be grounded.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage	+20V
Input Voltage	(V_{DD} + 0.3V) to (GND – 5V)
Enable Voltage	(V_{DD} + 0.3V) to (GND – 5V)
Input Current ($V_{IN} > V_{DD}$)	50 mA
Package Power Dissipation (T_A = +50°C)	
8L-DFN	Note 3
8L-PDIP	1.12W
8L-SOIC	669 mW

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS(2)

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic ‘1’, High Input Voltage	V_{IH}	2.4	1.5	—	V	
Logic ‘0’, Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Current	I_{IN}	-1	—	1	µA	0V ≤ V_{IN} ≤ V_{DD}
Input Voltage	V_{IN}	-5	—	V_{DD} + 0.3	V	
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	5	8	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	5	8	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	2	—	A	V_{DD} = 18V(2)
Switching Time(1)						
Rise Time	t_R	—	12	30	ns	Figure 4-1, Figure 4-2, C_L = 1000 pF
Fall Time	t_F	—	15	35	ns	Figure 4-1, Figure 4-2, C_L = 1000 pF
Propagation Delay Time	t_{D1}	—	45	55	ns	Figure 4-1, Figure 4-2
Propagation Delay Time	t_{D2}	—	45	55	ns	Figure 4-1, Figure 4-2
Enable Function (ENB_A, ENB_B)						
High-Level Input Voltage	V_{EN_H}	2.4	1.6	—	V	V_{DD} = 12V, Low-to-High Transition
Low-Level Input Voltage	V_{EN_L}	—	1.2	0.8	V	V_{DD} = 12V, High-to-Low Transition
Hysteresis	V_{HYST}	—	400	—	mV	
Enable Pull-up Impedance	R_{ENBL}	0.7	1.6	3.0	MΩ	V_{DD} = 14V, ENBL = GND
Enable Pin Leakage Current	I_{ENBL}	—	10	—	µA	V_{DD} = 12V, ENB_A = ENB_B = GND

Note 1: Switching times are ensured by design.

2: Tested during characterization, not production tested.

3: Package power dissipation is dependent on the copper pad area of the PCB.

DC CHARACTERISTICS[2] (CONTINUED)

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Propagation Delay Time	t_{D3}	—	35	65	ns	V_{DD} = 12V, Figure 4-3
Propagation Delay Time	t_{D4}	—	35	65	ns	V_{DD} = 12V, Figure 4-3
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18.0	V	
Supply Current	I_{DD}	—	1000	1800	µA	V_{IN_A} = 3V, V_{IN_B} = 3V, ENB_A = ENB_B = High
	I_{DD}	—	600	900	µA	V_{IN_A} = 0V, V_{IN_B} = 0V, ENB_A = ENB_B = High
	I_{DD}	—	800	1600	µA	V_{IN_A} = 3V, V_{IN_B} = 0V, ENB_A = ENB_B = High
	I_{DD}	—	800	1600	µA	V_{IN_A} = 0V, V_{IN_B} = 3V, ENB_A = ENB_B = High
	I_{DD}	—	600	1000	µA	V_{IN_A} = 3V, V_{IN_B} = 3V, ENB_A = ENB_B = Low
	I_{DD}	—	300	450	µA	V_{IN_A} = 0V, V_{IN_B} = 0V, ENB_A = ENB_B = Low
	I_{DD}	—	500	800	µA	V_{IN_A} = 3V, V_{IN_B} = 0V, ENB_A = ENB_B = Low
	I_{DD}	—	500	800	µA	V_{IN_A} = 0V, V_{IN_B} = 3V, ENB_A = ENB_B = Low

Note 1: Switching times are ensured by design.
2: Tested during characterization, not production tested.
3: Package power dissipation is dependent on the copper pad area of the PCB.

DC CHARACTERISTICS (OVER OPERATING TEMP. RANGE)[2]

Electrical Specifications: Unless otherwise indicated, operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic ‘`1`’, High Input Voltage	V_{IH}	2.4	—	—	V	
Logic ‘`0`’, Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	8	11		I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	8	11	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time[1]						
Rise Time	t_R	—	23	35	ns	Figure 4-1, Figure 4-2, C_L = 1000 pF
Fall Time	t_F	—	23	40	ns	Figure 4-1, Figure 4-2, C_L = 1000 pF
Propagation Delay Time	t_{D1}	—	50	65	ns	Figure 4-1, Figure 4-2
Propagation Delay Time	t_{D2}	—	50	65	ns	Figure 4-1, Figure 4-2

Note 1: Switching times are ensured by design.
2: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMP. RANGE)(2) (CONTINUED)

Electrical Specifications: Unless otherwise indicated, operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Enable Function (ENB_A, ENB_B)						
High-Level Input Voltage	V_{EN_H}	2.4	—	—	V	V_{DD} = 12V, Low-to-High Transition
Low-Level Input Voltage	V_{EN_L}	—	—	0.8	V	V_{DD} = 12V, High-to-Low Transition
Hysteresis	V_{HYST}	—	0.4	—	V	
Enable Pull-up Impedance	R_{ENBL}	0.7	1.6	3.0	MΩ	V_{DD} = 14V, ENB_A = ENB_B = GND
Propagation Delay Time	t_{D3}	—	60	80	ns	V_{DD} = 12V, **Figure 4-3**
Propagation Delay Time	t_{D4}	—	70	85	ns	V_{DD} = 12V, **Figure 4-3**
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18.0	V	
Supply Current	I_{DD}	—	1400	2200	µA	V_{IN_A} = 3V, V_{IN_B} = 3V, ENB_A = ENB_B = High
	I_{DD}	—	800	1100	µA	V_{IN_A} = 0V, V_{IN_B} = 0V, ENB_A = ENB_B = High
	I_{DD}	—	1300	2000	µA	V_{IN_A} = 3V, V_{IN_B} = 0V, ENB_A = ENB_B = High
	I_{DD}	—	1300	2000	µA	V_{IN_A} = 0V, V_{IN_B} = 3V, ENB_A = ENB_B = High
	I_{DD}	—	800	1200	µA	V_{IN_A} = 3V, V_{IN_B} = 3V, ENB_A = ENB_B = Low
	I_{DD}	—	500	600	µA	V_{IN_A} = 0V, V_{IN_B} = 0V, ENB_A = ENB_B = Low
	I_{DD}	—	600	900	µA	V_{IN_A} = 3V, V_{IN_B} = 0V, ENB_A = ENB_B = Low
	I_{DD}	—	600	900	µA	V_{IN_A} = 0V, V_{IN_B} = 3V, ENB_A = ENB_B = Low

Note 1: Switching times are ensured by design.

2: Tested during characterization, not production tested.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 8L-6x5 DFN	θ_{JA}	—	35.7	—	°C/W	Typical four-layer board with vias to ground plane
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25°C$ with $4.5V \le V_{DD} \le 18V$.

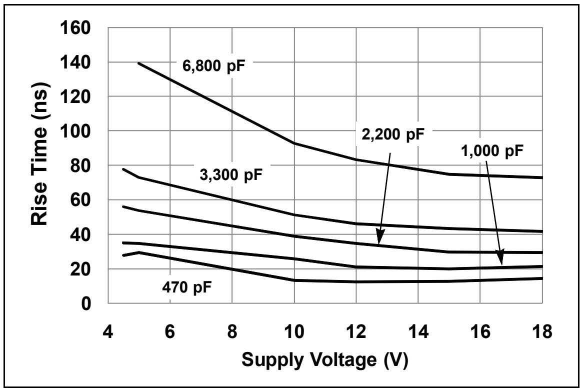


FIGURE 2-1: Rise Time vs. Supply Voltage.

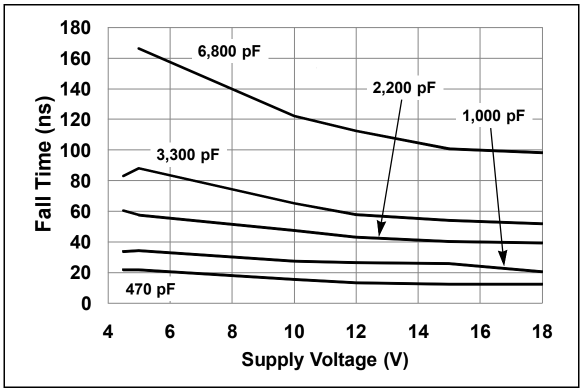


FIGURE 2-4: Fall Time vs. Supply Voltage.

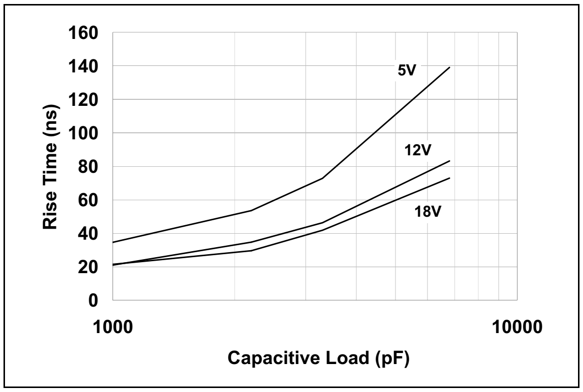


FIGURE 2-2: Rise Time vs. Capacitive Load.

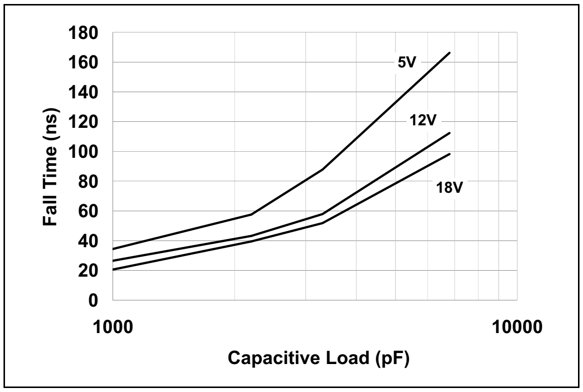


FIGURE 2-5: Fall Time vs. Capacitive Load.

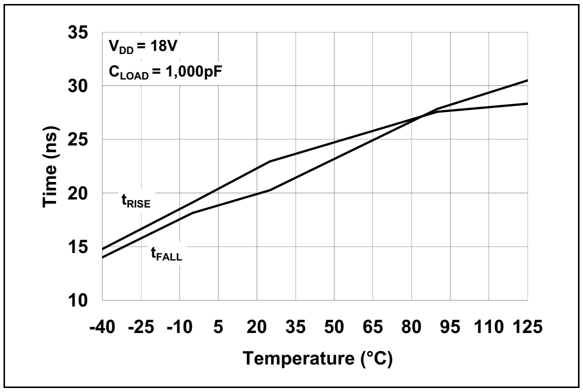


FIGURE 2-3: Rise and Fall Times vs. Temperature.

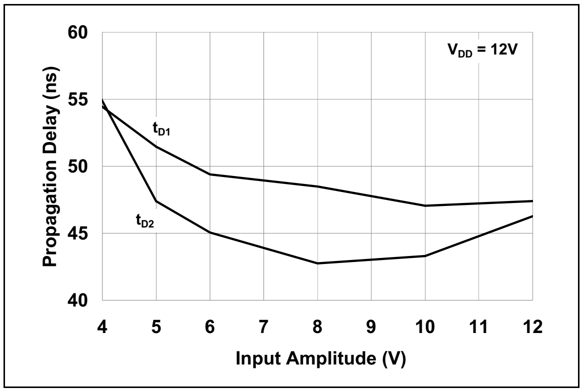


FIGURE 2-6: Propagation Delay vs. Input Amplitude.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

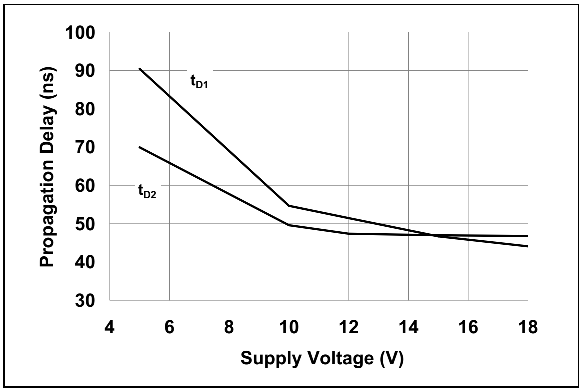


FIGURE 2-7: *Propagation Delay Time vs. Supply Voltage.*

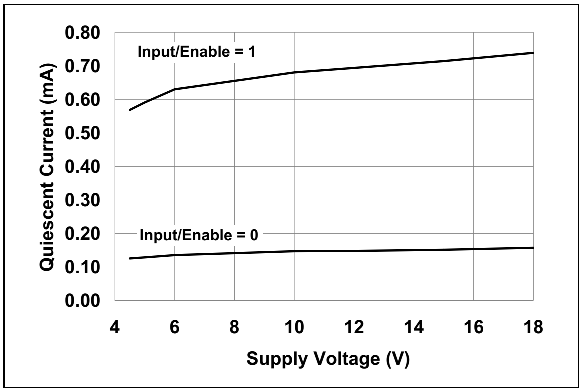


FIGURE 2-8: *Quiescent Current vs. Supply Voltage.*

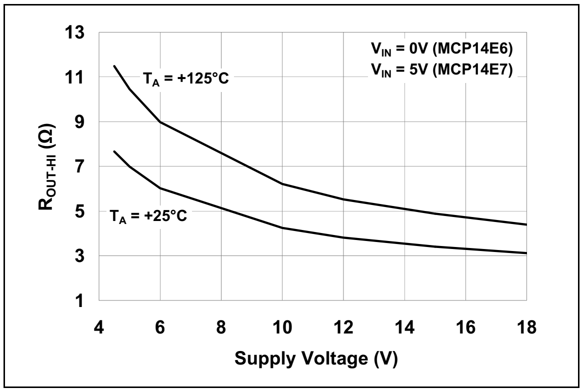


FIGURE 2-9: *Output Resistance (Output High) vs. Supply Voltage.*

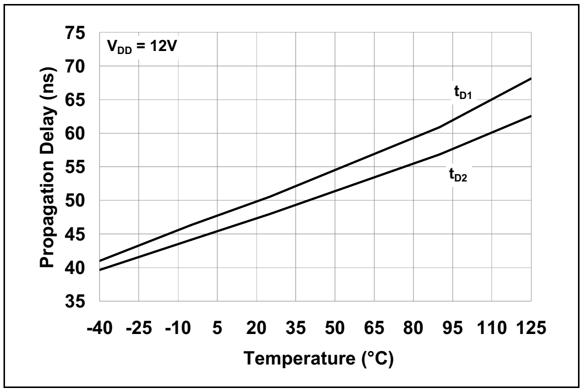


FIGURE 2-10: *Propagation Delay Time vs. Temperature.*

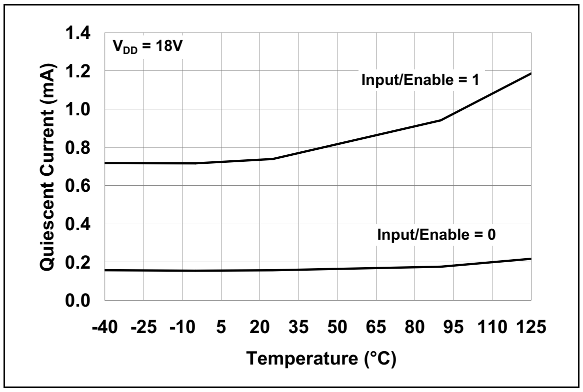


FIGURE 2-11: *Quiescent Current vs. Temperature.*

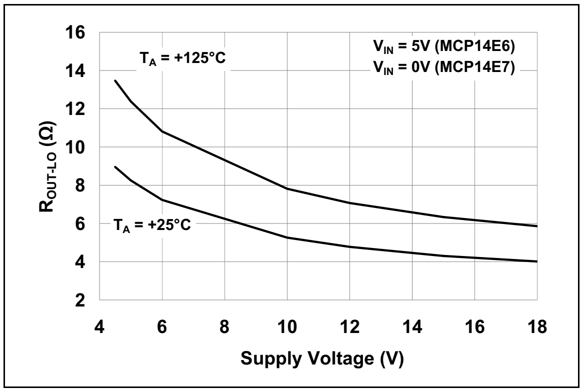


FIGURE 2-12: *Output Resistance (Output Low) vs. Supply Voltage.*

Note: Unless otherwise indicated, $T_A = +25°C$ with $4.5V \le V_{DD} \le 18V$.

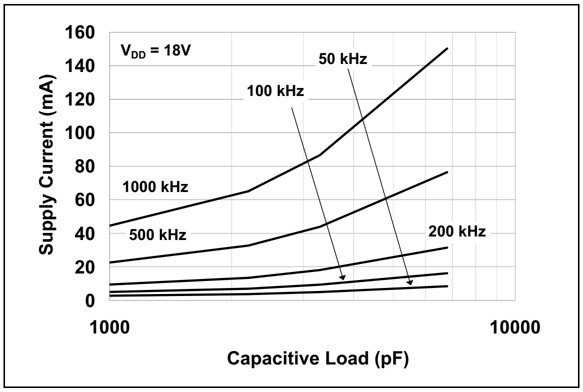


FIGURE 2-13: Supply Current vs. Capacitive Load.

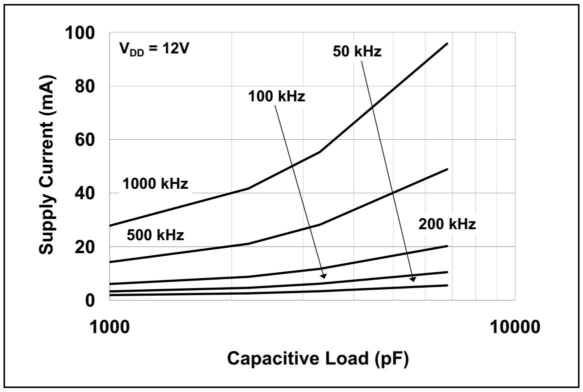


FIGURE 2-14: Supply Current vs. Capacitive Load.

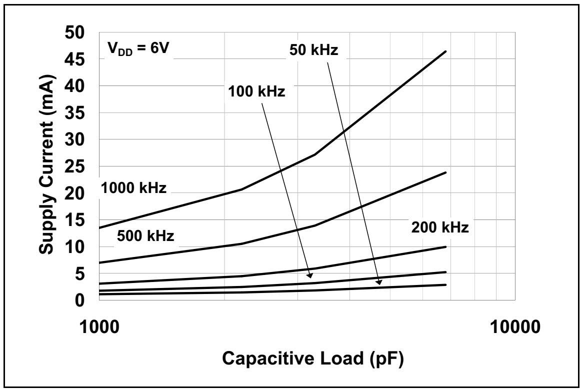


FIGURE 2-15: Supply Current vs. Capacitive Load.

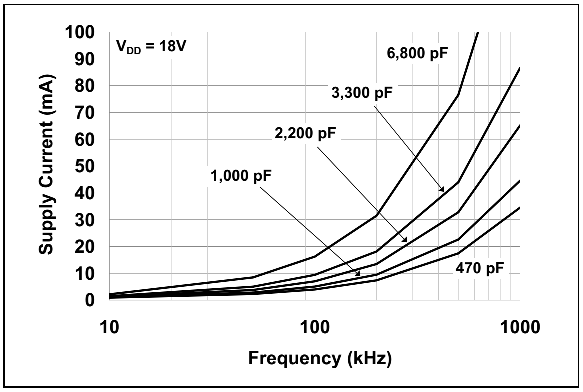


FIGURE 2-16: Supply Current vs. Frequency.

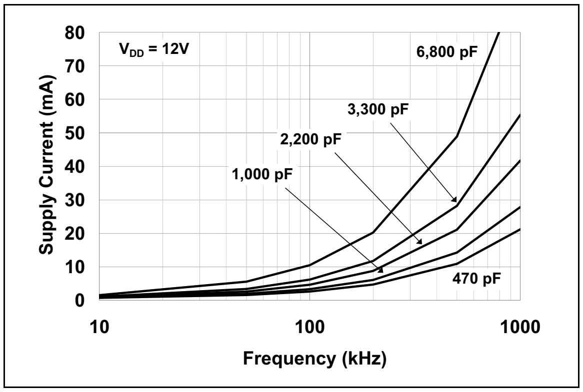


FIGURE 2-17: Supply Current vs. Frequency.

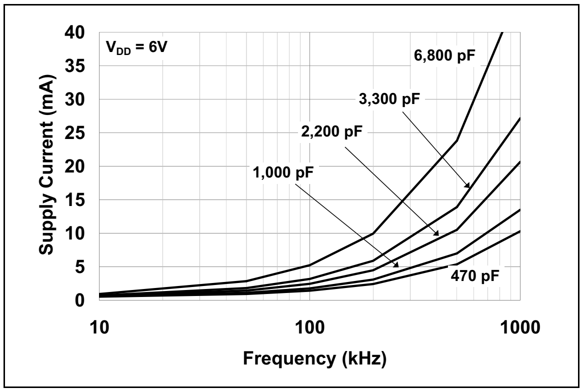


FIGURE 2-18: Supply Current vs. Frequency.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

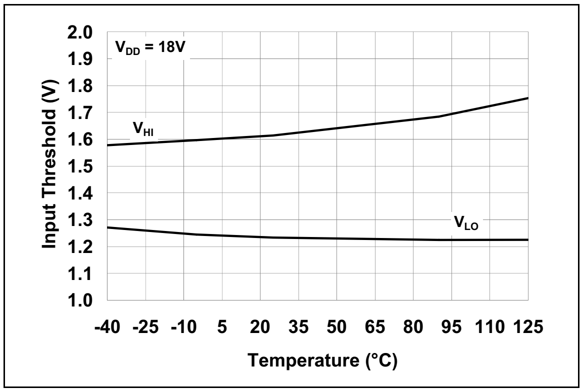


FIGURE 2-19: *Input Threshold vs. Temperature.*

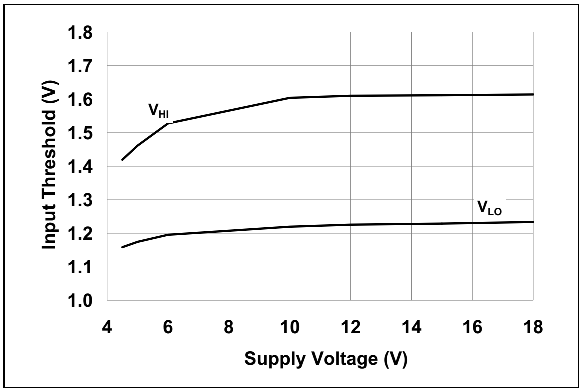


FIGURE 2-20: *Input Threshold vs. Supply Voltage.*

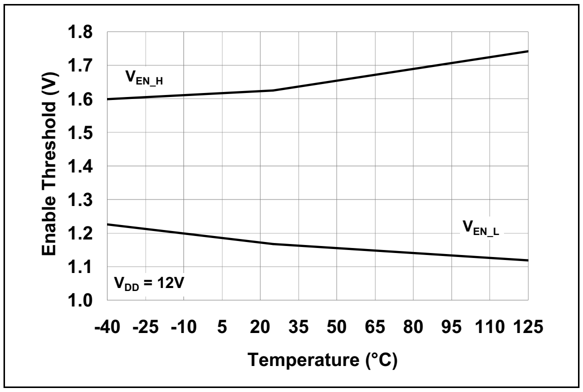


FIGURE 2-21: *Enable Threshold vs. Temperature.*

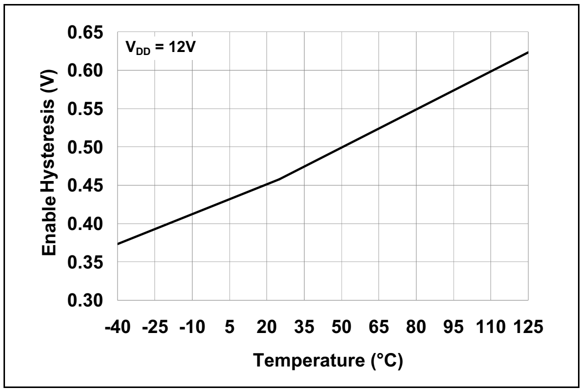
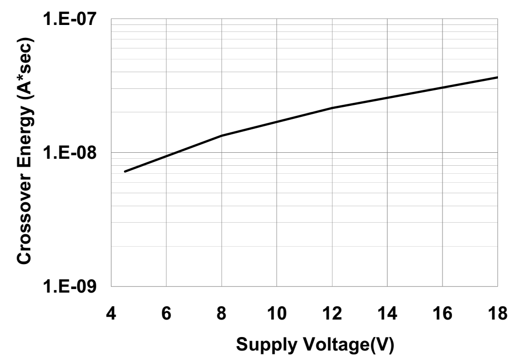


FIGURE 2-22: *Enable Hysteresis vs. Temperature.*



Note: The values in this graph represent the loss seen by both drivers in a package during a complete cycle.
For a single driver, divide the stated value by 2.
For a single transition of a single driver, divide the stated value by 4.

FIGURE 2-23: *Crossover Energy vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

PDIP, SOIC, 6x5 DFN	Symbol			Description
	MCP14E6	MCP14E7	MCP14E8	
1	ENB_A	ENB_A	ENB_A	Output A Enable
2	IN A	IN A	IN A	Input A
3	GND	GND	GND	Ground
4	IN B	IN B	IN B	Input B
5	$\overline{\text{OUT B}}$	OUT B	OUT B	Output B
6	V_{DD}	V_{DD}	V_{DD}	Supply Input
7	$\overline{\text{OUT A}}$	OUT A	$\overline{\text{OUT A}}$	Output A
8	ENB_B	ENB_B	ENB_B	Output B Enable
9	EP	EP	EP	Exposed Metal Pad (**DFN package only**). Exposed pad is electrically isolated.

3.1 Enable A (ENB_A)

The ENB_A pin is the enable control for Output A. This enable pin is internally pulled up to V_{DD} for active-high operation and can be left floating for standard operation. When the ENB_A pin is pulled below the enable pin, Low Level Input Voltage (V_{EN_L}), Output A will be in the OFF state, regardless of the input pin state.

3.2 Control Inputs A and B (IN A; IN B)

The MOSFET driver inputs are a high-impedance TTL/CMOS compatible input. The inputs also have hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals, and to provide noise immunity.

3.3 Ground (GND)

Ground is the device return pin. The ground pin should have a low-impedance connection to the bias supply source return. High peak currents will flow out the ground pin when the capacitive load is being discharged.

3.4 Outputs A and B (OUT A; OUT B)

Outputs, A and B, are CMOS push-pull outputs that are capable of sourcing and sinking 2.0A of peak current (V_{DD} = 18V). The low output impedance ensures the gate of the MOSFET will stay in the intended state, even during large transients.

3.5 Supply Input (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local ceramic capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are provided to the load.

3.6 Enable B (ENB_B)

The ENB_B pin is the enable control for Output B. This enable pin is internally pulled up to V_{DD} for active-high operation, and can be left floating for standard operation. When the ENB_B pin is pulled below the enable pin, Low-Level Input Voltage (V_{EN_L}), Output B will be in the OFF state, regardless of the input pin state.

3.7 Exposed Metal Pad (EP)

The exposed metal pad of the DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane, or other copper plane on a printed circuit board, to aid in heat removal from the package.

4.0 APPLICATION INFORMATION

4.1 General Information

MOSFET drivers are high-speed, high-current devices which are intended to source/sink high-peak currents to charge/discharge the gate capacitance of external MOSFETs, or insulated gate bipolar transistors (IGBTs). In high-frequency switching power supplies, the Pulse-Width Modulation (PWM) controller may not have the drive capability to directly drive the power MOSFET. MOSFET drivers, like the MCP14E6/7/8 family, can be used to provide additional source/sink current capability.

An additional degree of control has been added to the MCP14E6/7/8 family. There are seperate enable functions for each driver that allow for the immediate termination of the output pulse, regardless of the state of the input signal.

4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully OFF state to a fully ON state are characterized by the drivers' rise time (t_R), fall time (t_F) and propagation delays (t_{D1} and t_{D2}). The MCP14E6/7/8 family of drivers can typically charge and discharge a 1000 pF load capacitance, in approximately 12 ns, along with a typical matched propagation delay of 45 ns. Figure 4-1 and Figure 4-2 show the test circuit and timing waveform used to verify the MCP14E6/7/8 timing.

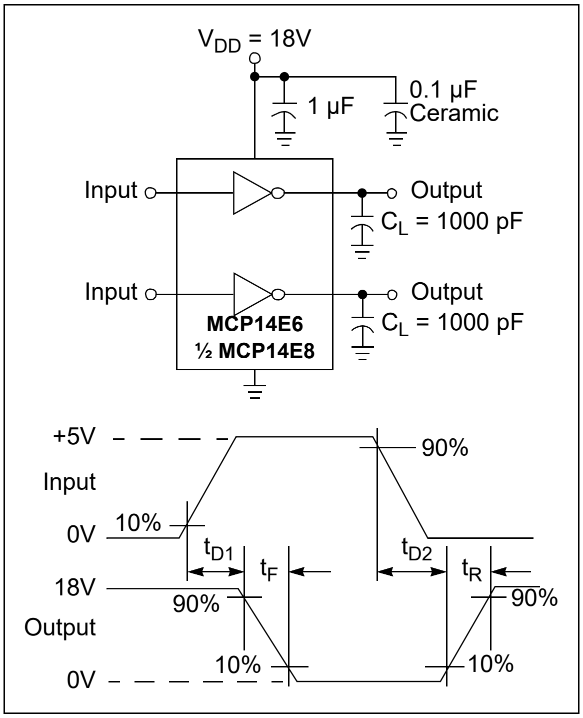


FIGURE 4-1: Inverting Driver Timing Waveform.

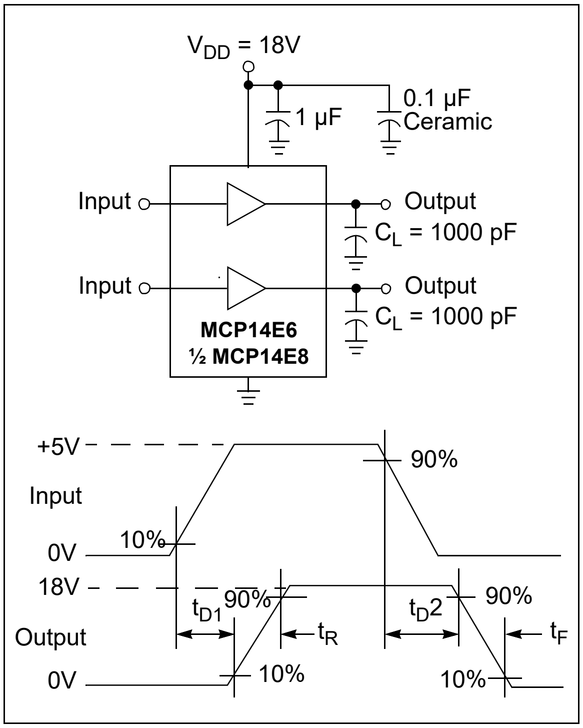


FIGURE 4-2: Non-Inverting Driver Timing Waveform.

4.3 Enable Function

The ENB_A and ENB_B enable pins allow the independent control of OUT A and OUT B, respectively. They are active-high and are internally pulled up to V_{DD} so that the default state is to enable the driver. These pins can be left floating for normal operation.

When an enable pin voltage is above enable pin high threshold voltage, (V_{EN_H}), that driver output is enabled and allowed to react to changes in the INPUT pin voltage state. Similarly, when the enable pin voltage falls below the enable pin low threshold voltage, (V_{EN_L}), that driver output is disabled and does not respond to the changes in the INPUT pin voltage state. When the driver is disabled, the output goes to a low state. Refer to Table 4-1 for enable pin logic. The threshold voltages of the enable function are compatible with logic levels. Hysteresis is provided to help increase the noise immunity of the enable function, avoiding false triggers of the enable signal during driver switching. For robust designs, it is recommended that the slew rate of the enable pin signal be greater than 1V/ns.

There are propagation delays associated with the driver receiving an enable signal and the output reacting. These propagation delays, t_{D3} and t_{D4}, are graphically represented in Figure 4-3.

TABLE 4-1: ENABLE PIN LOGIC

				MCP14E6		MCP14E7		MCP14E8	
ENB_A	**ENB_B**	**IN A**	**IN B**	**OUT A**	**OUT B**	**OUT A**	**OUT B**	**OUT A**	**OUT B**
H	H	H	H	L	L	H	H	L	H
H	H	H	L	L	H	H	L	L	L
H	H	L	H	H	L	L	H	H	H
H	H	L	L	H	H	L	L	H	L
L	L	X	X	L	L	L	L	L	L

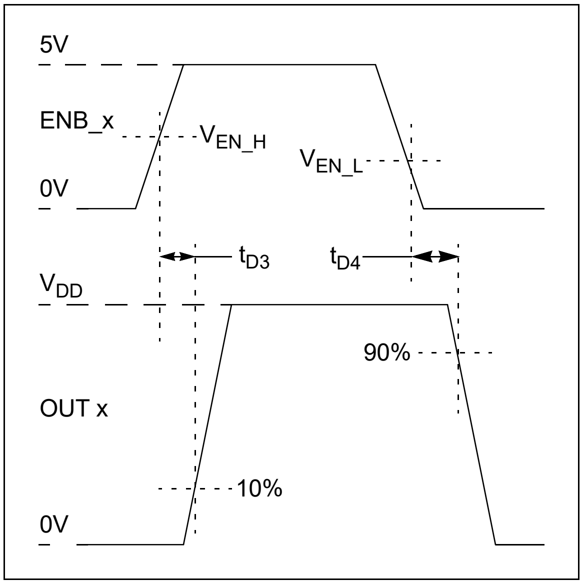


FIGURE 4-3: *Enable Timing Waveform.*

4.4 Decoupling Capacitors

Careful layout and decoupling capacitors are highly recommended when using MOSFET drivers. Large currents are required to charge and discharge capacitive loads quickly. For example, approximately 1.8A are needed to charge a 1000 pF load with 18V in 10 ns.

To operate the MOSFET driver over a wide frequency range, with low supply impedance, a ceramic and low-ESR film capacitors are recommended to be placed in parallel between the driver, V_{DD} and GND. A 1.0 µF low-ESR film capacitor and a 0.1 µF ceramic capacitor placed between pins, 6 and 3, should be used. These capacitors should be placed close to the driver to minimize the circuit board parasitics and provide a local source for the required current.

4.5 PCB Layout Considerations

Proper PCB layout is important in a high-current, fast switching circuit to provide proper device operation and robustness to the design. The PCB trace loop area and inductance should be minimized by the use of ground planes or trace under MOSFET gate drive signals, separate analog and power grounds, and local driver decoupling.

Placing a ground plane beneath the MCP14E6/7/8 will help as a radiated noise shield, as well as providing some heat sinking for power dissipated within the device.

4.6 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements (Figure 4-1).

EQUATION 4-1:

$$P_T = P_L + P_Q + P_{CC}$$

Where:

P_T = Total Power Dissipation
P_L = Load Power Dissipation
P_Q = Quiesent Power Dissipation
P_{CC} = Operating Power Dissipation

4.6.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of frequency, total capacitive load and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is:

EQUATION 4-2:

$$P_L = f \times C_T \times V_{DD}^{\ 2}$$

Where:

f = Switching frequency
C_T = Total load capacitance
V_{DD} = MOSFET driver supply voltage

4.6.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw depends upon the state of the input pin. The MCP14E6/7/8 devices have a quiescent current draw with a Logic '`1`' on the input pin of 1 mA (typical) and 300 µA (typical) with a Logic '`0`'. The quiescent power dissipation is:

EQUATION 4-3:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

I_{QH} = Quiescent Current in the High State
D = Duty Cycle
I_{QL} = Quiescent Current in the Low State
V_{DD} = MOSFET Driver Supply Voltage

4.6.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions, because for a very short period of time, both MOSFETs in the output stage are ON, simultaneously. This cross-conduction current leads to a power dissipation described as:

EQUATION 4-4:

$$P_{CC} = CC \times f \times V_{DD}$$

Where:

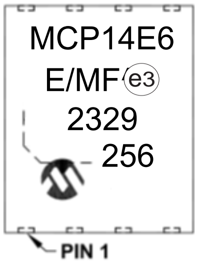
CC = Cross-Conduction Constant (A * sec)
f = Switching Frequency
V_{DD} = MOSFET Driver Supply Voltage

5.0 PACKAGING INFORMATION

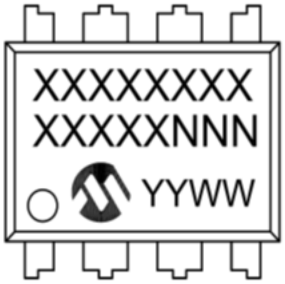
5.1 Package Marking Information

8-Lead DFN-S (5x6x1 mm)

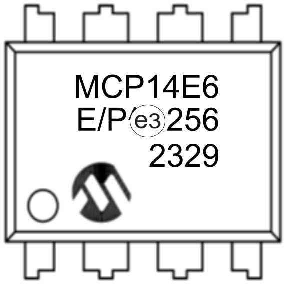
Example



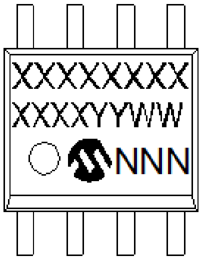
8-Lead PDIP



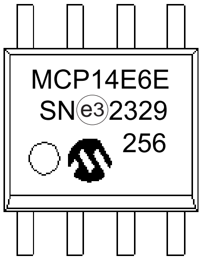
Example



8-Lead SOIC (.150”)



Example

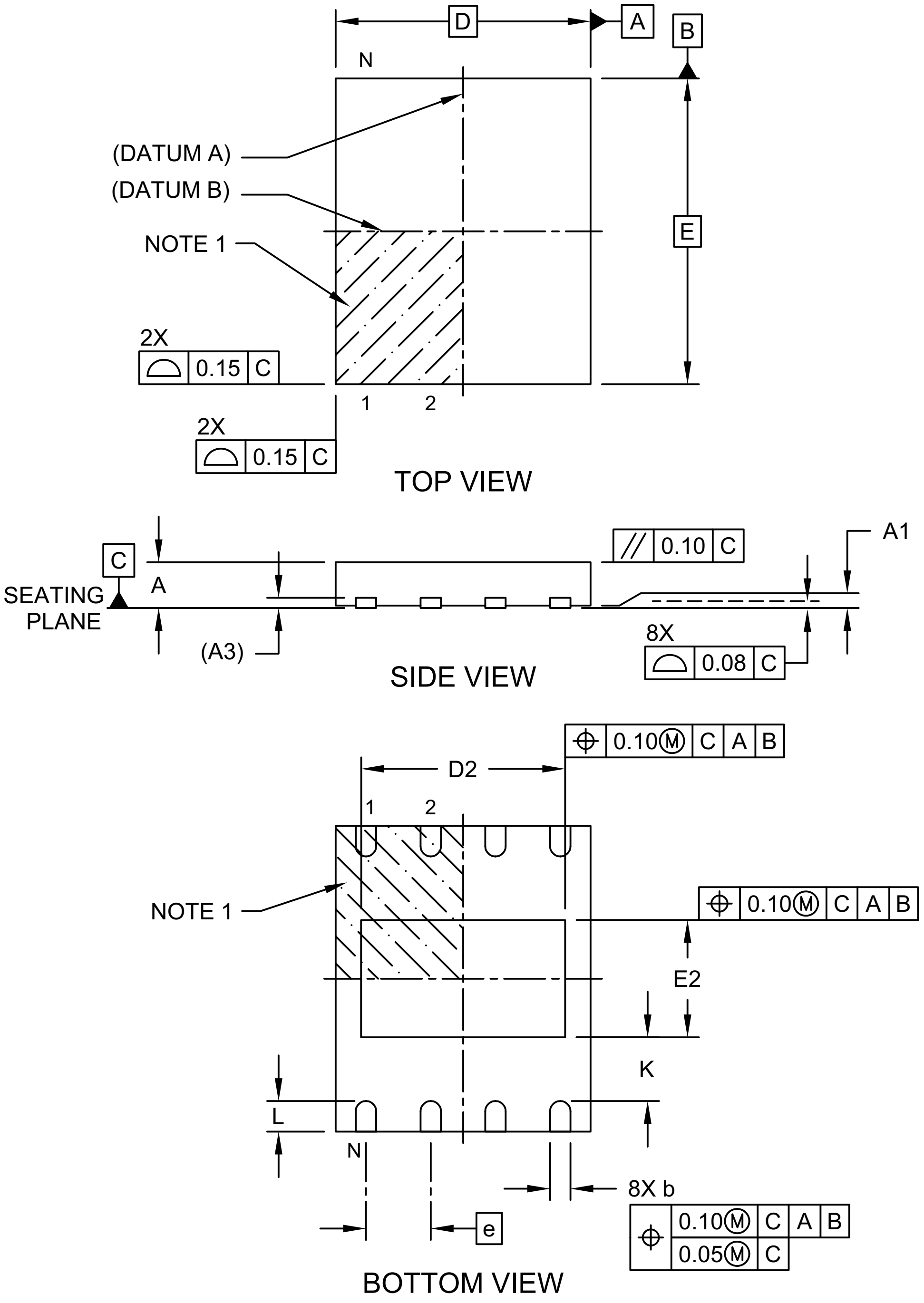


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

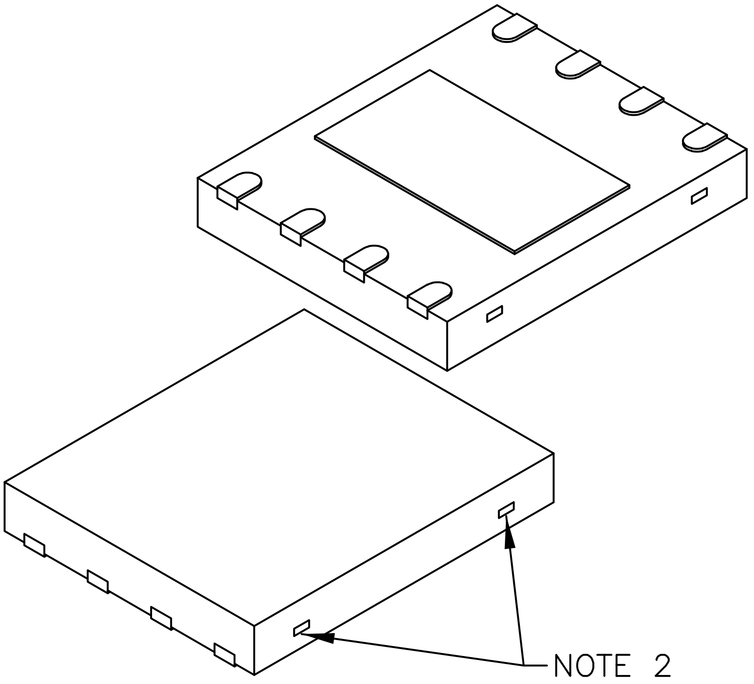
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-122 Rev D Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.90	4.00	4.10
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	2.20	2.30	2.40
Terminal Width	b	0.30	0.40	0.50
Terminal Length	L	0.50	0.60	0.75
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one ore more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

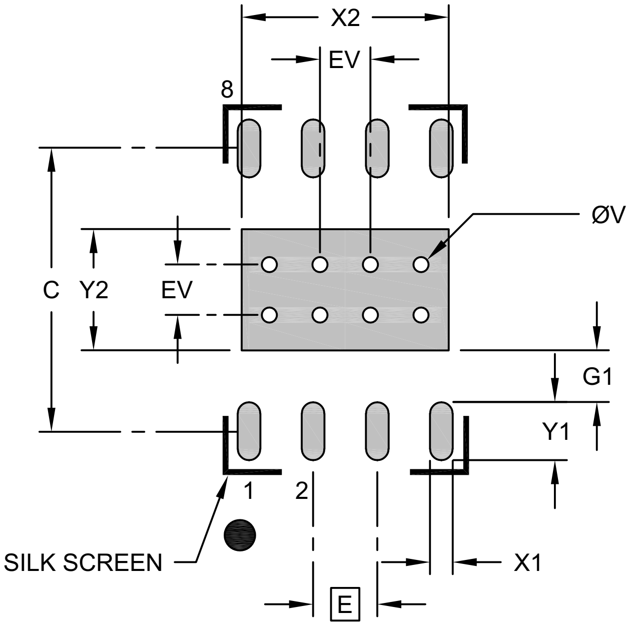
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122 Rev D Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Optional Center Pad Length	X2			4.10
Optional Center Pad Width	Y2			2.40
Contact Pad Spacing	C		5.60	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.15
Contact Pad to Center Pad (X20)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

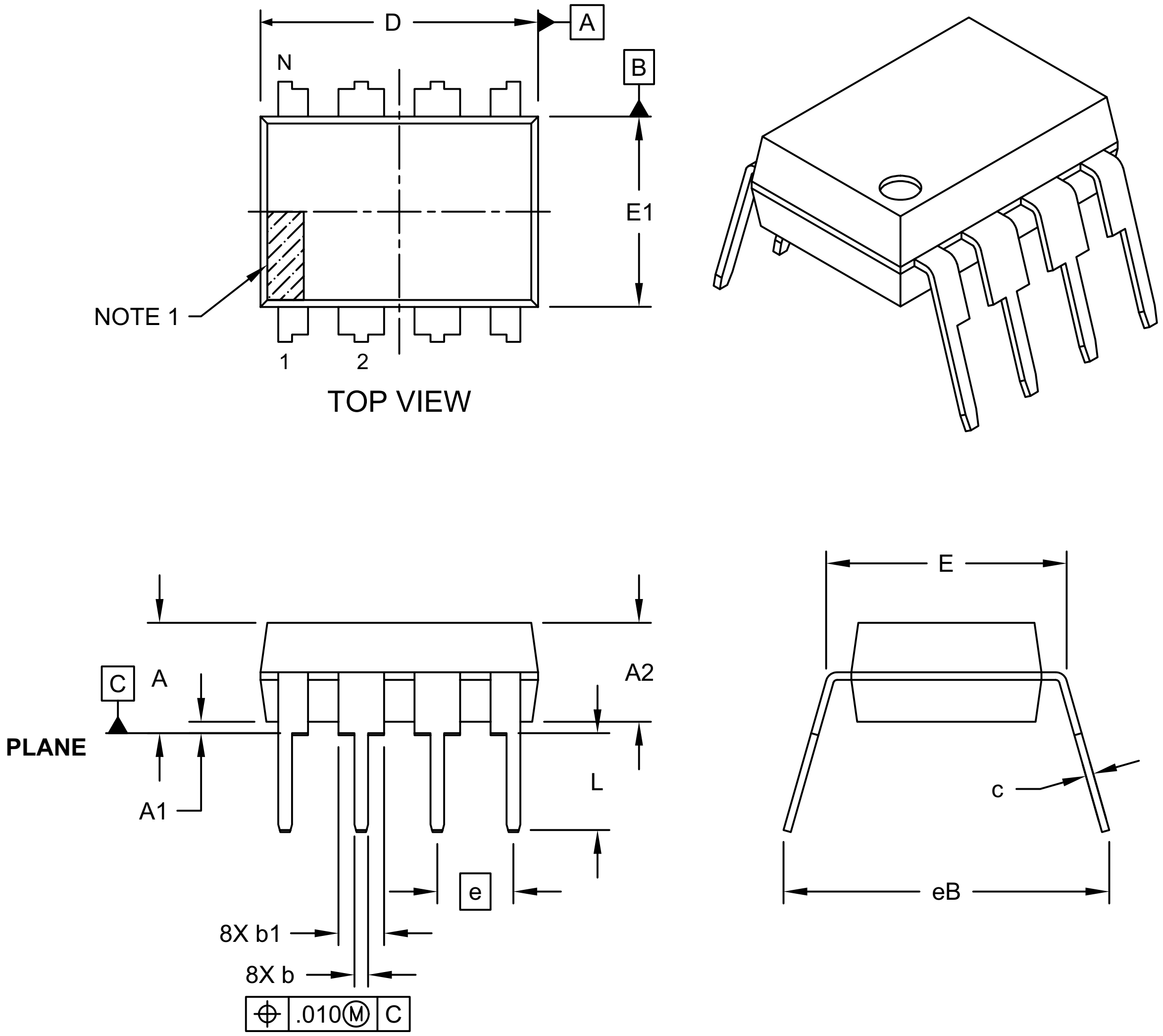
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2122 Rev D

8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

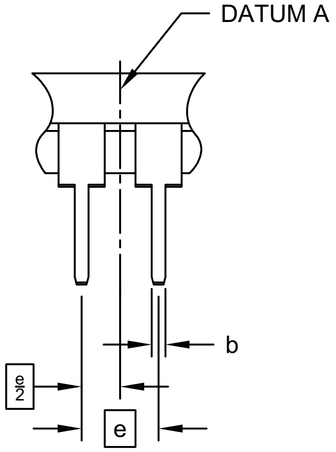
SIDE VIEW

END VIEW

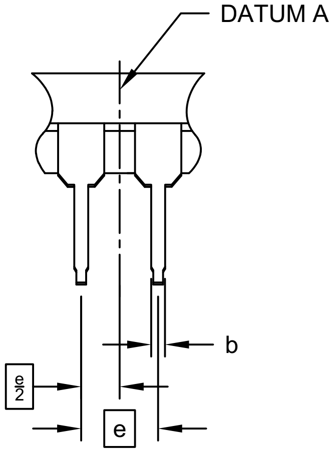
Microchip Technology Drawing No. C04-018-PA Rev F Sheet 1 of 2

8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



ALTERNATE LEAD DESIGN
(NOTE 5)



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

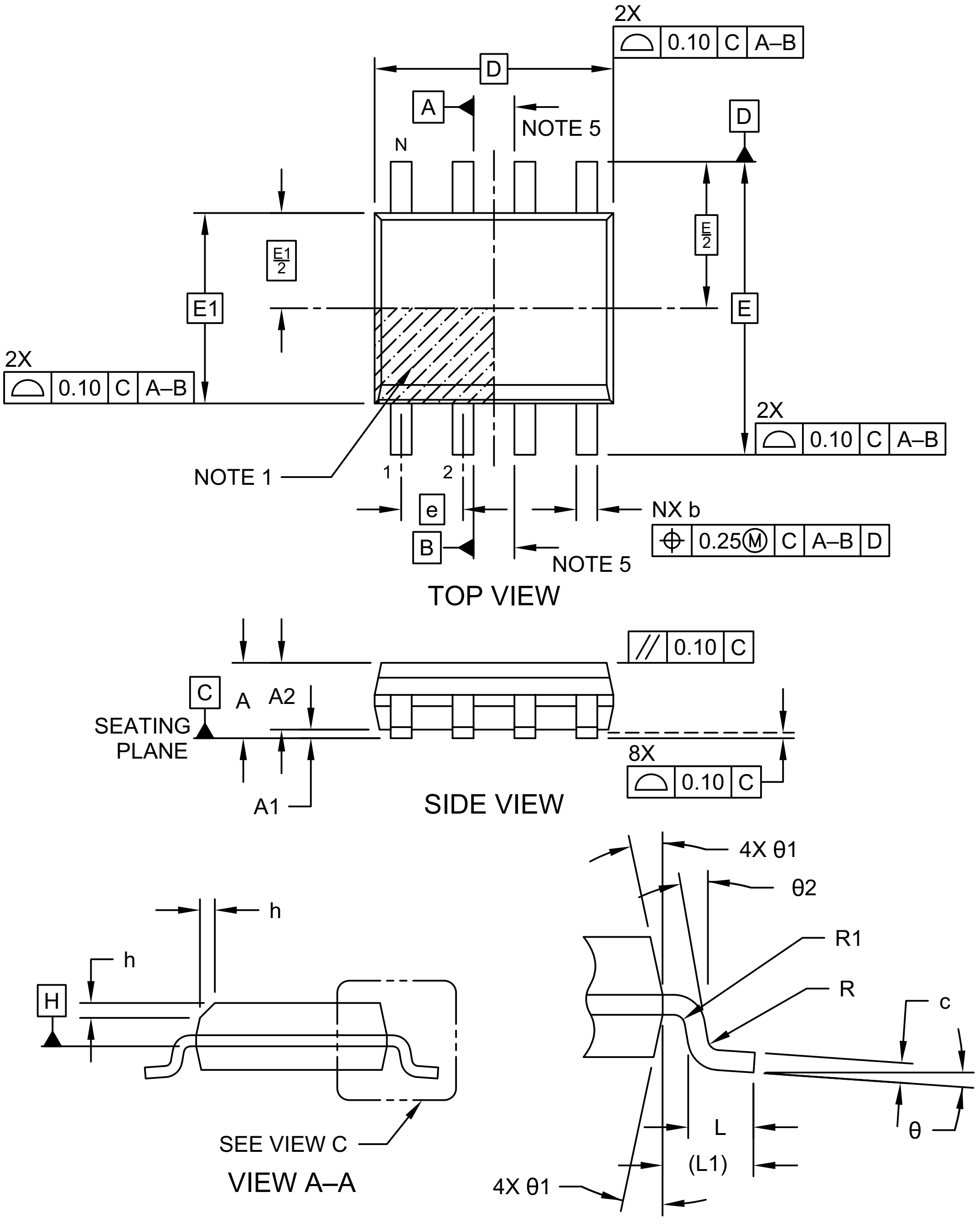
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-PA Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

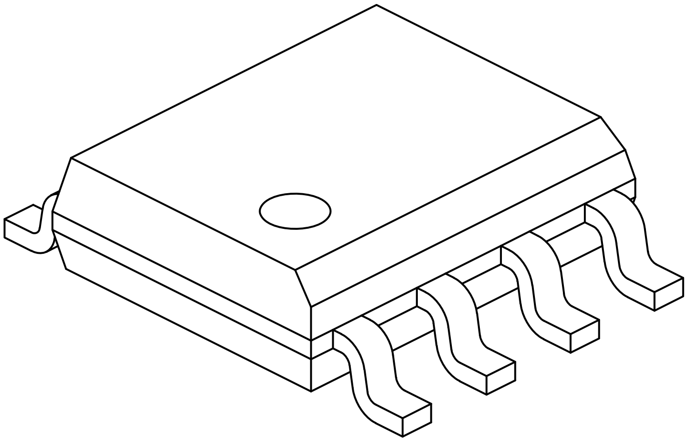
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

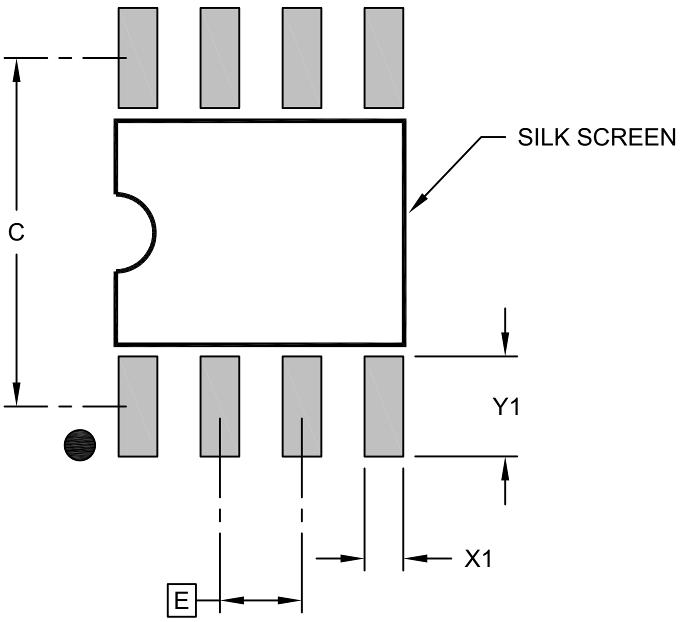
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-C2X Rev K

APPENDIX A: REVISION HISTORY

Revision B (August 2023)

- Updated Functional Block Diagram.
- Updated Section 5.0, Packaging Information.
- Minor text and format changes throughout.

Revision A (March 2011)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	**-X**	**/XX**
Device	**Temperature Range**	**Package**

Device:	MCP14E6:	2.0A Dual MOSFET Driver, Inverting
	MCP14E6T:	2.0A Dual MOSFET Driver, Inverting, Tape and Reel (DFN and SOIC only)
	MCP14E7:	2.0A Dual MOSFET Driver, Non-Inverting
	MCP14E7T:	2.0A Dual MOSFET Driver, Non-Inverting, Tape and Reel (DFN and SOIC only)
	MCP14E8:	2.0A Dual MOSFET Driver, Complementary
	MCP14E8T:	2.0A Dual MOSFET Driver, Complementary, Tape and Reel (DFN and SOIC only)

Temperature Range: E = -40°C to +125°C

Package: *
MF = Dual, Flat, No Lead (6x5 mm Body), 8-lead
P = Plastic DIP, (300 mil body), 8-lead
SN = Plastic SOIC (150 mil Body), 8-lead

Examples:

a) MCP14E6-E/MF: 2.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD 6x5 DFN package
b) MCP14E6T-E/MF: 2.0A Dual Inverting MOSFET Driver, Extended Temperature, Tape and Reel 8LD 6x5 DFN package
c) MCP14E6-E/P: 2.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD PDIP package
d) MCP14E6-E/SN: 2.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD SOIC package
e) MCP14E6T-E/SN: 2.0A Dual Inverting MOSFET Driver, Tape and Reel, Extended Temperature, 8LD SOIC package

a) MCP14E7-E/MF: 2.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD 6x5 DFN package
b) MCP14E7-E/P: 2.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD PDIP package
c) MCP14E7-E/SN: 2.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD SOIC package

a) MCP14E8-E/MF: 2.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD 6x5 DFN package
b) MCP14E8-E/P: 2.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD PDIP package
c) MCP14E8-E/SN: 2.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD SOIC package

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