Datasheet

APM32F103xB

Arm® Cortex® -M3 based 32-bit MCU

Chip version: Version E

Manual version: V 1.1

1 Product characteristics

System and Architecture

- 32-bit Arm® Cortex®-M3 core
- Up to 96MHz working frequency

Clock and memory

- HSECLK: 4MHz~16 MHz external crystal oscillator supported
- LSECLK: 32.768KHz crystal/ceramic oscillator supported
- HSICLK: 8MHz RC oscillator calibrated by factory
- LSICLK: 40KHz RC oscillator
- Flash capacity is up to 128KB
- SRAM capacity is up to 36KB

Power supply and low-power mode

- Reset power supply voltage 2.0V~3.6V
- Programmable voltage detector (PVD) supported
- Sleep, stop and standby three low-power modes supported
- V_{BAT} power supply can support RTC and backup register to work

ADC and Temperature sensor

- 2 12bit-precision ADC, supporting 16 input channels
- ADC voltage conversion range: 0~V_{DDA}
- Support double sampling and holding functions
- 1 internal temperature sensor

I/O

- 80/51/37/26 I/O can be selected, which is determined by package model
- All I/O can be mapped to 16 external interrupts

DMA

- 1 DMA, supporting 7 independent configurable channels

Timer

- 1 16-bit advanced timer TMR1, which supports dead zone control and emergency braking functions
- 3 16-bit general-purpose timers TMR2/3/4, each with up to 4 independent channels to support input capture, output compare, PWM, pulse count and other functions
- 2 watchdog timers, which are independent IWDT and window WWDT respectively
- 1 24-bit autodecrement system timer SysTick Timer

Communication interfaces

- 3 USART, supporting ISO7816, LIN and IrDA functions
- 2 I2C, supporting SMBus/PMBus
- 2 SPI, with up to 18Mbps transmission speed
- 1 QSPI, supporting single-line and four-line access to flash and DMA
- 1 USB 2.0 FS Device
- 2 CAN 2.0B; USBD and CAN can work independently at the same time

1 CRC unit

96-bit UID

Serial wire debug SWD and JTAG interfaces

Chip packaging

- LQFP100/LQFP64/LQFP48/QFN36

Applications

- Medical devices, PC peripherals, industrial control, smart meters and household appliance

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2 Product information

See the following table for APM32F103xB product functions and peripheral configuration.

Table1 Functions and Peripherals of APM32F103xB Series Chips

Product		**APM32F103xB**							
Model		T8U6	TBUx	C8T6	CBT6	R8T6	RBTx	V8T6	VBT6
Package		QFN36		LQFP48		LQFP64		LQFP100	
Core and maximum working frequency		Arm® 32-bit Cortex®-M3@96MHz							
Working voltage		2.0~3.6V							
Flash(KB)		64	128	64	128	64	128	64	128
SRAM(KB)		36							
GPIOs		26		37		51		80	
Communication interface	USART	2		3					
	SPI	1		2					
	QSPI	0						1	
	CAN	2							
	I2C	1		2					
	USBD	1							
Timer	16-bit advanced	1							
	16-bit general	3							
	System tick timer	1							
	Watchdog	2							
Real-time clock		1							
12-bit ADC	Unit	2							
	Number of channels	10				16			
Operating temperature		Ambient temperature: -40℃ to 85℃/-40℃ to 105℃ Junction temperature: -40℃ to 105℃/-40℃ to 125℃							

Note: When x is 6, ambient temperature is from -40℃ to 85℃, and the junction temperature is from -40℃ to 105℃;

When x is 7, ambient temperature is from -40℃ to 105℃, and the junction temperature is from -40℃ to 125℃.

3 Pin information

3.1 Pin distribution

Figure 1 Distribution Diagram of APM32F103xB Series LQFP100 Pins

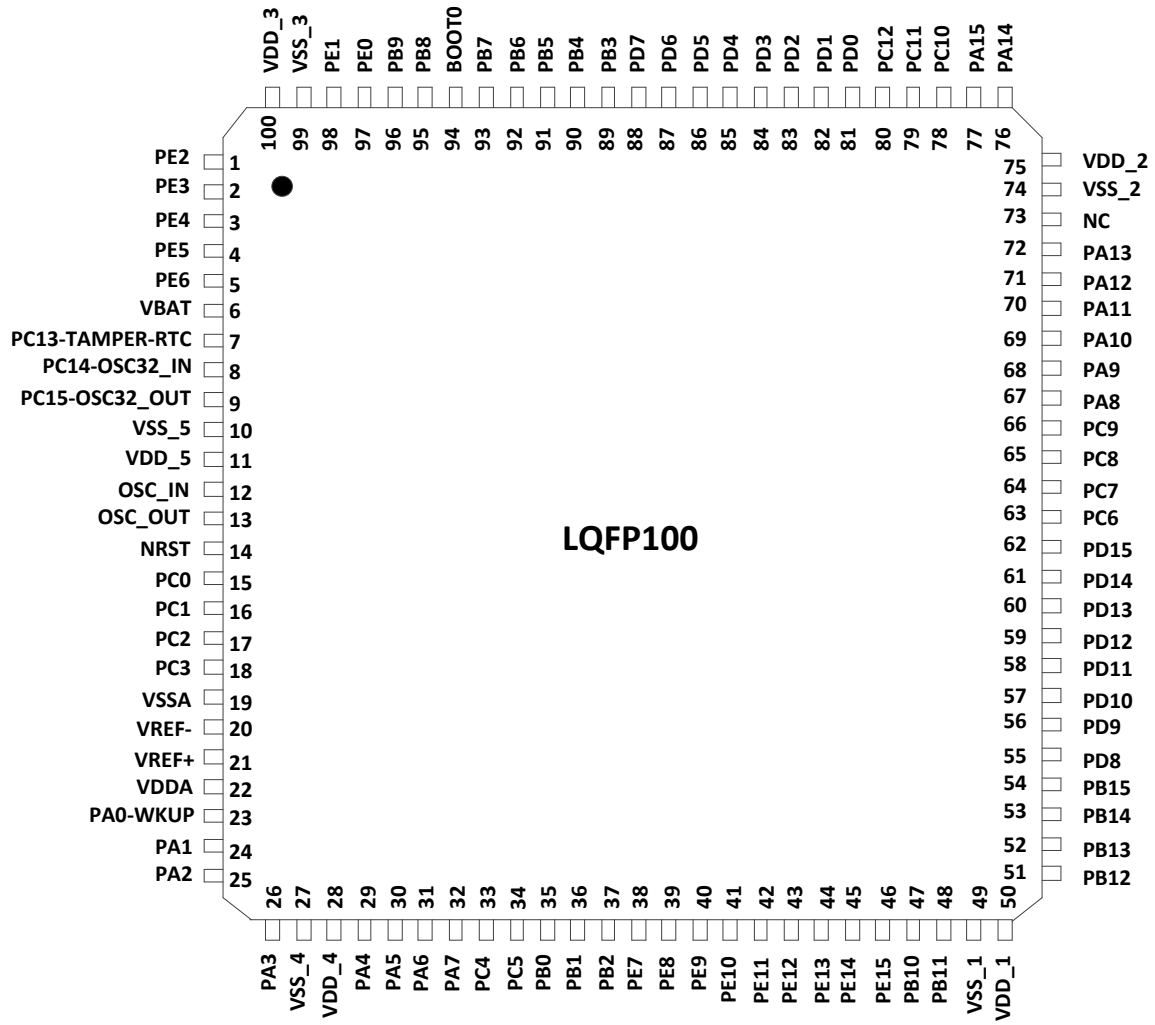


Figure 2 Distribution Diagram of APM32F103xB Series LQFP64 Pins

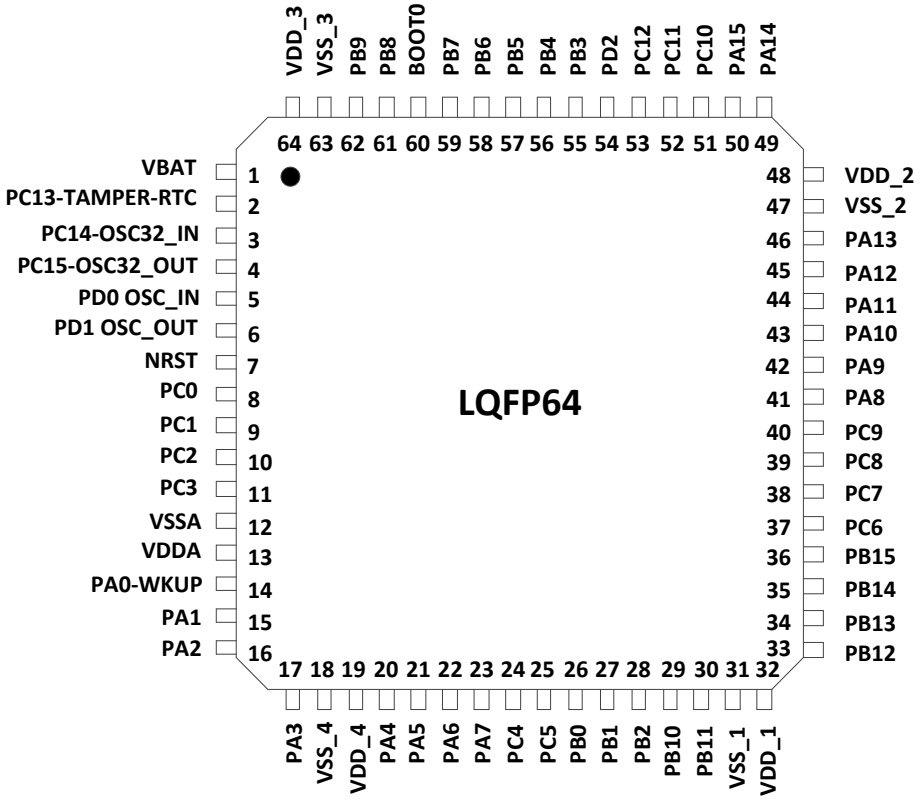


Figure 3 Distribution Diagram of APM32F103xB Series LQFP48 Pins

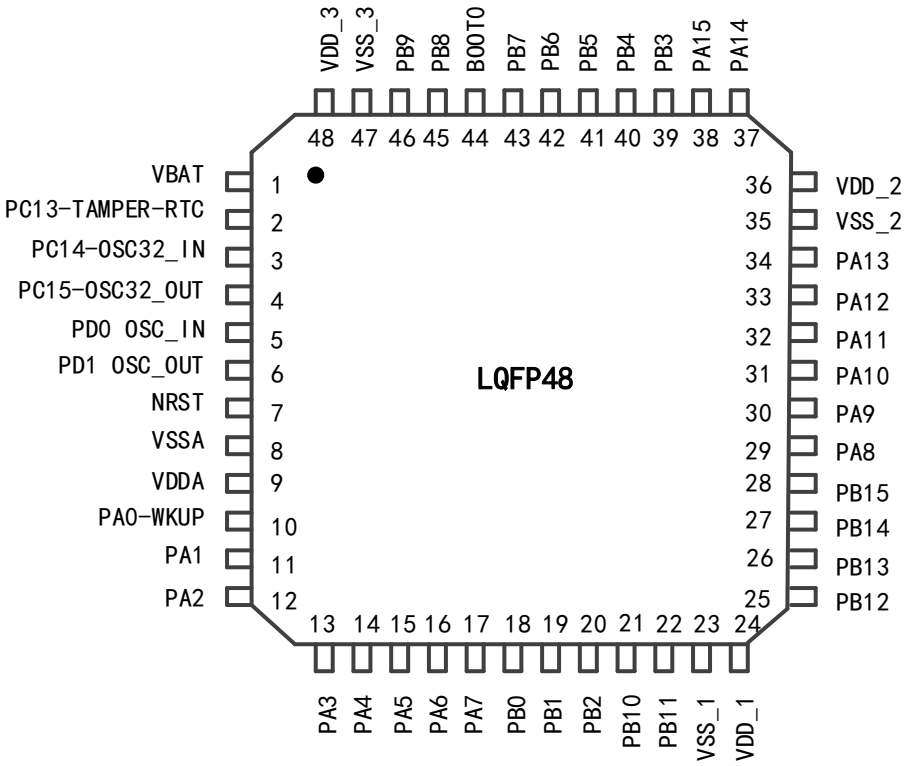
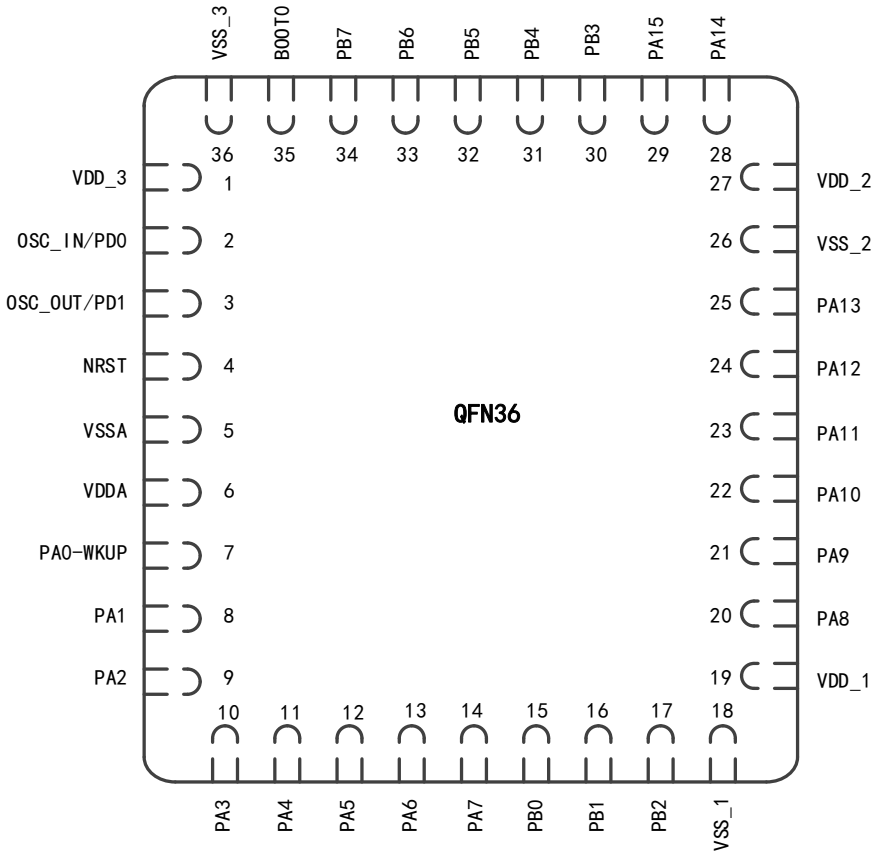


Figure 4 Distribution Diagram of APM32F103xB Series QFN36 Pins



3.2 Pin function description

Table2 Legends/Abbreviations Used in Output Pin Table

Name		Abbreviations	Definitions
Pin Name		Unless otherwise specified in the bracket below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		S	Power pin
		I	Only input pin
		I/O	I/O pin
I/O structure		FT	FT I/O
		5Tf	FT I/O, FM+ function
		STDA	3.3V standard I/O, directly connected to ADC
		STD	3.3V standard I/O
		BOOT0	Dedicated Boot0 pin
		NRST	Bidirectional reset pin with built-in weak pull-up resistor
Cautions		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin	Default	Select/enable this function directly through peripheral register	

Name		Abbreviations	Definitions
function	multiplexing function		
	Redefining function	Select this function through AFIO remapping register	

Table3 APM32F103xB Pin Function Description

Pin Name	Pin No.				Type (1)	I/O level (2)	Main function (3)	Optional multiplexing function	
	LQFP48	LQFP64	LQFP100	QFN36			(After reset)	Default multiplexing function	Redefining function
PE2	-	-	1	-	I/O	FT	PE2	TRACECK	-
PE3	-	-	2	-	I/O	FT	PE3	TRACED0	-
PE4	-	-	3	-	I/O	FT	PE4	TRACED1	-
PE5	-	-	4	-	I/O	FT	PE5	TRACED2	-
PE6	-	-	5	-	I/O	FT	PE6	TRACED3	-
V_{BAT}	1	1	6	-	S	-	V_{BAT}	-	-
PC13-TAMPER-RTC(4)	2	2	7	-	I/O	-	PC13(3)	TAMPER-RTC	-
PC14-OSC32_IN(4)	3	3	8	-	I/O	-	PC14(3)	OSC32_IN	-
PC15-OSC32_OUT(4)	4	4	9	-	I/O	-	PC15(3)	OSC32_OUT	-
V_{SS_5}	-	-	10	-	S	-	V_{SS_5}	-	-
V_{DD_5}	-	-	11	-	S	-	V_{DD_5}	-	-
OSC_IN	5	5	12	2	I	-	OSC_IN	-	PD0(5)
OSC_OUT	6	6	13	3	O	-	OSC_OUT	-	PD1(5)
NRST	7	7	14	4	I/O	-	NRST	-	-
PC0	-	8	15	-	I/O	-	PC0	ADC12_IN10	-
PC1	-	9	16	-	I/O	-	PC1	ADC12_IN11	-
PC2	-	10	17	-	I/O	-	PC2	ADC12_IN12	-
PC3	-	11	18	-	I/O	-	PC3	ADC12_IN13	-
V_{SSA}	8	12	19	5	S	-	V_{SSA}	-	-
V_{REF-}	-	-	20	-	S	-	V_{REF-}	-	-
V_{REF+}	-	-	21	-	S	-	V_{REF}+	-	-
V_{DDA}	9	13	22	6	S	-	V_{DDA}	-	-
PA0-WKUP	10	14	23	7	I/O	-	PA0	WKUP/ USART2_CTS(6)/ ADC12_IN0/ TMR2_CH1_ETR(6)	-
PA1	11	15	24	8	I/O	-	PA1	USART2_RTS(6)/ ADC12_IN1/ TMR2_CH2(6)	-

Pin Name	Pin No.				Type (1)	I/O level (2)	Main function (3) (After reset)	Optional multiplexing function	
	LQFP48	LQFP64	LQFP100	QFN36				Default multiplexing function	Redefining function
PA2	12	16	25	9	I/O	-	PA2	USART2_TX(6)/ ADC12_IN2/ TMR2_CH3(6)	-
PA3	13	17	26	10	I/O	-	PA3	USART2_RX(6)/ ADC12_IN3/ TMR2_CH4(6)	-
V_{SS_4}	-	18	27	-	S	-	V_{SS_4}	-	-
V_{DD_4}	-	19	28	-	S	-	V_{DD_4}	-	-
PA4	14	20	29	11	I/O	-	PA4	SPI1_NSS(6)/ USART2_CK(6)/ ADC12_IN4	-
PA5	15	21	30	12	I/O	-	PA5	SPI1_SCK(6)/ ADC12_IN5	-
PA6	16	22	31	13	I/O		PA6	SPI1_MISO(6)/ ADC12_IN6/ TMR3_CH1(6)	TMR1_BKIN
PA7	17	23	32	14	I/O		PA7	SPI1_MOSI(6)/ ADC12_IN7/ TMR3_CH2(6)	TMR1_CH1N
PC4	-	24	33	-	I/O	-	PC4	ADC12_IN14	-
PC5	-	25	34	-	I/O	-	PC5	ADC12_IN15	-
PB0	18	26	35	15	I/O	-	PB0	ADC12_IN8/ TMR3_CH3(6)	TMR1_CH2N
PB1	19	27	36	16	I/O	-	PB1	ADC12_IN9/ TMR3_CH4(6)	TMR1_CH3N
PB2	20	28	37	17	I/O	FT	PB2/BOOT1	-	-
PE7	-	-	38	-	I/O	FT	PE7	-	TMR1_ETR
PE8	-	-	39	-	I/O	FT	PE8	-	TMR1_CH1N
PE9	-	-	40	-	I/O	FT	PE9	-	TMR1_CH1
PE10	-	-	41	-	I/O	FT	PE10	-	TMR1_CH2N
PE11	-	-	42	-	I/O	FT	PE11	-	TMR1_CH2
PE12	-	-	43	-	I/O	FT	PE12	-	TMR1_CH3N
PE13	-	-	44	-	I/O	FT	PE13	-	TMR1_CH3
PE14	-	-	45	-	I/O	FT	PE14	-	TMR1_CH4
PE15	-	-	46	-	I/O	FT	PE15	-	TMR1_BKIN
PB10	21	29	47	-	I/O	FT	PB10	I2C2_SCL/ USART3_TX(6)	TMR2_CH3
PB11	22	30	48	-	I/O	FT	PB11	I2C2_SDA/ USART3_RX(6)	TMR2_CH4

Pin Name	Pin No.				Type (1)	I/O level (2)	Main function (3)	Optional multiplexing function	
	LQFP48	LQFP64	LQFP100	QFN36			(After reset)	Default multiplexing function	Redefining function
V_{SS_1}	23	31	49	18	S	-	V_{SS_1}	-	-
V_{DD_1}	24	32	50	19	S	-	V_{DD_1}	-	-
PB12	25	33	51	-	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBAI/ USART3_CK(6)/ TMR1_BKIN(6))/ CAN2_RX	
PB13	26	34	52	-	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(6)/ TMR1_CH1N(6)/ QSPI_IO0/ CAN2_TX	
PB14	27	35	53	-	I/O	FT	PB14	SPI2_MISO/ USART3_RTS(6)/ TMR1_CH2N(6)/ QSPI_IO1	
PB15	28	36	54	-	I/O	FT	PB15	SPI2_MOSI/ TMR1_CH3N(6)/ QSPI_IO2	-
PD8	-	-	55	-	I/O	FT	PD8	QSPI_IO3	USART3_TX
PD9	-	-	56	-	I/O	FT	PD9	-	USART3_RX
PD10	-	-	57	-	I/O	FT	PD10	QSPI_CLK	USART3_CK
PD11	-	-	58	-	I/O	FT	PD11	-	USART3_CTS
PD12	-	-	59	-	I/O	FT	PD12	QSPI_SS_N	TMR4_CH1/ USART3_RTS
PD13	-	-	60	-	I/O	FT	PD13	-	TMR4_CH2
PD14	-	-	61	-	I/O	FT	PD14	-	TMR4_CH3
PD15	-	-	62	-	I/O	FT	PD15	-	TMR4_CH4
PC6	-	37	63	-	I/O	FT	PC6	-	TMR3_CH1
PC7	-	38	64	-	I/O	FT	PC7	-	TMR3_CH2
PC8	-	39	65	-	I/O	FT	PC8	-	TMR3_CH3
PC9	-	40	66	-	I/O	FT	PC9	-	TMR3_CH4
PA8	29	41	67	20	I/O	FT	PA8	USART1_CK/ TMR1_CH1(6)/ MCO	-
PA9	30	42	68	21	I/O	FT	PA9	USART1_TX(6)/ TMR1_CH2(6)	-

Pin Name	Pin No.				Type (1)	I/O level (2)	Main function (3)	Optional multiplexing function	
	LQFP48	LQFP64	LQFP100	QFN36			(After reset)	Default multiplexing function	Redefining function
PA10	31	43	69	22	I/O	FT	PA10	USART1_RX(6)/ TMR1_CH3(6)	-
PA11	32	44	70	23	I/O	FT	PA11	USART1_CTS/ USBD1DM/ USBD2DM/ CAN1_RX(6)/ TMR1_CH4(6)	-
PA12	33	45	71	24	I/O	FT	PA12	USART1_RTS/ USBD1DP USBD2DP/ CAN1_TX(6)/ TMR1_ETR(6)	-
PA13	34	46	72	25	I/O	FT	JTMS/ SWDIO	-	PA13
Not connected	-	-	73	-	-	-	-	Not connected	-
V_{SS_2}	35	47	74	26	S		V_{SS_2}	-	-
V_{DD_2}	36	48	75	27	S		V_{DD_2}	-	-
PA14	37	49	76	28	I/O	FT	JTCK/ SWCLK	-	PA14
PA15	38	50	77	29	I/O	FT	JTDI	-	TMR2_CH1_ ETR/ PA15/ SPI1_NSS
PC10	-	51	78	-	I/O	FT	PC10	-	USART3_TX
PC11	-	52	79	-	I/O	FT	PC11	-	USART3_RX
PC12	-	53	80	-	I/O	FT	PC12	-	USART3_CK
PD0	-	-	81	2	I/O	FT	PD0	-	CAN1_RX
PD1	-	-	82	3	I/O	FT	PD1	-	CAN1_TX
PD2	-	54	83	-	I/O	FT	PD2	TMR3_ETR	-
PD3	-	-	84	-	I/O	FT	PD3	-	USART2_CTS
PD4	-	-	85	-	I/O	FT	PD4	-	USART2_RTS
PD5	-	-	86	-	I/O	FT	PD5	-	USART2_TX
PD6	-	-	87	-	I/O	FT	PD6	-	USART2_RX
PD7	-	-	88	-	I/O	FT	PD7	-	USART2_CK

Pin Name	Pin No.				Type (1)	I/O level (2)	Main function (3)	Optional multiplexing function	
	LQFP48	LQFP64	LQFP100	QFN36			(After reset)	Default multiplexing function	Redefining function
PB3	39	55	89	30	I/O	FT	JTDO	-	PB3/ TRACESWO/ TMR2_CH2/ SPI1_SCK
PB4	40	56	90	31	I/O	FT	NJTRST	-	PB4/ TMR3_CH1/ SPI1_MISO
PB5	41	57	91	32	I/O	-	PB5	I2C1_SMBAI	TMR3_CH2/ SPI1_MOSI/ CAN2_RX
PB6	42	58	92	33	I/O	FT	PB6	I2C1_SCL(6)/ TMR4_CH1(6)	USART1_TX/ CAN2_TX
PB7	43	59	93	34	I/O	FT	PB7	I2C1_SDA(6)/ TMR4_CH2(6)	USART1_RX
BOOT0	44	60	94	35	I	-	BOOT0	-	-
PB8	45	61	95	-	I/O	FT	PB8	TMR4_CH3(6)	I2C1_SCL/ /CAN1_RX
PB9	46	62	96	-	I/O	FT	PB9	TMR4_CH4(6)	I2C1_SDA /CAN1_TX
PE0	-	-	97	-	I/O	FT	PE0	TMR4_ETR	-
PE1	-	-	98	-	I/O	FT	PE1	-	-
V_{SS_3}	47	63	99	36	S	-	V_{SS_3}	-	-
V_{DD_3}	48	64	100	1	S	-	V_{DD_3}	-	-

1. Power supply capacity of PC13, PC14 and PC15 pins is weak. Therefore, there are the following restrictions on these three pins: only one pin can be used as an output at the same time, and can only work in 2MHz mode, the maximum driving load is 30pF, and they cannot be used as a current source (such as driving LED).
2. The status of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system).
3. For Pin 2 and Pin 3 of QFN36 package, and Pin 5 and Pin 6 of LQFP48 and LQFP64 package, the default configuration after the chip is reset is OSC_IN and OSC_OUT function pins, and the software can reset these two pins with PD0 and PD1 functions; for LQFP100 package, PD0 and PD1 are inherent function pins.
4. This multiplexing function can be configured to other pins by software (if the corresponding package model has this pin). For details, please refer to the multiplexing function I/O section and debugging setting section of the user manual.

4 Functional Description

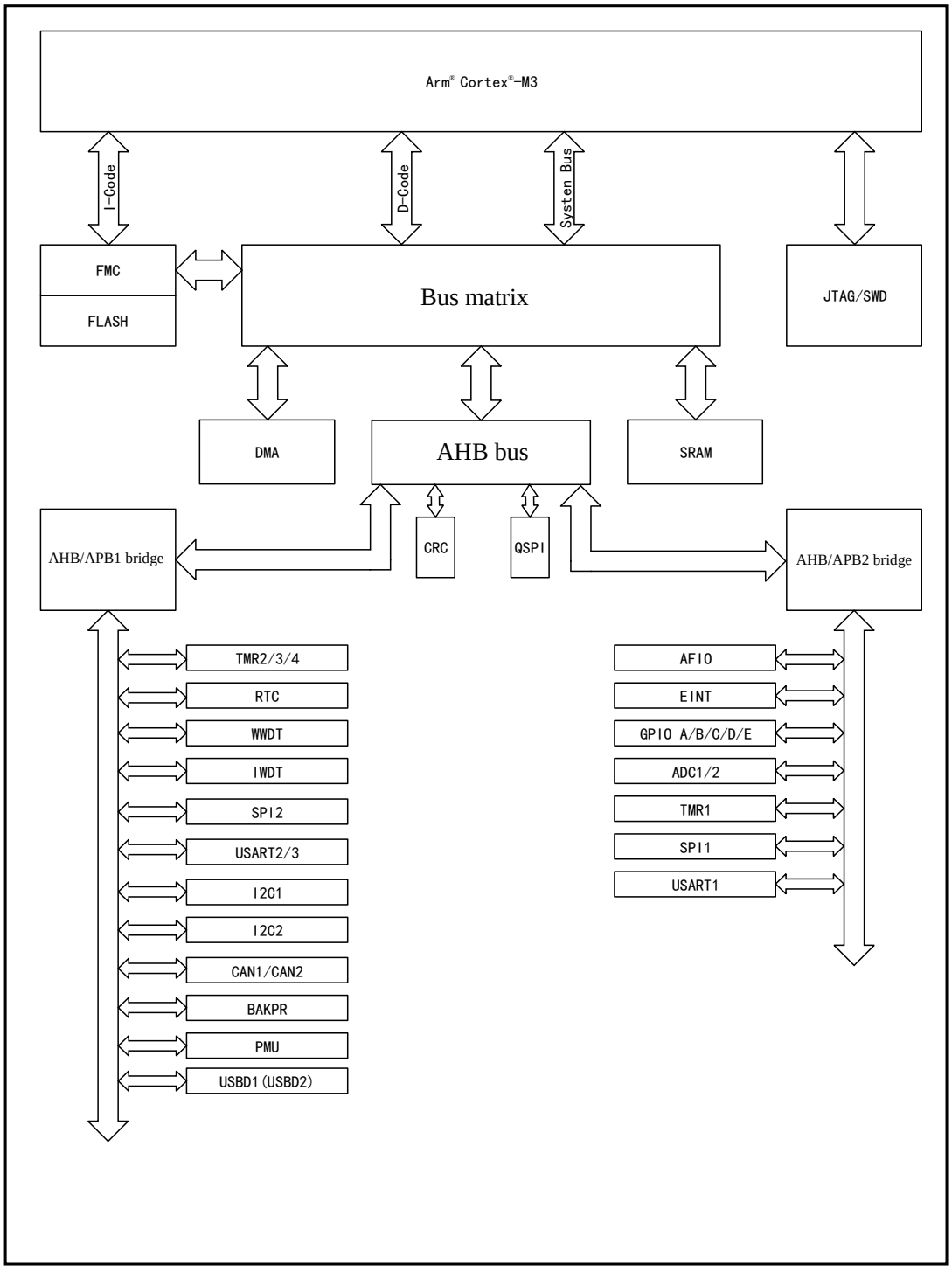
This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32F103xB series products; for information about the Arm® Cortex®-M3 core, please refer to the Arm® Cortex®-M3 Technical Reference Manual, which can be downloaded from Arm's website.

This version is applicable to APM32F103xB series E version models.

4.1 System architecture

4.1.1 System Block Diagram

Figure 5 APM32F103xB Series System Block Diagram



1. The maximum frequency of AHB and high-speed APB of APM32F103xB series is 96MHz;
2. The maximum frequency of low-speed APB of APM32F103xB series is 48MHz.

4.1.3 Address mapping

Table4 Address Mapping Table of APM32F103xB Series

Region	Start address	Peripheral name
Code	0x0000 0000	Code mapping area
Code	0x0800 0000	FLASH
Code	0x0801 FFFF	Reserved
Code	0x1FFF F000	System memory area
Code	0x1FFF F800	Option byte
Code	0x1FFF F80F	Reserved
SRAM	0x2000 0000	SRAM
APB 1 bus	0x4000 0000	TMR2
APB 1 bus	0x4000 0400	TMR3
APB 1 bus	0x4000 0800	TMR4
APB 1 bus	0x4000 0C00	Reserved
APB 1 bus	0x4000 2800	RTC
APB 1 bus	0x4000 2C00	WWDT
APB 1 bus	0x4000 3000	IWDT
APB 1 bus	0x4000 3400	Reserved
APB 1 bus	0x4000 3800	SPI2
APB 1 bus	0x4000 3C00	Reserved
APB 1 bus	0x4000 4400	USART2
APB 1 bus	0x4000 4800	USART3
APB 1 bus	0x4000 4C00	Reserved
APB 1 bus	0x4000 5400	I2C1
APB 1 bus	0x4000 5800	I2C2
APB 1 bus	0x4000 5C00	USBD1(USBD2)
APB 1 bus	0x4000 6000	USBD/CAN SRAM
APB 1 bus	0x4000 6400	CAN1
APB 1 bus	0x4000 6800	CAN2
APB 1 bus	0x4000 6C00	BAKPR
APB 1 bus	0x4000 7000	PMU
—	0x4000 7400	Reserved
APB2 bus	0x4001 0000	AFIO
APB2 bus	0x4001 0400	EINT
APB2 bus	0x4001 0800	Port A
APB2 bus	0x4001 0C00	Port B
APB2 bus	0x4001 1000	Port C
APB2 bus	0x4001 1400	Port D

Region	Start address	Peripheral name
APB2 bus	0x4001 1800	Port E
APB2 bus	0x4001 1C00	Reserved
APB2 bus	0x4001 2400	ADC1
APB2 bus	0x4001 2800	ADC2
APB2 bus	0x4001 2C00	TMR1
APB2 bus	0x4001 3000	SPI1
APB2 bus	0x4001 3400	Reserved
APB2 bus	0x4001 3800	USART1
APB2 bus	0x4001 3C00	Reserved
AHB bus	0x4002 0000	DMA
AHB bus	0x4002 0400	Reserved
AHB bus	0x4002 1000	RCM
AHB bus	0x4002 1400	Reserved
AHB bus	0x4002 2000	Flash interface
AHB bus	0x4002 2400	Reserved
AHB bus	0x4002 3000	CRC
AHB bus	0x4002 3400	Reserved
AHB bus	0xA000 0000	QSPI
—	0xA000 2000	Reserved

4.1.2 Startup configuration

At startup, the user can select one of the following three startup modes by setting the Boot pin:

- Startup from main memory
- Startup from system memory
- Startup from built-in SRAM

Boot loader is stored in the system memory. With it, users can reprogram flash memory through USART1.

4.2 Core

APM32F103xB core is Arm® Cortex®-M3, with working frequency of 96MHz, compatible with mainstream Arm tools and software.

4.3 Interrupt controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

It embeds a nested vector interrupt controller (NVIC) and NVIC can handle up to 49 maskable interrupt channels (not including16 interrupt lines of Cortex®-M3) and 16 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 19 edge detectors that generate event/interrupt requests. Its trigger events (rising edge or falling edge or double edge) can be independently configured or shielded; there is a suspend register that maintains the status of all interrupt requests. Up to 80 general-purpose I/O can be connected to 16 external interrupt lines. EINT can detect that the pulse width is less than the clock cycle of the internal APB2.

4.4 Memory

The memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program when leaving the factory and cannot be erased.

Table5

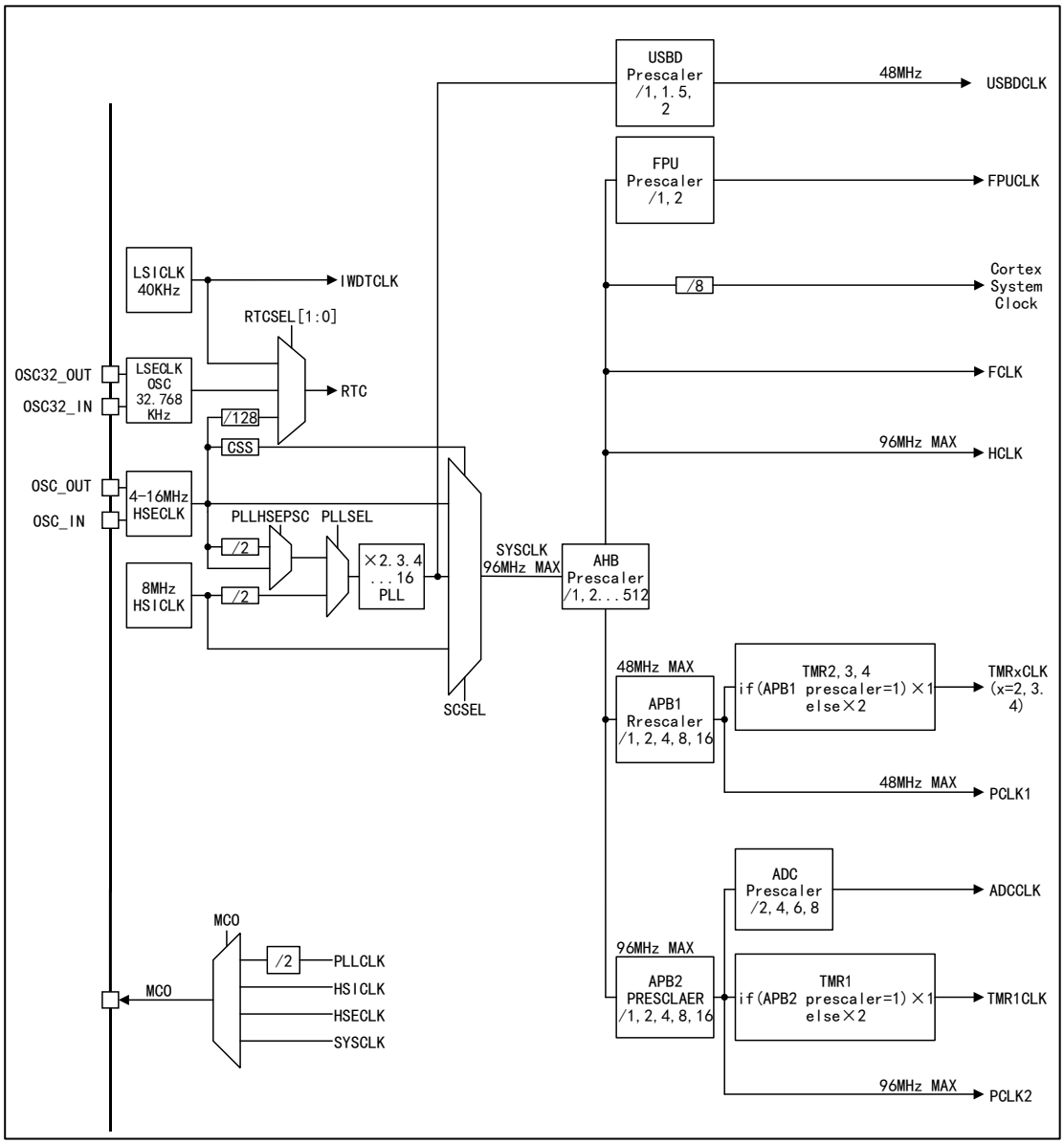
Memory	Maximum bytes	Function
Main memory area	128 KB	Store user programs and data
SRAM	36KB	Can be accessed by byte, half word (16 bits) or word (32 bits).
System memory area	2 KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

4.5 Clock

4.5.1 Clock tree

The clock tree of APM32F103xB series is shown in the figure below:

Figure 6 APM32F103xB Series Clock Tree



1. The maximum frequency of AHB and high-speed APB of APM32F103xB series is 96MHz;
2. The maximum frequency of low-speed APB of APM32F103xB series is 48MHz.

4.5.2 Clock and startup

The internal 8MHz RC oscillator is used as the default clock for system startup. It can be switched to an external 4~16MHz clock with failure monitoring through configuration; when an external clock failure is detected, the system will automatically switch to the internal RC oscillator. If an interrupt is set, the software can receive the corresponding interrupt.

The frequency of AHB, high-speed APB (APB2) and low-speed APB (APB1) can be configured by prescaler. The maximum frequency of AHB and high-speed APB is 96MHz, and that of low-speed APB is 48MHz.

For the clock tree of APM32F103xB, refer to Figure 6.

4.5.3 RTC and backup register

RTC has a set of continuously running counters, which can provide calendar, alarm interrupt and periodic interrupt functions together with software. Its clock source can be an external 32.768KHz crystal oscillator, an internal 40KHz low-speed RC oscillator or an external high-speed clock with 128 frequency division. In addition, RTC clock error can be calibrated by a 512Hz signal.

Backup register of 10 16-bit registers is used to save 20 bytes of user data when V_{DD} is disabled.

RTC and backup register are powered by V_{DD} when V_{DD} is valid; otherwise, they are powered by V_{BAT} pin. Reset of system or power reset source and wake-up from standby mode will not cause reset of RTC and backup register.

4.6 Power supply and power supply management

4.6.1 Power supply scheme

Table6 Power Supply Scheme

Name	Voltage range	Description
V_{DD}	2.0～3.6V	V_{DD} powers IO interface directly, and powers core circuit through voltage regulator.
V_{DDA}	2.4～3.6V	It is connected to V_{DD}, and supplies power to ADC, reset module, RC oscillator and PLL analog part. When ADC is used, VDDA is greater than or equal ato 2.4V. V_{DDA} and V_{SSA} should be connected to V_{DD} and V_{SS} respectively.
V_{BAT}	1.8～3.6V	When V_{DD} is disabled, RTC, external 32KHz oscillator and backup register are powered automatically.

Note: See Figure 7 Power Supply Scheme for more detailed information about how to connect the power pins

4.6.2 Voltage regulator

The working mode of MCU can be adjusted through voltage regulator so as to reduce power consumption. It mainly has three working modes.

Table7 Operating Mode of Voltage Regulator

Name	Description
Main mode (MR)	Provide 1.6 power supply (core, memory and peripheral) in normal power mode.
Low-power mode (LPR)	Provide 1.6V power supply in low-power mode, to save the content of register and SRAM.
Power-down mode	Used in the standby mode of CPU; the voltage regulator stops power supply, and except for the standby circuit and backup area, all contents of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3 Power monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. When V_{DD} reaches the set threshold $V_{POR/PDR}$, the system works normally; when the V_{DD} is lower than the set threshold $V_{POR/PDR}$, the system will remain in the reset state without connecting the external reset circuit.

4.7 Low-power mode

The product supports three low-power modes. Users can switch between these modes by setting.

Table8 Low-power Mode

Mode	Description
Sleep mode	In sleep mode, all peripherals are in working status, but the CPU stops working. If an interrupt/event occurs, the CPU will be waked up.
Stop mode	The stop mode is the mode that can achieve the lowest power consumption without losing the content of SRAM and register. At this time, internal 1.6V power supply stops, causing the HSECLK, HSICLK and PLL clocks to turn off, and the voltage regulator is set to the normal mode or low-power mode. Interrupt and event wake-up configured as EINT can wake the CPU from the stop mode. EINT signal includes 16 external I/O ports, PVD output, RTC alarm or USBD wake-up signal.
Standby mode	The standby mode is the lowest-power mode used by the chip. At this time, the internal voltage regulator is disabled, causing power supply of the internal 1.6V part to be cut off; HSECLK, HSICLK and PLL clocks are disabled; the content of SRAM and register will disappear. However, the content of the backup register will remain and the standby circuit will still work. The external reset signal on NRST, IWDT reset, a rising edge on WKUP pin or RTC alarm will terminate the standby mode of the chip.

Note: When entering the stop or standby mode, RTC, IWDT and corresponding clock will not stop, and the interrupt of QSPI cannot wake up the low power.

4.8 DMA

The product has 7-channel general-purpose DMA, which can manage the data transmission from memory to memory, device to memory, and memory to device.

Each channel has hardware DMA request logic, and the source address, destination address and transmission length of each channel can be set separately by software.

DMA can be used for main peripherals: SPI, I2C, USART, timer TMRx and ADC, QSPI.

4.9 GPIO

The product can have up to 80 GPIO pins. Every pin can be switched between input (pull-up, pull-down), output (push-pull, open-drain) or multiplexing functions through software configuration. Most GPIO pins are shared with multiplexed peripherals. To avoid accidental writing of I/O registers, the peripheral functions of I/O pins can be locked by specific

operations.

I/O pin turnover speed on the APB2 can reach 18MHz.

4.10 Communication peripherals

4.10.1 USART

Three USART communication interfaces are embedded. Among them, the USART1 interface can support the communication rate of 4.5Mbit/s, and the other interfaces support the communication rate of 2.25Mbit/s. It has hardware signal CTS and RTS, compatible with ISO7816 smart card, supports IrDA SIR ENDEC transmission encoding and decoding, and provides LIN master/slave mode.

4.10.2 I2C

I2C1/2 can work in multi-master mode or slave mode and support 7-bit and 10-bit addressing. The protocol supports standard and fast modes. Built-in hardware CRC generator/calibrator. DMA operation can be used and SMBus bus version 2.0/PMBus bus is supported.

4.10.3 SPI

Two SPI interfaces are embedded, supporting the chip to communicate with external devices in half/full duplex serial mode. It can be configured as master mode or slave mode, with 8 or 16 bits per frame. The communication rate in full-duplex and half-duplex mode can be 18 Mbit/s. All SPI interfaces support DMA operation.

4.10.4 QSPI

1 QSPI special communication interface is embedded, which can connect external flash through single-line, double-line or four-line SPI mode, and support 8-bit, 16-bit and 32-bit access. There are 8-byte transmit FIFO and 8-byte receive FIFO inside. DMA operation is supported.

4.10.5 CAN

2 built-in CAN bus interfaces (CAN1 and CAN2 can be used at the same time), compatible with 2.0A and 2.0B (active) specifications, which can communicate at a rate of up to 1Mbit/s. Support standard frame with 11-bit identifier and extended frame with 29-bit identifier, and have 3 transmitting mailboxes and 2 receiving FIFO, and 14 3-level adjustable filters.

4.10.6 USBD

The product embeds USBD modules (USBD1 and USBD2) compatible with full-speed USBD devices, which comply with the standard of full-speed USBD devices (12Mb/s), and the endpoints can be configured by software, and have standby/wake-up functions. The dedicated 48MHz clock for USBD is directly generated by internal PLL. When using the USBD function, the system clock can only be one of 48MHz, 72MHz and 96MHz, which can obtain 48MHz required for USBD through 1 divided frequency, 1.5 fractional frequency, and 2 fractional frequency respectively.

USBD1 and USBD2 share register address and pin interface, so only one of them can be used at the same time.

4.10.7 Simultaneous use of USBD and CAN interfaces

When USBD and CAN are used at the same time, you need to:

- Write 0x00000001 at the base address offset 0x100 of USBD.
- PA11 and PA12 pins are for USBD, and CAN is used to multiplex other pins.

4.11 Analog peripherals

4.11.1 ADC

2 built-in ADCs with 12-bit accuracy, up to 16 external channels; each ADC can realize the conversion between single mode and scanning mode. It can support DMA operation and liberate the CPU. ADC interface supports single sampling, synchronous sampling and holding, and cross sampling and holding logic functions. The analog watchdog function can monitor multiple channels and generate an interrupt when the monitored signal exceeds the preset value.

The timer can be used to synchronize the analog-to-digital conversion with the clock.

4.11.1.1 Temperature sensor

An embedded temperature sensor connected to ADC1_IN16 input channel can convert the ambient temperature of the chip into digital signal.

4.12 SWJ-DP

The product supports serial debugging interface (SW-DP) and JTAG (JTAG-DP) debugging interface.

JTAG interface provides 5-pin standard JTAG interface for AHB access port.

SW-DP interface provides 2-pin (data + clock) interface for AHB module. Among them, some of 2 pins of SW-DP interface and 5 pins of JTAG interface are multiplexed.

4.13 Timer

The product includes 1 advanced-control timer (TMR1), 3 general-purpose timers (TMR2/3/4) and 1 system tick timer.

The following table compares the functions of advanced timer and general-purpose timer:

Table9 Function Comparison of Timers

Timer type	System tick timer	General-purpose timer			Advanced timer
Timer name	Sys Tick Timer	TMR2	TMR3	TMR4	TMR1
Counter resolution	24 bits	16 bits			16 bits
Counter type	Down	Up, down, up/down			Up, down, up/down

Timer type	System tick timer	General-purpose timer	Advanced timer
Prescaler factor	-	Any integer between 1 and 65536	Any integer between 1 and 65536
Generate DMA request	-	Yes	Yes
Capture/compare register	-	4	4
Complementary output	-	None	Yes
Pin characteristics	-	There are 5 pins in total: 1-way external trigger signal input pins, 4-way channel (non-complementary channel) pins	There are 9 pins in total: 1-way external trigger signal input pins, 1-way braking input signal pins, 3-pair complementary channel pins, 1-way channel (non-complementary channel) pins
Function Description	– Special for real-time operating system – Automatic reloading function supported – When the counter is 0, it can generate a maskable system interrupt – Can program the clock source	– Synchronization or event chaining function provided – The counter in debug mode can be frozen. – Can be used to generate PWM output – Each timer has an independent DMA request mechanism. – It can process signals of the incremental encoder and digital output of 1 to 3 Hall sensors.	– It has complementary PWM output with dead band insertion – When configured as a 16-bit standard timer, it has the same function as the TMRx timer. – When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). – In debug mode, timers can be frozen, and PWM output is disabled. – Synchronization or event chaining function is provided.

4.14 WDT

The product has two built-in watchdog timers, providing higher safety, time accuracy and flexibility in use. Two watchdog devices (independent watchdog and window watchdog) can be used to detect and solve faults caused by software errors; when the counter reaches the given timeout value, an interrupt is triggered (only applicable to the window watchdog) or a system reset is generated.

Table10 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler factor	Functional Description
Hardware watchdog	12 bits	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 40KHz, so it can run in shutdown and standby modes; the whole system can be reset in case of problems; It can provide timeout management for applications;

Name	Counter resolution	Counter type	Prescaler factor	Functional Description
				It can be configured as a software or hardware startup watchdog; In debug mode, the counter can be paused for convenience of debugging.
Window watchdog	7 bits	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early warning interrupt function; The counter in debug mode can be frozen.

4.15 CRC

The cyclic redundancy check (CRC) computing unit can calculate the CRC code of a 32-bit data word.

This application calculates the signature of the software in real time to facilitate comparison with the original signature.

5 Electrical characteristics

5.1 Test conditions of electrical characteristics

5.1.1 Maximum and minimum values

Unless otherwise specified, test is conducted for all products on the production line at T_A =25℃.

Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; On the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2 Typical value

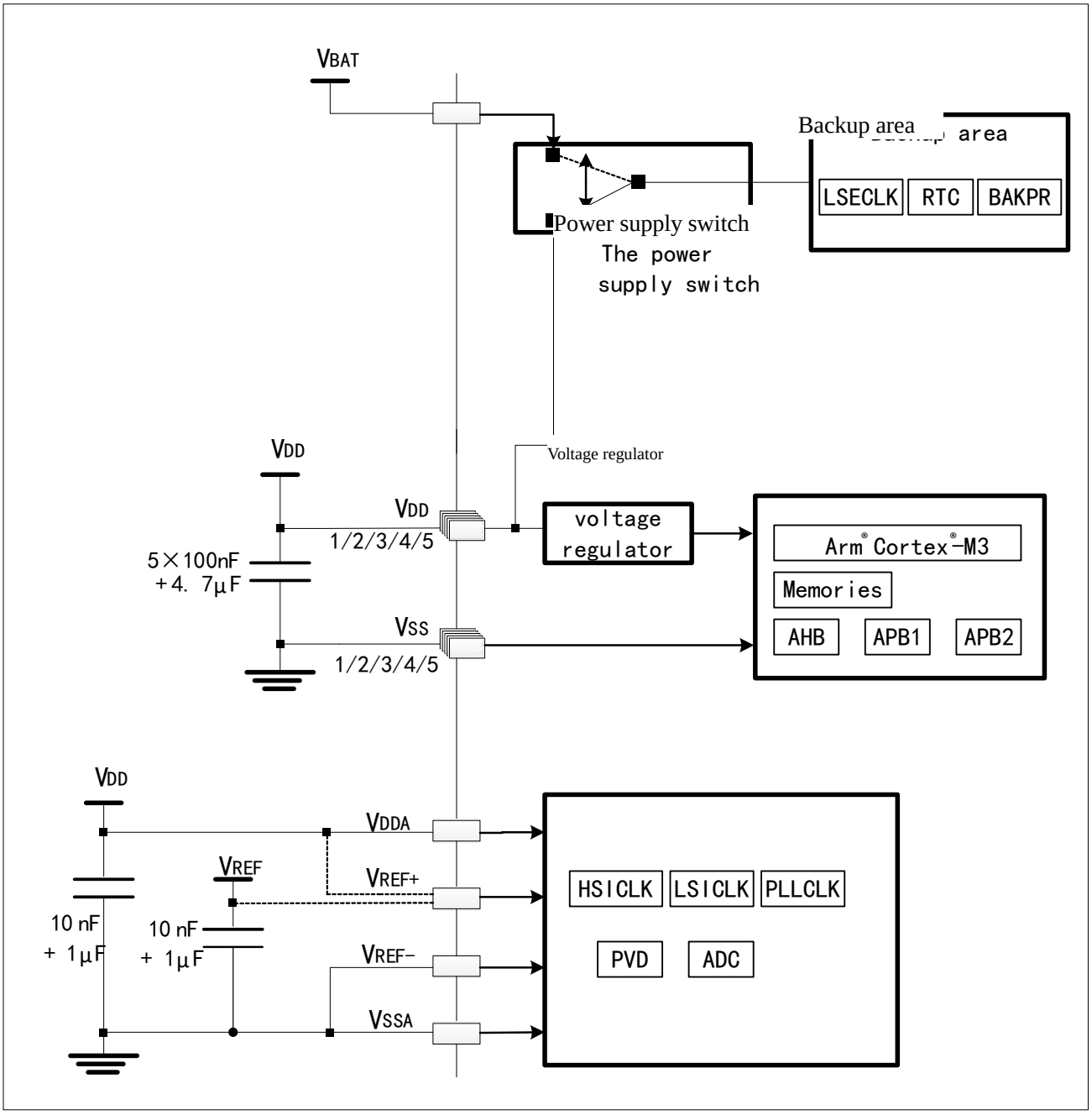
Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}=3.3V (2V ≤ V_{DD} ≤ 3.3V voltage range).

5.1.3 Typical curve

Typical curves will only be used for design guidance.

5.1.4 Power supply scheme

Figure 7 Power Supply Scheme



Note:the 4.7μF capacitor must be connected to VDD_3.

5.1.5 Load capacitance

Figure 8 Load conditions when measuring pin parameters

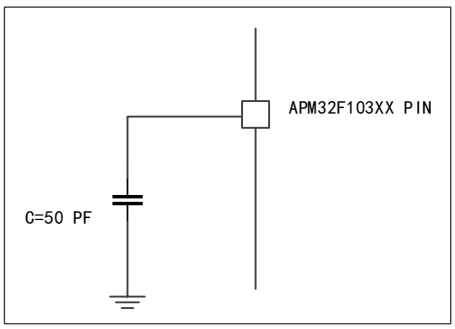


Figure 9 Pin Input Voltage Measurement Scheme

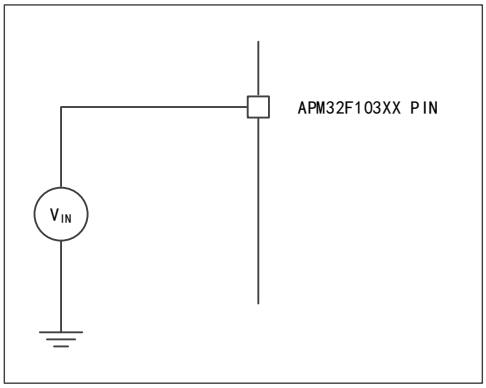
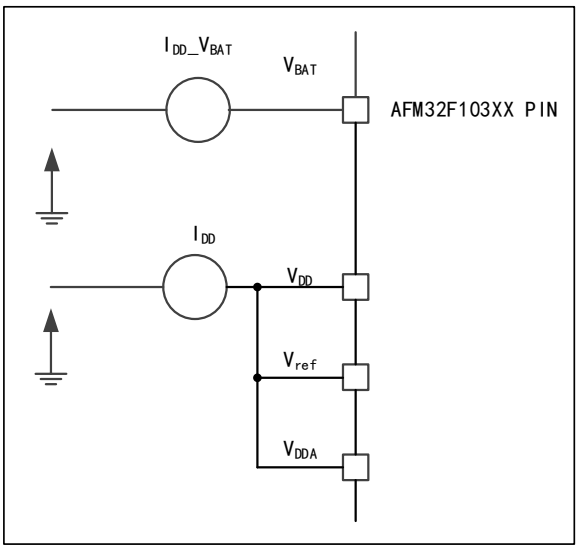


Figure 10 Current Consumption Measurement Scheme



5.2 Test under general operating conditions

Table11 General Operating Conditions

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	48	
f_{PCLK2}	Internal APB2 clock frequency	-	0	96	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Working voltage of analog part (ADC is not used)	Must be the same as V_{DD} (2)	2	3.6	V
	Working voltage of analog part (ADC is used)		2.4	3.6	
V_{BAT}	Working voltage of backup part	-	1.6	3.6	V
T_A	Ambient temperature (temperature number 6)	Maximum power dissipation	-40	85	℃
	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	℃
T_J	Junction temperature range	-	-40	150	℃

1. When ADC is used, see 5.12.1
2. V_{DD} and V_{DDA} should be powered from the same power supply during power-up and normal operation, with a maximum of 300mV difference allowed between V_{DD} and V_{DDA}.

5.3 Absolute maximum rated value

If the load on the device exceeds the absolute maximum rated value, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1 Maximum temperature characteristics

Table12 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-55 ~ +150	℃
T_J	Maximum junction temperature	150	℃

5.3.2 Maximum rated voltage characteristics

Table13 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{DD}) (1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V pins (2)	V_{SS}-0.3	5.5	
	Input voltage on other pins (2)	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins		50	mV

$\lvert V_{SSx}-V_{SS} \rvert$	Voltage difference between different grounding pins		50	

1. All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) must always be within the allowed range.
2. If V_{IN} exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited not to exceed the maximum value. When $V_{IN} > V_{DD}$, the current flows into the pins; when $V_{IN} < V_{SS}$, the current flows out of the pins.

5.3.3 Maximum rated current characteristics

Table14 Maximum Rated Current Characteristics

Symbol	Description	Maximum value	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) (1)	150	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) (1)	150	
I_{IO}	Sink current on any I/O and control pin	25	
	Source current on any I/O and control pin	-25	
$I_{INJ(PIN)}$ (2) (3)	Injection current of NRST pin	±5	
	Injection current of HSECLK OSC_IN pin and LSECLK OSC_IN pin	±5	
	Injection current of other pins (4)	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins (4)	±25	

All power supply (VDD, V_{DDA}) and ground (V_{SS}, V_{SSA}) must always be within the allowed range.

If VIN exceeds the maximum value, IINJ(PIN) must be externally limited not to exceed the maximum value. When V_{IN}> V_{DD}, the current flows into the pins; when VIN<V_{SS}, the current flows out of the pins.

The outflow current will interfere with the simulation performance of the ADC.

When the current is injected into several I/O ports at the same time, the maximum value of ΣIINJ(PIN) is the sum of instantaneous absolute value of inflow current and outflow current.

5.3.4 Electrostatic discharge (ESD)

The implementation method of electrostatic discharge is a positive pulse followed by a negative pulse after an interval of one second. All pins of the sample should be measured. The size of the sample is related to the number of power supply pins on the chip (3 x (n+1) power supply pins). This test conforms to JS-001-2017/JS-002-2018 standard.

Table15 Electrostatic Discharge (ESD)

Symbol	Parameter	Condition	Maximum	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A= +25℃, conforming to JS-001-2017 3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A= +25℃, conforming to JS-002-2018	1000	

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5 Static latch-up (LU)

When running a simple application (controlling the flashing of two LED through the I/O port), the test sample is subject to false electromagnetic interference until an error is generated, and the LED flashing indicates the generation of error. In order to evaluate the latch performance, two complementary static latch tests need to be conducted on 6 samples:

- Provide power supply voltage exceeding the limit for each power supply pin.
- Inject current on each input, output and configurable I/O pin.

This test conforms to EIA/JESD78E integrated circuit latch standard.

Table16Static Latch-up

Symbol	Parameter	Condition	Type
LU	Class of static latch-up	T_A=105℃, conforming to EIA/JESD78E	Class II A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4 Memory

5.4.1 Flash characteristics

Table17 Flash Memory Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{prog}	16-bit programming time	T_A = -40~105℃ V_{DD}=2.4~3.6V	32.2	33.2	35.2	μs
t_{ERASE}	Page (1K bytes) erase time	T_A = -40~105℃ V_{DD}=2.4~3.6V	1.34	1.38	1.50	ms
t_{ME}	Mass erase time	T_A = 25℃ V_{DD}=3.3V	-	-	6.5	ms
V_{prog}	Programming voltage	T_A = -40~105℃	2.0	3.3	3.6	V

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Table18 FLASH Memory Life and Data Retention Period

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
N_{END}	Erasure cycles	T_A =-40~85℃	100	-	-	1,000 cycles
t_{RET}	Data retention period	T_A = 55℃	20	-	-	Year

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.5 Clock

5.5.1 Characteristics of external clock source

5.5.1.1 A high-speed external clock generated crystal/ceramic resonator

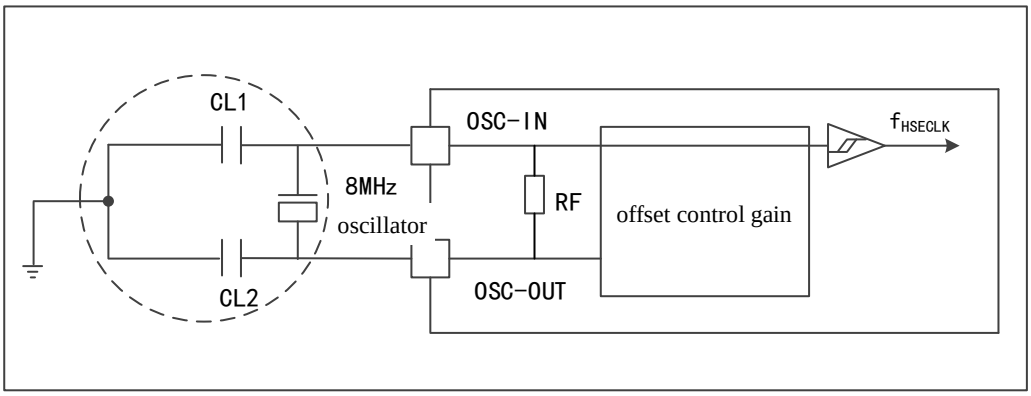
A high-speed external clock (HSECLK) can be generated using a 4~16MHz crystal/ceramic resonator. The following table shows the information of evaluated external devices. In the applications, the resonator and load capacitor must be as close to the oscillator pins as possible to reduce distortion and stable time of startup. For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table19 HSECLK4~16MHz Oscillator Characteristics (1) (2)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistance	-	-	400	-	kΩ
C_{L1}& C_{L2}(3)	Recommended load capacitance and corresponding crystal serial impedance (RS) (4)	R_S = 30kΩ	-	30	-	pF
i_2	HSECLK drive current	V_{DD}=3.3V，V_{IN}=V_{SS} 30pF load	-	-	1.1	mA
g_m	Transconductance of oscillator	Start	25	-	-	mA/V
$t_{SU(HSECLK)}$(5)	Start Time	V_{DD} is stable	-	1.33	-	ms

1. The characteristic parameters of the resonator are given by the manufacturer of crystal/ceramic resonator.
2. The above is obtained through comprehensive evaluation.
3. It is recommended that high-quality ceramic capacitors between 5pF and 25pF (typical value) designed for high frequency applications should be used for CL1 and CL2, and the capacitance value selected should meet the requirements of crystals or resonators. Typically, CL1 and CL2 have the same parameters. The load capacitance parameters usually given by crystal manufacturers are the serial combination values of C_{L1} and C_{L2}. When selecting C_{L1} and C_{L2}, the capacitive reactance of PCB and MCU pins shall be considered (usually the capacitance is estimated at 10pF).
4. Relatively low R_F resistance value should be adopted when it is used in wet environment. However, if the MCU is used in a harsh humid environment, attention should be paid to protection during design.
5. $t_{SU(HSECLK)}$ is the startup time, which defines the time when HSECLK is enabled by software to the time when stable oscillation at 8MHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

Figure 11 Typical Applications Using 8MHz Crystals



5.5.1.2 A low-speed external clock generated using a crystal/ceramic resonator

The low-speed external clock (LSECLK) can be generated using a 32.768 kHz crystal/ceramic resonator. The following table shows the information of evaluated external devices. In the applications, the resonator and load capacitor must be as close to the oscillator pins as possible to reduce distortion and stable time of startup. For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer

Table20 LSECLK Oscillator Characteristics (f_{LSECLK} =32.768KHz) (1)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	-	32.768	-	KHz
R_F	Feedback resistance	-	-	2	-	MΩ
C_{L1}& C_{L2}(2)	Recommended load capacitance and corresponding crystal serial impedance (R_S) (3)	R_S = 30kΩ	-	-	15	pF
i_2	LSECLK drive current	V_{DD}=3.3V, V_{IN}=V_{SS}	-	-	0.1	μA
$t_{SU(LSECLK)}$(4)	Start Time	V_{DD} is stable	-	2.03	-	s

1. This table is assessment table.
2. See prompt and warning paragraphs.
3. A high-quality oscillator with a small R_S value (such as MSIV-TIN 32.768kHz) can be selected to optimize the current consumption. Please consult the crystal manufacturer for details.
4. $t_{SU(HSECLK)}$ is the startup time, which defines the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

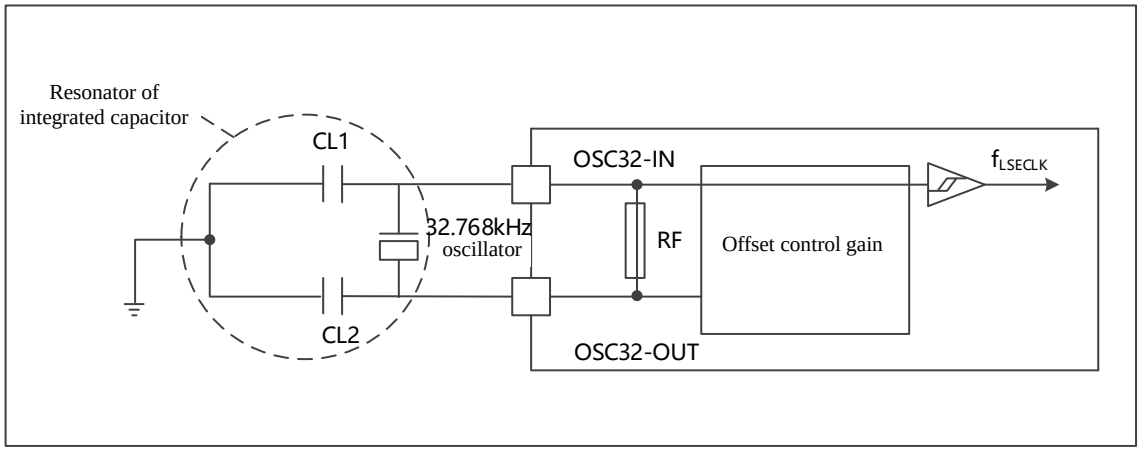
Prompt: It is recommended that high-quality ceramic dielectric capacitors between 5pF and 15pF should be selected for C_{L1} and C_{L2}, and the capacitance value selected should meet the requirements of crystals or resonators. Generally, C_{L1} and C_{L2} have the same parameters. The load capacitance parameters usually given by crystal manufacturers are the serial combination values of C_{L1} and C_{L2}. The calculation formula of load capacitance C_L: $C_L = C_{L1} \times C_{L2} / (C_{L1} +$

C_{L2}) + C_{stray}, where C_{stray} is the capacitance of the pin and the capacitance of the PCB or related to the PCB, which is usually between 2pF and 7pF.

Warning: It is recommended to use resonators with load capacitance C_L ≤7pF instead of resonators with load capacitance of 12.5 pF.

For example, if a resonator with load capacitance C_L=6pF is selected and C_{stray}=2pF, C_{L1}=C_{L2}=8pF

Figure 12 Typical Applications Using 32.768kHz



5.5.2 Characteristics of internal clock source

5.5.2.1 Test of high-speed internal (HSICLK) oscillator

Table21 HSICLK Oscillator Characteristics

SymbolOSC	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	8	-	MHz
ACC_{HSICLK}	Accuracy of HSICLK oscillator	Factory calibration	T_A=25℃ V_{DD} = 3.3V	1	-	1	%
			T_A=-40~105℃ V_{DD} = 2-3.6V	-2.63	-	3.56	%
			T_A =25℃ V_{DD} = 2-3.6V	-0.88	-	3.28	%
		User calibration		-1	-	1	%
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD} = 3.3V T_A =-40~105℃		1.03	-	1.24	μs
$I_{DD(HSICLK)}$	Power consumption of HSICLK oscillator	V_{DD} = 3.6V T_A =-40~105℃		-	-	120	μA

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.5.2.2 Low-speed internal (LSICLK) RC oscillator

Table22 LSICLK Oscillator Characteristics (1)

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LSICLK}	Frequency (V_{DD}=2-3.6V, T_A=-40~105℃)	30	40	50	KHz
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator, (V_{DD}=3.3V，T_A=-40~105℃)	-	-	60	μs
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator, (V_{DD}=3.3V，T_A=-40~105℃)	-	0.65	1.2	μA

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.5.3 PLL Characteristics

Table23 PLL Characteristics

Symbol	Parameter	Value			Unit
		Minimum value	Typical value	Maximum (1)	
f_{PLL_IN}	PLL input clock (2)	2	8	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock (V_{DD} = 3.3V，T_A = -40~105℃）	16	-	96	MHz
t_{LOCK}	PLL phase locking time	-	-	105	μs

1. The data are obtained from a comprehensive evaluation and are not tested in production.
2. Note that appropriate multiplication factor shall be used so that the PLL input clock frequency is consistent with the range determined by f_{PLL_OUT}.

5.6 Power supply and power supply management

5.6.1 Test of Embedded Reset and Power Control Module Characteristics

Table24 Embedded Reset and Power Control Module Characteristics (T_A=25℃) (-40℃~105℃) (1)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{PVD}(3)	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.17	2.20	2.24	V
		PLS[2:0]=000 (falling edge)	2.07	2.10	2.12	V
		PLS[2:0]=001 (rising edge)	2.28	2.30	2.32	V
		PLS[2:0]=001 (falling edge)	2.16	2.20	2.22	V
		PLS[2:0]=010 (rising edge)	2.38	2.41	2.44	V
		PLS[2:0]=010 (falling edge)	2.27	2.30	2.32	V

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
		PLS[2:0]=011 (rising edge)	2.47	2.51	2.54	V
		PLS[2:0]=011 (falling edge)	2.37	2.40	2.46	V
V_{PVD}(3)	Programmable power supply voltage detector voltage level selection	PLS[2:0]=100 (rising edge)	2.57	2.60	2.63	V
		PLS[2:0]=100 (falling edge)	2.46	2.50	2.58	V
		PLS[2:0]=101 (rising edge)	2.66	2.71	2.74	V
		PLS[2:0]=101 (falling edge)	2.56	2.61	2.69	V
		PLS[2:0]=110 (rising edge)	2.77	2.81	2.86	V
		PLS[2:0]=110 (falling edge)	2.65	2.70	2.8	V
		PLS[2:0]=111 (rising edge)	2.86	2.91	2.92	V
		PLS[2:0]=111 (falling edge)	2.76	2.80	2.83	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	107	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.86(1)	1.87	1.88	V
		Rising edge	1.92	1.94	1.96	V
$V_{PDRhyst}$ (2)	PDR hysteresis	-	-	50	-	mV
$T_{RSTTEMPO}$	Reset duration	-	0.9	-	2.4	ms

1. The characteristics of the product are guaranteed by design to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design and not tested in production.
3. The data are obtained from a comprehensive evaluation and are not tested in production.

5.7 Power Consumption

5.7.1 Power consumption test environment

The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L3 compilation optimization level.

All I/O pins are in analog input mode and are connected to a static level at V_{DD} or V_{SS} (no load)

Unless otherwise specified, all peripherals are disabled

The relationship between Flash wait cycle setting and f_{HCLK}:

- 0~24MHz: 0 wait cycle
- 24~48MHz: 1 wait cycle
- 48~72MHz: 2 wait cycles
- 72~96MHz: 3 wait cycles

The instruction prefetch function is enabled (note: it must be set before clock setting and bus frequency division)

When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/2$, $f_{PCLK2}=f_{HCLK}$

5.7.2 Power consumption in operation mode

Table25 Power consumption of data processing code running in Flash in operation mode

Parameter	Condition	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
Power consumption in operation mode	External clock (2), enabling all peripherals	96MHz	206.26	30.47	247.93	35.64
		72MHz	131.44	25.26	155.42	25.36
		48MHz	97.02	17.99	119.82	20.82
		36MHz	73.59	13.79	95.39	15.68
		24MHz	54.06	9.89	74.46	11.54
		16MHz	42.85	6.82	62.58	8.14
		8MHz	2.66	3.64	5.8	4.61
	External clock (2), disabling all peripherals	96MHz	205.98	20.02	242.41	22.74
		72MHz	130.91	14.99	153.66	16.74
		48MHz	96.92	12.67	114.87	14.33
		36MHz	73.54	9.69	89.39	11.05
		24MHz	54.06	7.21	68.85	8.45
		16MHz	42.85	5.06	57.38	6.11
		8MHz	2.66	2.75	5.68	3.63

1. The data are obtained from a comprehensive evaluation and are not tested in production.
2. The external clock is 8MHz. When f_{HCLK} > 8MHz, the PLL is enabled.

Table26 Power consumption of data processing code running in RAM in operation mode

Parameter	Condition	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
Power consumption in operation mode	External clock (2), enabling all peripherals	96MHz	206.68	29.97	250.48	59.83
		72MHz	131.66	20.61	161.87	24.58
		48MHz	97.59	15.71	122.43	67.9
		36MHz	74.15	11.95	96.93	14.16
		24MHz	54.80	8.36	72.68	9.93
		16MHz	43.44	5.68	60.53	6.97
		8MHz	2.63	3.07	11	3.96
	External clock (2), disabling all peripherals	96MHz	183.81	22.82	245.72	27.37
		72MHz	117.42	17.14	159.32	18.66

Parameter	Condition	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
		48MHz	96.67	10.45	119.9	14.42
		36MHz	73.502	8.02	93.38	11.25
		24MHz	54.12	5.61	72.03	8.06
		16MHz	43.17	3.98	59.51	6.01
		8MHz	2.65	2.28	12.95	3.81

1. The data are obtained from a comprehensive evaluation and are not tested in production.
2. The external clock is 8MHz. When f_{HCLK} > 8MHz, the PLL is enabled.

5.7.3 Power consumption in sleep mode

Table27 Power consumption of code running in Flash or RAM in sleep mode

Parameter	Condition	fHCLK	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA} (μA)	I_{DD} (mA)	I_{DDA} (μA)	I_{DD} (mA)
Power consumption in sleep mode	External clock (2), enabling all peripherals	96 MHz	205.89	18.77	242.73	20.99
		72MHz	130.77	12.92	153.78	14.38
		48MHz	96.77	9.93	114.87	10.97
		36MHz	73.42	7.68	89.42	9.69
		24MHz	53.85	5.36	68.74	6.14
		16MHz	42.64	3.83	57.25	4.57
		8MHz	2.65	2.12	5.7	2.84
	External clock (2), disabling all peripherals	96 MHz	205.62	7.13	242.64	8.17
		72MHz	130.66	5.02	153.71	5.91
		48MHz	96.68	3.95	114.84	4.76
		36MHz	73.36	3.14	89.36	3.89
		24MHz	53.82	2.34	68.73	3.08
		16MHz	42.61	1.8	57.25	2.52
		8MHz	2.65	1.16	5.71	1.83

1. The data are obtained from a comprehensive evaluation and are not tested in production.
2. The external clock is 8MHz. When f_{HCLK} > 8MHz, the PLL is enabled.

5.7.4 Power consumption in stop mode

Table28 Power Consumption in Stop Mode

Condition		Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)	
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=105℃	
		I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)
Power consumption in stop mode	Regulator in operation mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	2.12	20.57	2.65	20.8	2.86	22.06	4.51	237.81
	Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	2.12	8.27	2.65	8.48	-	13.6	-	79.18

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.7.5 Power consumption in standby mode

Table29 Power Consumption in Standby Mode

Condition		Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)	
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=105℃	
		IDDA (μA)	IDD (μA)	IDDA (μA)	IDD (μA)	IDDA (μA)	IDD (μA)	IDDA (μA)	IDD (μA)
Power consumption in standby mode	Low-speed internal RC oscillator and independent watchdog ON	2.32	0.36	2.98	0.73	3.25	0.93	4.23	12.4
	Low-speed internal RC oscillator on, independent watchdog OFF	2.32	0.25	2.98	0.52	3.24	0.73	4.23	12.2
	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.97	0.07	2.49	0.08	2.69	0.17	3.69	11.55

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.7.6 Peripheral power consumption

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table30 Peripheral Power Consumption

Parameter	Peripheral Clock	Typical value (1) T_A=25℃, V_{DD}=3.3V	Unit
AHB	DMA1	0.29	mA
	CRC	0.28	
APB1	TMR2	0.42	
	TMR3	0.48	
	TMR4	0.55	
	WWDT	0.17	
	IWDT	0.29	
	SPI2	0.23	
	USART2	0.39	
	USART3	0.43	
	I2C1	0.35	
	I2C2	0.43	
	USBD	0.74	
	CAN1	0.49	
	CAN2	0.40	
	BAKPR	0.28	
	PMU	0.46	
APB2	GPIOA	0.28	
	GPIOB	0.28	
	GPIOC	0.31	
	GPIOD	0.41	
	GPIOE	0.31	
	ADC1	0.66	
	ADC2	0.62	
	TMR1	0.71	
	SPI1	0.33	
	USART1	0.53	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.7.7 Backup Domain Power Consumption

Table 31V_{BAT} Power Consumption

Symbol	Parameter	Condition	Typical value (1), T_A=25℃			Maximum value (1), V BAT=3.6V		Unit
			V_{BAT}=2.4V	V_{BAT}=3.3V	V_{BAT}=3.6V	T_A=85℃	T_A=105℃	
I_{DD_VBAT}	Backup area Supply current	The low-speed oscillator and RTC are in ON state	1.03	1.34	1.47	3.31	4.95	μA

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.8 Wake-up time in low-power mode

The time values in the table are measured using an 8MHz HSICLK oscillator as the wake-up clock source at the wake-up stage. The clock source used when wake-up depends on the current operation mode:

- Stop or standby mode: The clock source is RC oscillator
- Sleep mode: The clock source is the clock set when entering sleep mode

Table 32Wake-up time in low-power mode

Symbol	Parameter	Typical value	Unit
$t_{WUSLEEP}$(1)	Wake up from sleep mode	0.56	μs
t_{WUSTOP}(1)	Wake up from stop mode (the voltage regulator is in operation mode)	2.29	μs
	Wake up from stop mode (the voltage regulator is in low-power mode)	3.66	
$t_{WUSTDBY}$(1)	Wake up from standby mode	32.62	μs

1. The wake-up time is measured from the start of the wake-up event to the first instruction read by the user program.

5.9 I/O port characteristics

Table33 DC Characteristics (T_A=-40℃-105℃, V_{DD}=2.7~3.6V)

Symbol	Parameter	Condition	Minimum value	Typical	Maximum value	Unit
V_{IL}	Low-level input voltage	TTL port	-0.5	-	0.8	V
V_{IH}	Standard I/O pin, high-level input voltage		2	-	V_{DD}+0.5	
	FT I/O pin (1), high-level input voltage		2	-	5.5	

Symbol	Parameter	Condition	Minimum value	Typical	Maximum value	Unit
V_{IL}	Low-level input voltage	CMOS port	-0.5	-	$0.3V_{DD}$	
V_{IH}	High-level input voltage		$0.7V_{DD}$	-	$V_{DD}+0.5$	
V_{hys}	Standard I/O pin Schmitt trigger voltage hysteresis (2)	-	150	-	-	mV
	5V FT I/O pin Schmitt trigger voltage hysteresis (2)		$5\%V_{DD}$	-	-	mV
I_{lkg}	Input leakage current (3)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/O port	-	-	±1	μA
		V_{IN} = 5V， FT port, T_A=25℃,V_{DD}=5V	-	-	3	
R_{PU}	Weak pull-up equivalent resistance (4)	$V_{IN} = V_{SS}$	32	40	49	kΩ
R_{PD}	Weak pull-down equivalent resistance (4)	$V_{IN} = V_{DD}$	32	40	49	kΩ
C_{IO}	Capacitance of I/O pin	-	-	5	-	pF

1. FT=5V tolerant. To withstand the voltage higher than VDD+0.3, the internal pull-up or pull-down resistance must be turned off.
2. The hysteresis voltage of Schmitt trigger switch level is obtained from a comprehensive evaluation and is not tested in production.
3. If there is reverse current flow-backwards at adjacent pins, the leakage current may be higher than the maximum value.
4. The pull-up and pull-down resistor is designed as a real resistor connected in series with a controllable PMOS/NMOS switch.

Output drive current test

GPIO (general-purpose input/output port) normally supports ±8mA current, up to ±20mA current (V_{OL}/V_{OH} reduction standard). In application, the number of I/O that can drive the current shall be restricted to ensure that the consumed current cannot exceed the absolute maximum rated value:

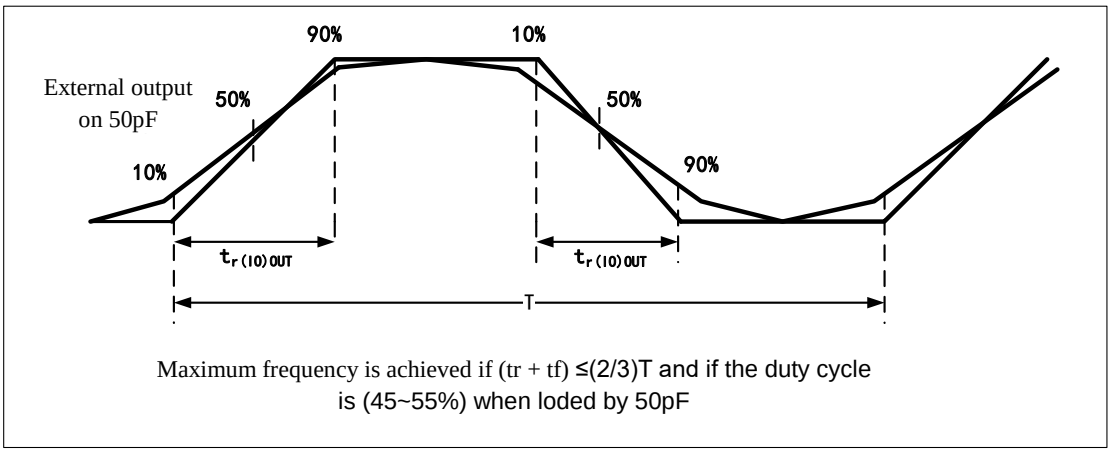
- The total current outputted by all I/O, plus the maximum operating current of MCU, cannot exceed the absolute maximum rated value I_{VDD}.
- The total current absorbed by all I/O, plus the maximum operating current of MCU, cannot exceed the absolute maximum rated value I_{VSS}.

Table34 AC Characteristics (T_A=25℃)

MODEx[1:0] Configuration	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency (2)	C_L = 50 pF, V_{DD} = 2~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	C_L = 50 pF, V_{DD} = 2~3.6V	-	50(3)	ns
	$t_{r\ (IO)out}$	Output rise time from low to high level		-	50(3)	
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency (2)	C_L = 50 pF, V_{DD} = 2~3.6V	-	10	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	C_L = 50 pF, V_{DD} = 2~3.6V	-	24(3)	ns
	$t_{r\ (IO)out}$	Output rise time from low to high level		-	23	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency (2)	C_L = 30 pF, V_{DD} = 2.7~3.6V	-	50	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	C_L = 30 pF, V_{DD} = 2.7~3.6V	-	6(3)	ns
	$t_{r\ (IO)out}$	Output rise time from low to high level		-	8(3)	

1. The rate of I/O port can be configured through MODEx[1:0].
2. The maximum frequency is defined by the figure below.
3. Guaranteed by design and not tested in production.

Figure 13 I/O AC Characteristics Definition



Maximum frequency is achieved if (tr + tf) ≤(2/3)T and if the duty cycle is (45~55%) when loded by 50pF

Table35 Output Voltage Characteristics (test condition V_{CC}=2.7~3.6V, T_A=-40~105℃)

Symbo	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OL}(1)	Output low level when 8 pins absorbs	TTL port, I_{IO} = +8mA	-	0.4	V

Symbo	Parameter	Condition	Minimum value	Maximum value	Unit
	current at the same time	2.7V < V_{DD} < 3.6V			
V_{OH}(2)	Output high level when 8 pins output current at the same time		V_{DD}-0.4	-	
V_{OL}(1)	Output low level when 8 pins absorbs current at the same time	CMOS port, I_{IO} = +8mA 2.7V < V_{DD} < 3.6V	-	0.4	V
V_{OH}(2)	Output high level when 8 pins output current at the same time		2.4	-	
V_{OL}(1)(3)	Output low level when 8 pins absorbs current at the same time	I_{IO} = +20mA 2.7V < V_{DD} < 3.6V	-	1.3	V
V_{OH}(2)(3)	Output high level when 8 pins output current at the same time		V_{DD}-1.3(4)	-	

1. The current I_{IO} absorbed by I/O must always comply with the absolute maximum rated value requirements, and the sum of I_{IO} (all I/O and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} outputted by I/O must always comply with the absolute maximum rated value requirements, and the sum of I IO (all I/O and control pins) cannot exceed I_{VDD}.
3. The data are obtained from a comprehensive evaluation and are not tested in production.
4. The drive capability of PC13-15 is not included in this item. The specification of other PC ports is 3.3V<V_{DD}<3.6V within the voltage range.

5.10 NRST pin characteristics

The NRST pin input drive adopts CMOS process, and is connected with a permanent pull-up resistor R_{PU}.

Table36 NRST Pin Characteristics (T_A=-40~105℃, V_{DD}=3.3V)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$(1)	NRST low-level input voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST high-level input voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	300	-	mV
R_{PU}	Weak pull-up equivalent resistance (2)	V_{IN} = V_{SS}	32	40	49	kΩ

1. Guaranteed by design and not tested in production.
2. The pull-up resistor is realized by connecting a pure resistor in series with a turn-off PMOS/NMOS switch. The resistance of this PMOS/NMOS switch is very small.

5.11 Communication peripherals

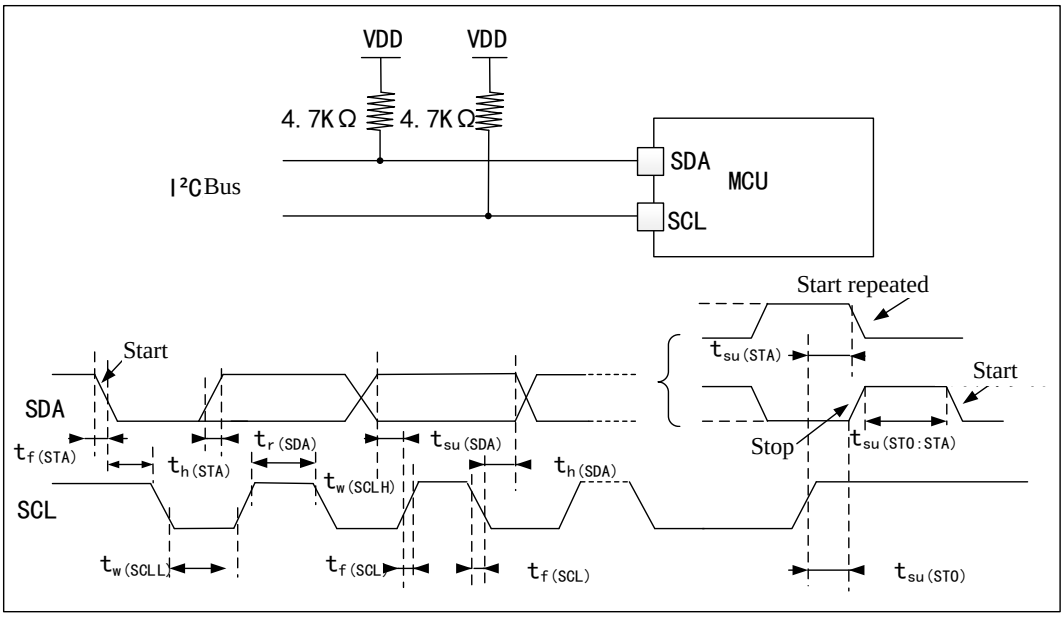
5.11.1 I2C peripheral characteristics

Table37 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C (1)		Standard I2C (1) (2)		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Setup time of repeated start condition	4.7	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4.0	-	0.6	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (the bus is idle)	10.86	-	3.85	-	μs

1. Guaranteed by design and not tested in production.
2. To achieve the maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.
3. If you do not want to prolong the low-level time of SCL signal, the maximum hold time of the start condition must be met.
4. In order to cross the undefined area of the falling edge of SCL, the SDA signal must have a hold time of at least 300ns in the MCU.

Figure 14 Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11.2 SPI peripheral characteristics

Table38 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master Mode	-	18	MHz
		Slave Mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SP clock rise and fall time	Load capacitance: C = 30pF	-	7.1	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode, f_{PCLK}= 36MHz	111.4	-	ns
$t_{h(NSS)}$(2)	NSS hold time	Slave mode, f_{PCLK}= 36MHz	55.6	-	ns
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Main mode, f_{PCLK} = 36MHz, Prescaler factor=4	55.1	55.9	ns
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master Mode	10.9	-	ns
		Slave Mode	21.3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master Mode	35	-	ns
		Slave Mode	25	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode, f_{PCLK} = 20MHz	6.5	8.7	ns

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{dis(SO)}$(2)(4)	Disable time of data output	Slave Mode	12	-	ns
$t_{v(SO)}$(2)(1)	Effective time of data output	Slave mode (after enabling the edge)	-	19.3	ns
$t_{v(MO)}$(2)(1)	Effective time of data output	Master mode (after enabling the edge)	-	7.6	ns
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enabling the edge)	10.7	-	ns
$t_{h(MO)}$(2)		Master mode (after enabling the edge)	2	-	

1. The SPI1 feature of remapping needs to be further determined.
2. The data are calculated and are not tested in production.
3. The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to make the data valid.
4. The minimum value represents the minimum time to disable the output, and the maximum value represents the maximum time to put the data cable in high-impedance state.

Figure 15 SPI Timing Diagram - Slave Mode and CPHA=0

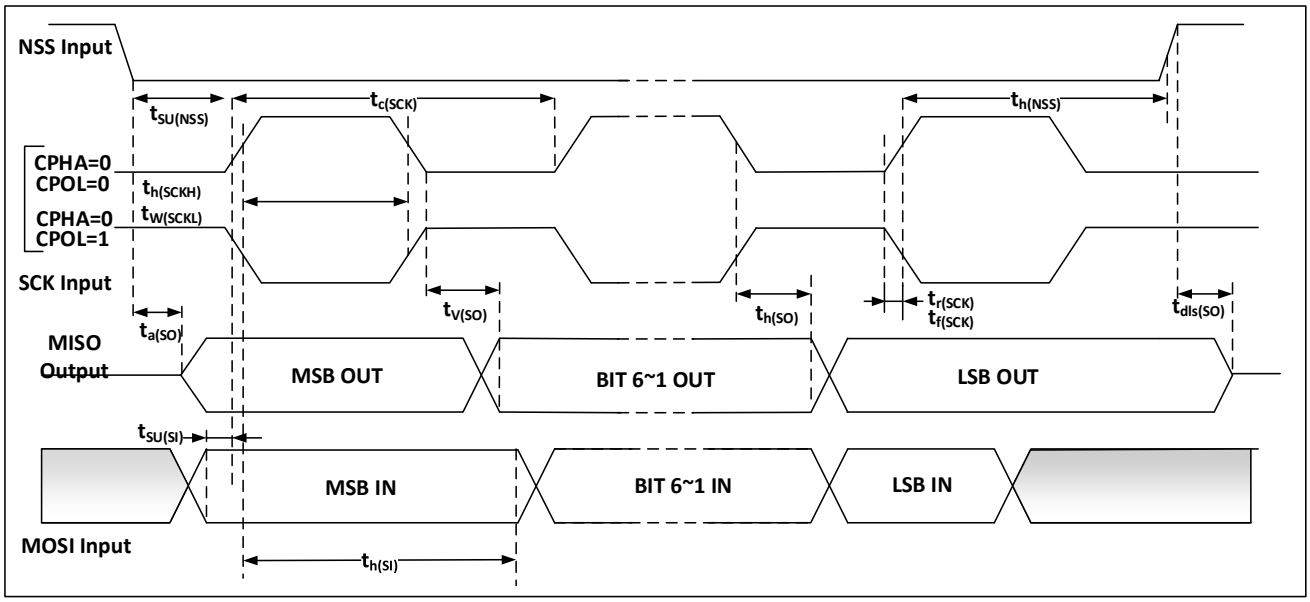
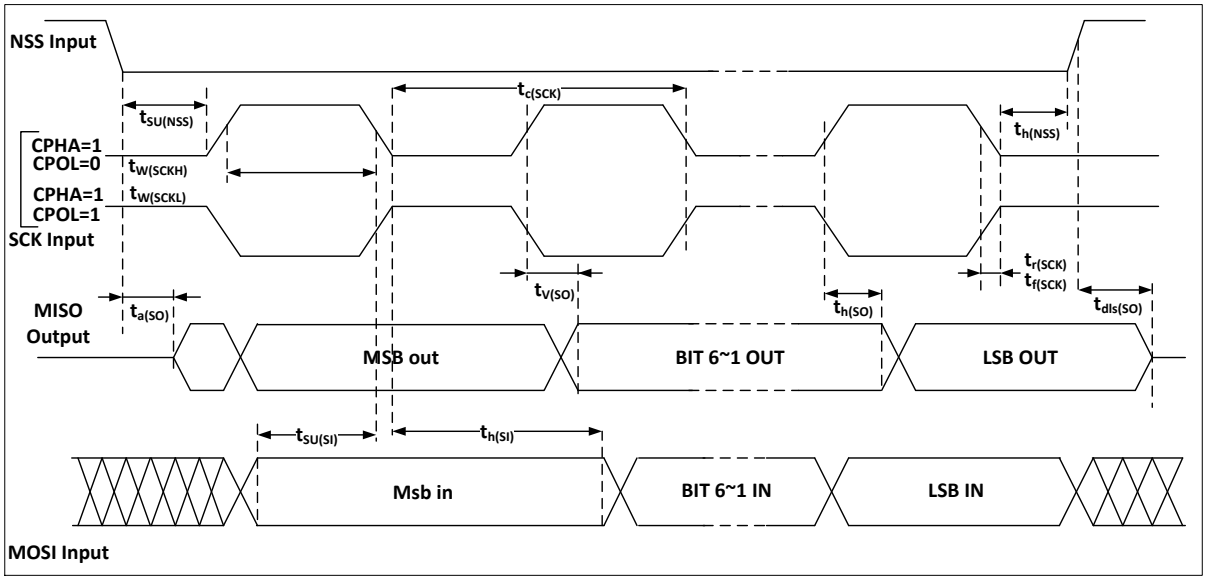
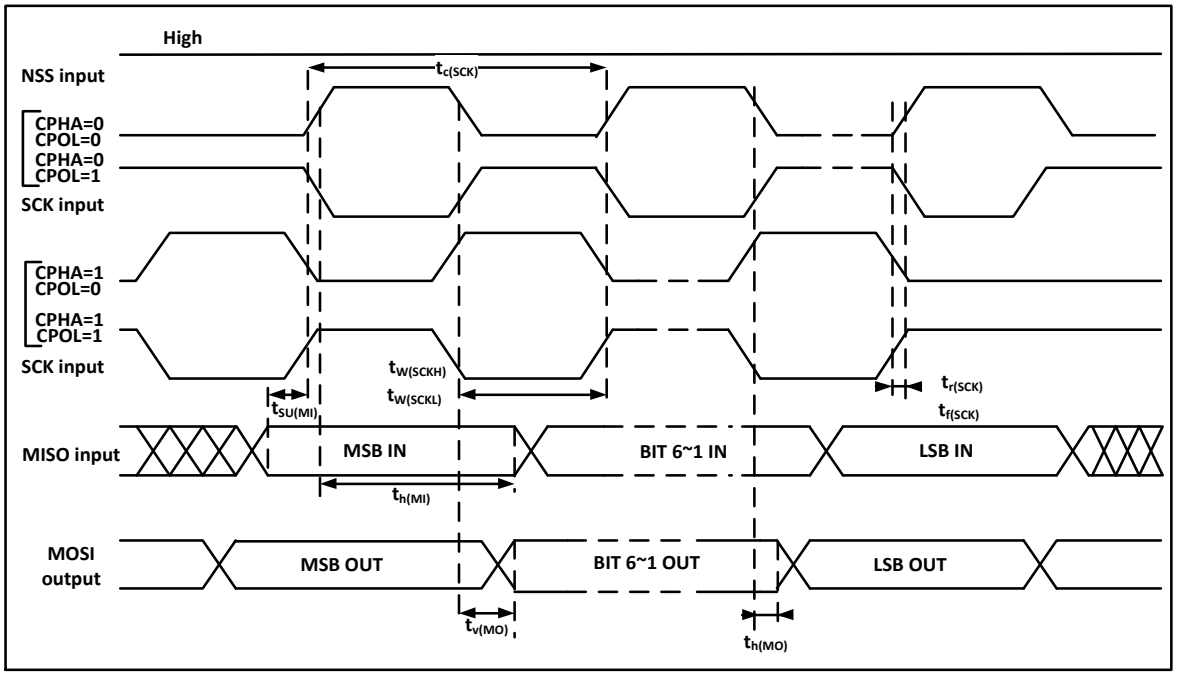


Figure 16 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 17 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11.3 USBD peripheral characteristics

Table39 USBD DC Characteristics

Symbol	Parameter	Condition	Minimum value (1)	Maximum value (1)	Unit
Input level					
V_{DD}	USBD operating voltage (2)	-	3.0 (3)	3.6	V
V_{DI} (4)	Differential input sensitivity	I (USBDP, USBDM)	0.2	-	V
V_{CM} (4)	Differential common mode range	Including V_{DI} range	0.8	2.5	
V_{SE} (4)	Single-ended receiver threshold	-	1.3	2.0	
Output level					
V_{OL}	Static output low level	1.5kΩ RL connected to 3.6V (5)	-	0.3	V
V_{OH}	Static output high level	5kΩ RL connected to V_{SS} (5)	2.8	3.6	

1. All voltage measurement is subject to device-end ground wire.
2. In order to be compatible with the USB2.0 full-speed electrical specification, the USBDP (D+) pin must be connected to a voltage of 3.0~3.6V through a 1.5kΩ resistor.
3. The correct USBD function of APM32F103xx can be guaranteed at 2.7V, rather than the electrical

characteristics degraded under the voltage range of 2.7~3.0V.

4. Guaranteed by comprehensive evaluation and not tested in production.
5. RL is the load connected to the USBD drive.

Figure 18 USBD Timing: Definition of Rise and Fall Time of Data Signal

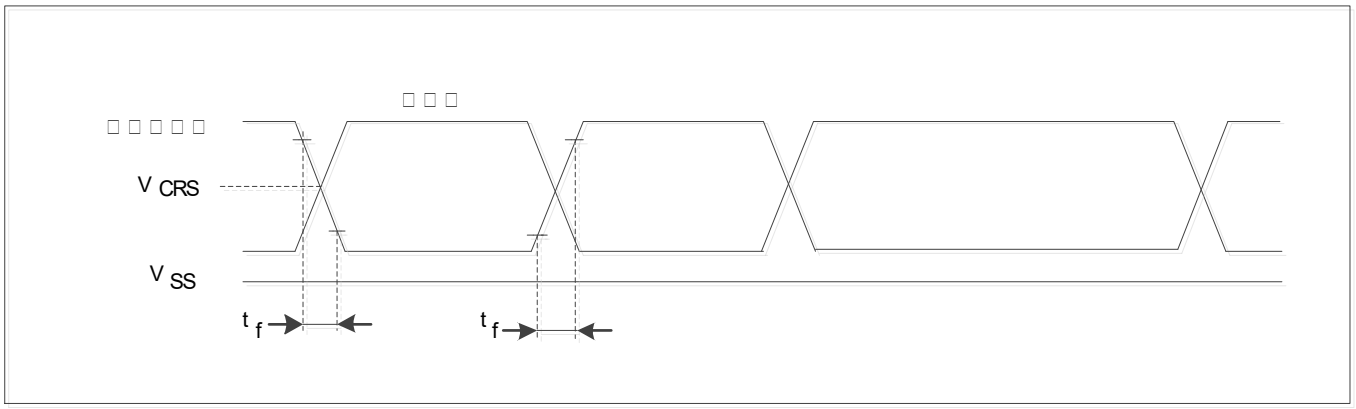


Table40 USBD Full-speed Electrical Characteristics (V_{DD}=3.0~3.6V, T_A =25℃)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
t_r	Rise time	C_L = 50pF	4	20	ns
t_f	Fall time	C_L = 50pF	4	20	ns
t_{rfm}	Match of rise and fall time	t_r / t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

5.12 Analog peripherals

5.12.1 ADC

Test parameter description:

- Sampling rate: The number of conversion of analog quantity to digital quantity by ADC per second
- Sample rate=ADC clock/(number of sampling periods + number of conversion periods)

5.12.1.1 12-bit ADC characteristics

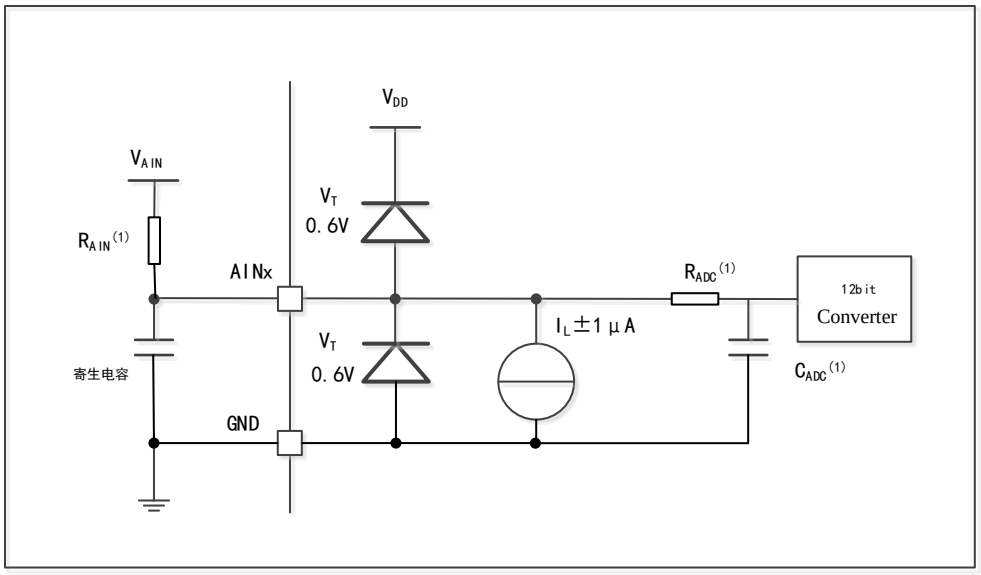
Table41 Characteristics of 12-bit ADC (V_{DD} =2.4~3.6V, T_A =-40~105℃)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Supply voltage	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on V_{REF} input pin	-	-	260	484	μA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling rate	-	0.05	-	1	MHz
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V
t_{CAL}	Calibration time	f_{ADC} = 14MHz	5.9			μs
		-	83			1/f_{ADC}
R_{ADC}	Sampling resistor	-	1			kΩ
C_{ADC}	Sample and hold capacitance	-	12			Pf

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_S	Sampling time	f_{ADC} = 14MHz	0.107	-	17.1	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14MHz	1	-	18	μs
		-	14~252 (sampling t_S + gradually approaching 12.5			$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation and not tested in production.
2. $C_{parasitic}$ refers to the parasitic capacitance (about 7PF) on the PCB (related to the welding and PCB layout quality) and the pad. Large $C_{parasitic}$ value will reduce the conversion accuracy. The solution is to reduce $f_{AD}C$.

Figure 19 Typical Application of ADC



The calculation formula for maximum value of external input impedance is as follows:

Formula 1: Maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

$$\frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})}$$

Where f_{ADC}=14MHZ, CADC=12PF (Table41), RADC=1kΩ (Table41); the relationship between T_S and R_{AIN} under the condition of 0.25LSB sampling error accuracy is shown in the following table:

Table42 Maximum R_{AIN} at f_{ADC}=14MHz (1)

T_S (cycle)	t_S（μs）	Maximum R_{AIN} (kΩ)

T_S (cycle)	t_S（μs）	Maximum R_{AIN} (kΩ)
1.5	0.11	1.2
7.5	0.54	10
13.5	0.96	19
28.5	2.04	41
41.5	2.96	60
55.5	3.96	80
71.5	5.11	104
239.5	17.1	350

1. Guaranteed by design and not tested in production.

Table43 ADC Accuracy (1) (2)

Symbol	Parameter	Test conditions	Typical value	Maximum value (3)	Unit
ET	Composite error	f_{PCLK2}=56MHz, f_{ADC}=14MHz,R_{AIN}<10KΩ, V_{DDA}=2.4~3.6V,T_A=-40~105℃ Measurement is conducted after ADC calculation	±2.5	±4.5	LSB
EO	Offset error		±1.0	±2	
EG	Gain error		±2.0	±3.5	
ED	Differential linear error		±1.5	±3	
EL	Integral linear error		±2.5	±4	

1. DC accuracy value of ADC is measured after internal calibration.
2. The backward injection of current will significantly affect the ADC accuracy. It is recommended to add a Schottky diode (between the pin and the ground) on the standard analog pin that may generate backward injection of current.

   As long as the forward injection current is within the range of $I_{INJ\ (PIN)}$ and $\Sigma I_{INJ\ (PIN)}$ given in 5.9, the ADC accuracy will not be affected.
3. It is assessed value.

5.12.1.2 Test of Built-in Reference Voltage Characteristics

Table44 Built-in Reference Voltage Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REFINT}(1)	Built-in Reference Voltage	-40℃ < T_A < +125℃ V_{DD}= 2-3.6 V	1.16	1.21	1.26	V
$T_{S\_vrefint}$(2)	Sampling time of ADC when reading out internal reference voltage	-	-	5.1	17.1	μs
V_{REFINT}	Change of built-in reference voltage value in the full temperature range	VDD=3V±10mV	-	-	10	mV
T_{Coeff}	-	-	-	-	126	ppm/℃

1. The data are obtained from a comprehensive evaluation and are not tested in production.
2. Guaranteed by design and not tested in production.

5.13 Temperature sensor characteristics

Table45 Temperature Sensor Characteristics

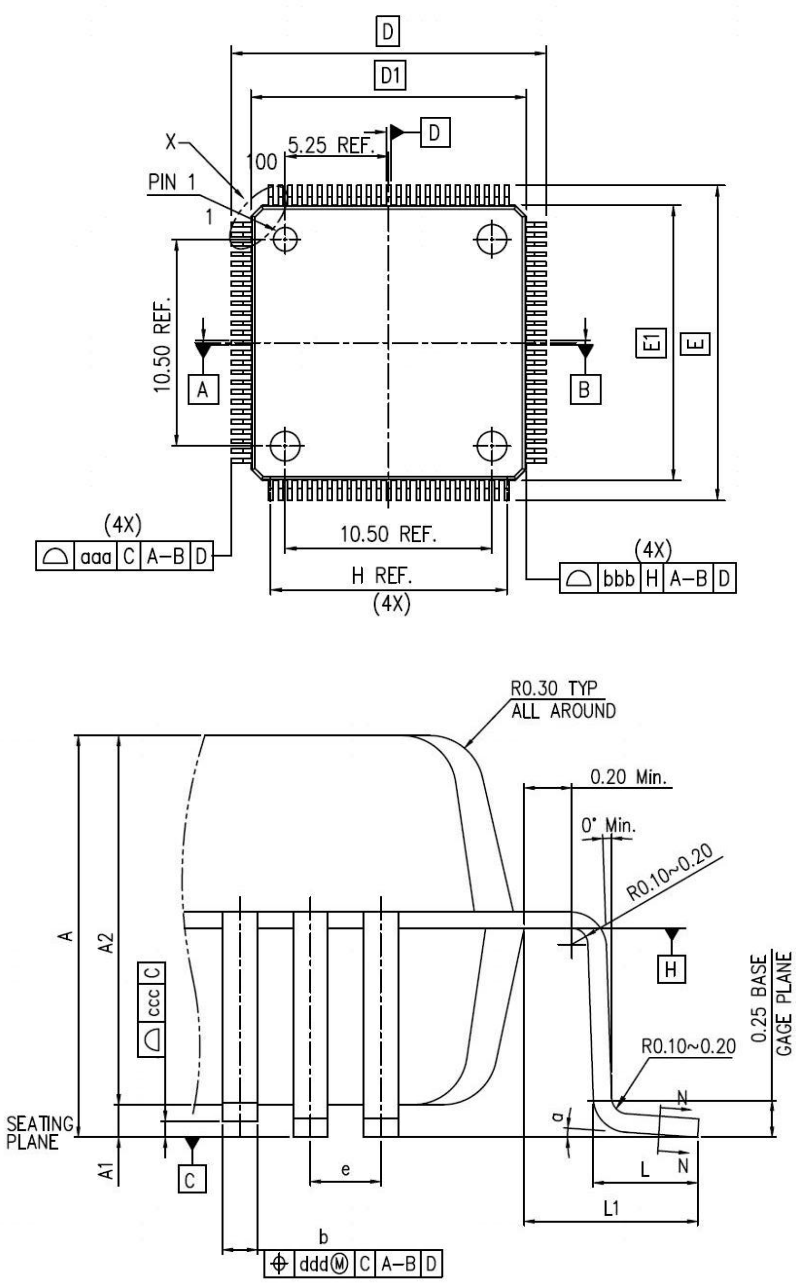
Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
Avg_Slope(1)	Average slope (V_{DD} = 3.3V, T_A = -40~105℃)	2.7	3.6	3.9	mV/ºC
V_{25}	Voltage at 25ºC (V_{DD} = 2.0-3.6V)	1.38	1.41	1.45	V
t_{START}(2)	Setup time	4	-	10	μs
T_{S_temp}(2)(3)	ADC sampling time when reading the temperature	-	-	17.1	μs

1. Guaranteed by characteristic analysis and not tested in production.
2. Guaranteed by design and not tested in production.
3. The minimum sampling time can be determined by multiple loops in the application.

6 Package information

6.1 LQFP100 Package Diagram

Figure 20LQFP100 Package Diagram



1. The figure is not drawn to scale.
2. The back pad inside is not connected to V_{SS} or V_{DD}.
3. There is a pad at the bottom of the LQFP package, which should be welded on the PCB.
4. All pins should be soldered to the PCB.

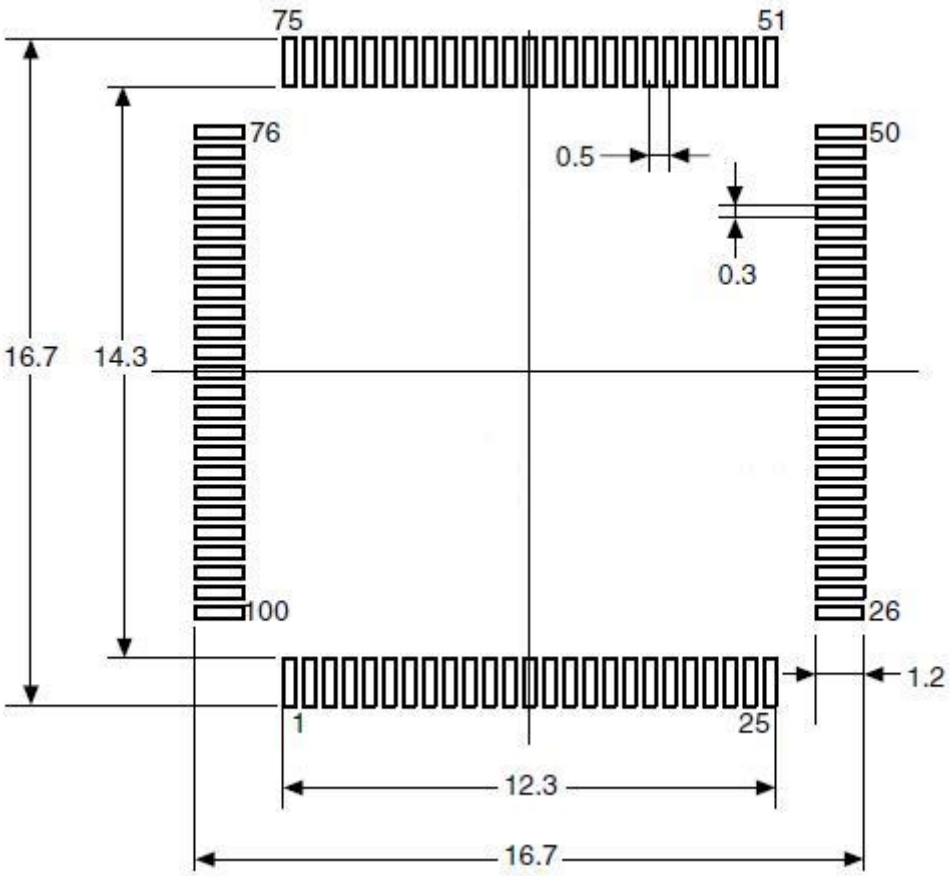
Table46 LQFP100 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)

S/N	SYM	DIMENDIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	16.00±0.20	LEAD TIP TO TIP
5	D1	14.00±0.10	PKG LENGTH
6	E	16.00±0.20	LEAD TIP TO TIP
7	E1	14.00±0.10	PKG WDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	0.15	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(12.00)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

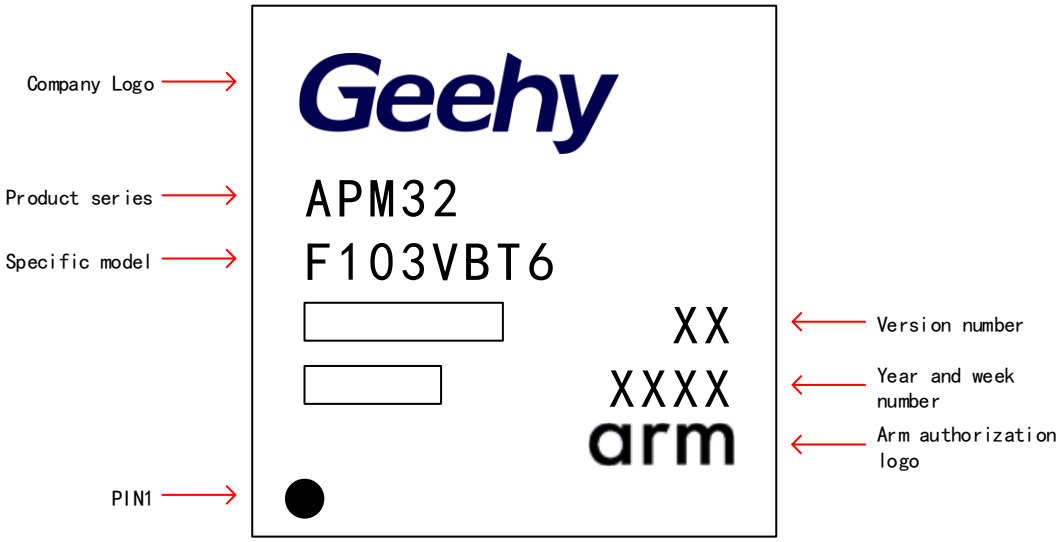
1. Dimensions are expressed in mm.

Figure 21 LQFP100 - 100 Pins, 14 x 14mm Welding Layout Recommendations



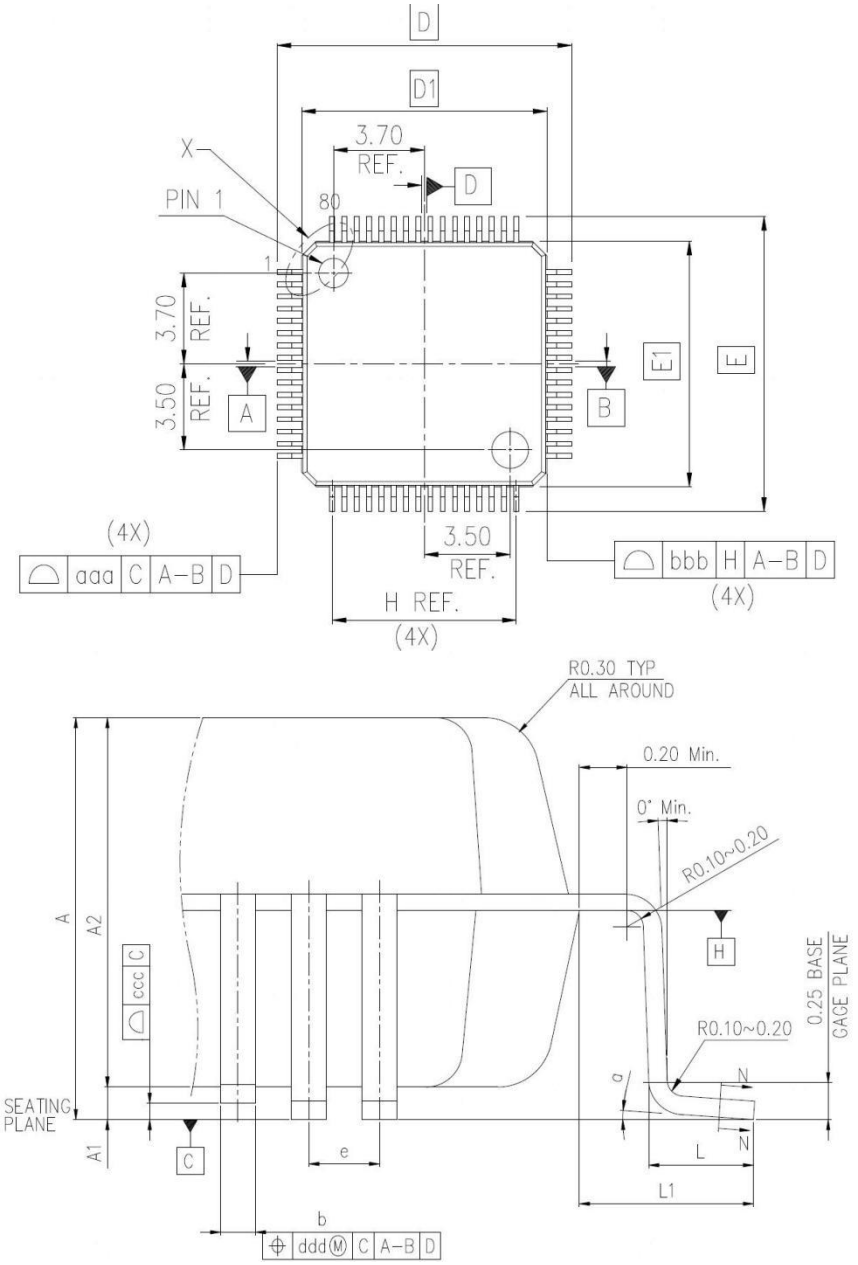
1. Dimensions are expressed in mm.

Figure 22 LQFP100 - 100 Pins, 14 x 14mm Package Identification



6.2 LQFP64 Package Diagram

Figure 23 LQFP64 Package Diagram



1. The figure is not drawn to scale.
2. The back pad inside is not connected to V_{SS} or V_{DD}.
3. There is a pad at the bottom of the LQFP package, which should be welded on the PCB.
4. All pins should be soldered to the PCB.

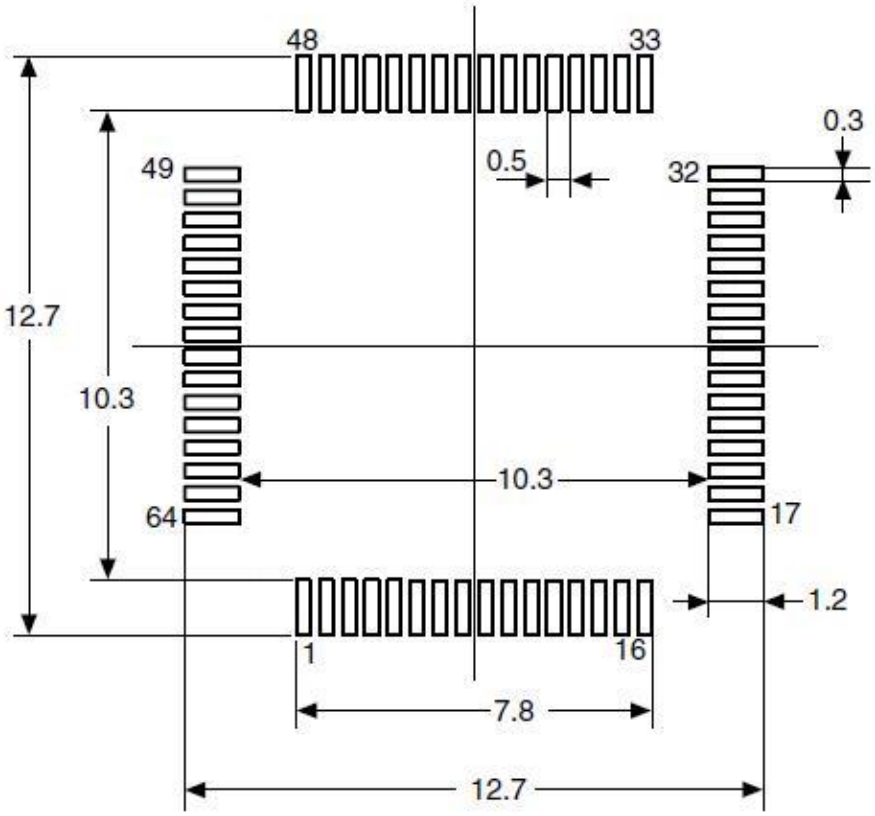
Table47 LQFP64 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)

S/N	SYM	DIMENDIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A1	0.100±0.050	STANDOFF
3	A2	1.400±0.050	PKG THICKNESS
4	D	12.000±0.200	LEAD TIP TO TIP
5	D1	10.000±0.100	PKG LENGTH
6	E	12.000±0.200	LEAD TIP TO TIP
7	E1	10.000±0.100	PKG WDTH
8	L	0.600±0.150	FOOT LENGTH
9	L1	1.000 REF	LEAD LENGTH
10	T	0.150	LEAD THICKNESS
11	T1	0.127±0.030	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.220±0.050	LEAD WIDTH
14	b1	0.200±0.030	LEAD BASE METAL WIDTH
15	e	0.500 BASE	LEAD PITCH
16	H(REF.)	(7.500)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

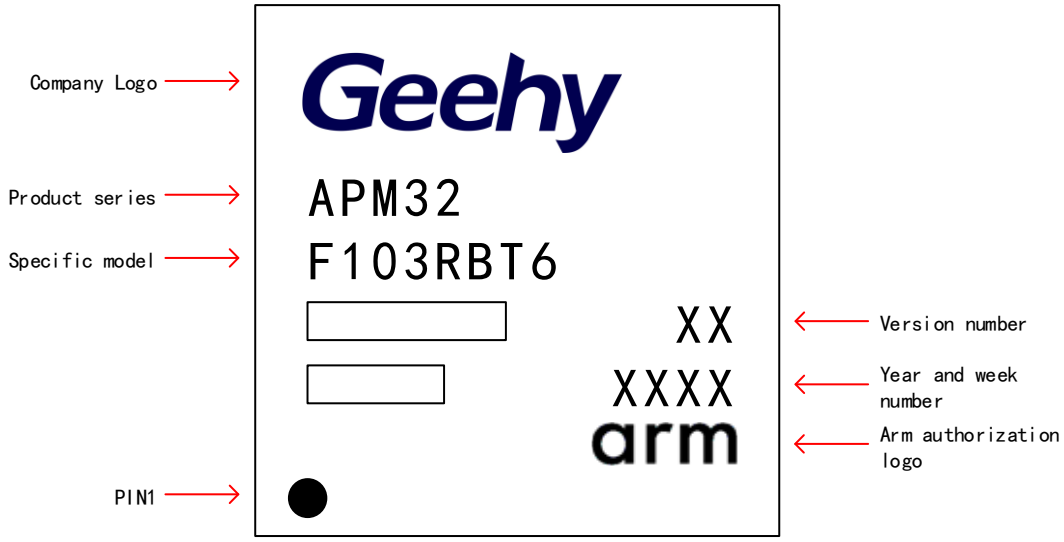
1. Dimensions are expressed in mm.

Figure 24 QFP64 - 64 Pins, 10 x 10mm Welding Layout Recommendations



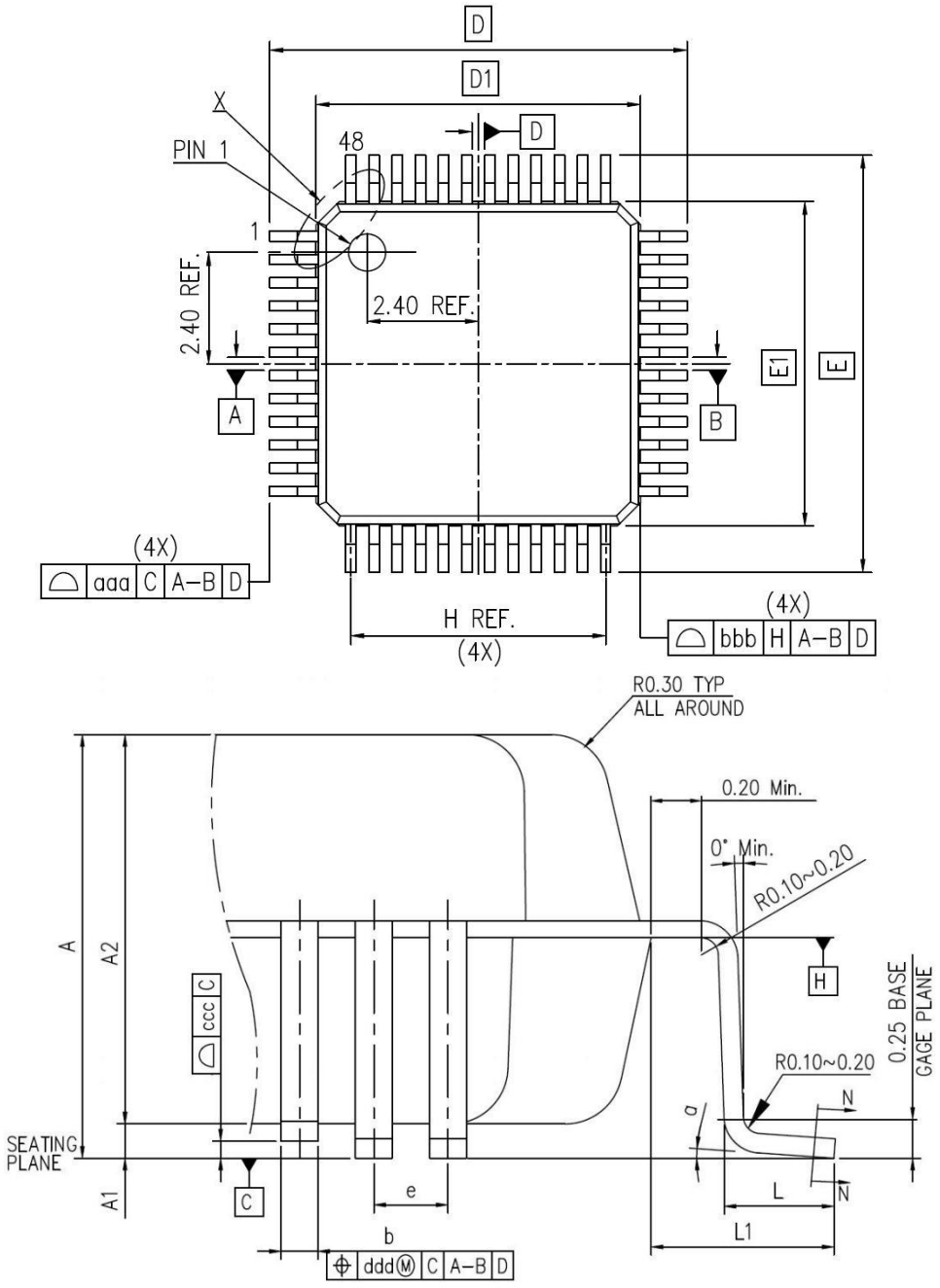
1. Dimensions are expressed in mm.

Figure 25 LQFP64 - 64 Pins, 10 x 10mm Package Identification



6.3 LQFP48 Package Diagram

Figure 26 LQFP48 Package Diagram



1. The figure is not drawn to scale.
2. The back pad inside is not connected to V_{SS} or V_{DD}.
3. There is a pad at the bottom of the LQFP package, which should be welded on the PCB.
4. All pins should be soldered to the PCB.

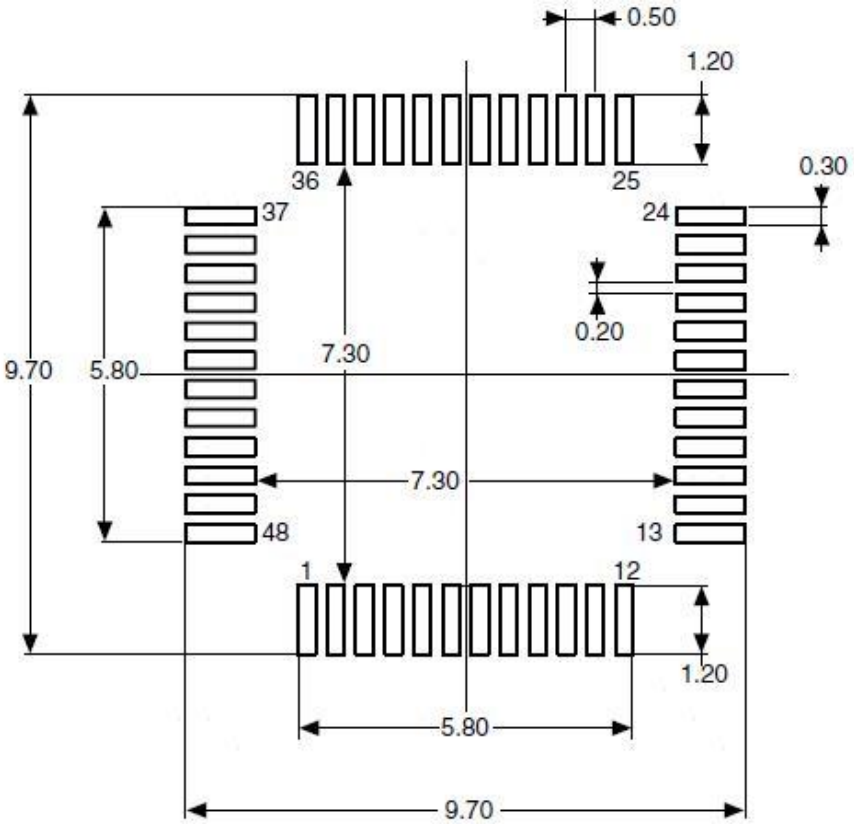
Table48 LQFP48 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)

S/N	SYM	DIMENDIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	9.00±0.20	LEAD TIP TO TIP
5	D1	7.00±0.10	PKG LENGTH
6	E	9.00±0.20	LEAD TIP TO TIP
7	E1	7.00±0.10	PKG WDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	0.15	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(5.50)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

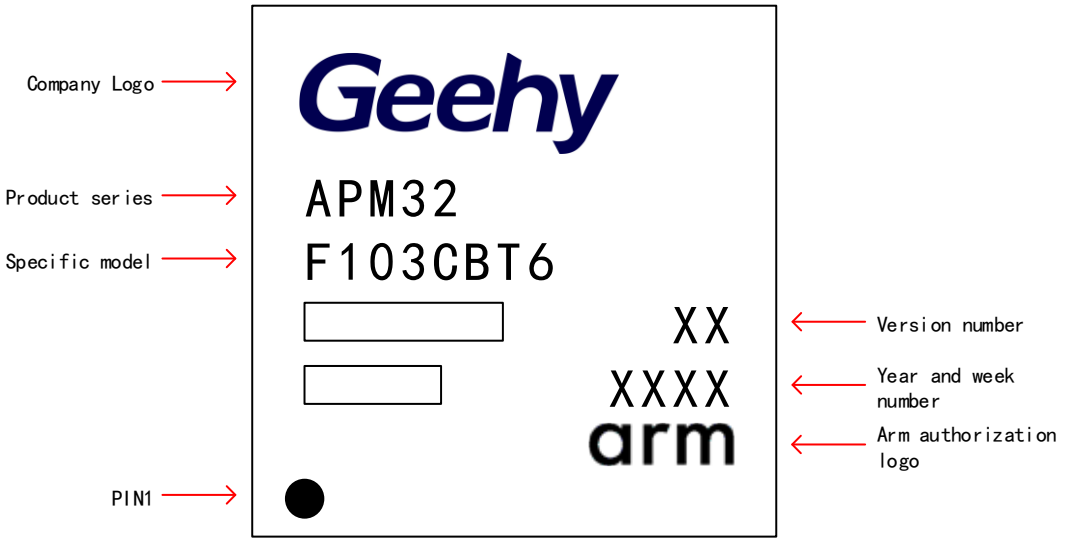
1. Dimensions are expressed in mm.

Figure 27 LQFP48 - 48 Pins, 7 x 7mm Welding Layout Recommendations



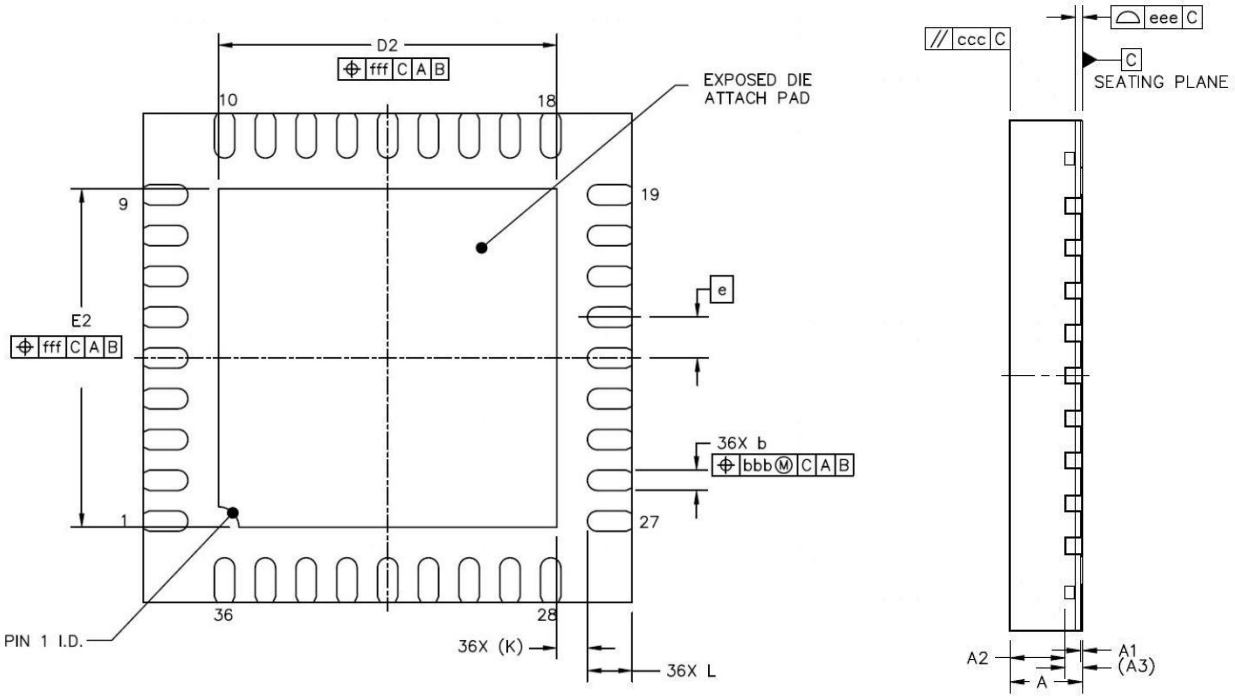
1. Dimensions are expressed in mm.

Figure 28 LQFP48 -48 Pins, 7 x 7mm Identification



6.4 QFN36 Package Diagram

Figure 29 QFN36 Package Diagram



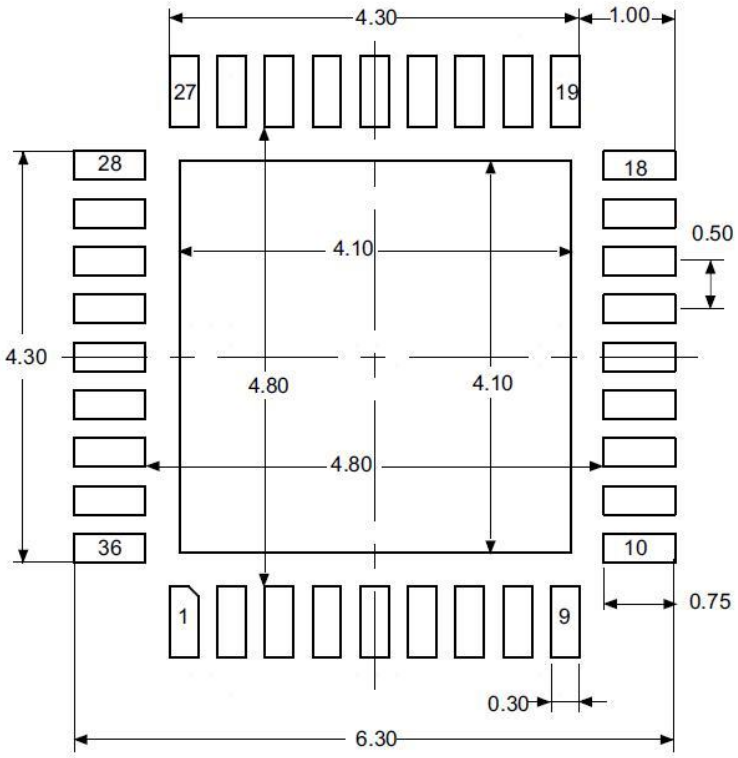
1. The figure is not drawn to scale.
2. The back pad inside is not connected to V_{SS} or V_{DD}.
3. There is a pad at the bottom of the QFN package, which should be welded on the PCB.
4. All pins should be soldered to the PCB.

Table 49 QFN36 Package Data

		SYMBOL	MIN	NOD	MAX
TOTAL THCKNESS		A	0.8	0.85	0.9
STANO OFF		A1	0	0.02	0.05
MOLO THCKNESS		A2	---	0.65	---
L/F THCKNESS		A3	0.203REF		
LEAD WIDTH		b	0.2	0.25	0.3
BOOY SIZE	X	D	6 BSC		
	Y	E	6 BSC		
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D2	4.05	4.15	4.25
	Y	E2	4.05	4.15	4.25
LEAD LENGTH		L	0.45	0.55	0.65
LEAD TIP TO EXPOSE PAD EDGE		k	0.375 REF		
PACKAGE EOGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		
EXPOSED PAD OFFSET		fff	0.1		

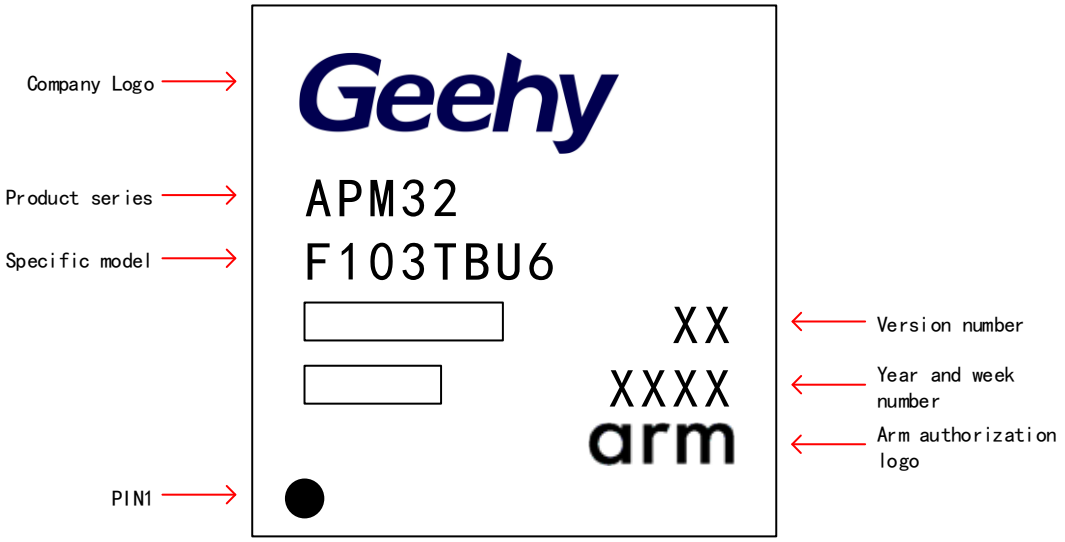
1. Dimensions are expressed in mm.

Figure 30 QFN36 - 36 Pins, 6 x 6mm Welding Layout Recommendations



1. Dimensions are expressed in mm.

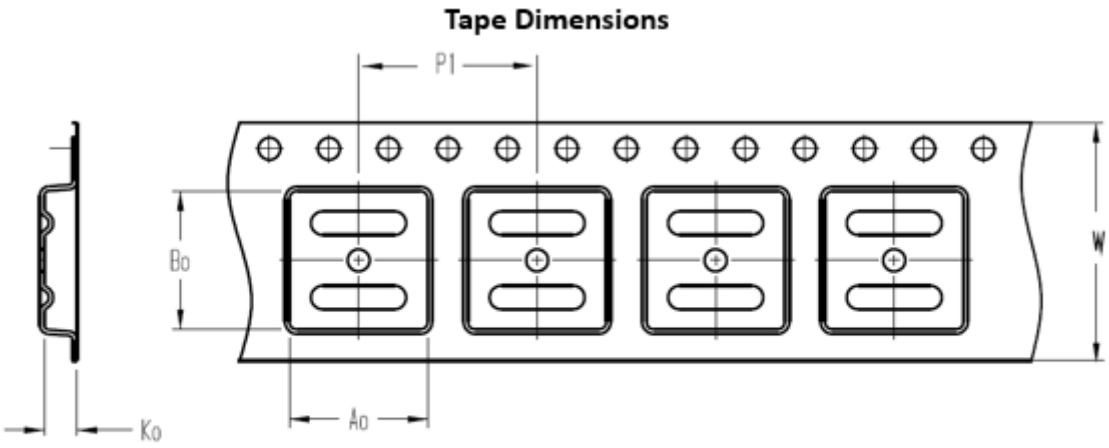
Figure 31 QFN36 - 36 Pins, 6 x 6mm Identification



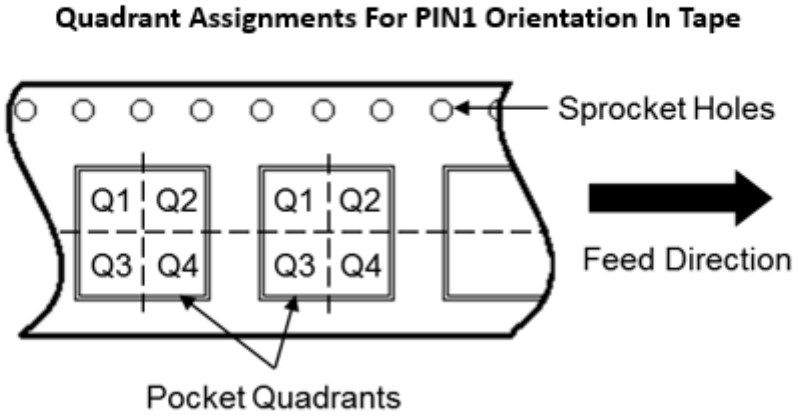
7 Packaging Information

7.1 Reel Packaging

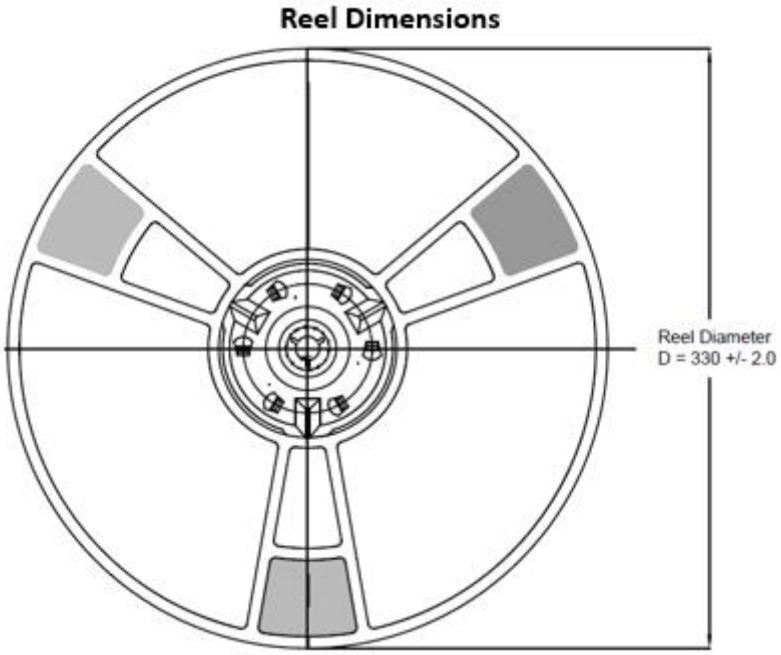
Figure 32 Specification Drawing of Reel Packaging



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Reel Dimensions



All photos are for reference only, and the appearance is subject to the product.

Table50 Reel Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
APM32F103RBT7	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F103RBT6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F103R8T6	LQFP	64	1000	330	12.35	12.35	2.2	16	24	Q1
APM32F103CBT6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F103C8T6	LQFP	48	2000	330	9.3	9.3	2.2	12	16	Q1
APM32F103TBU7	QFN	36	2500	330	6.4	6.4	1.4	8	16	Q1
APM32F103TBU6	QFN	36	2500	330	6.4	6.4	1.4	8	16	Q1
APM32F103T8U6	QFN	36	2500	330	6.4	6.4	1.4	8	16	Q1

7.2 Tray packaging

Figure 33 Tray Packaging Diagram

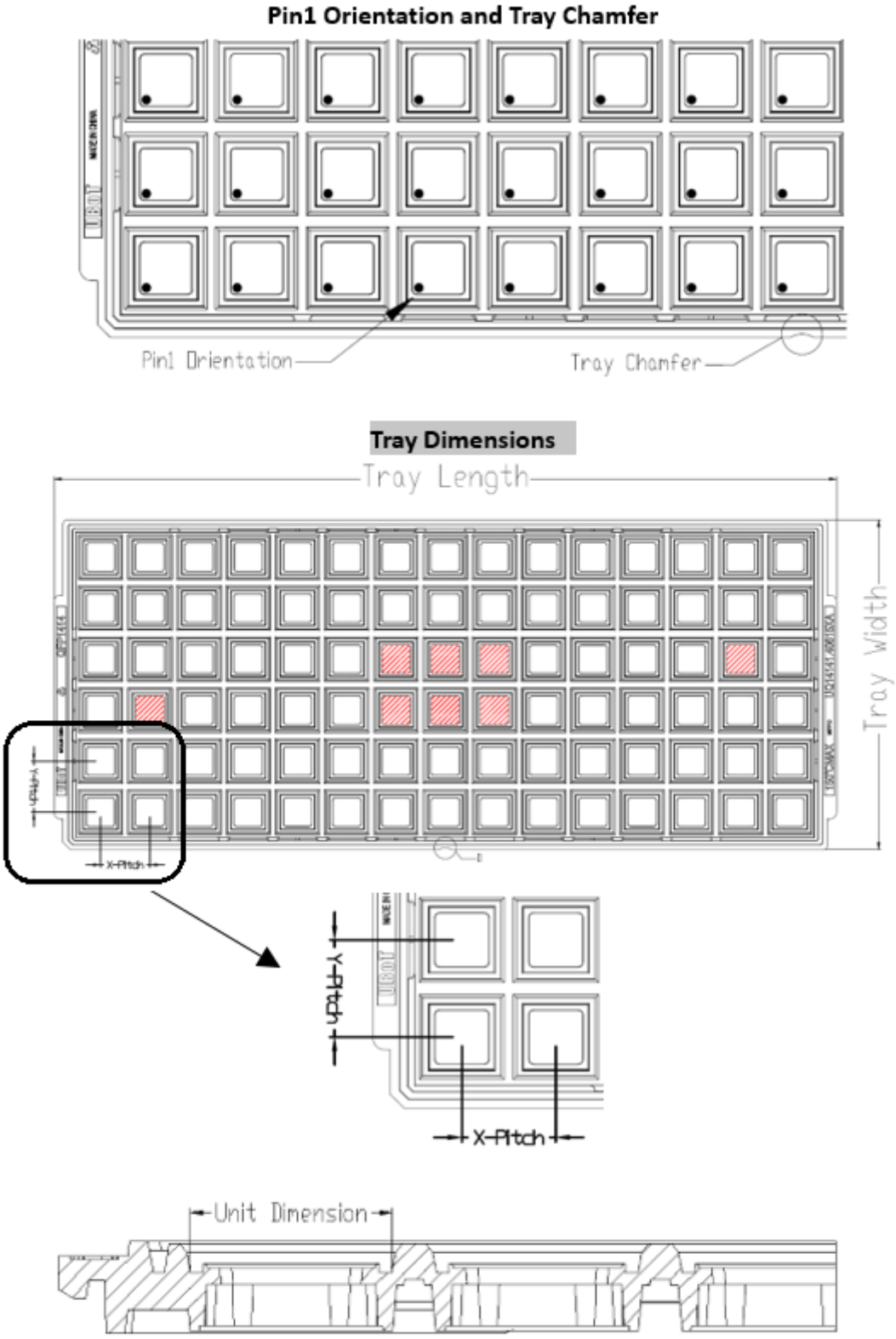


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Table51 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension	Y-Dimension	X-Pitch	Y-Pitch	Tray Length	Tray Width
				(mm)	(mm)	(mm)	(mm)	(mm)	(mm)
APM32F103VBT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F103V8T6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F103RBT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F103RBT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F103R8T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F103CBT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F103C8T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F103TBU7	QFN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32F103TBU6	QFN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32F103T8U6	QFN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9

8 Ordering Information

Figure 34 APM32F103xB Series Ordering Information Diagram

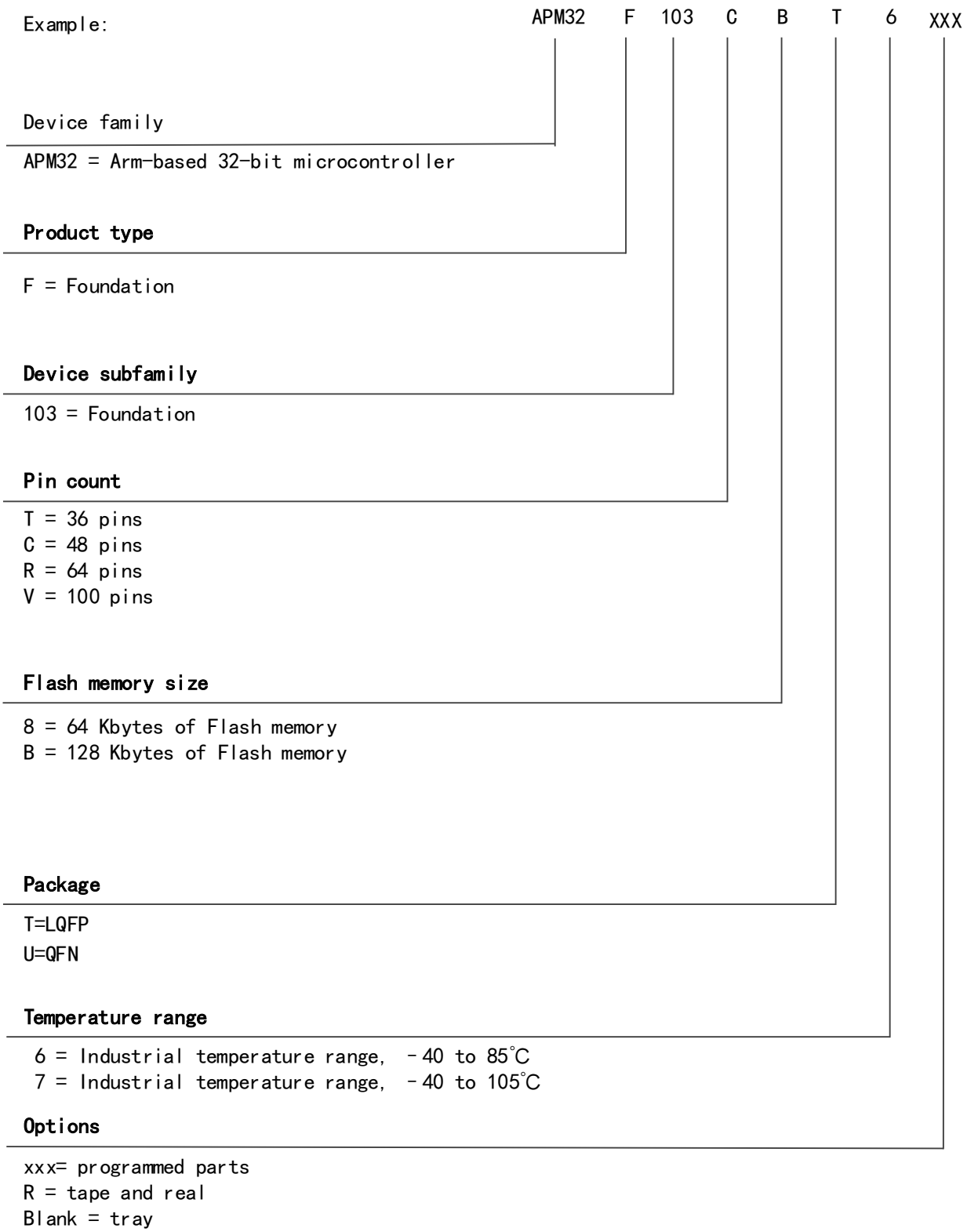

Table52 Ordering Information Table

Order Code	FLASH(KB)	SRAM(KB)	Package	SPQ	Temperature range
APM32F103T8U6-R	64	36	QFN36	2500	Industrial grade -40℃~85℃
APM32F103T8U6	64	36	QFN36	4900	Industrial grade -40℃~85℃
APM32F103TBU6-R	128	36	QFN36	2500	Industrial grade -40℃~85℃
APM32F103TBU6	128	36	QFN36	4900	Industrial grade -40℃~85℃
APM32F103TBU7-R	128	36	QFN36	2500	Industrial grade -40℃~105℃
APM32F103TBU7	128	36	QFN36	4900	Industrial grade -40℃~105℃
APM32F103C8T6-R	64	36	LQFP48	2000	Industrial grade -40℃~85℃
APM32F103C8T6	64	36	LQFP48	2500	Industrial grade -40℃~85℃
APM32F103CBT6-R	128	36	LQFP48	2000	Industrial grade -40℃~85℃
APM32F103CBT6	128	36	LQFP48	2500	Industrial grade -40℃~85℃
APM32F103R8T6-R	64	36	LQFP64	1000	Industrial grade -40℃~85℃
APM32F103R8T6	64	36	LQFP64	1600	Industrial grade -40℃~85℃
APM32F103RBT6-R	128	36	LQFP64	1000	Industrial grade -40℃~85℃
APM32F103RBT6	128	36	LQFP64	1600	Industrial grade -40℃~85℃
APM32F103RBT7-R	128	36	LQFP64	1000	Industrial grade -40℃~105℃
APM32F103RBT7	128	36	LQFP64	1600	Industrial grade -40℃~105℃
APM32F103V8T6	64	36	LQFP100	900	Industrial grade -40℃~85℃
APM32F103VBT6	128	36	LQFP100	900	Industrial grade -40℃~85℃

1. SPQ=Smallest Packaging Quantity

9 Commonly Used Function Module Denomination

Table53 Commonly Used Function Module Denomination

Chinese description	Abbreviation
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management unit	RCM
External Interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power management unit	PMU
Backup register	BAKPR
DMA controller	DMA
Analog-to-digital converter	ADC
Digital-to-analog converter	DAC
Real-time clock	RTC
External memory controller	EMMC
SDIO interface	SDIO
USBD device controller	USBD
Controller local area network	CAN
USBD OTG	OTG
Ethernet	ETH
I2C Interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

10 Version history

Table54 Document Revision History

Date	Version	Change History
2023.9	1.0	New
2024.1	1.1	(1) Modify the figure of Power Supply Scheme,and add the note.

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The information in this document replaces the information provided in all previous versions of the document.