MICROCHIP

RE46C194

CMOS Low-Voltage Photoelectric Smoke Detector ASIC with Interconnect and Timer Mode

Features

- 3V Lithium or Two AA Battery Operation
- Low Quiescent Current Consumption
- Programmable Infrared Emitting Diode (IRED) Drive Current
- End-of-Life Capability
- Programmable Photoelectric Amplifier Setup
- 6-Bit Analog-to-Digital Converter (ADC)
- Programmable Alarm Limits
- Long-Term Drift Adjustment
- Chamber Test
- 9-Minute Timer for Hush Operation
- Programmable Feature Selection
- Low-Battery Test
- Temporal or Continuous Horn Pattern
- Horn Synchronization
- Auto-Alarm Locate
- Local Alarm Memory
- Interconnect Up to 40 Detectors
- Remote Carbon Monoxide (CO) Alarm Response
- Compatible with RE46C191
- Packaging:
  - 3.9 mm, 16-Lead SOIC

Description

RE46C194 is a low-power, low-voltage CMOS photoelectric-type smoke detector IC. With minimal external components, this circuit provides all the required features for a photoelectric smoke detector.

The design incorporates a programmable gain photo amplifier for use with an infrared emitter/detector pair.

An internal oscillator strobes power to the smoke detection circuitry every 10 seconds to keep the Standby current to a minimum. If smoke is sensed, the detection rate is increased to verify an Alarm condition. High-Gain mode is available for push-button chamber testing.

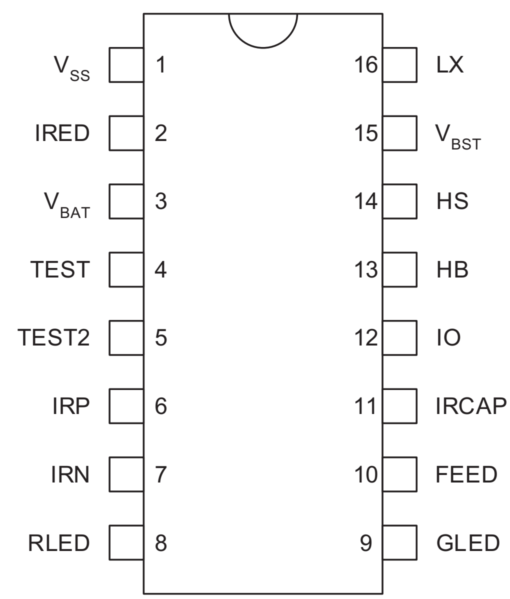
A check for a Low-Battery condition is performed every 86 seconds, and chamber integrity is tested once every 43 seconds when in Standby mode. The temporal horn pattern supports the NFPA 72 (*National Fire Alarm and Signaling Code*) emergency evacuation signal.

An interconnect pin allows multiple detectors to be connected, so when one RE46C194 device alarms, all devices sound.

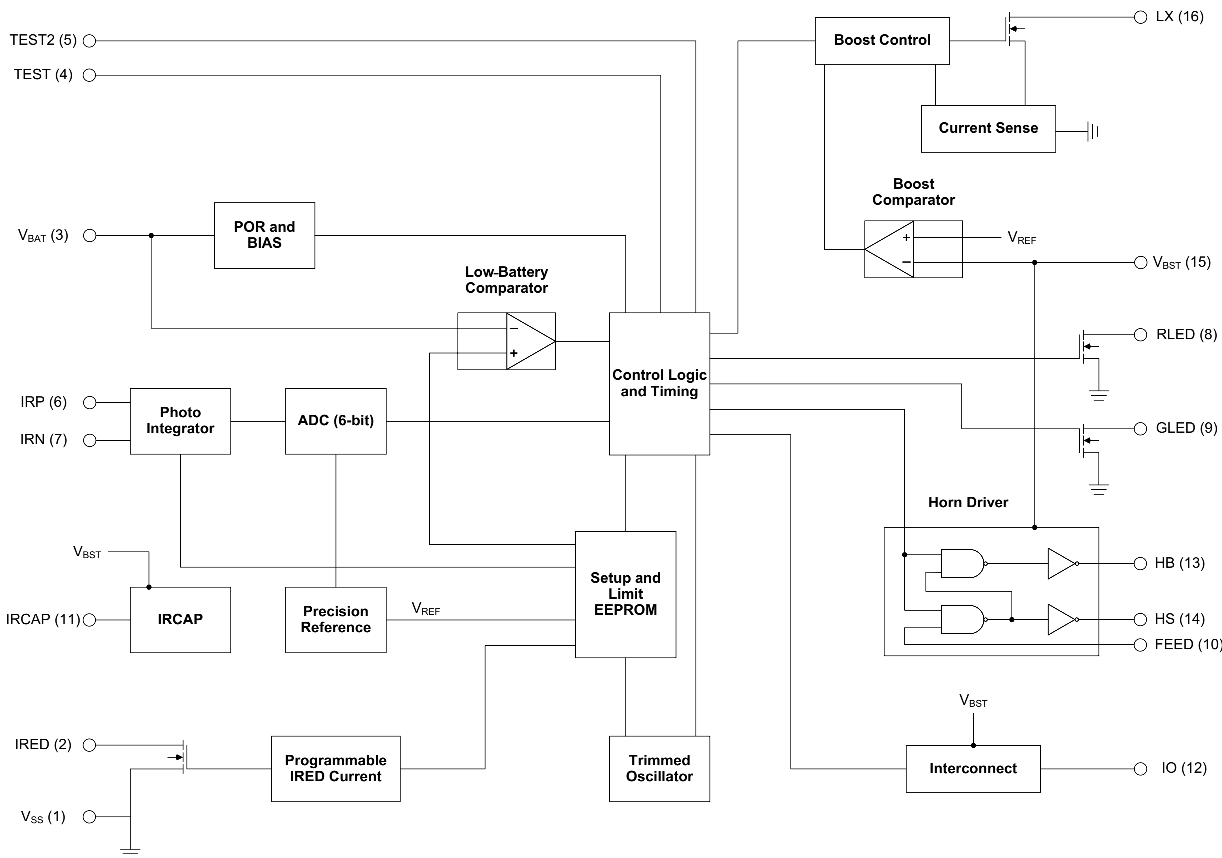
An internal 9-minute timer can be used for Hush mode.

Package Type

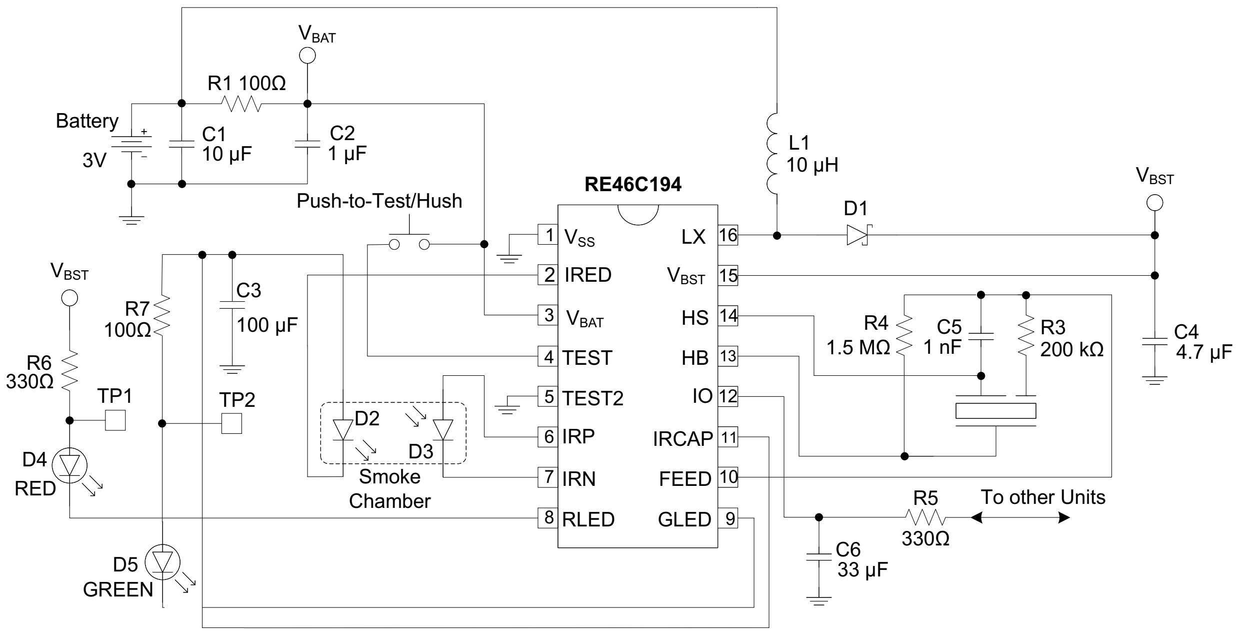
16-Lead SOIC



Functional Block Diagram



Typical Application



Note 1: C1 must be located as close as possible to the V_{SS} power input connection. C2 must be located as close as possible to the device power pins.

2: R3, R4 and C5 are typical values and may be adjusted to maximize sound pressure.

3: The boost regulator in High Boost mode (for example, V_{BST} = 8.5V or 10V) can draw current pulses greater than 0.6A and is, therefore, very sensitive to series resistance. Critical components of this resistance are the inductor DC resistance, the internal resistance of the battery and the resistance in the connections from the inductor to the battery, as well as from the inductor to the LX pin and from the V_{SS} pin to the battery. In order to function properly under full load at V_{BAT} = 2V, the total of the inductor and IC resistances must not exceed 0.3Ω. The internal battery resistance must not be more than 0.5Ω and a low-ESR capacitor of 10 µF or more must be connected in parallel with the battery to average the current draw over the boost converter cycle.

4: Schottky diode D1 must have a maximum peak current rating of at least 0.8A. For best results, it must have a forward-voltage specification of less than 0.5V at 0.8A and low reverse leakage.

5: Inductor L1 must have a maximum peak current rating of at least 0.8A.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings (†)

Supply Voltage .... V_{BAT} = 5.5V, V_{BST} = 13V
Input Voltage Range Except FEED and TEST Pins .... V_{IN} = –0.3V to V_{BAT} + 0.3V
FEED Input Voltage Range .... V_{INFD} = –10V to +22V
TEST Input Voltage Range .... V_{INTEST} = –0.3V to V_{BST} + 0.3V
LX Voltage .... V_{LX} = –0.3V to +13V
IRCAP Voltage .... V_{IRCAP} = 5.5V
Input Current Except FEED Pin .... I_{IN} = 10 mA
Continuous Operating Current (HS, HB and V_{BST} Pins) .... I_O = 20 mA
Continuous Operating Current (IRED Pin) .... I_{OIR} = 300 mA
Operating Temperature .... T_A = –10°C to +60°C
Storage Temperature .... T_{STG} = –55°C to +125°C
ESD Human Body Model .... V_{HBM} = 2 kV
ESD Machine Model .... V_{MM} = 150V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.2 Electrical Specifications

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = –10°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** through **Note 7**).

Parameters	Symbol	Test Pin	Min.	Typical	Max.	Units	Conditions
System Supply							
Supply Voltage	V_{BAT}	3	2	—	5	V	Operating
Supply Current	I_{BAT1}	3	—	1	2	µA	Standby, inputs low, no loads, boost off, no smoke check
Boost Regulator							
Standby Boost Current	I_{BST1}	15	—	100	—	nA	Standby, inputs low, no loads, boost off, no smoke check
Boost Voltage	V_{BST1}	15	3.3	3.6	3.9	V	IRCAP charging for smoke check, GLED operation, I_{OUT} = 20 mA
	V_{BST2}	15	8	8.5	9	V	No local alarm, RLED operation, I_{OUT} = 20 mA, IO as an input
	V_{BST3}	15	9.4	10	10.6	V	
Photo Detection							
Input Leakage	I_{INOPP}	6	–200	—	200	pA	I_{RP} = V_{BAT} or V_{SS}
	I_{INOPN}	7	–200	—	200	pA	I_{RN} = V_{BAT} or V_{SS}
IRCAP Supply Current	I_{IRCAP}	11	—	500	—	µA	During smoke check
IRCAP Turn-On Voltage	V_{TIR1}	11	3.6	4	4.4	V	Falling edge, V_{BST} = 5V, I_{OUT} = 20 mA
IRCAP Turn-Off Voltage	V_{TIR2}	11	4	4.4	4.8	V	Rising edge, V_{BST} = 5V, I_{OUT} = 20 mA
IRED On Time	t_{IRON}	2	—	100	—	µs	Prog bits 38, 39 = `0, 0`
				200			Prog bits 38, 39 = `1, 0`
				300			Prog bits 38, 39 = `0, 1`
				400			Prog bits 38, 39 = `1, 1`
Smoke Check Duration	t_{PUL}	2	2.82	3	3.18	ms	Standby

Note 1: Wherever a specific V_{BST} value is listed under test conditions, the V_{BST} is forced externally with the inductor disconnected and the DC-DC converter NOT running.

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4: Not production tested.

5: See timing diagram for the horn pattern (Figure 4-2).

6: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

7: See timing diagram for horn synchronization and AAL (Figure 5-5).

1.2 Electrical Specifications (Continued)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = –10°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** through **Note 7**).

Parameters	Symbol	Test Pin	Min.	Typical	Max.	Units	Conditions
Smoke Check Period with Temporal Horn Pattern	t_{PER0}	2	10	10.7	11.4	s	Standby, no alarm
	t_{PER1A}	2	1.88	2	2.12	s	Standby, after one valid smoke sample
	t_{PER2A}	2	0.94	1	1.06	s	Standby, after two consecutive valid smoke samples
	t_{PER3A}	2	0.94	1	1.06	s	Local alarm (three consecutive valid smoke samples)
	t_{PER4A}	2	235	250	265	ms	Push button test, >1 chamber detections
	t_{PER4C}	2	313	333	353	ms	Push button test, no chamber detections
	t_{PER5A}	2	7.5	8	8.5	s	In remote alarm
Smoke Check Period with Continuous Horn Pattern	t_{PER0}	2	10	10.7	11.4	s	Standby, no alarm
	t_{PER1B}	2	2.5	2.7	2.9	s	Standby, after one valid smoke sample
	t_{PER2B}	2	1.25	1.33	1.41	s	Standby, after two consecutive valid smoke samples
	t_{PER3B}	2	1.25	1.33	1.41	s	Local alarm (three consecutive valid smoke samples)
	t_{PER4B}	2	313	333	353	ms	Push button test
	t_{PER5B}	2	10	10.7	11.4	s	In remote alarm
Chamber Test Period	t_{PCT1}	2	40	43	46	s	Standby, no alarm
Long-Term Drift Sample Period	t_{LTD}	2	400	430	460	s	Standby, no alarm, LTD enabled
IO Function							
IO Hysteresis	V_{HYST1}	12	—	150	—	mV	—
Input Pull-Down Current	I_{PD1}	4, 5	3	10	30	µA	V_{IN} = V_{BAT}
	I_{PDIO1}	12	20	—	80	µA	V_{IN} = V_{BAT}
	I_{PDIO2}	12	—	—	140	µA	V_{IN} = 15V
Output Current	I_{IOH1}	12	-4	-5	—	mA	Alarm, V_{IO} = 3V or V_{IO} = 0V, V_{BST} = 9V
	I_{IODMP}	12	5	15	—	mA	At conclusion of local alarm or test, V_{IO} = 1V
Input-Voltage Low	V_{IL2}	12	—	—	800	mV	No local alarm, IO as an input
Input-Voltage High	V_{IH2}	12	2	—	—	V	No local alarm, IO as an input

Note 1: Wherever a specific V_{BST} value is listed under test conditions, the V_{BST} is forced externally with the inductor disconnected and the DC-DC converter NOT running.

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4: Not production tested.

5: See timing diagram for the horn pattern (Figure 4-2).

6: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

7: See timing diagram for horn synchronization and AAL (Figure 5-5).

1.2 Electrical Specifications (Continued)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = –10°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** through **Note 7**).

Parameters	Symbol	Test Pin	Min.	Typical	Max.	Units	Conditions
IRCAP LED Supply							
IRED Current Temperature Coefficient	T_{CIRED}	—	—	0.5	—	%/°C	V_{BST} = 5V, IRCAP = 5V (**Note 4**)
Output Current	I_{IRED50}	2	45	50	55	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V (50 mA option selected; T_A = +25°C)
	$I_{IRED100}$	2	90	100	110	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V (100 mA option selected; T_A = +25°C)
	$I_{IRED150}$	2	135	150	165	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V (150 mA option selected; T_A = +25°C)
	$I_{IRED200}$	2	180	200	220	mA	IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V (200 mA option selected; T_A = +25°C)
Battery							
Low-Battery Alarm Voltage	V_{LB1}	3	2.05	2.1	2.15	V	Falling edge, 2.1V nominal selected
	V_{LB2}	3	2.15	2.2	2.25	V	Falling edge, 2.2V nominal selected
	V_{LB3}	3	2.25	2.3	2.35	V	Falling edge, 2.3V nominal selected
	V_{LB4}	3	2.35	2.4	2.45	V	Falling edge, 2.4V nominal selected
	V_{LB5}	3	2.45	2.5	2.55	V	Falling edge, 2.5V nominal selected
	V_{LB6}	3	2.55	2.6	2.65	V	Falling edge, 2.6V nominal selected
	V_{LB7}	3	2.65	2.7	2.75	V	Falling edge, 2.7V nominal selected
	V_{LB8}	3	2.75	2.8	2.85	V	Falling edge, 2.8V nominal selected
Low-Battery Hysteresis	V_{LBHYST}	3	—	100	—	mV	—
Low-Battery Sample Period	t_{PLB1}	3	320	344	368	s	RLED on
	t_{PLB2}	3	80	86	92	s	RLED off
Time Base							

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5: See timing diagram for the horn pattern (Figure 4-2).

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1.2 Electrical Specifications (Continued)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = –10°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** through **Note 7**).

Parameters	Symbol	Test Pin	Min.	Typical	Max.	Units	Conditions
Internal Clock Period	t_{PCLK}	—	9.8	10.4	11	ms	PROGSET, IO = High
RLED Indicator							
On Time	t_{ON1}	8	9.8	10.4	11	ms	Operating
Standby Period	t_{PLED1}	8	320	344	368	s	Standby, no alarm
Local Alarm Period	t_{PLED2A}	8	0.94	1	1.06	s	Local Alarm condition with temporal horn pattern
	t_{PLED2B}	8	625	667	710	ms	Local Alarm condition with continuous horn pattern
External Alarm Period	t_{PLED0}	8	LED IS NOT ON			s	Remote alarm only
Hush Timer RLED Indicator Period	t_{PLED4}	8	10	10.7	11.4	s	Timer mode, no local alarm
Output-Voltage Low	V_{OL2}	8	—	—	300	mV	I_{OL} = 10 mA, V_{BST} = 9V

Note 1: Wherever a specific V_{BST} value is listed under test conditions, the V_{BST} is forced externally with the inductor disconnected and the DC-DC converter NOT running.

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1.2 Electrical Specifications (Continued)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = –10°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** through **Note 7**).

Parameters	Symbol	Test Pin	Min.	Typical	Max.	Units	Conditions
GLED Indicator							
Latched Alarm Period	t_{PLED3}	9	40	43	46	s	Latched Alarm condition, LED enabled
Latched Alarm Pulse Train (3x) Off Time	t_{OFLED}	9	1.25	1.33	1.41	s	
Latched Alarm LED Enabled Duration	t_{LALED}	9	22.4	23.9	25.3	h	
Output-Voltage Low	V_{OL3}	9	—	—	300	mV	I_{OL} = 10 mA, V_{BST} = 3.6V
Hush Timer Operation							
Hush Timer Period	t_{TPER}	—	480	516	546	s	No alarm
Horn							
Input Leakage	I_{IHF}	10	—	20	50	µA	FEED = 22V, V_{BST} = 9V
	I_{ILF}	10	–50	–15	—	µA	FEED = –10V, V_{BST} = 10.7V
Input-Voltage Low	V_{IL1}	10	—	—	2.7	V	FEED, V_{BST} = 9V
Input-Voltage High	V_{IH1}	10	6.2	—	—	V	FEED, V_{BST} = 9V
Output-Voltage Low	V_{OL1}	13, 14	—	—	500	mV	I_{OL} = 16 mA, V_{BST} = 9V
Output-Voltage High	V_{OH1}	13, 14	8.5	—	—	V	I_{OL} = 16 mA, V_{BST} = 9V
Horn Operation							
Low Battery Horn Period	t_{HPER1}	13	40	43	46	s	Low battery, no alarm
Chamber Fail Horn Period	t_{HPER2}	13	40	43	46	s	Chamber failure
Low Battery Horn On Time	t_{HON1}	13	9.8	10.4	11	ms	Low battery, no alarm
Chamber Fail Horn On Time	t_{HON2}	13	9.8	10.4	11	ms	Chamber failure
Chamber Fail Horn Off Time	t_{HOF1}	13	305	325	345	ms	Failed chamber, no alarm, 3x chirp option
Alarm On Time with Temporal Horn Pattern	t_{HON2A}	13	470	500	530	ms	Local or remote alarm (**Note 5**)
Alarm Off Time with Temporal Horn Pattern	t_{HOF2A}	13	470	500	530	ms	Local or remote alarm (**Note 5**)
	t_{HOF3A}	13	1.4	1.5	1.6	s	Local or remote alarm (**Note 5**)
Alarm On Time with Continuous Horn Pattern	t_{HON2B}	13	235	250	265	ms	Local or remote alarm (**Note 5**)

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4: Not production tested.

5: See timing diagram for the horn pattern (Figure 4-2).

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7: See timing diagram for horn synchronization and AAL (Figure 5-5).

1.2 Electrical Specifications (Continued)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = –10°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** through **Note 7**).

Parameters	Symbol	Test Pin	Min.	Typical	Max.	Units	Conditions
Alarm Off Time with Continuous Horn Pattern	t_{HOF2B}	13	78	83	88	ms	Local or remote alarm (**Note 5**)
Push-to-Test (PTT) Alarm Memory On Time	t_{HON4}	13	9.8	10.4	11	ms	Alarm memory active, Push-to-Test
Push-to-Test Alarm Memory Horn Period	t_{HPER4}	13	235	250	265	ms	Alarm memory active, Push-to-Test
CO Alarm Period	t_{HPER5}	13, 14	5.5	5.8	6.1	s	CO alarm horn period
CO Alarm On Time	t_{HON5}	13, 14	95	100	105	ms	CO alarm
CO Alarm Off Time	t_{HOF6}	13, 14	95	100	105	ms	CO alarm horn off time between pulses
	t_{HOF7}	13, 14	4.8	5.1	5.4	s	CO alarm horn off time between pulse trains
Horn Synchronization							
IO Pulse Period	t_{PIO1}	2	3.8	4	4.2	s	Local alarm, temporal horn pattern, SyncEn = 1 (**Note 7**)
IO Pulse On Time	t_{ONIO}	2	3.41	3.59	3.77	s	Local alarm, temporal horn pattern, HS = 1
Horn Sync IO Dump	t_{IODMP2}	2	95	100	105	ms	Local alarm, HS = 1, IO dump active
Horn Sync IO Dump Delay	t_{IODLY4}	2	285	300	315	ms	Local alarm, HS = 1
Horn Sync Contention Window	t_{IOCW}	2	294	310	326	ms	Local alarm, HS = 1, IO = 0, no IO dump, IO pull-down
Interconnect Signal Operation (IO)							
IO Active Delay	t_{IODLY1}	12	3.5	3.7	3.9	s	From start of local alarm to IO active
Remote Alarm Delay with Temporal Horn Pattern	$t_{IODLY2A}$	12	0.77	0.81	0.86	s	No local alarm, from IO active to alarm
Remote Alarm Delay with Continuous Horn Pattern	$t_{IODLY2B}$	12	0.29	0.31	0.34	s	No local alarm, from IO active to alarm
IO Filter	t_{IOFILT}	12	—	—	290	ms	IO pulse width filtered
IO Pulse On Time for CO Alarm	t_{IOPW1}	12	23	—	290	ms	No local alarm, two valid pulses required for CO

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7: See timing diagram for horn synchronization and AAL (Figure 5-5).

1.2 Electrical Specifications (Continued)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = –10°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** through **Note 7**).

Parameters	Symbol	Test Pin	Min.	Typical	Max.	Units	Conditions
IO Pulse Off Time for CO Alarm	t_{IOTO1}	12	—	—	5.4	s	IO = Low
IO Charge Dump Duration	t_{IODMP}	12	0.475	0.5	0.525	s	At conclusion of local alarm or test
Auto-Alarm Locate (AAL)							
IO Cycle Period	t_{PIO2}	2	15.2	16	16.8	s	Local alarm, temporal horn pattern, HS = 1, AAL = 1
IO Cycle Off Time	t_{OFIO}	2	4.19	4.41	4.63	s	Local alarm, temporal horn pattern, HS = 1, AAL = 1, IO off time between IO pulse trains (3x)
End-of-Life							
End-of-Life Sample Time	t_{EOL}	—	314	334	354	h	EOL Enabled, Standby

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1.3 Temperature Specifications

Electrical Characteristics: All limits specified for V_{BAT} = 3V, V_{BST} = 4.2V and V_{SS} = 0V, except where noted in **Section 1.2 "Electrical Specifications"**.

Parameters	Symbol	Min.	Typical	Max.	Units
Temperature Ranges					
Operating Temperature Range	T_A	–10	—	+60	°C
Storage Temperature Range	T_{STG}	–55	—	+125	°C
Thermal Package Resistances					
Thermal Resistance, 16L-SOIC (150 mil.)	θ_{JA}	—	86.1	—	°C/W

2.0 PIN DESCRIPTIONS

Table 2-1 describes the pins of RE46C194.

TABLE 2-1: PIN FUNCTION TABLE

Pin	Symbol	Function
1	V_{SS}	Connects to the negative supply voltage.
2	IRED	Provides a regulated and programmable pulsed current for the infrared emitter diode.
3	V_{BAT}	Connects to the positive supply or battery voltage.
4	TEST	Used to invoke Test modes and the Timer mode. Input has an internal pull down.
5	TEST2	Test input for Test and Programming modes. Input has an internal pull down.
6	IRP	Connects to the anode of the photodiode.
7	IRN	Connects to the cathode of the photodiode.
8	RLED	Open-drain NMOS output used to drive a visible Red LED that is a visual indicator for Alarm and Hush modes. Pin provides load current for the low battery test.
9	GLED	Open-drain NMOS output used to drive a visible Green LED that is a visual indicator of the Alarm Memory condition.
10	FEED	Usually connected to the feedback electrode through a current-limiting resistor. If not used, this pin must be connected to V_{BAT} or V_{SS}.
11	IRCAP	Used to charge and monitor the IRED capacitor.
12	IO	Bidirectional pin that provides the capability to interconnect multiple detectors in a single system. Pin has an internal pull-down device and a charge dump device.
13	HB	Connects to the metal electrode of a piezoelectric transducer.
14	HS	Complementary output to pin HB. Connects to the ceramic electrode of the piezoelectric transducer.
15	V_{BST}	Boosted voltage produced by DC-DC converter.
16	LX	Open-drain NMOS output used to drive the boost converter inductor. The inductor must be connected from this pin to the positive supply through a low-resistance path.

3.0 DEVICE DESCRIPTION

3.1 Standard Internal Timing

The internal oscillator is trimmed to ±6% tolerance. In Standby operation, the boost regulator is powered on once every 10 seconds, IRCAP is charged from V_{BST} and then the detection circuitry is active for 3 ms. During these 3 ms, the infrared emitting diode (IRED) is active for a user-programmable duration of 100 µs to 400 µs. During this IRED pulse, the photodiode current is integrated and then digitized. The result is compared to a limit value stored in EEPROM (electrically erasable programmable read-only memory) during calibration to determine the photo chamber status. If a smoke condition is present, the period to the next detection decreases and additional checks are made.

3.2 Smoke Detection Circuit

The smoke detection circuitry consists of an IRED driver and an integrating photo amplifier with gain. The output of the photo amplifier is digitized by a 6-bit ADC. A smoke check consists of two integrations: one with the IRED off and one with the IRED on. The integration with the IRED off allows light leakage, leakage current and offset effects to be measured. This digitized result is subtracted from the result with the IRED on to produce the final digitized result. The digitized result is compared to the stored alarm limit at the conclusion of the smoke check.

When the digitized result is ≥ to the alarm limit, a smoke detection occurs. Three consecutive smoke detections cause the device to go into local alarm and activate the horn and interconnect circuits. The RLED turns on in local alarm for 10 ms at a 1 Hz rate. Once in local alarm, the alarm limit is changed to the hysteresis alarm limit and the boost regulator operates in High-Boost mode, which provides consistent audibility of the horn over battery life.

The IRED driver is all internal, and both the IRED on time and the IRED current are user-programmable. The IRED on time and the photo amplifier integration period are the same.

The integrating photo amplifier has three separate gain settings:

- Normal Gain for Standby and Hysteresis Operation
- Low Gain for Hush Operation
- High Gain for Chamber Test and Push-to-Test Operation

There are four separate sets of user-programmable alarm limits:

- Normal Alarm Limit
- Hysteresis Alarm Limit
- Hush Alarm Limit
- Chamber Test Alarm Limit

3.3 Battery Test

Once every 86 seconds, the status of the battery voltage is checked by enabling the boost converter for 10 ms and comparing a fraction of the V_{BAT} voltage to an internal reference. In each period of 344 seconds, the battery voltage is checked four times. Three checks are unloaded and one check is performed with the RLED enabled, which provides a battery load. The High Boost mode is active only for the loaded low-battery test. If the low-battery test fails, the horn pulses on for 10 ms, every 43 seconds, and continues to pulse until the failing condition passes.

Optionally, a Low-Battery Hush mode can be invoked. If a Low-Battery condition exists and pin TEST is driven high, the RLED turns on. If pin TEST is held for more than 0.5 seconds, the RE46C194 device enters into a Push-to-Test (PTT) operation. For more details, see **Section 3.5 "Push-to-Test"**. After pin TEST is driven low, RE46C194 enters Low-Battery Hush mode and the 10 ms horn pulse is silenced for eight hours. At the end of the eight hours, the audible indication resumes if the Low-Battery condition still persists. The activation of the test button also initiates the 9-minute Hush mode. For more details, see **Section 3.6 "Hush Operation"**.

3.4 Chamber Test

Once every 43 seconds, a chamber test is activated. A check of the photo chamber is made by amplifying the background reflections of the chamber. During chamber test, the normal gain is doubled and the chamber test alarm limit is used for the alarm limit. If the signal level exceeds the chamber test alarm limit, the chamber test passes. If two consecutive chamber tests fail, the horn pulses on for 10 ms, three times, with a pulse separation of 330 ms and a 43 second period. The three-pulse sequence continues until the failing condition passes. The boost regulator operates in Low-Boost mode for the chamber test.

The chamber test and battery test audible indicators are separated by approximately 20 seconds.

3.5 Push-to-Test

Push-to-Test (PTT) occurs when pin TEST is driven high (V_{IH}). The smoke detection rate increases to once every 250 ms after one internal clock cycle. The photo chamber is checked by amplifying the background reflections of the chamber. In PTT, the normal gain is doubled and the chamber test alarm limit is used for the alarm limit. After the required three consecutive smoke detections, the device goes into a Local Alarm condition. When pin TEST is driven low (V_{IL}), the photo amplifier normal gain and normal alarm limit are selected after one clock cycle. The detection rate continues once every 250 ms until three consecutive No Smoke conditions are detected. At this point, the device returns to standby timing. In addition, after pin TEST goes low, the device enters Hush mode (see **Section 3.6 "Hush Operation"**).

3.6 Hush Operation

When Hush mode is started, RE46C194 is immediately reset out of the local alarm and the horn is silenced. In Hush mode, the photo amplifier gain is reduced to half the normal gain setting to lower the sensitivity of RE46C194. In addition, a separate user-selectable hush alarm level exists that sets the Local Alarm condition in Hush mode. When a High Local Smoke condition exceeds the hush alarm level, RE46C194 can be placed into a Local Alarm condition. RLED is turned on for 10 ms, every 10 seconds, to indicate RE46C194 is in Hush mode. The Hush mode period is nine minutes. After this period times out, RE46C194 goes back to its standby operation.

If RE46C194 is currently in Hush mode, then PTT tests the device with the chamber test gain and alarm limits. Upon release of PTT, a new Hush mode is initiated.

Four user-selectable options control a hush operation:

1. The first option disables the hush function.
2. Hush-In-Alarm-Only allows RE46C194 to enter the hush operation only for a Local Alarm condition when pin TEST goes low. The smoke detector is immediately reset out of the alarm, and the horn is silenced. If the Hush-In-Alarm-Only option is not selected, then anytime a release of PTT occurs, Hush mode is initiated. This is called Hush-On-Demand.
3. The Smart-Hush option allows Hush mode to be terminated early. Hush mode can be canceled by a high local smoke alarm, a remote smoke alarm or PTT. A high local smoke alarm is the local smoke alarm caused by a smoke level that exceeds the hush alarm level.
4. Hush-With-No-Alarm allows the local alarm to be canceled with the PTT, but a High Local Smoke condition does not place RE46C194 into a Local Alarm condition.

3.7 Long-Term Drift Adjustment

A Long-Term Drift (LTD) adjustment for the photo chamber can be enabled. If this option is selected during calibration, a normal no-smoke baseline integration measurement must be made using Test mode T8. This value is stored in EEPROM. During normal operation, a new baseline value is calculated by making 64 integration measurements over a period of eight hours. The measurements are averaged, and the averaged value is used to calculate the LTD adjustment.

The LTD adjustment is calculated by subtracting the original baseline LTD value from the averaged LTD value. The LTD adjustment is scaled for the Operating mode and added to the alarm limits stored in EEPROM during calibration. The new alarm limits are not stored in EEPROM. LTD adjustment only affects normal, hysteresis and hush alarm limits. The chamber test limit is not changed by the LTD adjustment.

LTD sampling is suspended during Hush, Local Alarm or Remote Alarm conditions. Any LTD values being saved for a new LTD average calculation are discarded when LTD sampling is suspended. LTD sampling is restarted when Hush, Local Alarm or Remote Alarm conditions end.

In order to limit the amount of change the LTD adjustment can make, a normal alarm limit maximum value, NAM[5:0], must be set. The NAM[5:0] value must be larger than the normal alarm limit value. When the LTD adjustment to the normal alarm limit is ≥ the NAM[5:0] value, the chamber failure triple horn chirp is sounded.

3.8 Alarm Memory

The Alarm Memory feature is used to easily identify any RE46C194 device that previously was in a Local Alarm condition. Local Alarm Memory is user-programmable.

When a detector exits a Local Alarm condition, the alarm memory latch is set. GLED can be used to visually identify any RE46C194 device that previously was in a Local Alarm condition. GLED flashes three times. The duration of the flash is 10 ms. Consecutive flashes are separated by 1.3 seconds. This pattern repeats every 43 seconds. In order to preserve battery power, this visual indication stops after a period of 24 hours.

Identify RE46C194 devices with active Alarm Memory by pressing the PTT button. When this button is active, the horn pulses on for 10 ms every 250 ms.

If the Alarm Memory condition is set, then any time the PTT button is pressed and released, the alarm memory latch is reset.

The initial 24-hour visual indication is not displayed if a Low-Battery condition exists.

3.9 Interconnect Operation

The bidirectional IO pin allows the interconnection of multiple detectors. In a Local Alarm condition, this pin is driven high immediately through a constant-current source that is biased by the boost regulator (V_{BST}), operating in High-Boost mode (see **Section 3.13 "Boost Regulator"**). Shorting this pin to ground does not cause excessive current. Pin IO is ignored as an input during a local alarm.

Pin IO also has a NMOS discharge device that is active for 1.3 seconds after the conclusion of any local alarm. This device helps to quickly discharge any capacitance associated with the interconnect line.

If a remote, active-high signal is detected, RE46C194 goes into a remote alarm, and the horn is activated. RLED is off, indicating a Remote Alarm condition. Internal protection circuitry allows the signaling unit to have a higher supply voltage than the signaled unit, without excessive current draw.

The interconnect pin has a 336 ms nominal digital filter. This allows interconnecting other types of alarms (for example, CO) that may have a pulsed interconnect signal.

Smart interconnect (smart IO) is a user-selectable function. If pin IO is pulsed high twice with a nominal pulse on time > 23 ms and with a period < 5.4 seconds, a CO Alarm condition is detected and the CO temporal horn pattern sounds. The CO temporal pattern sounds at least two times if a CO Alarm condition is detected.

3.10 Horn Pattern

The smoke alarm horn pattern can either be a temporal or continuous horn pattern, depending on user selection. The temporal horn pattern supports the NFPA 72 emergency evacuation signal. The continuous horn pattern is a 70% duty cycle continuous horn pattern.

If a CO alarm is detected through pin IO, RE46C194 sounds the CO horn pattern. The CO horn pattern consists of four chirps every 5.8 seconds. Each chirp is 100 ms long and the chirps are separated by 100 ms.

RLED does not turn on when the horn is sounding.

3.11 Horn Synchronization

Horn synchronization is a user-programmable function.

In an interconnected system, if one RE46C194 device goes into local alarm, then other devices go into remote alarm. The IO line is driven high by the originating local smoke unit and stays high during the alarm.

If horn synchronization is enabled, then at the end of every temporal horn pattern and when the horn is off, the origination RE46C194 device drives the IO line low, then high again. This periodic IO line pulsing high and low causes the remote smoke units to go into and out of remote alarm repeatedly. Each time when a RE46C194 device goes into remote alarm, its timing is reset. The horn pattern of all remote smoke units is synchronized with the horn pattern of the originating RE46C194 device.

A protection circuit ensures the RE46C194 device that goes into local alarm first is the master unit and conducts the horn synchronization. The RE46C194 devices that go into local alarm later do not drive the IO line. This avoids bus contention problems.

This function works with the temporal horn pattern only.

3.12 Auto-Alarm Locate

Auto-Alarm Locate (AAL) is a user-programmable function. To use AAL, horn synchronization must be selected for the temporal horn pattern. AAL may be used with either the temporal or the continuous horn pattern.

The purpose of AAL is to let users quickly find the local alarm units (RE46C194 devices) just by listening. The local alarm units sound the horn pattern without interruption. The remote alarm units sound the pattern with an interruption. Every 16 seconds, the remote units are silenced for 4.7 seconds.

The originating RE46C194 device conducts the IO cycling. For the temporal horn pattern (every fourth temporal pattern), the IO line is driven low for the length of time of one temporal horn pattern. For the remaining three temporal patterns, the IO line still pulses normally to keep the horn synchronized. For continuous horn patterns, the IO line sends no synchronization pulse, but it is driven low for 4.4 seconds to produce a 4.7 second silence on remote alarms, so users can identify which room/area that the fire alarm went off first. It's done in 16 second cycles.

The RLED of the originating RE46C194 and other devices that detected smoke are turned on for 10 ms every one second. The remote units that did not detect a smoke condition will have their RLED off.

3.13 Boost Regulator

RE46C194 uses a boost regulator to provide a 3.6V regulated voltage in standby operation. This provides consistent operation during Low-Battery conditions. During a local alarm, remote alarm, PTT or battery test, the boost regulator operates in High-Boost mode. This high-boost voltage insures the horn achieves the correct sound pressure level, and the IO signal is compatible with products that operate from 9V. The high boost voltage is user-selectable and may be set to 8.5V or 10.0V.

The boost regulator uses an adjustable minimum off time hysteretic architecture with current-mode control. The peak inductor current is 0.6A with a minimum fixed off time of 1.6 µs.

The boost regulator uses a soft start when switching from low boost to high boost operation to limit inrush current. The inrush current is the result of charging the boost capacitor from the low-boost voltage to the high-boost voltage. Once the high-boost voltage is reached, the boost regulator only has to provide the load current. Limiting the boost voltage ramp rate controls the magnitude of the inrush current.

During a soft start, the effective charging current is approximately 12 mA. This corresponds to a maximum boost voltage ramp rate of 2 ms for a boost voltage of 8.5V. RLED does not turn on during a boost regulator soft start.

3.14 End-of-Life Indicator

The End-of-Life (EOL) indicator sounds an audible warning after 10 years of powered operation. The EOL operation is user-programmable.

EOL operation uses a 9-bit EEPROM register to store the EOL age count. The register is loaded with a value of 262. After every 14 days of continuous operation, RE46C194 decrements the EOL age count. If power to the device is stopped and then restored, the 14-day count is restarted from zero, but the EOL age value stored in EEPROM is not affected. When the EOL age count reaches zero at the end of 10 years of powered operation, an audible warning occurs, indicating that the RE46C194 device must be replaced. The warning pulses the horn on five times for 10 ms separated by 330 ms every 43 seconds. The EOL audible warning is separated from the low-battery audible warning by approximately 20 seconds.

Test mode T13 allows the EOL age count to be changed to a higher or lower value. Its maximum value is 511 and it is equivalent to 19.5 years. The EOL age count is determined by multiplying the number of years by 26.25. During final testing of RE46C194, the EOL age value stored in EEPROM is set to 262 (10 years) and counts down to zero, not up to 262.

4.0 USER PROGRAMMING AND TEST MODES

User Programming and Test modes provide the means to configure RE46C194 for a particular application and evaluate the performance of the smoke detector. Parametric programming allows the selection of the photo amplifier gain and integration time, along with the IRED current and low-battery voltage. Table 4-1 lists the parametric characteristics that can be selected for the application. The table includes the typical full-scale photodiode current that can be accommodated by a particular combination of photo amplifier gain and integration time. Only one photo integration gain factor (GF) and one integration time can be used for the smoke detector at any time.

TABLE 4-1: PARAMETRIC PROGRAMMING(1,2,3)

Parametric Programming		Range		Resolution	
IRED Period		100 µs to 400 µs		100 µs	
IRED Current Sink		50 mA to 200 mA		50 mA	
Low Battery Detection Voltage		2.1V to 2.8V		100 mV	
Photo Detection Limits		**Integration Time**			
Gain		**100 µs**	**200 µs**	**300 µs**	**400 µs**
		Typical Full-Scale Photodiode Input Current (nA)			
Normal Gain	GF = 1	58	29	19.4	14.5
	GF = 2	29	14.5	9.6	7.2
	GF = 3	14.5	7.2	4.8	3.6
	GF = 4	7.2	3.6	2.4	1.8
Hush Gain	GF = 1	116	58	38.8	29
	GF = 2	58	29	19.4	14.5
	GF = 3	29	14.5	9.6	7.2
	GF = 4	14.5	7.2	4.8	3.6
Chamber Test Gain	GF = 1	29	14.5	9.6	7.2
	GF = 2	14.5	7.2	4.8	3.6
	GF = 3	7.2	3.6	2.4	1.8
	GF = 4	3.6	1.8	1.2	0.9

Note 1: GF is the user-selectable photo integration gain factor. Once selected, it applies to all operation modes. For example, if GF = 1 and the integration time is selected to be 100 µs, the ranges are as follows: Normal/Hysteresis = 58 nA, Hush = 116 nA and Chamber Test = 29 nA.

2: Nominal measurement resolution in each case is 1/63 of the maximum input range.

3: The same current resolution and ranges apply to the limits.

Besides the parametric setup of the smoke detector, different features can be selected to customize RE46C194 for a particular application. The features are described in Table 4-2.

TABLE 4-2: FEATURES PROGRAMMING

Feature	Options
Long-Term Drift Adjustment	Enable/Disable
Low Battery Hush	Enable/Disable
Hush	Enable/Disable
Hush in Alarm Only versus Hush On Demand	Enable/Disable
Hush with No Alarm (for Europe)	Enable/Disable
Smart Hush (Cancel Hush for High Smoke, Remote Alarm, PTT)	Enable/Disable
Alarm Memory	Enable/Disable
Smart IO with CO Alarm Sensing	Enable/Disable
Horn Pattern	Temporal/Continuous
Horn Synchronization	Enable/Disable
Auto-Alarm Locate	Enable/Disable
Boost Voltage	8.5V or 10V
10 Year End-of-Life (EOL) Indicator	Enable/Disable

4.1 Calibration and Programming Procedures

Fourteen separate Programming and Test modes are available for user customization of RE46C194. To enter these modes after power-up, pin TEST2 must be driven to V_{BAT} and held at that level. Pin TEST is then clocked to step through the Test modes. Pin TEST has two logic high conditions. Pins FEED and IO are reconfigured to become Test mode inputs, while pins RLED, GLED and HB become Test mode outputs. The Test mode functions for each pin are outlined in Table 4-3.

When pin TEST2 is held at V_{BAT}, pin TEST becomes a tri-state input with nominal input levels at V_{SS}, V_{BAT} and V_{BST}. A test clock occurs whenever pin TEST switches between V_{SS} and V_{BST}.

In Table 4-3, the **TEST Data** column represents the state of pin TEST when used as a data input, which is either V_{SS} or V_{BAT}. Pin TEST can therefore be used as both a clock to change modes and as a data input once a mode is set. Other pin functions are described in Table 4-3.

The 6-bit ADC used to digitize the integrator output is composed of a counter, a DAC and a comparator. The comparator output is available on the HB output for certain Test modes and is designated as 'SmkComp' in Table 4-3. The DAC output is available in certain Test modes on pin RLED and is designated as 'DAC' in Table 4-3.

TABLE 4-3: TEST MODE FUNCTIONS[5]

Mode	Description	TEST Clock	TEST Data	TEST2	FEED	IO	RLED	GLED	HB
	V_{IH}	V_{BST}	V_{BAT}	V_{BAT}	V_{BST}	V_{BAT}	—	—	—
	V_{IL}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	—	—	—
T0	Horn Test	0	HornEn	V_{BAT}	FEED	IO	RLED	GLED	HB
T1	Low-Battery Test	1	not used	V_{BAT}	FEED	LBstrb	RLED	GLED	LBout
T2	System Setup (22 bits)	2	ProgData	V_{BAT}	ProgCLK	ProgEn	RLED	GLED	HB
T3	Norm Lim Set (6 bits)	3	not used	V_{BAT}	CalCLK	IntLat[3]	DAC	IntegOut	SmkComp[1]
T4	Hyst Lim Set (6 bits)	4	not used	V_{BAT}	CalCLK	IntLat[3]	DAC	IntegOut	SmkComp[1]
T5	Hush Lim Set (6 bits)	5	not used	V_{BAT}	CalCLK	IntLat[3]	DAC	IntegOut	SmkComp[1]
T6	Ch Test Lim Set (6 bits)	6	not used	V_{BAT}	CalCLK	IntLat[3,4]	DAC	IntegOut	SmkComp[1]
T7	Normal Alarm Max. Limit (6 bits)	7	not used	V_{BAT}	CalCLK	IntLat[3,4], ProgEn	DAC	IntegOut	SmkComp[1]
T8	Serial Read/Write (58 bits)	8	ProgData	V_{BAT}	ProgCLK	ProgEn	RLED	GLED	Serial Out
T9	LTD Baseline (6 bits)	9	not used	V_{BAT}	MeasEn	ProgEn	DAC	IntegOut	HB
T10	Norm Lim Check	10	not used	V_{BAT}	MeasEn	not used	DAC	IntegOut	SCMP[2]
T11	Hyst Lim Check	11	not used	V_{BAT}	MeasEn	not used	DAC	IntegOut	SCMP[2]
T12	Hush Lim Check	12	not used	V_{BAT}	MeasEn	not used	DAC	IntegOut	SCMP[2]
T13	Ch Test Lim Check	13	not used	V_{BAT}	MeasEn	not used	DAC	IntegOut	SCMP[2]
T14	Normal Alarm Max. Limit Check	14	not used	V_{BAT}	MeasEn	not used	DAC	IntegOut	SCMP[2]
T15	EOL Serial Read/Write (9 bits)	15	ProgData	V_{BAT}	ProgCLK	ProgEn	RLED	GLED	Serial Out

Note 1: SmkComp (HB) – digital comparator output (high if DAC < IntegOut; low if DAC > IntegOut).

2: SCMP (HB) – digital output representing comparison of measurement value and associated limit. Signal is valid only after MeasEn is asserted and measurement is made (SCMP high if measured value > limit; low if measured value < limit).

3: IntLat (IO) – digital input used for two purposes. If pin FEED is at a logic high level, then a low-to-high transition on IntLat initiates an integration cycle. If pin FEED is at a logic low level, then a low-to-high transition on IntLat latches the present state of the limits (DAC level) for later storage. T3-T6 limits are latched but not stored until ProgEn is asserted in T7 mode.

4: At the end of T7 mode, in order to store the limits, the IO pin must be pulsed twice consecutively with pin FEED held low. The first pulse latches the data and the second pulse stores the data in EEPROM.

5: Test modes are only intended for product development and agency qualification. They are not intended for use during the normal operation of the smoke detector.

Pin HS is used as an error flag when programming RE46C194. When an Error condition exists, pin HS is asserted high after the program enable (ProgEn) pulse on pin IO is driven low. Pin HS remains high until the particular Test mode is exited. The HS error flag can be asserted for Test modes T7, T8 and T9.

Two possible Error conditions can cause pin HS to be asserted high. First, if the hysteresis alarm limit is set to a value ≥ the normal alarm limit, this can cause normal operation problems. Second, if the normal alarm limit maximum is set to a value ≤ the normal alarm limit when LTD is enabled. In the second case, RE46C194 can indicate a chamber fail after power-up.

4.2 Horn Test

Test mode T0 allows the horn to be enabled indefinitely for audibility testing.

To enter Test mode T0, follow these steps:

1. Power-up with bias conditions as shown in Figure 4-3 or Figure 4-5.
2. Drive pin TEST to V_{BAT} while holding pin TEST2 at V_{SS}.
3. Drive pin TEST2 high to V_{BAT} to enable the horn and drive it to V_{SS} to disable the horn.

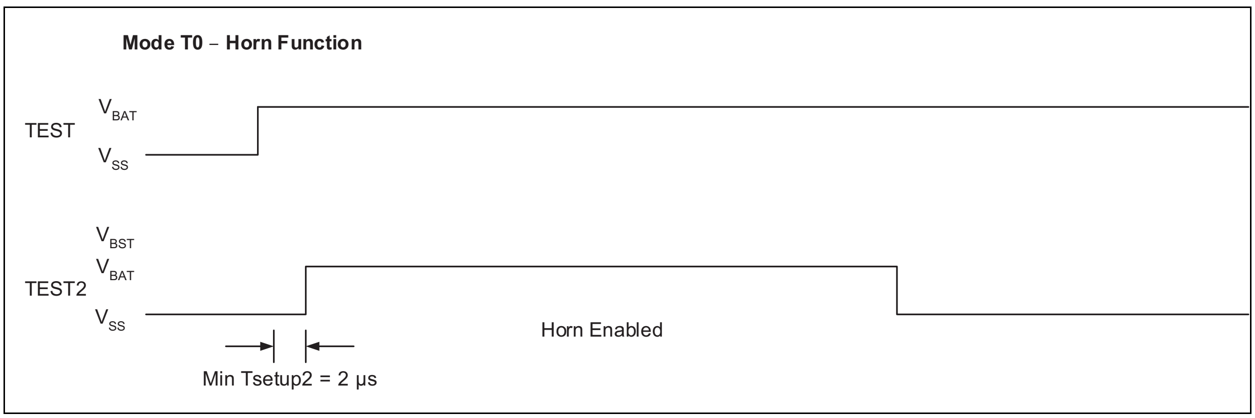


FIGURE 4-1: *Timing Diagram for Test Mode T0.*

4.3 Low-Battery Test

Test mode T1 allows the enabling of the internal low battery circuitry to perform a low-battery test.

To enter Test mode T1, follow these steps:

1. Power-up with the bias conditions shown in Figure 4-3 or Figure 4-5. Connect pin V_{BST} to 5V through a diode, so pin V_{BST} can enter high boost operation.
2. Drive pin TEST2 from V_{SS} to V_{BAT} to enter the Programming mode. Pin TEST2 must remain high at V_{BAT} through Steps 3 through 5.
3. Apply one clock pulse to pin TEST to enter Test mode T1. RLED and GLED turn on.
4. Drive pin IO from V_{SS} to V_{BAT}. This enables the boost converter. Monitor the HB output for the low-battery comparator status.
5. Lower or increase V_{BAT} and repeat Step 4.

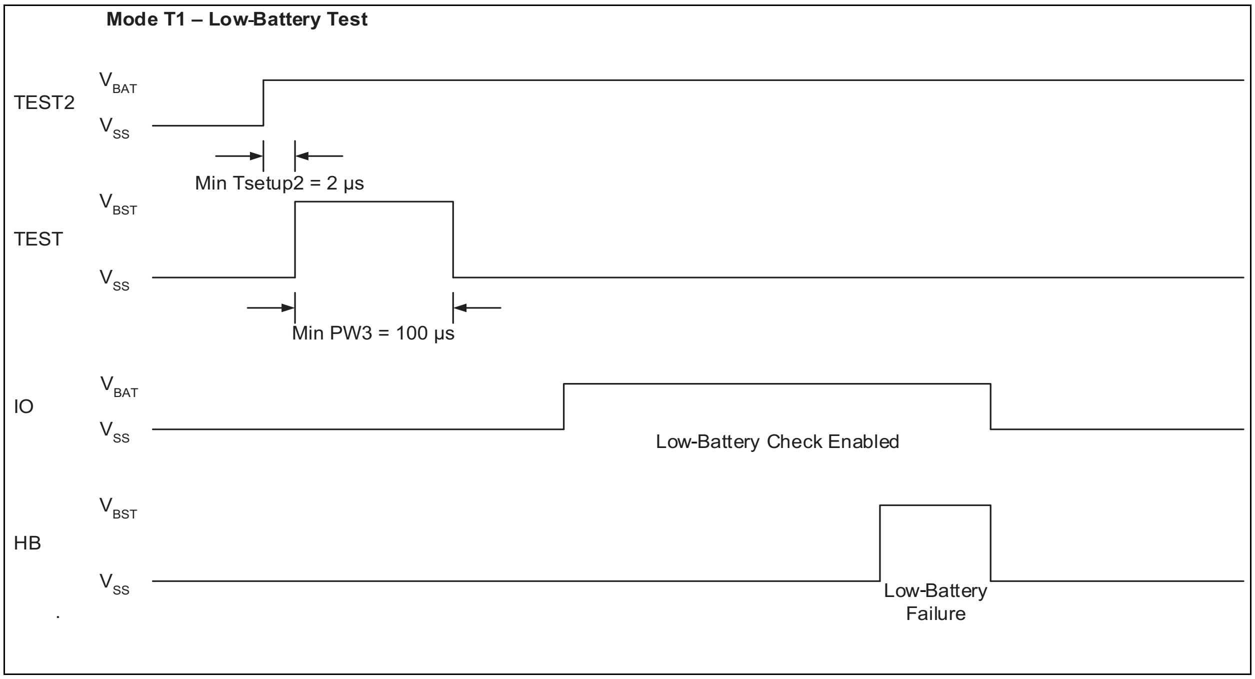


FIGURE 4-2: *Timing Diagram for Test Mode T1.*

4.4 System Setup

Test mode T2 allows parametric and feature selections to be programmed into EEPROM. For Test mode T2, only 22 bits (36 to 57) of Register 4-1 are loaded. Alternatively, Test mode T8 "Serial Read/Write" allows parametric selections, feature selections and alarm limits to be programmed into EEPROM and read back. For Test mode T8, all 58 bits of Register 4-1 are loaded. For Test mode T2, 22 bits are clocked in serially using pin TEST as a data input and pin FEED as a clock input. The 22 bits are then stored in EEPROM.

The system setup steps are as follows:

1. Power-up with bias conditions as shown in Figure 4-3 or Figure 4-5.
2. At power-up, drive pins TEST, TEST2, FEED and IO to V_{SS}.
3. Drive pin TEST2 from V_{SS} to V_{BAT} to enter the Programming mode. TEST2 must remain high at V_{BAT}, between 2.7V andO 3.0V, through Step 5.
4. Using pin TEST as the data input and pin FEED as the clock, shift in the values selected from Register 4-1.
5. After shifting in the data, pulse pin IO high to V_{BAT} 10 times with a cycle of 5 ms on, then 5 ms off, to store the shift register contents into EEPROM.
6. If any changes are required, drive pin TEST2 low to V_{SS} and return to Step 2. All bit values must be reentered.

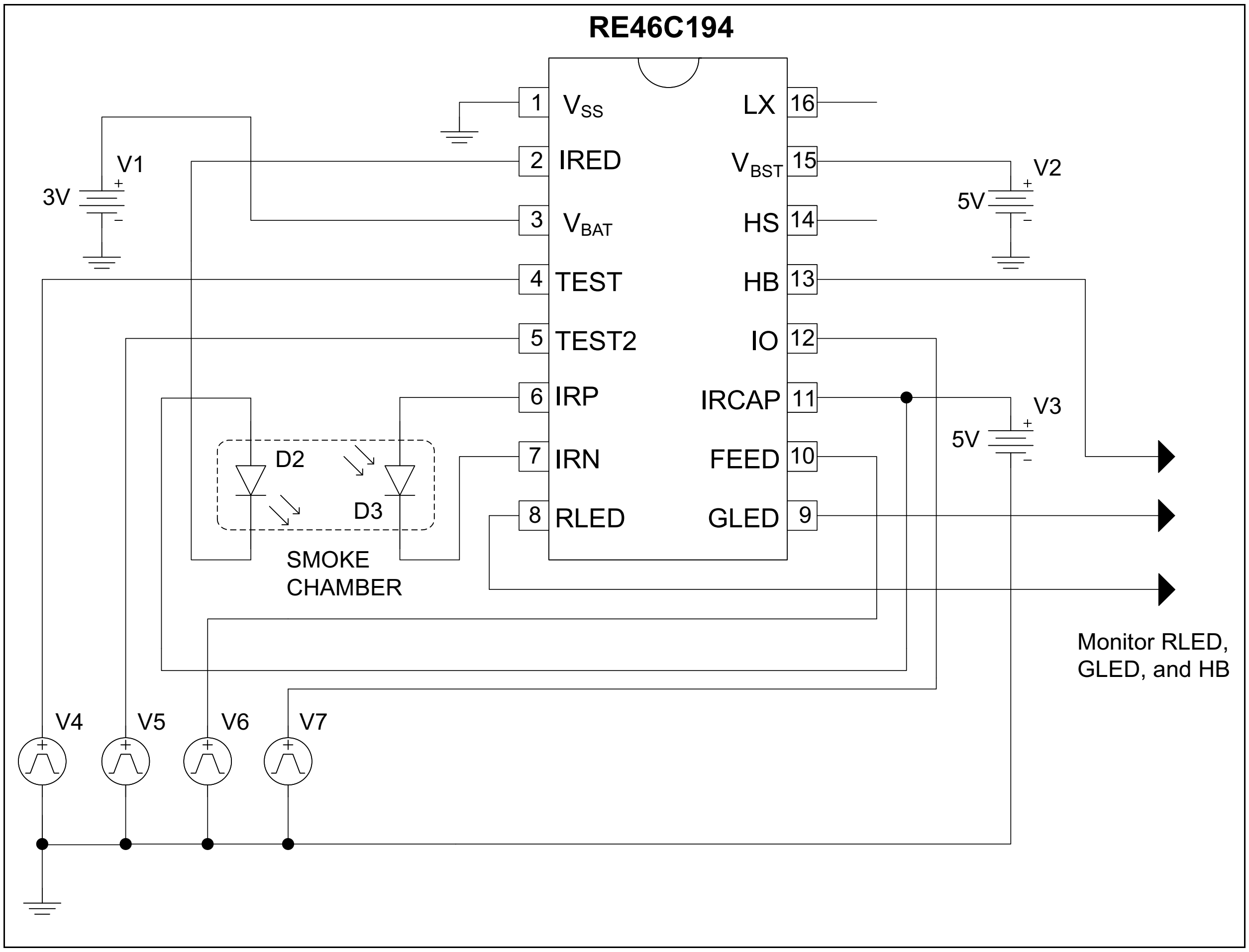


FIGURE 4-3: *Nominal Application Circuit for Programming RE46C194.*

REGISTER 4-1: CONFIGURATION AND CALIBRATION SETTINGS REGISTER

U	U	U	U	U	U	R/W	R/W
—	—	—	—	—	—	EOL	HBV
						bit 57	bit 56

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
AM	AAL	HS	HP	CO	LTD	HNA	HIAO
bit 55							bit 48

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SHush	Hush	LBH	LB2	LB1	LB0	IRC1	IRC0
bit 47							bit 40

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IT1	IT0	GF1	GF0	NL5	NL4	NL3	NL2
bit 39							bit 32

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
NL1	NL0	HYL5	HYL4	HYL3	HYL2	HYL1	HYL0
bit 31							bit 24

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HUL5	HUL4	HUL3	HUL2	HUL1	HUL0	CTL5	CTL4
bit 23							bit 16

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CTL3	CTL2	CTL1	CTL0	NAM5	NAM4	NAM3	NAM2
bit 15							bit 8

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
NAM1	NAM0	LTD5	LTD4	LTD3	LTD2	LTD1	LTD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 57 **EOL:** End-of-Life
- `0` = Disable
- `1` = Enable

bit 56 **HBV:** High V_{BST} Voltage
- `0` = 10.0V
- `1` = 8.5V

bit 55 **AM:** Alarm Memory
- `0` = Disable
- `1` = Enable

REGISTER 4-1: CONFIGURATION AND CALIBRATION SETTINGS REGISTER (CONTINUED)

bit 54	**AAL:** Auto-Alarm Locate 0 = Disable 1 = Enable
bit 53	**HS:** Horn Synchronization 0 = Disable 1 = Enable
bit 52	**HP:** Horn Pattern 0 = Continuous horn pattern 1 = Temporal horn pattern
bit 51	**CO:** Smart IO – CO Alarm 0 = Disable 1 = Enable
bit 50	**LTD:** Long-Term Drift Enable 0 = Disable 1 = Enable
bit 49	**HNA:** Hush No Alarm Option 0 = Disable (hush with high smoke alarm threshold enabled) 1 = Enable (hush with high smoke alarm threshold disabled)
bit 48	**HIAO:** Hush in Alarm Only Option 0 = Disable (hush on demand) 1 = Enable (hush in alarm only)
bit 47	**SHush:** Smart Hush Option 0 = Never cancel 1 = Canceled for high smoke level, interconnect alarm or second push of the TEST button (as described above)
bit 46	**Hush:** Hush Option 0 = Disable 1 = Enable
bit 45	**LBH:** Low-Battery Hush Enable 0 = Disable 1 = Enable
bit 44-42	**LB[2:0]:** Low-Battery Trip Point 000 = 2.1V 001 = 2.2V 010 = 2.3V 011 = 2.4V 100 = 2.5V 101 = 2.6V 110 = 2.7V 111 = 2.8V
bit 41-40	**IRC[1:0]:** IRED Current 00 = 50 mA 01 = 100 mA 10 = 150 mA 11 = 200 mA
bit 39-38	**IT[1:0]:** Integration Time 00 = 100 µs 01 = 200 µs 10 = 300 µs 11 = 400 µs

REGISTER 4-1: CONFIGURATION AND CALIBRATION SETTINGS REGISTER (CONTINUED)

bit 37-36	**GF[1:0]:** Gain Factor 00 = 1 01 = 2 10 = 3 11 = 4
bit 35-30	**NL[5:0]:** Normal Limits (see **Section 3.2 "Smoke Detection Circuit"**) 000000 = 0 000001 = 1 ... 111110 = 62 111111 = 63
bit 29-24	**HYL[5:0]:** Hysteresis Limits (see **Section 3.2 "Smoke Detection Circuit"**) 000000 = 0 000001 = 1 ... 111110 = 62 111111 = 63
bit 23-18	**HUL[5:0]:** Hush Limits (see **Section 3.6 "Hush Operation"**) 000000 = 0 000001 = 1 ... 111110 = 62 111111 = 63
bit 17-12	**CTL[5:0]:** Chamber Test Limits (see **Section 3.3 "Battery Test"**) 000000 = 0 000001 = 1 ... 111110 = 62 111111 = 63
bit 11-6	**NAM[5:0]:** Normal Alarm Maximum Value (see **Section 3.9 "Interconnect Operation"**) 000000 = 0 000001 = 1 ... 111110 = 62 111111 = 63
bit 5-0	**LTD[5:0]:** Long-Term Drift (see **Section 3.9 "Interconnect Operation"**) 000000 = 0 000001 = 1 ... 111110 = 62 111111 = 63

For the following options, the sequence to be loaded into the register is shown in Example 4-1:

- Photo Amp Gain Factor = 1
- Integration Time = 200 µs
- IRED Current = 100 mA
- Low-Battery Trip = 2.2V
- Smart Hush Option = Never Cancel
- Tone Select = Temporal
- High Boost Voltage = 8.5V
- Enable: Low Battery Hush, Hush Option, Hush In Alarm Only, Smart IO, Alarm Memory
- Disable: Long-Term Drift, End-of-Life (EOL), Horn Synchronization, Auto-Alarm Locate, Smart Hush, Hush No Alarm Option

EXAMPLE 4-1:

Data	—	—	—	—	—	—	0	1
Bit #	—	—	—	—	—	—	57	56

Data	1	0	0	1	1	0	0	1
Bit #	55	54	53	52	51	50	49	48

Data	0	1	1	0	0	1	0	1
Bit #	47	46	45	44	43	42	41	40

Data	0	1	0	0	—	—	—	—
Bit #	39	38	37	36	—	—	—	—

The timing diagram for Test mode T2 is shown in Figure 4-4. The minimum pulse width for pin FEED is 10 µs while the minimum pulse width for pin TEST is 100 µs.

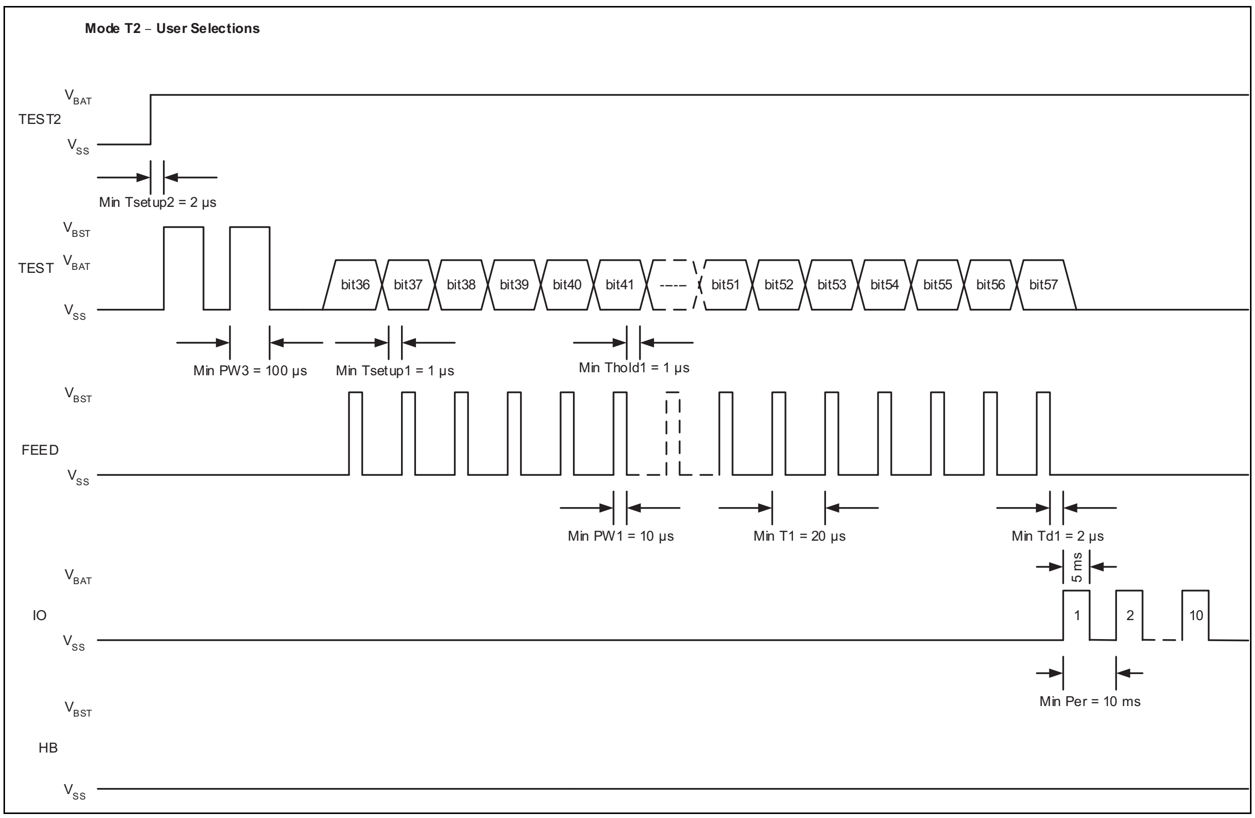


FIGURE 4-4: *Timing Diagram for Test Mode T2.*

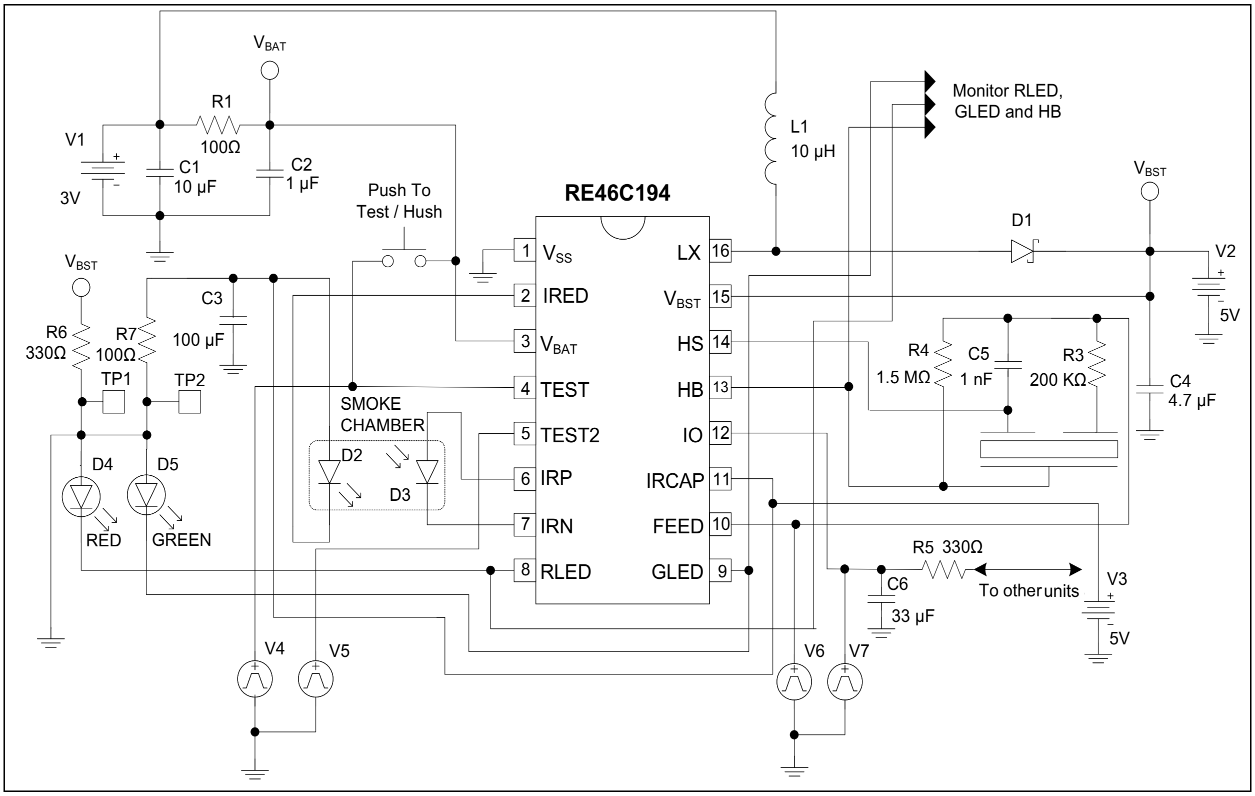


FIGURE 4-5: *Circuit for Programming in the RE46C194 Typical Application.*

4.5 Smoke Calibration

A separate Calibration mode is entered for each Measurement mode (Normal, Hysteresis, Hush, Chamber Test and Alarm Max) so that independent limits can be set for each. In all Calibration modes, the integrator output can be accessed at the GLED output. The DAC output voltage, that represents the smoke detection level, can be accessed at the RLED output. The SmkComp output voltage is the result of the comparison of the DAC with the integrator output and can be accessed at pin HB. Pin FEED can be clocked to step up the smoke detection level at pin RLED. Once the desired smoke threshold is reached, pin IO is pulsed from low-to-high to store the result.

The calibration procedure is described in the following steps:

1. Power-up with the bias conditions shown in Figure 4-3 or Figure 4-5.
2. Drive pin TEST2 from V_{SS} to V_{BAT} to enter the Programming mode. Pin TEST2 must remain high at V_{BAT} through Step 8.
3. Apply three clock pulses to pin TEST to enter Test mode T3. This initiates the Calibration mode for normal limit setting. The integrator output appears at GLED and the smoke detection level at RLED.
4. At this point, each clock pulse to the FEED pin will increase the smoke detection level as needed. Pulling pin IO high with pin FEED at a logic high level initiates an integration measurement. The integrator output signal appears at GLED. The sequence of incrementing the limit, performing an integration measurement and monitoring the HB output for the resulting comparison can be repeated until the desired threshold is reached. Once the desired smoke threshold is reached, with pin FEED held low, pulse pin IO low-to-high to latch the smoke detection level.
5. Apply a clock pulse to pin TEST input to enter Test mode T4. This initiates the Calibration mode for the hysteresis limit. Repeat the sequence in Step 4 to set the hysteresis limit.
6. Apply a clock pulse to pin TEST to enter Test mode T5 and initiate calibration for the hush limit. Repeat Step 4 to set the hush limit.
7. Apply a clock pulse to pin TEST to enter Test mode T6 and initiate calibration for the chamber test limit. Repeat Step 4 to set the chamber test limit.
8. Apply a clock pulse to pin TEST to enter Test mode T7 and initiate calibration for the normal alarm maximum limit. Repeat Step 4 to set the normal alarm maximum limit. If LTD is not enabled, this limit set function does not have to be performed, but the value must be latched as described in the next step.
9. After pulsing pin IO to latch the normal alarm maximum limit, pulse pin IO 10 times, with 5 ms pulses, using a 10 ms period to store the latched limits into EEPROM.
10. Pin HS is asserted high if the normal alarm maximum limit is ≤ the normal alarm limit or if the

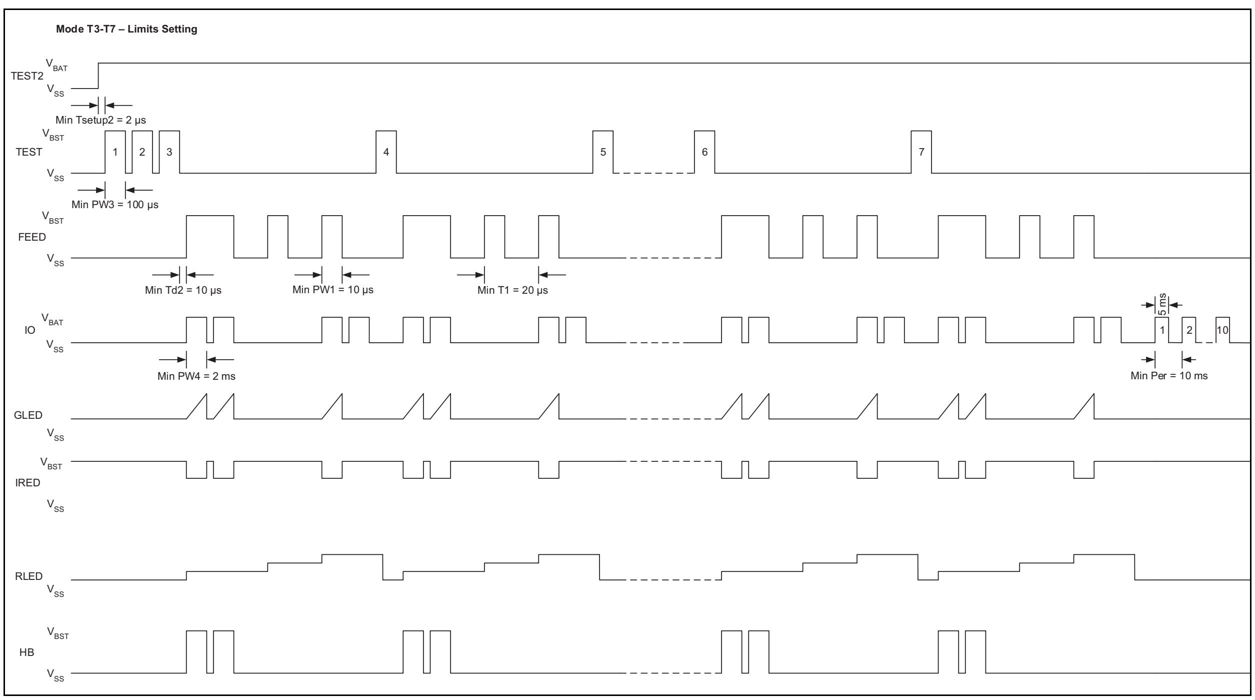


FIGURE 4-6: Timing Diagram for Test Modes T3 to T7.

4.6 Serial Read/Write

The alarm limits, LTD baseline and system setup information can be entered directly from the Serial Read/Write mode.

To enter the Serial Read/Write mode or Test mode T8, follow these steps:

1. Power-up with the bias conditions shown in Figure 4-3 or Figure 4-5.
2. Drive pin TEST2 from V_{SS} to V_{BAT} to enter into Programming mode. Pin TEST2 must remain high at V_{BAT} until all data is entered and stored in EEPROM.
3. Pulse pin TEST eight times to V_{BST} to enter Test mode T8. This enables the Serial Read/Write mode.
4. Pin TEST now acts as a data input (High = V_{BAT}, Low = V_{SS}). Pin FEED acts as the clock input (High = V_{BST}, Low = V_{SS}). Clock in the alarm limits, LTD baseline, functional and parametric options. The data sequence follows the pattern described in Register 4-1. A serial data output is available at pin HB.
5. After the 58 bits are entered, pulse pin IO high to V_{BAT} 10 times with a 5 ms pulse width and a 10 ms period to store the shift register contents into EEPROM.
6. Pin HS is asserted high if the normal alarm maximum limit is ≤ the normal alarm limit or if the hysteresis alarm limit is ≥ the normal alarm limit.

Note: It is recommended that Serial Read/Write Test modes with V_{BAT} = 2.7V - 3.0V avoid possible data corruption seen at V_{BAT} >= 3.2V.

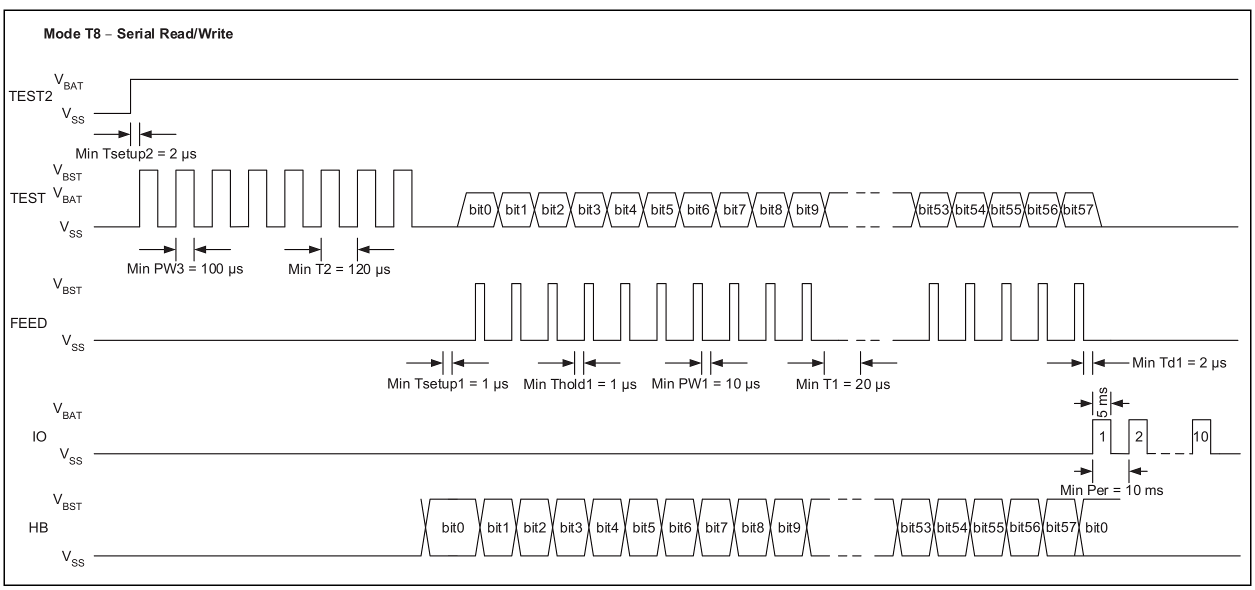


FIGURE 4-7: Timing Diagram for Test Mode T8.

4.7 LTD Baseline Measurement

If the LTD adjustment is enabled, a LTD baseline must be set. If an accurate value is known based on previous chamber characterization, it can be loaded in Test mode T8 with the serial data. If not, zeros can be entered as placeholders in T8 and a LTD baseline measurement must be made. To do this, connect RE46C194 to its smoke chamber and place it in a No Smoke condition.

To enter Test mode T9, follow these steps:

1. Power-up with the bias conditions shown in Figure 4-3 or Figure 4-5.
2. Drive pin TEST2 from V_{SS} to V_{BAT} to enter the Programming mode. Pin TEST2 must remain high at V_{BAT} until completing the measurement.
3. Apply nine clock pulses (V_{SS} to V_{BST}) to pin TEST to enter Test mode T9. This initiates the LTD baseline measurement. The integrator output appears at GLED and the smoke detection level at RLED.
4. Pulse pin FEED from V_{SS} to V_{BST} to make the baseline measurement. The duration of this pulse must be at least 2 ms.
5. To save the LTD baseline measurement to EEPROM, pulse pin IO 10 times from V_{SS} to V_{BAT} with pin FEED held low. The pulse must be 5 ms wide with a 10 ms period.
6. Pin HS is asserted high if the normal alarm maximum limit is ≤ the normal alarm limit or if the hysteresis alarm limit is ≥ the normal alarm limit.

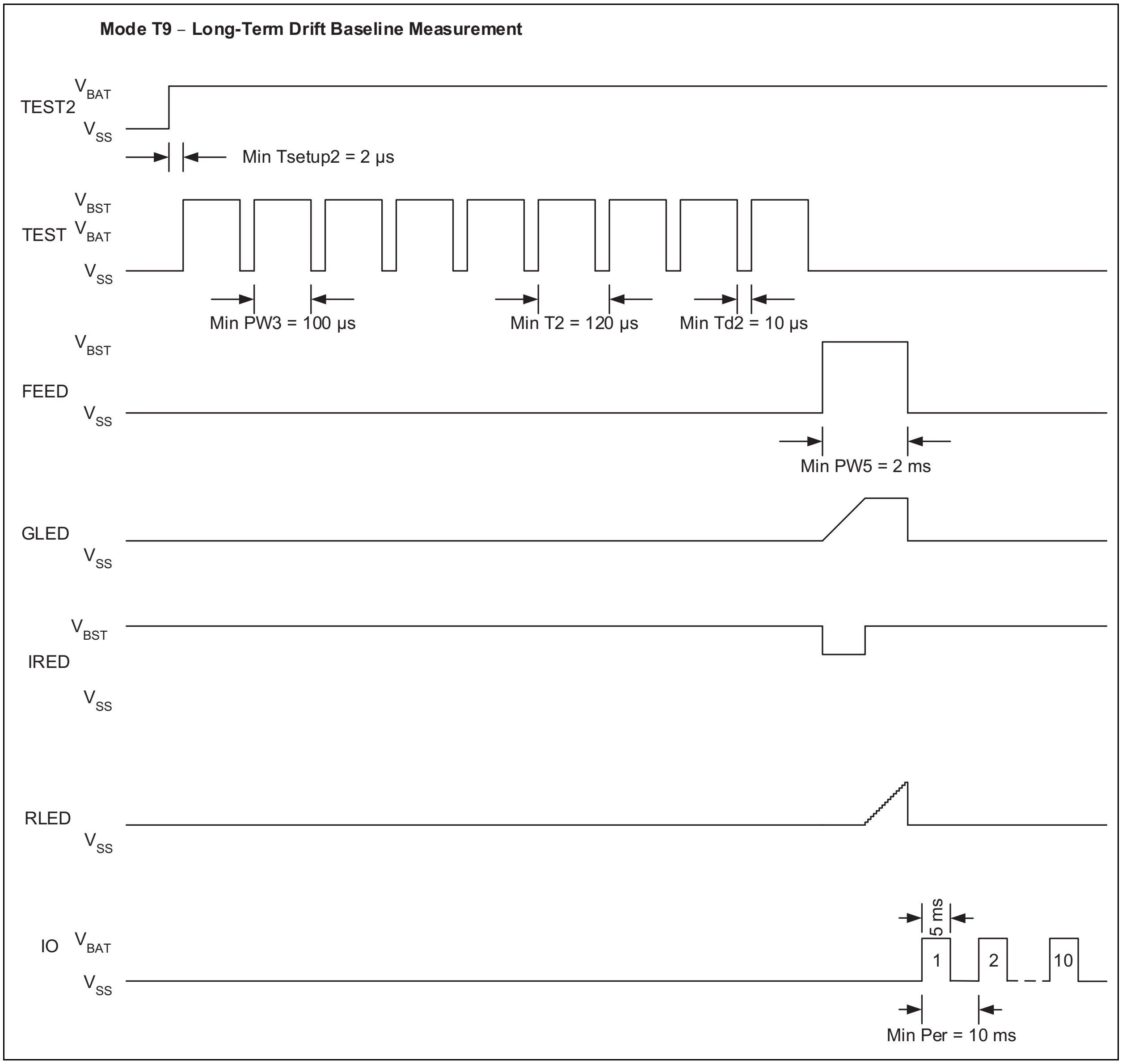


FIGURE 4-8: *Timing Diagram for Test Mode T9.*

4.8 Limits Verification

After all limits and the LTD baseline are entered and stored into EEPROM, other Test modes are available to verify if the limits are functioning as expected.

The limit verification procedure is described in the following steps:

1. Power-up with the bias conditions shown in Figure 4-3 or Figure 4-5.
2. Drive pin TEST2 from V_{SS} to V_{BAT} to enter the Programming mode. Pin TEST2 must remain high at V_{BAT} through Step 7.
3. Apply ten clock pulses to pin TEST to enter Test mode T10. This initiates the Verification mode for the normal limits setting. The integrator output appears at GLED and the smoke detection level at RLED.
4. Pulse pin FEED high for at least 2 ms to initiate a smoke check. When the smoke detection level exceeds the alarm threshold, the HB output is asserted high. The test is repeated each time pin FEED is clocked high.
5. Apply a clock pulse to pin TEST to enter Test mode T11 and initiate verification for hysteresis limits. Repeat Step 4 to verify the hysteresis limit.
6. Apply a clock pulse to pin TEST to enter Test mode T12 and initiate verification for hush limits. Repeat Step 4 to verify the hush limit.
7. Apply a clock pulse to pin TEST to enter Test mode T13 and initiate verification for chamber test limits. Repeat Step 4 to verify the chamber test limit.
8. Apply a clock pulse to pin TEST to enter Test mode T14 and initiate verification for alarm maximum limits. Repeat Step 4 to verify the alarm maximum limit.

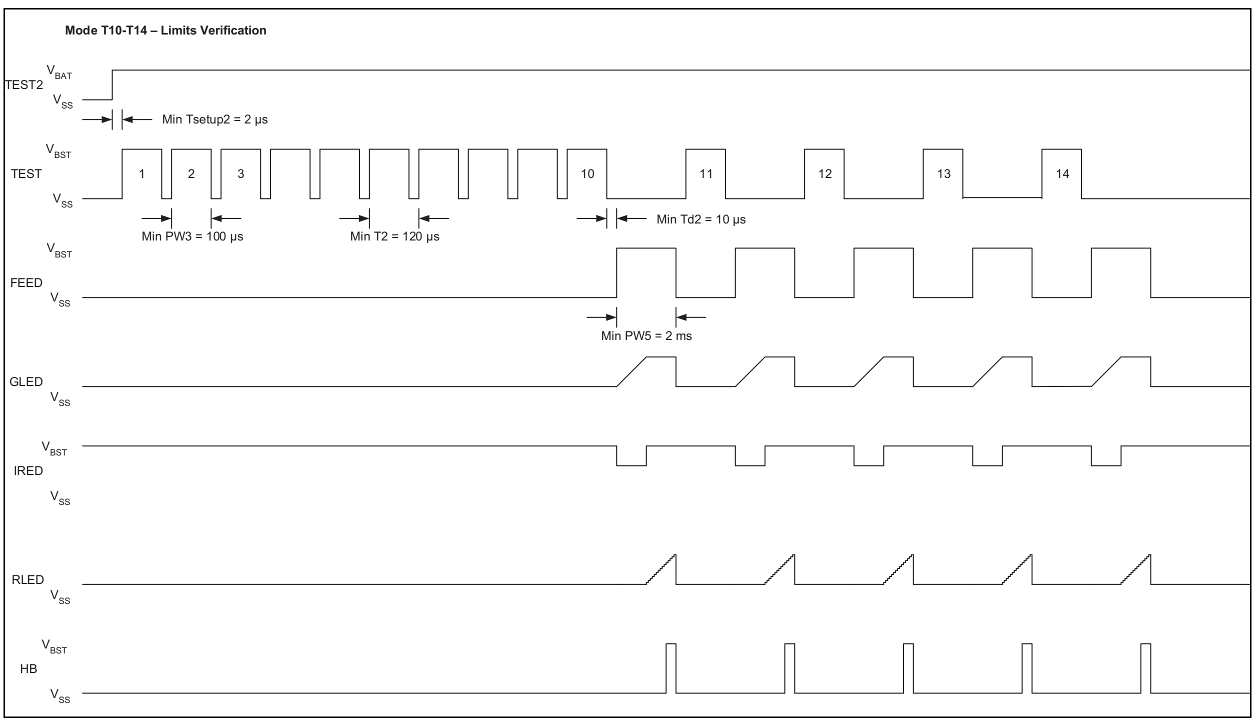


FIGURE 4-9: *Timing Diagram for Test Modes T10-14.*

4.9 End-of-Life Serial Read/Write

The 9-bit EOL register is set to a 10-year time out when the RE46C194 device is shipped. Using Test mode T15, EOL Serial Read/Write, the EOL feature can be read and modified. This allows for the possibility of setting longer or shorter EOL values for different applications, such as five or 15 years. The controls for data, clock and program are the same as used in **Section 4.4 "System Setup"**, except that the EOL EEPROM Register (Register 4-2) is affected and not the Configuration and Calibration Settings Register (Register 4-1).

To enter Test mode T15, follow these steps:

1. Power-up with the bias conditions shown in Figure 4-3 or Figure 4-5.
2. Drive pin TEST2 from V_{SS} to V_{BAT} to enter the Programming mode. Pin TEST2 must remain at V_{BAT} until all data is entered.
3. Apply 15 clock pulses (V_{SS} to V_{BST}) to pin TEST to enter Test mode T15. This enables the EOL Serial Read/Write mode.
4. Pin TEST now acts as a data input (High = V_{BAT}, Low = V_{SS}). Pin FEED acts as the clock input (High = V_{BST}, Low = V_{SS}). Clock in the EOL time. The data sequence follows the pattern described in Register 4-2. A serial data output is available at pin HB.
5. After all 9 bits are entered, drive pin IO to V_{BAT}, then to V_{SS} 10 times with a cycle of 5 ms on, 5 ms off, to store the shift register contents into EEPROM.

REGISTER 4-2: END-OF-LIFE REGISTER

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
EOL8	EOL7	EOL6	EOL5	EOL4	EOL3	EOL2	EOL1	EOL0
bit 9								bit 1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 9-1 **EOL[9:1]:** End-of-Life

`000000000` = 0
`000000001` = 1
...
`111111110` = 510
`111111111` = 511

To set a 10-year EOL time out, the EOL EEPROM register is loaded with a count of 262, as shown in Table 4-4. The EOL EEPROM register is decremented by one for every 334 hours (≈14 days). When the EOL EEPROM register value reaches 0, the audible warning of 5 horn chirps is sounded.

To read the EOL EEPROM register, enter Test mode T15. Then, pulse pin FEED 9 times and read the data on pin HB. Reading does not involve writing data on pin TEST.

TABLE 4-4: EOL EEPROM REGISTER LOADED WITH A COUNT OF 262

Bit	9	8	7	6	5	4	3	2	1
Binary Data	1	0	0	0	0	0	1	1	0
Decimal Value	256	0	0	0	0	0	4	2	0

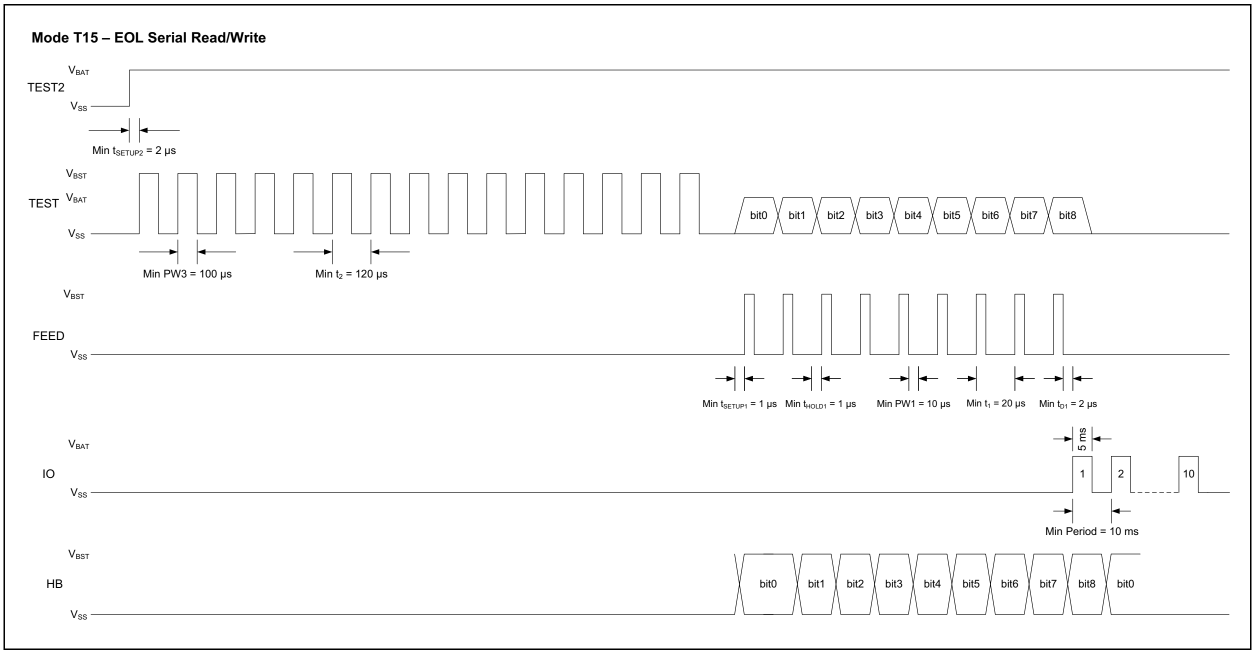


FIGURE 4-10: *Timing Diagram for Test Mode T15.*

5.0 APPLICATION NOTES

5.1 Standby Current Calculation and Battery Life

The supply current presented in the **Section 1.2 "Electrical Specifications"** table is only one component of the average standby current. In most cases, it can be a small fraction of the total because power consumption generally occurs in relatively infrequent bursts and depends on many external factors. These include the values selected for the IRED current and integration time, the V_{BST} and IR capacitor sizes and leakages, the V_{BAT} level and the magnitude of external resistances that adversely affect the boost converter efficiency.

Table 5-1 shows a calculation of the standby current for the battery life based on the following parameters:

- V_{BAT} = 3V
- V_{BST1} = 3.6V
- V_{BST2} = 9V
- Boost Capacitor Size = 4.7 x 10^{-6}F
- Boost Efficiency = 85%
- IRED On Time = 2 x 10^{-4}s
- IRED Current = 0.1A

TABLE 5-1: STANDBY CURRENT CALCULATION

I_{DD} Component	Voltage (V)	Current (A)	Duration (s)	Energy (J)	Period (s)	Average Power (W)	I_{DD} Contribution (A)	I_{BAT} (µA)
Fixed I_{DD}	3.0	10^{-6}	1.0	—	1	3 x 10^{-6}	10^{-6}	1.0
Photo Detection Current								
Chamber Test (excluding IR drive)	3.6	0.001	0.003	1.08 x 10^{-5}	43	2.95 x 10^{-7}	9.85 x 10^{-8}	0.1
IR Drive during Chamber Test	3.6	0.1	2 x 10^{-4}	7.2 x 10^{-5}	43	1.97 x 10^{-6}	6.57 x 10^{-7}	0.7
Smoke Detection (excluding IR drive)	3.6	0.001	0.003	1.08 x 10^{-5}	10.75	1.18 x 10^{-6}	3.94 x 10^{-7}	0.4
IR Drive during Smoke Detection	3.6	0.1	2 x 10^{-4}	7.2 x 10^{-5}	10.75	7.88 x 10^{-6}	2.63 x 10^{-6}	2.6
Low Battery Check Current								
Loaded Test								
Load	8.5	0.02	0.01	0.0017	344	5.81 x 10^{-6}	1.94 x 10^{-6}	2.1
Boost	V_{BST1} to V_{BST2}	—	—	6.85 x 10^{-6}	344	2.34 x 10^{-7}	7.81 x 10^{-8}	0.1
Unloaded Test								
Load	3.6	10^{-4}	0.01	3.6 x 10^{-6}	43	9.85 x 10^{-8}	3.28 x 10^{-8}	0
Total							6.82 x 10^{-6}	6.8

The following sections explain the components in Table 5-1 and the calculations in the example.

5.1.1 FIXED I_{BAT}

The battery current, I_{BAT}, is the "Supply Current" shown in the **Section 1.2 "Electrical Specifications"** table.

5.1.2 PHOTO DETECTION CURRENT

The photo detection current is the current draw caused by the smoke test every 10.75 seconds and the chamber test every 43 seconds. The current for both the IR diode and the internal measurement circuitry comes primarily from V_{BST}, so the average current must be scaled for both on time and boost voltage.

The contribution to I_{BAT} is determined by calculating the energy consumed by each component given its duration. An average power is then calculated based on the period of the event and the boost converter efficiency (assumed to be 85% in this case). An I_{BAT} contribution is then calculated based on this average power and the given V_{BAT}. For example, the IR drive contribution during the chamber test is detailed in Equation 5-1.

EQUATION 5-1:

$$I_{IRCAP} = \frac{V_{BST1} \times I_{IRED} \times t_{IRON}}{t_{PCT1} \times BCE \times V_{BAT}}$$

Where:

I_{IRCAP}	=	Photo Detection Current (µA)
V_{BST1}	=	Boost Voltage (V)
I_{IRED}	=	Photo Detection Output Current (A)
t_{IRON}	=	IRED On Time (s)
t_{PCT1}	=	Chamber Test Period (s)
BCE	=	Boost Converter Efficiency (%)
V_{BAT}	=	Supply Voltage (V)

$$I_{IRCAP} = \frac{3.6V \times 0.1A \times 200\ \mu s}{43s \times 0.85 \times 3V} = 0.657\ \mu A$$

5.1.3 LOW-BATTERY CHECK CURRENT

The low-battery check current is the current required for the low-battery test. It includes both loaded (RLED on) and unloaded (RLED off) tests.

The boost component of the loaded test represents the cost of charging the boost capacitor to the higher voltage level. This has a fixed cost for every loaded check because the capacitor is gradually discharged during subsequent operations and the energy is not recovered. The other calculations are similar to those shown in Equation 5-1.

The unloaded test has minimal contribution because it involves only some internal reference and comparator circuitry. The value of the RLED resistor, R6, in the typical application must be set to match the average horn current.

5.1.4 BATTERY LIFE

When estimating the battery life, several additional factors must be considered. These include battery resistance, battery self-discharge rate, capacitor leakages and the effect of the operating temperature on all of these characteristics. Some number of false alarms and user tests must also be included in any calculation.

For 10-year applications, Microchip recommends using a 3V spiral wound lithium manganese dioxide battery with a laser seal. These can be found with capacities from 1400 mAh to 1600 mAh.

5.1.5 BOOST REGULATOR

The boost regulator uses a Current-mode hysteretic architecture. The nominal peak current of the Current-mode control is 0.6A. The boost regulator has two operating modes:

- Low Boost-mode operation provides a nominal boost voltage of 3.6V and is typically used in standby operation.
- High Boost-mode operation provides 8.5V or 10V and is used for Alarm conditions and loaded low battery check.

The boost regulator uses soft start when switching from Low Boost to High Boost mode operation to limit inrush current.

The boost regulator efficiency is sensitive to series resistance in the high-current switching path, especially during High-Boost mode. From the RE46C194 **Typical Application** schematic, the critical components of this resistance are the inductor DC resistance, the internal resistance of the battery and the resistance in the connections from the inductor to the battery, from the inductor to pin LX and from pin V_{SS} to the battery.

In order to function properly under full load at V_{BAT} = 2V, the total of the inductor and interconnect resistances must be ≤ 0.3Ω.

The internal battery resistance must be < 0.5Ω and a low-ESR capacitor ≥ 10 µF must be connected in parallel with the battery to average the current draw over the boost converter cycle.

The Schottky diode, D1, must have a maximum peak current rating ≥ 0.8A. For best results, it must have a forward voltage specification < 0.5V at 0.8A and low reverse leakage.

Inductor L1 must have a peak current rating ≥ 0.8A.

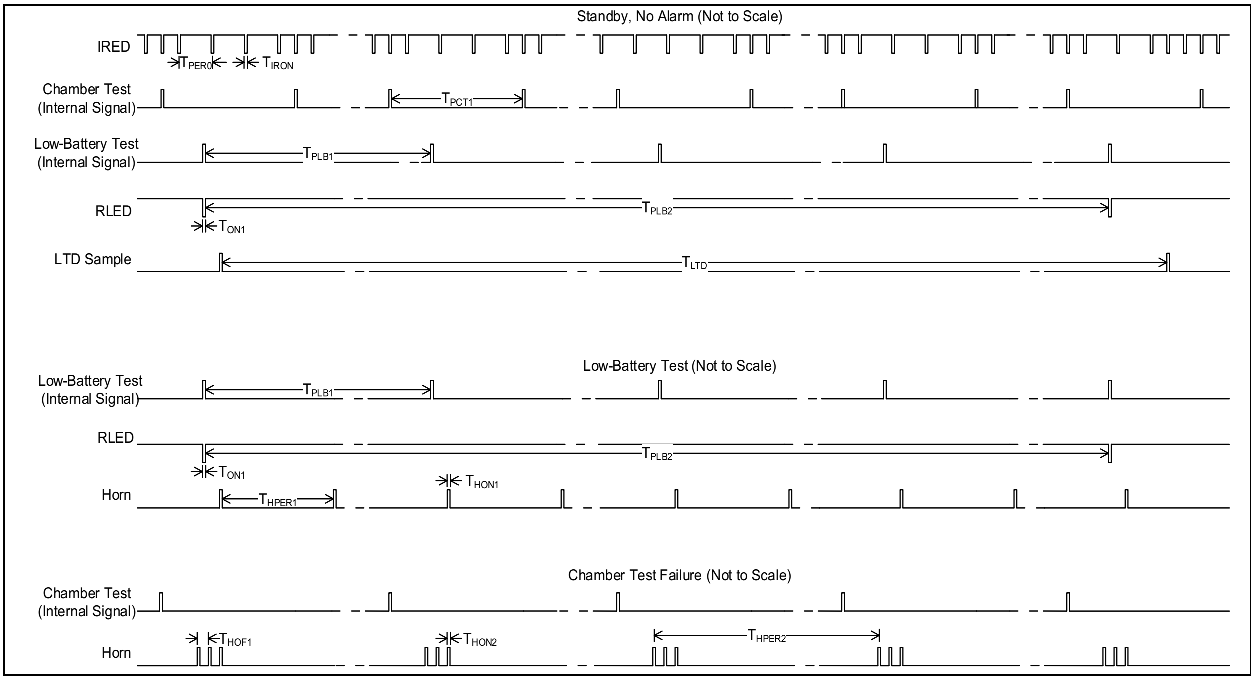


FIGURE 5-1: *RE46C194 Timing Diagram – Standby, No Alarm, Low Supply Test Failure and Chamber Test Failure.*

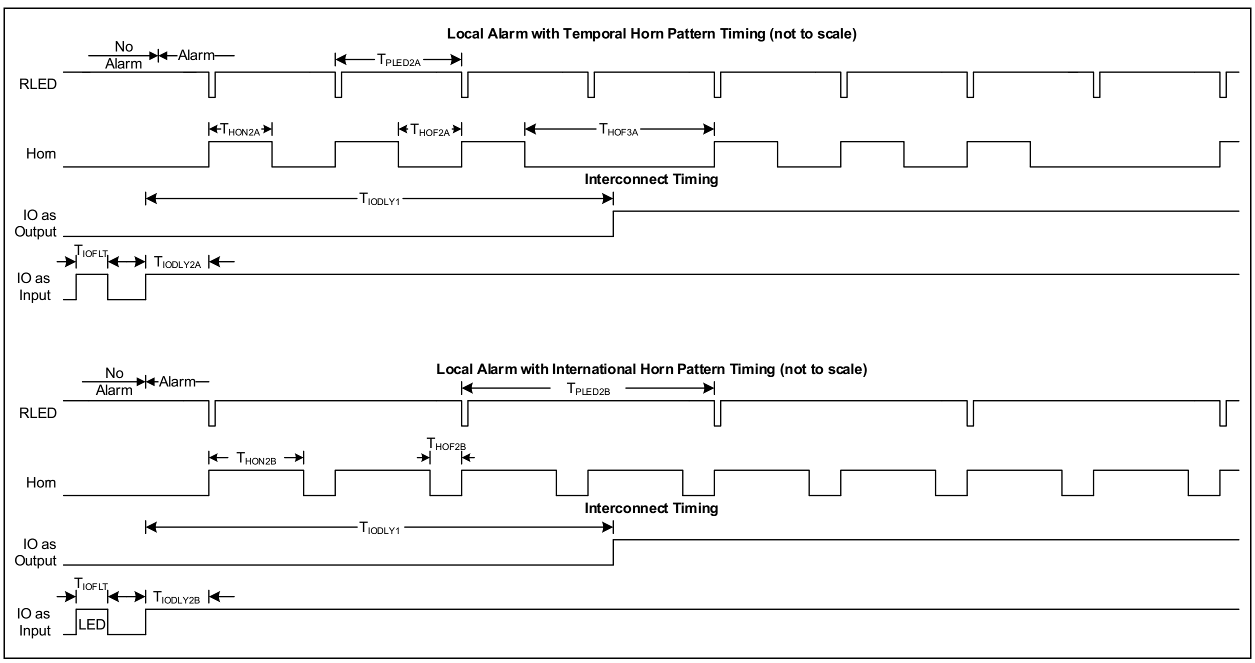


FIGURE 5-2: *RE46C194 Timing Diagram – Local Alarm with Temporal Horn Pattern, Local Alarm with International Horn Pattern.*

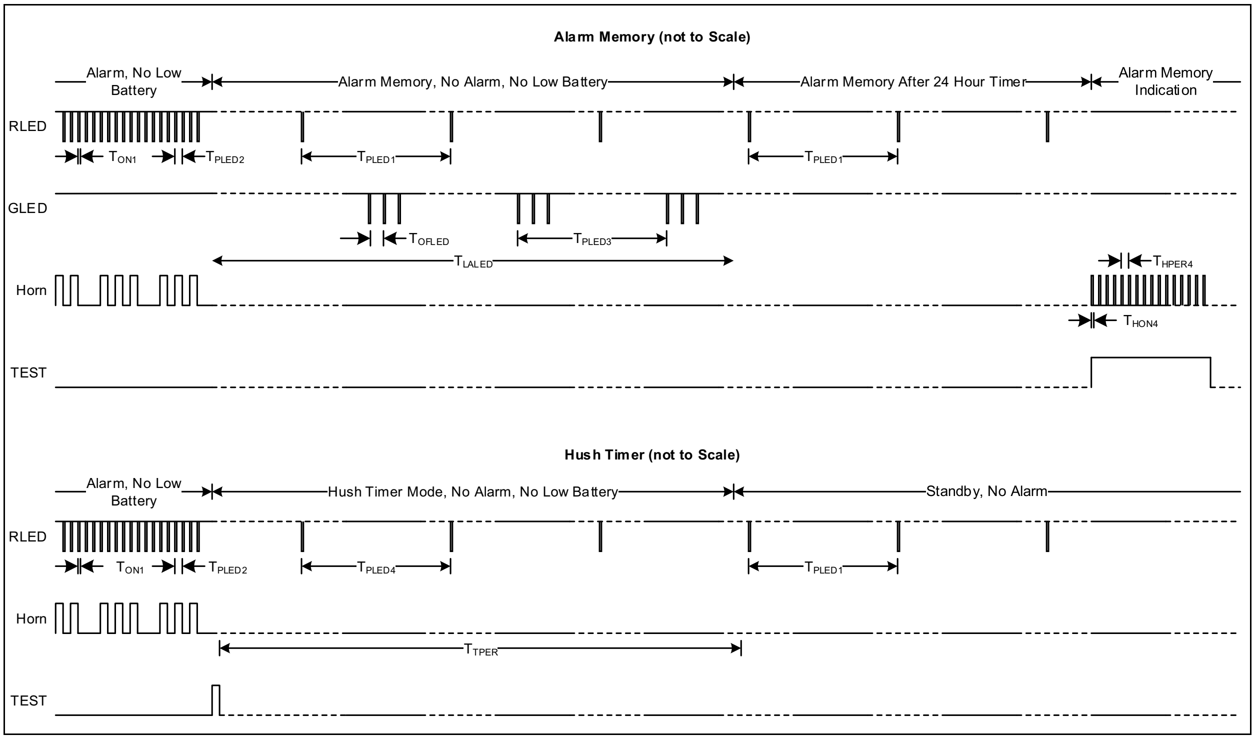


FIGURE 5-3: RE46C194 Timing Diagram – Alarm Memory and Hush Timer.

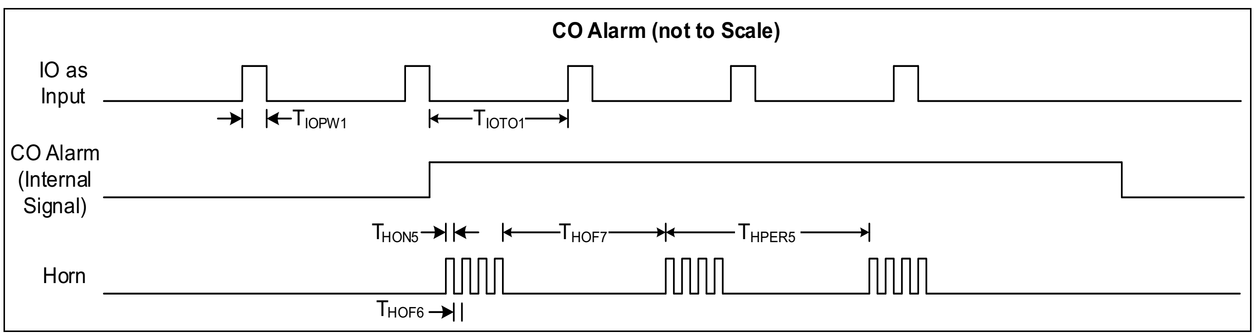


FIGURE 5-4: Timing Diagram – CO Alarm.

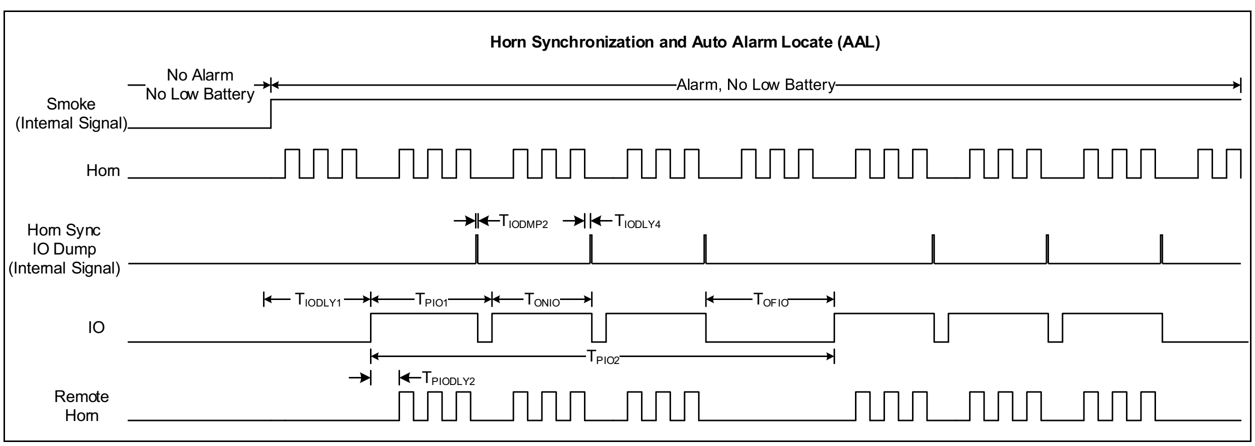
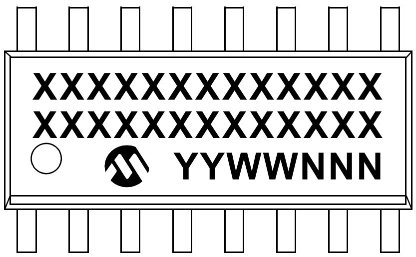


FIGURE 5-5: Timing Diagram – Horn Synchronization and AAL.

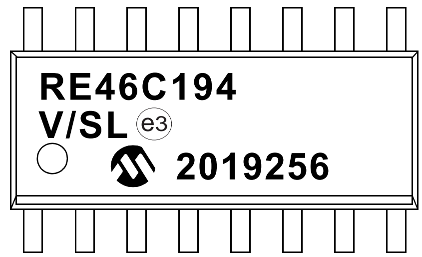
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

16-Lead SOIC, 3.9 mm



Example



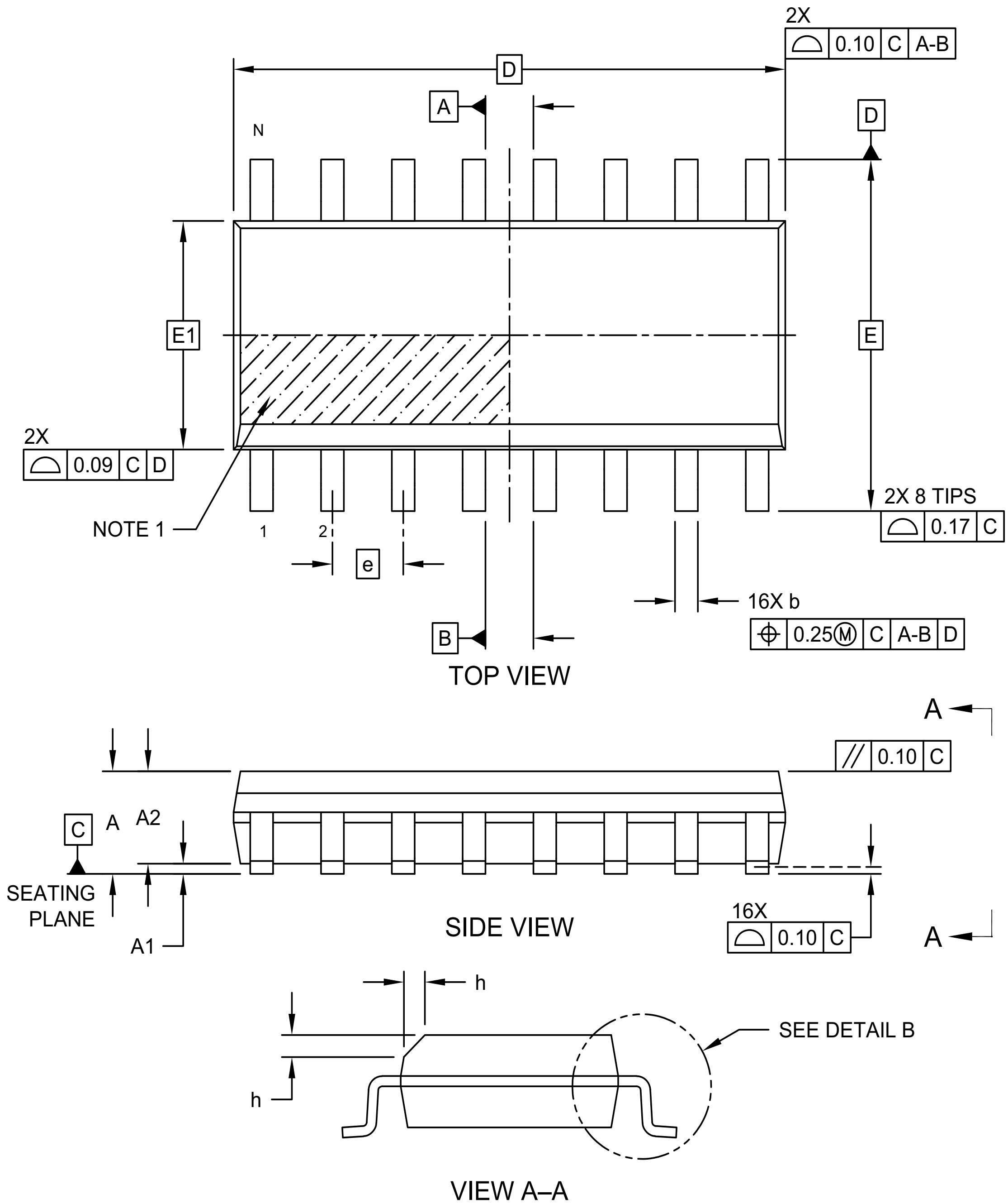
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*****	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6.2 Package Drawings

16-Lead Plastic Small Outline (D7X) - Narrow, 3.90 mm Body [SOIC]

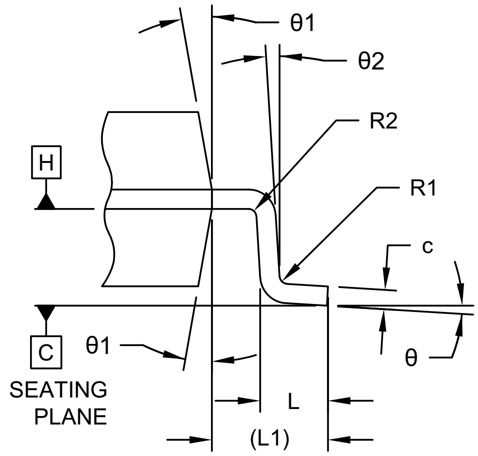
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



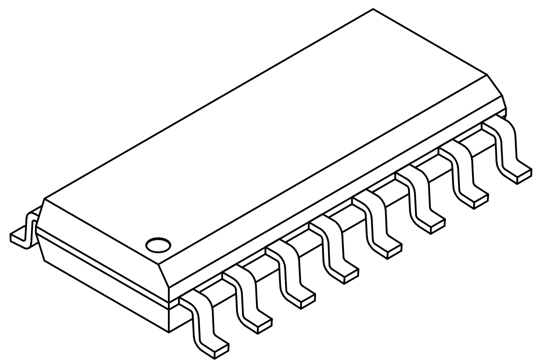
Microchip Technology Drawing C04-108-D7X Rev E Sheet 1 of 2

16-Lead Plastic Small Outline (D7X) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Standoff §	A1	0.10	-	0.25
Molded Package Thickness	A2	1.25	-	–
Overall Length	D		9.90 BSC	
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Terminal Width	b	0.31	-	0.51
Terminal Thickness	c	0.10	-	0.25
Corner Chamfer	h	0.25	-	0.50
Terminal Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Bend Radius	R1	0.07	-	-
Lead Bend Radius	R2	0.07	-	-
Foot Angle	θ	0°	-	8°
Mold Draft Angle	θ1	0°	-	15°
Lead Angle	θ2	0°	-	-

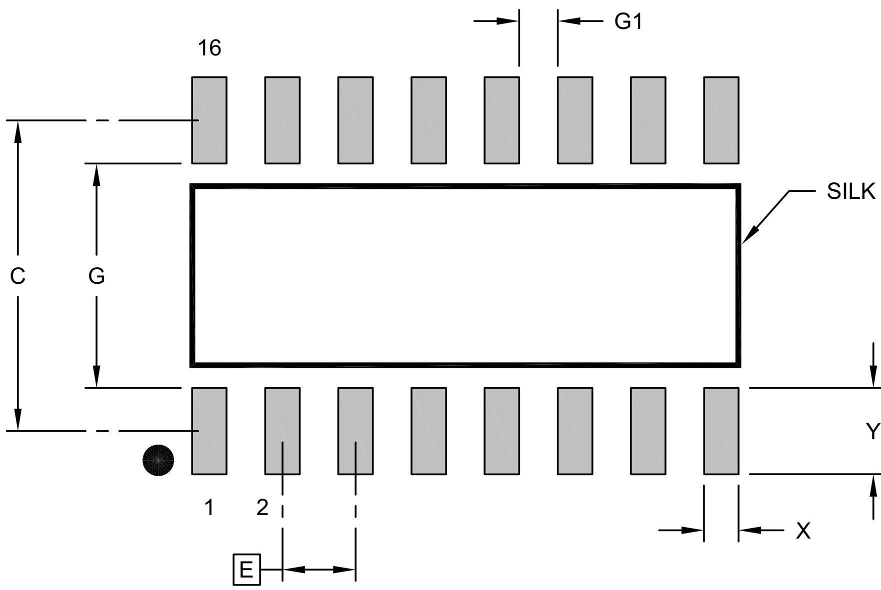
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-108-D7X Rev E Sheet 2 of 2

16-Lead Plastic Small Outline (D7X) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X16)	X			0.60
Contact Pad Length (X16)	Y			1.50
Contact Pad to Contact Pad (X8)	G	3.90		
Contact Pad to Contact Pad (X14)	G1	0.67		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2108-D7X Rev E

APPENDIX A: REVISION HISTORY

Revision E (August 2024)

- Added **End-of-Life** parameter to the **Section 1.2 "Electrical Specifications"** table.
- Added **Section 3.14 "End-of-Life Indicator"**.
- Added *10 Year End-of-Life (EOL) Indicator* to Table 4-2.
- Added *Test mode T15* to Table 4-3.
- Updated *bit 57 (EOL)* information in Register 4-1.
- Added **Section 4.9 "End-of-Life Serial Read/Write"**.
- Updated **Section 6.2 "Package Drawings"**.

Revision D (November 2023)

The following is the list of modifications:

- Timing chart changed in Figure 5-1.

Revision C (August 2022)

The following is the list of modifications:

- Updated Operating Temperature parameter in **Section 1.1 "Absolute Maximum Ratings (†)"**.
- Updated Electrical Specifications.
- Updated Table 4-3.
- Updated Register 4-1.

Revision B (January 2020)

The following is the list of modifications:

- Added Note 5 at Table 4-3.

Revision A (June 2019)

- Original Release of this Data Sheet.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	[X][(1)]
Device	Package Type	Number of Pins	Tape and Reel

Device:	RE46C194	= CMOS Low-Voltage Photoelectric Smoke Detector ASIC with Interconnect and Timer Mode
Package Type:	S	= SOIC (Plastic Small Outline)
Number of Pins:	16	= 16
Tape and Reel Option:	Blank	= Standard Packaging (tube or tray)
	T	= Tape and Reel[(1)]

Examples:

a)RE46C194S16 = 16-Lead SOIC

b)RE46C194S16T = 16-Lead SOIC, Tape and Reel

Note1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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