SAM9X60 MPU, 1-Gbit DDR2-SDRAM, 4-Gbit NAND Flash, 10/100 Ethernet PHY, Power Management IC, 1-Kbit EEPROM

SAM9X60 SOM Data Sheet

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Introduction

The Microchip SAM9X60 System-On-Module (SAM9X60D1G-I/LZB) is a small single-sided SOM based on a System-in-Package (SiP) ARM926EJ-S Arm® Thumb® CPU-based embedded microprocessor coupled to a 1-Gbit DDR2-SDRAM.

In addition to the SAM9X60 D1G SiP MPU running up to 600 MHz, the SAM9X60D1G-I/LZB embeds a 4-Gbit NAND Flash memory, a 10/100 Ethernet PHY and a dedicated power management unit.

The SAM9X60D1G-I/LZB is built on a common set of proven Microchip components to reduce time to revenue and lower risk in product design by simplifying hardware design and software development.

The SAM9X60D1G-I/LZB also limits design rules of the main application board, reducing overall PCB complexity and cost. It is supported by a free Linux® distribution and bare metal C examples.

Figure 1. SAM9X60D1G-I/LZB Overview

1. Features

- System-in-Package (SAM9X60D1GT-I/4FB) Including:
  - ARM926EJ-S Arm Thumb processor running up to 600 MHz
  - 1-Gbit DDR2 SDRAM
- 4-Gbit NAND Flash Memory
- On-Board Power Management Unit (MCP16501TA-E/RMB)
- 1-Kbit Serial EEPROM with EUI-48™ Node Identity (24AA025E48T-I/OT)
- 10Base-T/100Base-TX Ethernet PHY (KSZ8081RNAIA-TR)
- 24-MHz MEMS Oscillator for Main Clock Generation (DSC6102HI2B-024.0000T)
- 32.768-kHz Crystal Oscillator for Slow Clock Generation
- 25-MHz MEMS Oscillator for Ethernet Clock Generation (DSC6102HI2B-025.0000T)
- One High-Speed USB Device, Three High-Speed USB Hosts with Dedicated On-Chip Transceivers
- Shutdown and Reset Control Pins
- Up to 24-bit LCD Interface
- Up to 85 I/Os
- Independent Power Supplies Available for QSPI Memory and for Backup Depending on Voltage Domains
- Operational Conditions:
  - Main operating voltage (5V_MAIN): 3.3V to 5.5V ± 5%
  - Module ambient temperature range (T_A): -40°C to +85°C
- Package:
  - 28 x 28 mm 152-pin 0.65 mm pad pitch module, manually solderable for prototyping

2. Applications

- Industrial Control and Automation
- Smart Appliances
- Human Machine Interfaces (HMI)
- IoT Gateways
- Access Control Panels
- Security and Alarm Systems

3. Design Resources

3.1 Hardware Design Resources

As the SAM9X60 Series System-in-Package (SiP) MPU embeds a DDR SDRAM memory chip, most of the design complexity related to high-speed DDR interface routing is avoided when using the SAM9X60 System-On-Module.

For carrier board design, Microchip provides complete SAM9X60 System-On-Module schematics and PCB design files in Altium format (available upon request and under a license agreement), enabling electrical simulations for high-speed interfaces such as USB, as well as mechanical evaluation and simulation. For signal integrity simulation, Microchip provides IBIS models of the SAM9X60 Series SiP device.

3.2 Software Resources

Microchip Technology provides complete embedded Linux solutions for MPUs. For more information, refer to Linux® OS for MPUs.

4. Reference Documents

The following reference documents are available on www.microchip.com:

Type	Document Title	Literature No.
Data sheet	SAM9X60 SiP	DS60001580
Errata sheet	SAM9X60 SiP Device Silicon Errata and Data Sheet Clarifications	DS80000859
Data sheet	KSZ8081RNA/RND	DS00002199
Data sheet	24AA025E48	DS20002124
Data sheet	MCP16501	DS20006388
Data sheet	DSC61XXB	DS20006155

5. Description

The Microchip SAM9X60D1G-I/LZB is a high-performance System-On-Module based on ultra-low power ARM926EJ-S CPU-based embedded microprocessor (MPU) SAM9X60. The SAM9X60D1G-I/LZB is certified for industrial operating conditions over the [-40°C to 85°C] industrial ambient temperature range.

The SAM9X60D1G-I/LZB operates at a maximum CPU operating frequency of 600 MHz and a maximum bus speed of 200 MHz. It features up to:

- 1 Gbit of DDR2-SDRAM memory (SAM9X60D1GT-I/4FB)
- 4 Gbits of NAND Flash memory
- 1 Kbit of EEPROM memory with EUI-48 Node Identity (24AA025E48T-I/OT)

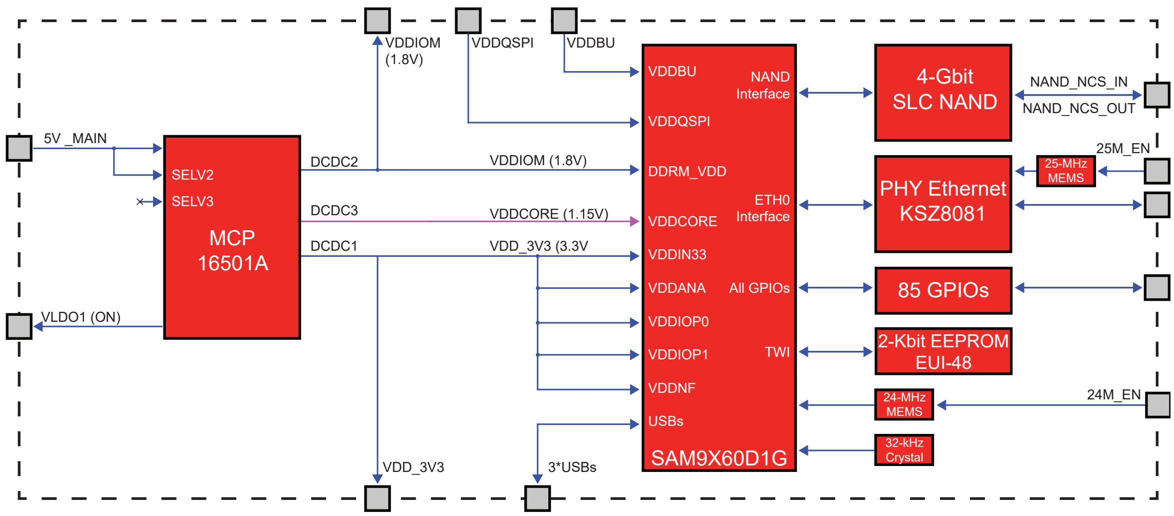
The SAM9X60D1G-I/LZB is a 152-pin, 0.65-mm pad pitch module, 28 mm x 28 mm in size.

The SAM9X60D1G-I/LZB offers an extensive peripheral set, including high-speed USB host and device, 10Base-T/100Base-TX Ethernet interface, system control and up to 85 I/Os featuring:

- Up to 11 FLEXCOMs
- Up to 6 ADC inputs
- Up to 2 CAN interfaces
- Up to 2 SD/MMC, SDIO Interfaces
- Up to 4 PWM interfaces
- Up to 11 wake-ups
- Serial interfaces such as QSPI, SSC and I²S
- LCD RGB interface up to 24 bits
- CMOS camera interface
- Half-bridge class-D stereo

6. Block Diagram

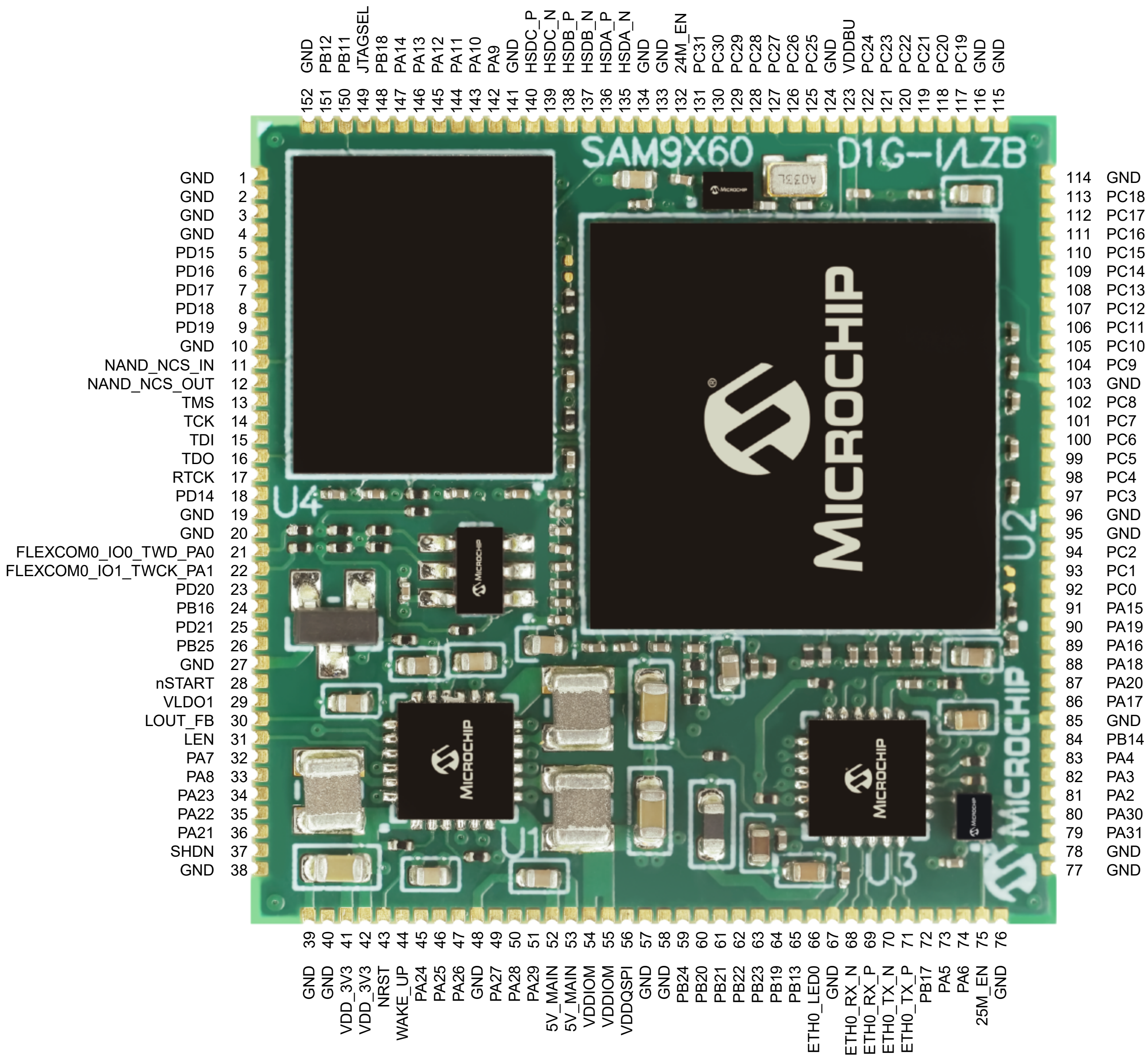
Figure 6-1. SAM9X60D1G-I/LZB Block Diagram



7. Pinout

7.1 Pinout Overview

Figure 7-1. SAM9X60D1G-I/LZB Pin Assignment



7.2 Pin List

The following tables provide the SAM9X60D1G-I/LZB pin description.

> **Important:** Compared to the SAM9X60 SiP (SAM9X60D1G), some PIO features are not listed. These features are used internally on the SAM9X60D1G-I/LZB SOM and cannot have other uses.

The device features several PIO controllers that multiplex the I/O lines of the peripheral set. The following PIOx Pin Description tables define how the I/O lines are multiplexed on the different PIO controllers. The "Reset State" column shows whether the PIO line resets in I/O mode or in Peripheral mode. If I/O is shown, the PIO line resets with the characteristics (input, output, pull-up or pull-down) indicated in this same column, so that the device is configured in a known state as soon as the reset is released. As a result, PIO_CFGR.FUNC resets to ‘0’. If a signal name is shown in the “Reset State” column, the PIO line is assigned to this function and PIO_CFGR.FUNC is not set to ‘0’. That is the case for pins controlling memories, in particular address lines, which require the pin to be driven as soon as the reset is released.

7.2.1 PIOA Pin List

Table 7-1. PIOA Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER	
21	VDDIOP0	GPIO	PA0	I/O	–	–	A	FLEXCOM0_IO0	I/O	PIO, I, PU, ST	1, 3
22	VDDIOP0	GPIO	PA1	I/O	–	–	A	FLEXCOM0_IO1	I/O	PIO, I, PU, ST	1, 3
81	VDDIOP0	GPIO	PA2	I/O	WKUP1	–	B	SDMMC1_DAT1	I/O	PIO, I, PU, ST	2
82	VDDIOP0	GPIO	PA3	I/O	–	–	B	SDMMC1_DAT2	I/O	PIO, I, PU, ST	2
83	VDDIOP0	GPIO	PA4	I/O	–	–	B	SDMMC1_DAT3	I/O	PIO, I, PU, ST	2
73	VDDIOP0	GPIO	PA5	I/O	–	–	A	FLEXCOM1_IO0	I/O	PIO, I, PU, ST	–
							B	CANTX1	O		
74	VDDIOP0	GPIO	PA6	I/O	–	–	A	FLEXCOM1_IO1	I/O	PIO, I, PU, ST	–
							B	CANRX1	I		
32	VDDIOP0	GPIO	PA7	I/O	–	–	A	FLEXCOM2_IO0	I/O	PIO, I, PU, ST	–
							B	FLEXCOM4_IO4	O		
							C	FLEXCOM5_IO4	O		
33	VDDIOP0	GPIO	PA8	I/O	–	–	A	FLEXCOM2_IO1	I/O	PIO, I, PU, ST	–
							B	FLEXCOM5_IO3	I/O		
							C	FLEXCOM4_IO5	O		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER	
142	VDDIOP0	GPIO	PA9	I/O	WKUP2	–	A	DRXD	I	PIO, I, PU, ST	–
							B	CANRX0	I		
143	VDDIOP0	GPIO	PA10	I/O	WKUP3	–	A	DTXD	O	PIO, I, PU, ST	–
							B	CANTX0	O		
144	VDDIOP0	GPIO	PA11	I/O	–	–	A	FLEXCOM4_IO1	I/O	PIO, I, PU, ST	–
							B	SDMMC1_DAT0	I/O		
145	VDDIOP0	GPIO	PA12	I/O	–	–	A	FLEXCOM4_IO0	I/O	PIO, I, PU, ST	–
							B	SDMMC1_CMD	I/O		
146	VDDIOP0	GPIO	PA13	I/O	–	–	A	FLEXCOM4_IO2	I/O	PIO, I, PU, ST	–
							B	SDMMC1_CK	I/O		
147	VDDIOP0	GPIO	PA14	I/O	–	–	A	FLEXCOM4_IO3	I/O	PIO, I, PU, ST	–
91	VDDIOP0	GPIO	PA15	I/O	–	–	A	SDMMC0_DAT0	I/O	PIO, I, PU, ST	–
89	VDDIOP0	GPIO	PA16	I/O	–	–	A	SDMMC0_CMD	I/O	PIO, I, PU, ST	–
86	VDDIOP0	GPIO	PA17	I/O	–	–	A	SDMMC0_CK	I/O	PIO, I, PU, ST	–
88	VDDIOP0	GPIO	PA18	I/O	–	–	A	SDMMC0_DAT1	I/O	PIO, I, PU, ST	–
90	VDDIOP0	GPIO	PA19	I/O	–	–	A	SDMMC0_DAT2	I/O	PIO, I, PU, ST	–
87	VDDIOP0	GPIO	PA20	I/O	–	–	A	SDMMC0_DAT3	I/O	PIO, I, PU, ST	–
36	VDDIOP0	GPIO	PA21	I/O	–	–	A	TIOA0	I/O	PIO, I, PU, ST	–
							B	FLEXCOM5_IO1	I/O		
35	VDDIOP0	GPIO	PA22	I/O	–	–	A	TIOA1	I/O	PIO, I, PU, ST	–
							B	FLEXCOM5_IO0	I/O		
34	VDDIOP0	GPIO	PA23	I/O	–	–	A	TIOA2	I/O	PIO, I, PU, ST	–
							B	FLEXCOM5_IO2	I/O		
45	VDDIOP0	GPIO	PA24	I/O	–	–	A	TCLK0	I	PIO, I, PU, ST	–
							B	TK	I/O		
							C	CLASSD_L0	O		
46	VDDIOP0	GPIO	PA25	I/O	–	–	A	TCLK1	I	PIO, I, PU, ST	–
							B	TF	I/O		
							C	CLASSD_L1	O		
47	VDDIOP0	GPIO	PA26	I/O	–	–	A	TCLK2	I	PIO, I, PU, ST	–
							B	TD	O		
							C	CLASSD_L2	O		
49	VDDIOP0	GPIO	PA27	I/O	–	–	A	TIOB0	I/O	PIO, I, PU, ST	–
							B	RD	I		
							C	CLASSD_L3	O		
50	VDDIOP0	GPIO	PA28	I/O	WKUP4	–	A	TIOB1	I/O	PIO, I, PU, ST	–
							B	RK	I/O		

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER	
51	VDDIOP0	GPIO	PA29	I/O	–	–	A	TIOB2	I/O	PIO, I, PU, ST	–
							B	RF	I/O		
							C	FLEXCOM2_IO 7	I		
80	VDDIOP0	GPIO	PA30	I/O	–	–	A	FLEXCOM6_IO 0	I/O	PIO, I, PU, ST	2
							B	FLEXCOM5_IO 6	O		
79	VDDIOP0	GPIO	PA31	I/O	–	–	A	FLEXCOM6_IO 1	I/O	PIO, I, PU, ST	2
							B	FLEXCOM5_IO 5	O		

Notes:
1. Fixed feature due to the SAM9X60D1G-I/LZB internal connection.
2. Limited feature compared to SAM9X60D1G due to the use of a part of the functionality for other features in the SAM9X60D1G-I/LZB, for example GMAC or FLEXCOM.
3. The signal is internally pulled up with a 4.7 kΩ resistor.

7.2.2 PIOB Pin List

Table 7-2. PIOB Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER	
--	VDDANA	GPIO	PB0	I/O	–	–	A	E0_RX0	I	PIO, I, PU, ST	1
--	VDDANA	GPIO	PB1	I/O	–	–	A	E0_RX1	I	PIO, I, PU, ST	1
--	VDDANA	GPIO	PB2	I/O	–	–	A	E0_RXER	I	PIO, I, PU, ST	1
--	VDDANA	GPIO	PB3	I/O	–	–	A	E0_RXDV	I	PIO, I, PU, ST	1
--	VDDANA	GPIO	PB4	I/O	–	–	A	E0_TXCK	I/O	PIO, I, PU, ST	1
--	VDDANA	GPIO	PB5	I/O	–	–	A	E0_MDIO	I/O	PIO, I, PU, ST	1
--	VDDANA	GPIO	PB6	I/O	–	–	A	E0_MDC	O	PIO, I, PU, ST	1
--	VDDANA	GPIO	PB7	I/O	–	–	A	E0_TXEN	O	PIO, I, PU, ST	1
--	VDDANA	GPIO	PB8	I/O	–	–	–	–	I	PIO, I, PU, ST	1
--	VDDANA	GPIO	PB9	I/O	–	–	A	E0_TX0	O	PIO, I, PU, ST	1

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER	
--	VDDANA	GPIO	PB10	I/O	–	–	A	E0_TX1	O	PIO, I, PU, ST	1
150	VDDANA	GPIO	PB11	I/O	AD0	–	B	PWM0	O	PIO, I, PU, ST	2
151	VDDANA	GPIO	PB12	I/O	AD1	–	B	PWM1	O	PIO, I, PU, ST	2
65	VDDANA	GPIO	PB13	I/O	AD2	–	B	PWM2	O	PIO, I, PU, ST	2
84	VDDANA	GPIO	PB14	I/O	AD3	–	B	PWM3	O	PIO, I, PU, ST	2
–	VDDANA	GPIO	PB15	I/O	AD4	–	–	–	–	PIO, I, PU, ST	2
24	VDDANA	GPIO	PB16	I/O	AD5	–	–	–	–	PIO, I, PU, ST	2
72	VDDANA	GPIO	PB17	I/O	AD6	–	–	–	–	PIO, I, PU, ST	2
148	VDDANA	GPIO	PB18	I/O	WKUP7	–	A	IRQ	I	PIO, I, PU, ST	–
							B	ADTRG	I		
64	VDDQSPI	GPIO	PB19	I/O	–	–	A	QSCK	O	PIO, I, PU, ST	–
							B	I2SMCC_CK	I/O		
							C	FLEXCOM11_IO0	I/O		
60	VDDQSPI	GPIO	PB20	I/O	–	–	A	QCS	O	PIO, I, PU, ST	–
							B	I2SMCC_WS	I/O		
							C	FLEXCOM11_IO1	I/O		
61	VDDQSPI	GPIO	PB21	I/O	–	–	A	QIO0	I/O	PIO, I, PU, ST	–
							B	I2SMCC_DIN0	I		
							C	FLEXCOM12_IO0	I/O		
62	VDDQSPI	GPIO	PB22	I/O	–	–	A	QIO1	I/O	PIO, I, PU, ST	–
							B	I2SMCC_DOUT0	O		
							C	FLEXCOM12_IO1	I/O		
63	VDDQSPI	GPIO	PB23	I/O	–	–	A	QIO2	I/O	PIO, I, PU, ST	–
							B	I2SMCC_MCK	O		
59	VDDQSPI	GPIO	PB24	I/O	–	–	A	QIO3	I/O	PIO, I, PU, ST	–
26	VDDIOP0	GPIO	PB25	I/O	WKUP8	–	A	NRST_OUT	O	NRST_OUT, O, PD	–
							B	NTRST	I		

Notes:

1. Fixed feature due to the SAM9X60D1G-I/LZB internal connection.
2. Limited feature compared to SAM9X60D1G due to the use of a part of the functionality for other features in the SAM9X60D1G-I/LZB, for example GMAC or FLEXCOM.

7.2.3 PIOC Pin List

Table 7-3. PIOC Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
92	VDDIOP1	GPIO	PC0	I/O	–	–	A	LCDDAT0	O	PIO, I, PU, ST
							B	ISI_D0	I	
							C	FLEXCOM7_IO0	I/O	
93	VDDIOP1	GPIO	PC1	I/O	–	–	A	LCDDAT1	O	PIO, I, PU, ST
							B	ISI_D1	I	
							C	FLEXCOM7_IO1	I/O	
94	VDDIOP1	GPIO	PC2	I/O	–	–	A	LCDDAT2	O	PIO, I, PU, ST
							B	ISI_D2	I	
							C	TIOA3	I/O	
97	VDDIOP1	GPIO	PC3	I/O	–	–	A	LCDDAT3	O	PIO, I, PU, ST
							B	ISI_D3	I	
							C	TIOB3	I/O	
98	VDDIOP1	GPIO	PC4	I/O	–	–	A	LCDDAT4	O	PIO, I, PU, ST
							B	ISI_D4	I	
							C	TCLK3	I	
99	VDDIOP1	GPIO	PC5	I/O	–	–	A	LCDDAT5	O	PIO, I, PU, ST
							B	ISI_D5	I	
							C	TIOA4	I/O	
100	VDDIOP1	GPIO	PC6	I/O	–	–	A	LCDDAT6	O	PIO, I, PU, ST
							B	ISI_D6	I	
							C	TIOB4	I/O	
101	VDDIOP1	GPIO	PC7	I/O	–	–	A	LCDDAT7	O	PIO, I, PU, ST
							B	ISI_D7	I	
							C	TCLK4	I	
102	VDDIOP1	GPIO	PC8	I/O	–	–	A	LCDDAT8	O	PIO, I, PU, ST
							B	ISI_D8	I	
							C	FLEXCOM9_IO0	I/O	
104	VDDIOP1	GPIO	PC9	I/O	–	–	A	LCDDAT9	O	PIO, I, PU, ST
							B	ISI_D9	I	
							C	FLEXCOM9_IO1	I/O	
105	VDDIOP1	GPIO	PC10	I/O	–	–	A	LCDDAT10	O	PIO, I, PU, ST
							B	ISI_D10	I	
							C	PWM0	O	
106	VDDIOP1	GPIO	PC11	I/O	–	–	A	LCDDAT11	O	PIO, I, PU, ST
							B	ISI_D11	I	
							C	PWM1	O	
107	VDDIOP1	GPIO	PC12	I/O	–	–	A	LCDDAT12	O	PIO, I, PU, ST
							B	ISI_PCK	I	
							C	TIOA5	I/O	
108	VDDIOP1	GPIO	PC13	I/O	–	–	A	LCDDAT13	O	PIO, I, PU, ST
							B	ISI_VSYNC	I	
							C	TIOB5	I/O	
109	VDDIOP1	GPIO	PC14	I/O	–	–	A	LCDDAT14	O	PIO, I, PU, ST
							B	ISI_HSYNC	I	
							C	TCLK5	I	
110	VDDIOP1	GPIO	PC15	I/O	–	–	A	LCDDAT15	O	PIO, I, PU, ST
							B	ISI_MCK	O	
							C	PCK0	O	

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Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
111	VDDIOP1	GPIO	PC16	I/O	–	–	A	LCDDAT16	O	PIO, I, PU, ST
							B	E1_RXER	I	
							C	FLEXCOM10_IO0	I/O	
112	VDDIOP1	GPIO	PC17	I/O	–	–	A	LCDDAT17	O	PIO, I, PU, ST
							B	FLEXCOM1_IO7	I	
							C	FLEXCOM10_IO1	I/O	
113	VDDIOP1	GPIO	PC18	I/O	–	–	A	LCDDAT18	O	PIO, I, PU, ST
							B	E1_TX0	O	
							C	PWM0	O	
117	VDDIOP1	GPIO	PC19	I/O	–	–	A	LCDDAT19	O	PIO, I, PU, ST
							B	E1_TX1	O	
							C	PWM1	O	
118	VDDIOP1	GPIO	PC20	I/O	–	–	A	LCDDAT20	O	PIO, I, PU, ST
							B	E1_RX0	I	
							C	PWM2	O	
119	VDDIOP1	GPIO	PC21	I/O	–	–	A	LCDDAT21	O	PIO, I, PU, ST
							B	E1_RX1	I	
							C	PWM3	O	
120	VDDIOP1	GPIO	PC22	I/O	–	–	A	LCDDAT22	O	PIO, I, PU, ST
							B	FLEXCOM3_IO0	I/O	
121	VDDIOP1	GPIO	PC23	I/O	–	–	A	LCDDAT23	O	PIO, I, PU, ST
							B	FLEXCOM3_IO1	I/O	
122	VDDIOP1	GPIO	PC24	I/O	WKUP9	–	A	LCDDISP	O	PIO, I, PU, ST
							B	FLEXCOM3_IO4	O	
125	VDDIOP1	GPIO	PC25	I/O	WKUP10	–	A	–	–	PIO, I, PU, ST
							B	FLEXCOM3_IO3	I/O	
126	VDDIOP1	GPIO	PC26	I/O	–	–	A	LCDPWM	O	PIO, I, PU, ST
							B	FLEXCOM3_IO2	I/O	
127	VDDIOP1	GPIO	PC27	I/O	–	–	A	LCDVSYNC	O	PIO, I, PU, ST
							B	E1_TXEN	O	
							C	FLEXCOM1_IO4	O	
128	VDDIOP1	GPIO	PC28	I/O	–	–	A	LCDHSYNC	O	PIO, I, PU, ST
							B	E1_CRSDV	I	
							C	FLEXCOM1_IO3	I/O	
129	VDDIOP1	GPIO	PC29	I/O	–	–	A	LCDDEN	O	PIO, I, PU, ST
							B	E1_TXCK	I/O	
							C	FLEXCOM1_IO2	I/O	
130	VDDIOP1	GPIO	PC30	I/O	–	–	A	LCDPCK	O	PIO, I, PU, ST
							B	E1_MDC	O	
							C	FLEXCOM3_IO7	I	
131	VDDIOP1	GPIO	PC31	I/O	WKUP11	–	A	FIQ	I	PIO, I, PU, ST
							B	E1_MDIO	I/O	
							C	PCK1	O	

7.2.4 PIOD Pin List

Table 7-4. PIOD Pin Description

Pad No.	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State	Note
			Signal	Dir	Signal	Dir	Func	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER	
--	VDDNF	GPIO	PD0	I/O	–	–	A	NANDOE	O	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD1	I/O	–	–	A	NANDWE	O	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD2	I/O	–	–	A	A21/NANDALE	O	A21,O, PD, ST	1
--	VDDNF	GPIO	PD3	I/O	–	–	A	A22/NANDCLE	O	A22,O, PD	1
12	VDDNF	GPIO	PD4	I/O	–	–	A	NCS3/NANDCS	O	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD5	I/O	–	–	A	NWAIT	I	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD6	I/O	–	–	A	D16	I/O	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD7	I/O	–	–	A	D17	I/O	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD8	I/O	–	–	A	D18	I/O	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD9	I/O	–	–	A	D19	I/O	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD10	I/O	–	–	A	D20	I/O	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD11	I/O	–	–	A	D21	I/O	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD12	I/O	–	–	A	D22	I/O	PIO, I, PU, ST	1
--	VDDNF	GPIO	PD13	I/O	–	–	A	D23	I/O	PIO, I, PU, ST	1
18	VDDNF	GPIO	PD14	I/O	–	–	–	–	–	PIO, I, PU, ST	2
5	VDDNF	GPIO	PD15	I/O	–	–	–	–	–	A20, O, PD	2
6	VDDNF	GPIO	PD16	I/O	–	–	–	–	–	A23, O, PD	2
7	VDDNF	GPIO	PD17	I/O	WKUP12	–	–	–	–	A24, O, PD	2
8	VDDNF	GPIO	PD18	I/O	WKUP13	–	–	–	–	A25, O, PD	2
9	VDDNF	GPIO	PD19	I/O	–	–	–	–	–	PIO, I, PU, ST	2
23	VDDNF	GPIO	PD20	I/O	–	–	–	–	–	PIO, I, PU, ST	2
25	VDDNF	GPIO	PD21	I/O	–	–	–	–	–	PIO, I, PU, ST	2

Notes:
1. Fixed feature due to the SAM9X60D1G-I/LZB internal connection.
2. Limited feature compared to SAM9X60D1G due to the use of a part of the functionality for other features in the SAM9X60D1G-I/LZB, for example GMAC or FLEXCOM.

7.2.5 System Pin List

Table 7-5. System Pin Description

Pin No.	Pin Name	Power Rail	I/O Type	Description	Note
136	HSDA_P	VDD_3V3	I/O	USB host port A high-speed data +	–
135	HSDA_N	VDD_3V3	I/O	USB host port A high-speed data -	–
138	HSDB_P	VDD_3V3	I/O	USB host port B high-speed data +	–
137	HSDB_N	VDD_3V3	I/O	USB host port B high-speed data -	–
140	HSDC_P	VDD_3V3	I/O	USB host port C high-speed data +	–
139	HSDC_N	VDD_3V3	I/O	USB host port C high-speed data -	–
44	WKUP0	VDDBU	I	Wake-up input	2
37	SHDN	VDDBU	O	Shutdown control	–
149	JTAGSEL	VDDBU	I	JTAG selection	–
14	TCK	VDD_3V3	I	Test clock	–
15	TDI	VDD_3V3	I	Test data in	–
16	TDO	VDD_3V3	O	Test data out	–
13	TMS	VDD_3V3	I	Test mode select	–
17	RTCK	VDD_3V3	O	Return test clock	–
43	NRST	VDD_3V3	I/O	External nReset input/output	1
28	NSTART	5V_MAIN	I/PU	Start event input. Drive to low to initiate a start-up sequence.	–
30	LOUT_FB	VLDO1	I	LDO feedback pin. Connect to external resistor divider to VLDO1 for output voltage adjustment.	–
31	LEN	5V_MAIN	I	VLDO1 enable input	–
68	ETH0_RX_N	–	I/O	Physical receive or transmit signal (– differential)	–
69	ETH0_RX_P	–	I/O	Physical receive or transmit signal (+ differential)	–
70	ETH0_TX_N	–	I/O	Physical transmit or receive signal (– differential)	–
71	ETH0_TX_P	–	I/O	Physical transmit or receive signal (+ differential)	–
66	ETH0_LED0	–	I/PU/O	Programmable LED0 output	1
132	24M_EN	VDD_3V3	I	24-MHz MEMS oscillator input pin used for main clock	–
75	25M_EN	VDD_3V3	I	25-MHz MEMS oscillator input pin used for Ethernet clock	–
11	NAND_CS_IN	VDD_3V3	I	NAND Flash chip select input. Connect to pin 12.	1

Notes:
1. The signal is internally pulled up with a 10 kΩ resistor.
2. The signal is internally pulled up with a 100 kΩ resistor.

7.2.6 Power Pin List

Table 7-6. Power Pin Description

Pin No.	Pin Name	Power Rail	Type	Description
54, 55	VDDIOM	VDDIOM	Output power	1.8V memory voltage output
52, 53	5V_MAIN	5V_MAIN	Input power	5V main input supply
123	VDDBU	VDDBU	Input power	Backup voltage input
41, 42	VDD_3V3	VDD_3V3	Output power	3.3V I/Os voltage output
29	VLDO1	VLDO1	Output power	Adjustable LDO voltage output
56	VDDQSPI	VDDQSPI	Input power	QSPI voltage input

...........continued

Pin No.	Pin Name	Power Rail	Type	Description
1, 2, 3, 4, 10, 19, 20, 27, 38, 39, 40, 48, 57, 58, 67, 76, 77, 78, 85, 95, 96, 103, 114, 115, 116, 124, 133, 134, 141, 152	GND	Ground	Ground	Ground connection

8. Power Considerations

8.1 Power Supplies

Table 8-1. SAM9X60D1G-I/LZB Power Supplies

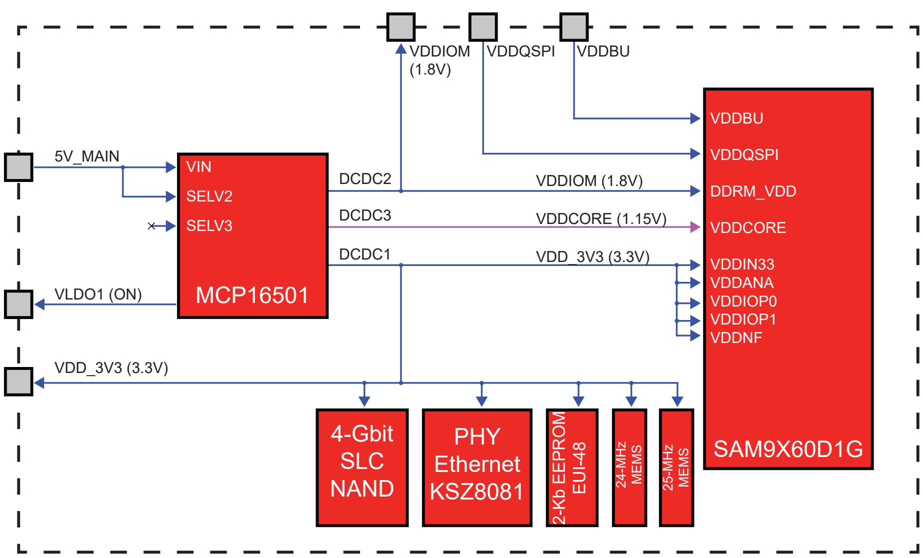
Pin No.	Name[1]	Power Type	Output Current Capability	Power Domains
123	VDDBU	Input	–	Backup supply input
56	VDDQSPI	Input	–	QSPI supply input
41, 42	VDD_3V3	Output	600 mA	I/O supply and customer application output
54, 55	VDDIOM	Output	600 mA	DDR memory supply and customer application output
52, 53	5V_MAIN	Input	–	System power input
29	VLDO1	Output	300 mA	Adjustable output depending on application settings

Note:

1. VDDBU and VDDQSPI need to be supplied externally on their respective pins. Failing to do so will prevent the MPU from working properly.

The SAM9X60D1G-I/LZB System-On-Module is supplied by a unique input (5V_MAIN) and its internal supplies are all delivered by a power management unit (MCP16501), as shown in the Power Architecture diagram below.

Figure 8-1. SAM9X60D1G-I/LZB Power Architecture



8.2 Power-Up/Down Considerations

8.2.1 System Power-Up

At power-up, from a power supply sequencing perspective, the SAM9X60D1G-I/LZB power supplies are categorized into five independent groups:

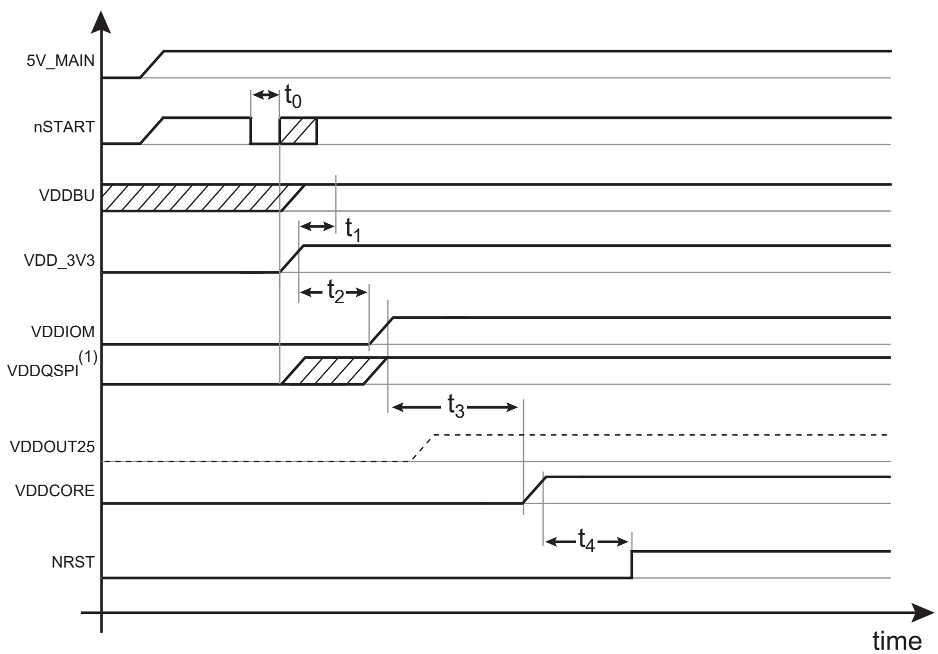
- 5V_MAIN (main supply)
- VDDBU (backup group)

- VDD_3V3 (periphery group) containing VDDUTMII, VDDANA, VDDOSC, VDDNF, VDDIOPx and VDDQSPI inputs
- VDDIOM (memory group)
- VDDCORE (core group)

The figure below shows the recommended power-up sequence. Note the following:

- VDDBU
  - When supplied from a precharged storage element (battery, supercapacitor or micro-battery), VDDBU is an always-on supply input and is therefore not part of the power supply sequencing.
  - When no storage element is used on VDDBU in the application, VDDBU must be tied to VDD_3V3.
  - When a supercapacitor or a micro-battery is used in the application to power VDDBU in Backup mode, this element must be isolated from VDDBU during its (slow) charge, so that VDDBU closely follows VDD_3V3. In table Power-Up Timing Specification, the parameter t_1 limits the delay to establish VDDBU after VDD_3V3.
- VDDOUT25 is the output of the internal 2.5V regulator, and therefore there is no power supply requirement on this pin. VDDOUT25 is automatically started at VDD_3V3 rise when VDD_3V3 is above its Power-On-Reset threshold.

Figure 8-2. Recommended Power-Up Sequence



Note:

1. If VDDQSPI is supplied externally, the power must be applied at the same time or after the presence of VDD_3V3 and before the presence of VDDIOM.

Table 8-2. Power-Up Timing Requirements

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
t_0	nSTRT deglitch time	nSTRT pin falling edge	0.5	–	–	ms
t_1	VDDBU delay	Delay from established VDD_3V3 to established VDDBU	–	–	0.2	ms

...........continued

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
t_2	VDD_3V3 to Periphery group delay	Delay from established VDD_3V3 to the periphery group established supply	–	8	–	ms
t_3	Periphery group to VDDCORE delay	Delay from the periphery group established supply to the VDDCORE supply turn-on	–	4	–	ms
t_4	Reset delay at power-up	From established VDDCORE to NRST high	–	16	–	ms

Note:

1. The term "established" refers to a power supply established to 90% of its final value.

8.2.2 System Power-Down

The following figure shows the SAM9X60D1G-I/LZB power-down sequence that starts by asserting the NRST line to 0.

Once NRST is asserted, the supply inputs can be immediately shut down without any specific timing or order. VDDBU may not be shut down if the application uses a backup storage element on this supply input.

Figure 8-3. Recommended Power-Down Sequence

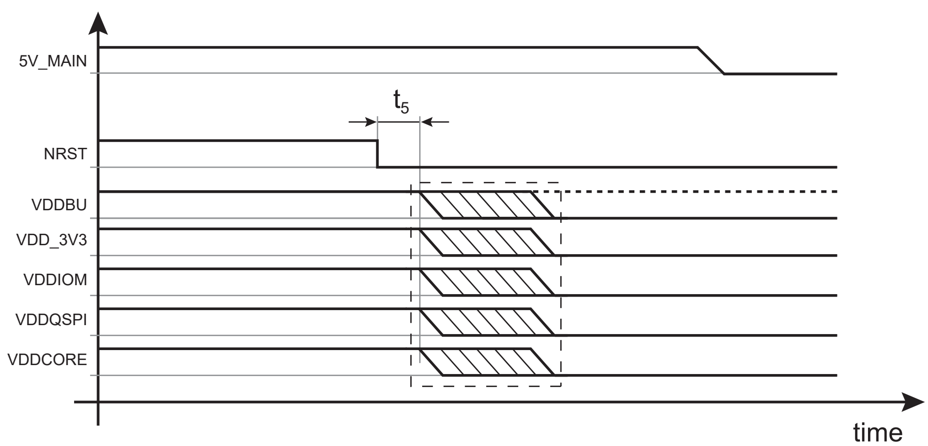


Table 8-3. Power-Down Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_5	NRST delay at power-down	Delay from NRST asserted to first supply turn-off	0	–	10	µs

8.2.3 Particular Considerations

Using the MCP16501, the system can be configured for automatic start-up (see Power Management Unit). Start-up occurs as soon as 5V_MAIN voltage is present, provided that an external capacitor is connected on nSTART_SOM (pin 75).

For this configuration, the external capacitor value must be selected with great care. The recommendations described in the MCP16501 PMIC data sheet under “nSTRT Capacitor for Automatic Turn-On on VIN Ramping” must be followed. For more information, refer to the MCP16501 PMIC data sheet (see Reference Documents).

8.3 Power Management Unit

The SAM9X60D1G-I/LZB System-On-Module is supplied by an external supply (5V_MAIN) and generates its own internal supplies via the Microchip MCP16501 power management unit.

The MCP16501 is a full-featured Power Management Integrated Circuit (PMIC), cost and size optimized for Microchip MPU devices such as the SAM9X60D1G.

The MCP16501 integrates three DC-DC buck regulators used for system supplying and one auxiliary LDO for customer purposes.

- All buck channels can support loads up to 1A. All bucks are 100% duty cycle capable.
  - DCDC1 set to 3.3 V supplies all pads of the embedded devices. This power rail offers a 600-mA load to customer application through pins 41 and 42 (VDD_3V3).
  - DCDC2 set to 1.8V supplies the DDR2 memory. This power rail offers a 600-mA load to customer application through pins 54 and 55 (VDDIOM).
  - DCDC3 set to 1.15V supplies the microprocessor core.
- One 300-mA LDO is provided so that sensitive analog loads can be supported.

The default power channel sequencing is built-in, as required by the Microchip SAM9X60D1G MPU device.

Active discharge resistors are provided on each output. All buck channels support safe start-up into pre-biased outputs.

The MCP16501 is available in a 4x4 mm 24-pin VQFN package.

The LPM pin of the Microchip SAM9X60 SOM, combined with the PWRHLD (also named SHDN) status pin of the MCP16501 PMIC, define different power states, which are illustrated in the table below.

PWRHLD	LPM	Buck1	Buck2	Buck3	LDO1	nRST	Power State (1)
0	0	Off	Off	Off	LEN Controlled	Low	Off
0	1	Off	On(2)	Off	LEN Controlled	Low	Hibernate mode
1	1	On(2)	On(2)	On(2)	LEN Controlled	HiZ	Low-Power mode
1	0	On(3)	On(3)	On(3)	LEN Controlled	HiZ	Active mode

For more information about the PMIC MCP16501, see Reference Documents.

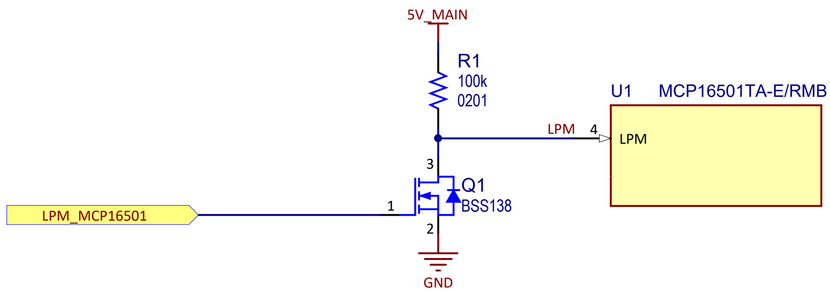
Notes:

1. Only allowed modes are listed. If the PWRHLD/LPM combination is not listed, the mode is not allowed.
2. In this mode, the DCDC is configured in Automatic Pulse-Frequency Modulation (Auto-PFM) mode.
3. In this mode, the DCDC is configured in Force Pulse-Width Modulation (FPWM) mode.

For more information about the use of the MCP16501 PMIC LPM feature, refer to the MCP16501 data sheet (see Reference Documents).

The LPM pin is controlled externally, as shown in the figure below.

Figure 8-4. LPM Schematic



8.4 Power Configurations

Two different configurations are described below, depending on customer use.

- Single supply—SAM9X60D1G-I/LZB can be supplied by only one input supply (for example, a 5V AC/DC wall adapter) and other input supplies can be connected to the internal 3.3V regulator VDD_3V3. All the PIO lines are supplied at 3.3V.
- Multiple supplies—SAM9X60D1G-I/LZB can be supplied by a 5V supply and a backup battery. Some PIO lines are supplied by different LDOs for specific applications, such as VDDQSPI.

Figure 8-5. SAM9X60D1G-I/LZB Single Supply Connection Example

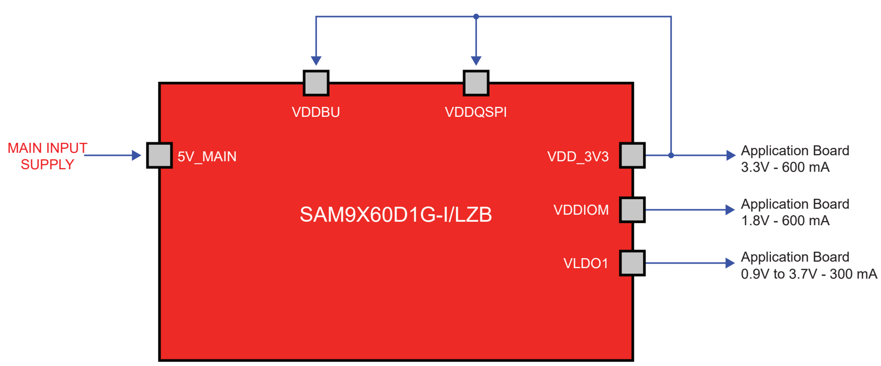
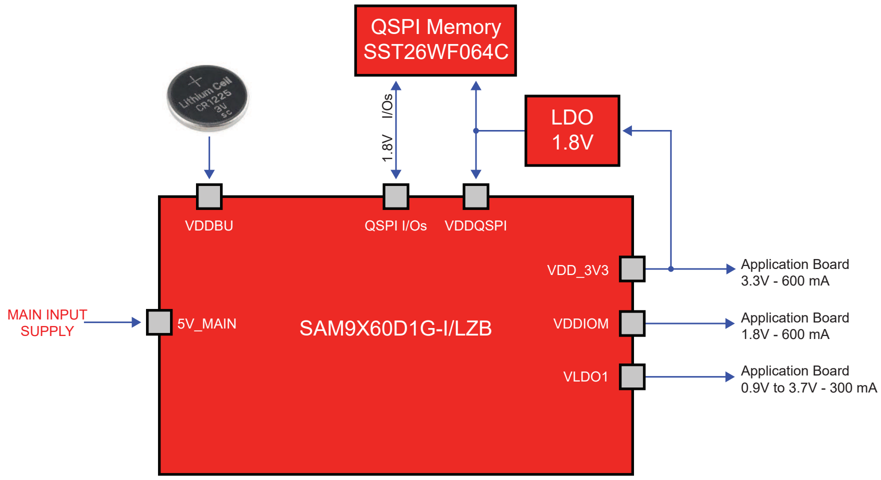


Figure 8-6. SAM9X60D1G-I/LZB Multiple Supplies Connection Example



9. MPU and Memory Subsystem

9.1 SAM9X60 System-in-Package (SiP)

The SAM9X60D1G-I/LZB System-On-Module embeds the SAM9X60 SiP (SAM9X60D1G), which integrates the ARM926EJ-S Arm Thumb processor-based SAM9X60 MPU with a 1-Gbit DDR2 SDRAM in a single package.

By combining the SAM9X60 with a DDR2 SDRAM memory in a single package, PCB routing complexity, area and number of layers are reduced. This makes board design easier and more robust by facilitating design for EMI, ESD and signal integrity.

For more information, refer to the SAM9X60 SiP data sheet (see Reference Documents).

The SAM9X60 SiP is available in a 14x14 mm 233-ball TFBGA package.

The SAM9X60D1G-I/LZB provides global system Reset (NRST) and Shutdown (SHDN) pins to the application board.

Notes:

- The NRST pin is an input/output pin generated by the power management unit (MCP16501) respecting power sequence timing. It is distributed internally to the microprocessor and to the Ethernet PHY, and it can be forced externally for system-level control.
- The SHDN pin is an output pin managed by the application software. In an application case, the pin can switch on/off the 5V_MAIN external main supply.

9.2 MPU Clocks

Two clock sources are necessary for the SAM9X60D1G-I/LZB microprocessor:

- 32.768-kHz oscillator for slow clock oscillator input and embedded RTC of the SAM9X60
- 24-MHz main oscillator for the SAM9X60

Each clock is generated by a Microchip ultra-low power MEMS oscillator:

1. DSC6102HI2B-024.0000 device: delivers a 24-MHz clock to the SAM9X60D1G. Can be enabled externally via the 24M_EN pin to control power consumption during activity.
   For more information about the MEMS DSC61xxB, see Reference Documents.

   The 24-MHz clock can be enabled/disabled as required by the application, through the 24M_EN signal available on pin 132. Three configurations are possible:
   - 24M_EN pin connected to VDD (VDD_3V3). The clock is enabled.
   - 24M_EN connected to GND. The clock is stopped.
   - 24M_EN connected to a GPIO. The clock is dynamically controlled by software.
2. Crystal device: delivers a 32.768-kHz clock to the SAM9X60D1G.

9.3 NAND Flash Memory

The SAM9X60D1G-I/LZB System-On-Module embeds a 4-Gbit SLC NAND Flash memory supported through its External Bus Interface controller.

The System-On-Module implements one of the following references to provide a 4-Gbit memory space:

- MX30LF4G28AD-XKI in VFBGA-63 package
- MT29F4G08ABAFAH4-IT:F in VFBGA-63 package

Notes:

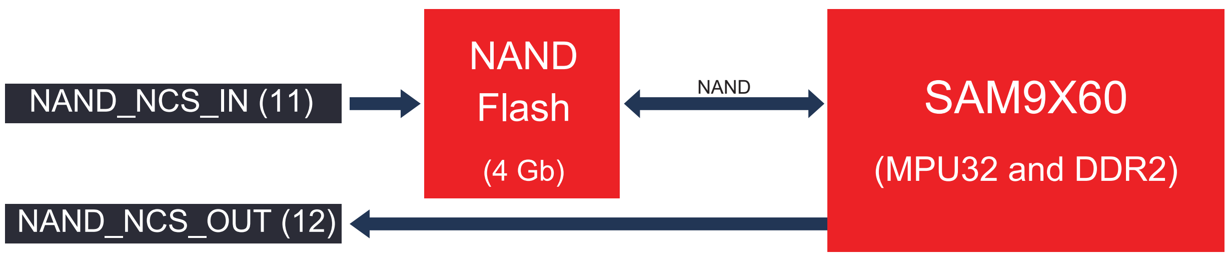
1. Either one of the above references can be mounted on the Microchip SAM9X75 System-On-Module Series.
2. Read/write speed may vary depending on the NAND Flash reference fitted to the module.

For more information about NAND Flash memories, refer to the relevant data sheets (see Reference Documents).

The software must be adapted to recognize the relevant NAND Flash manufacturer. Microchip Linux distribution supports all references. For details on how to build Linux software, refer to www.linux4microchip.com/.

The NAND_NCS_IN signal (pin 11) is accessible externally and can be uncoupled from the NAND_NCS_OUT signal (pin 12) so that the boot can be unselected from the NAND Flash memory during debug phases.

Figure 9-1. NAND Flash Memory Block Diagram



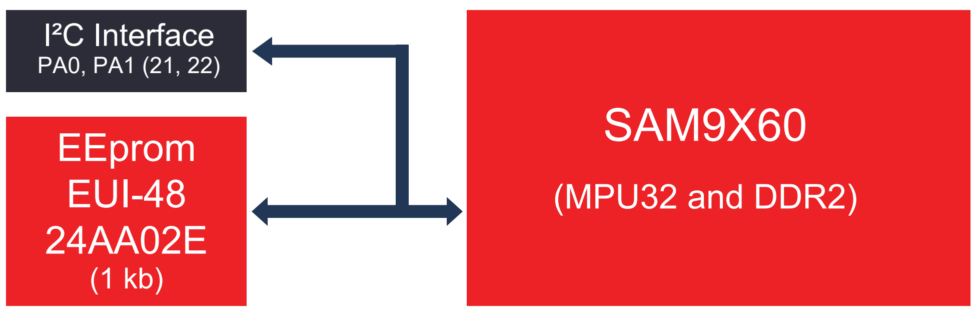
10. LAN Subsystem

10.1 EEPROM

The SAM9X60D1G-I/LZB System-On-Module embeds the 24AA025E48T-I/OT, a 1-Kbit Serial EEPROM with a pre-programmed EUI-48 MAC address. The device is organized as one block of 128 x 8-bit memory with a 2-wire serial interface. The second block is reserved for MAC address storage. The 24AA025E48T-I/OT also has a page write capability for up to 16 bytes of data. The 24AA025E48T-I/OT is available in the standard 5-lead SOT-23 package.

For more information about the 24AA025E48 EEPROM, see Reference Documents.

Figure 10-1. EEPROM Memory Block Diagram



Tip: The 2-wire serial interface can be externally shared with another device. A 2-wire data signal (pad 21) and a 2-wire clock signal (pad 22) are used.

Important: If the 2-wire serial interface is used externally, the connected device must have an I²C address different from the embedded EEPROM address. For more details, refer to the device data sheet and to the System-On-Module schematic.

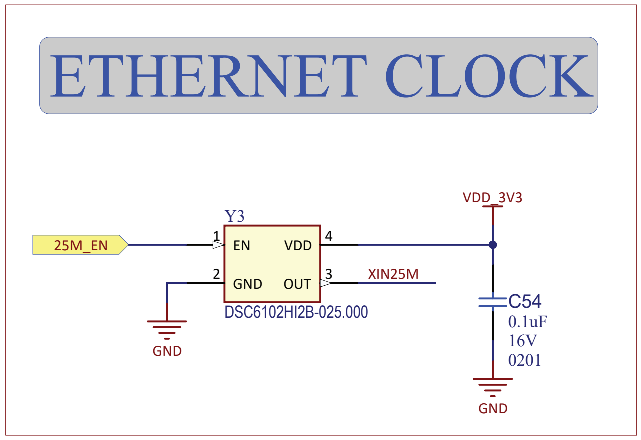
10.2 Ethernet Clock

One 25-MHz clock source is required by the SAM9X60D1G-I/LZB Ethernet port. The clock is generated by a Microchip ultra-low-power MEMS oscillator.

The DSC6102HI2B-025.0000 device delivers a controllable 25-MHz clock to the KSZ8081 Ethernet PHY with an ultra-low power consumption of about 3 mA in Active mode.

For more information about the MEMS DSC61xxB, see Reference Documents.

Figure 10-2. 25-MHz MEMS Oscillator Schematic



The 25-MHz clock can be enabled/disabled as required by the application through the 25M_EN signal available on pin 75. Three configurations are possible:

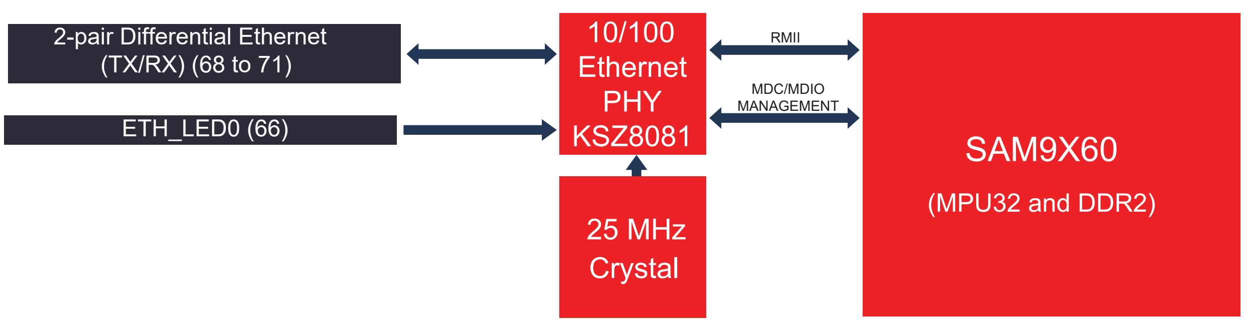
- 25M_EN pin connected to VDD (VDD_3V3). The clock is enabled.
- 25M_EN connected to GND. The clock is stopped.
- 25M_EN connected to a GPIO. The clock is controlled dynamically.

10.3 Ethernet PHY

The Microchip SAM9X60D1G-I/LZB embeds a single-supply 10BASE-T/100BASE-TX Ethernet physical-layer transceiver for transmission and reception of data over a standard CAT-5 Unshielded Twisted Pair (UTP) cable. The KSZ8081RNAIA is a highly-integrated PHY solution. The KSZ8081RNAIA offers the Reduced Media Independent Interface (RMII) for direct connection to RMII-compliant MACs in Ethernet processors. The KSZ8081RNAIA is available in 24-pin, lead-free QFN packages.

For more information about the Ethernet PHY KSZ8081, see Reference Documents.

Figure 10-3. Ethernet PHY Block Diagram

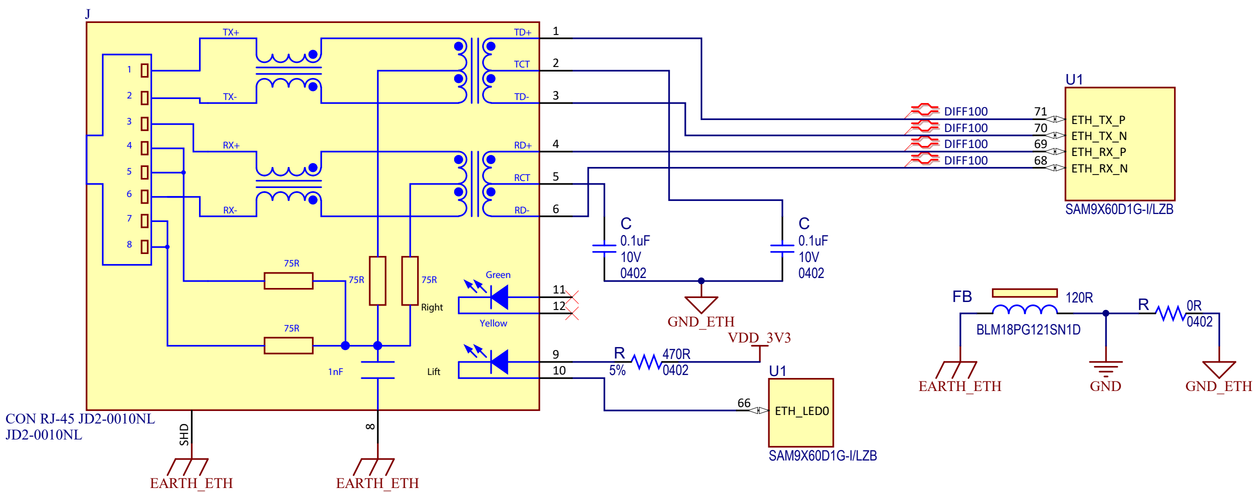


10.4 Interfacing with the Ethernet PHY

10.4.1 Ethernet Design Schematic Example

The figure below is a schematic example at main board level.

Figure 10-4. Ethernet PHY Schematic Example



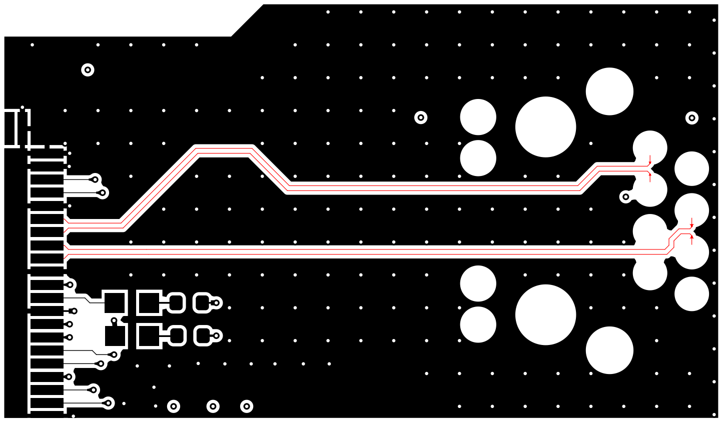
10.4.2 Ethernet Design Layout Recommendations

When designing the Ethernet interface, consider the following recommendations:

- ETH_TX_P, ETH_TX_N, ETH_RX_P and ETH_RX_N should be routed on the top layer without any vias.
- ETH_TX_P and ETH_TX_N should be matched in length to within 120 mils.
- ETH_RX_P and ETH_RX_N should be matched in length to within 120 mils.
- ETH_TX_x and ETH_RX_x must be symmetrical in shape and routing path.
- Place the TX_P and TX_N signals at least two times the trace width away from other signals for noise immunity.
- Place signals at least two times the trace width away from any copper plane.
- Place the TX and RX signals at least three times the trace width away from other signals for noise immunity.
- Check that the ETH_TX_x and ETH_RX_x line impedance is the same for all signal layers. Recommended differential impedance for net: 100Ω ± 5%.

10.4.3 Ethernet Design Layout Example

Figure 10-5. Ethernet Layout Example



11. External Interfacing

11.1 Interfacing with FLEXCOM Interfaces

FLEXCOM offers several serial communication protocols that are managed by the USART, SPI and TWI submodules.

11.1.1 Interfacing in I²C/TWI Mode

Eleven Flexible Serial Communication Controller (FLEXCOM) interfaces configurable in Two-Wire Interface (TWI) mode, and one TWI interface, are available on the SAM9X60D1G-I/LZB.

The Two-Wire Interface (TWI) can interconnect with external components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 Kbits/s in Fast mode and up to 3.4 Mbits/s in High-Speed Client mode only, based on a byte-oriented transfer format.

It can be used with any Two-Wire Interface bus Serial EEPROM and I²C-compatible devices, such as a Real-Time Clock (RTC), a dot matrix/graphic LCD controller or a temperature sensor. The TWI is programmable as a host or a client with sequential or single-byte access. Multiple host capability is supported.

Table 11-1. I²C/TWI Interface Configurations

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Comment
FLEXCOM0	1	21	PA0	FLEXCOM0_IO0_TWD_PA0	No external pull-up needed. Already integrated in the SAM9X60D1G-I/LZB.
		22	PA1	FLEXCOM0_IO1_TWCK_PA1	
FLEXCOM1	1	73	PA5	FLEXCOM1_IO0	External pull-up needed in case the FLEXCOM interface is used as an I²C/TWI interface.
		74	PA6	FLEXCOM1_IO1	
FLEXCOM2	1	32	PA7	FLEXCOM2_IO0	
		33	PA8	FLEXCOM2_IO1	
FLEXCOM3	1	120	PC22	FLEXCOM3_IO0	
		121	PC23	FLEXCOM3_IO1	
FLEXCOM4	1	145	PA12	FLEXCOM4_IO0	
		144	PA11	FLEXCOM4_IO1	
FLEXCOM5	1, 2	35	PA22	FLEXCOM5_IO0	
		36	PA21	FLEXCOM5_IO1	
FLEXCOM6	1	80	PA30	FLEXCOM6_IO0	
		79	PA31	FLEXCOM6_IO1	
FLEXCOM7	1	92	PC0	FLEXCOM7_IO0	
		93	PC1	FLEXCOM7_IO1	
FLEXCOM9	1	102	PC8	FLEXCOM9_IO0	
		104	PC9	FLEXCOM9_IO1	
FLEXCOM10	1	111	PC16	FLEXCOM10_IO0	
		112	PC17	FLEXCOM10_IO1	
FLEXCOM11	1	64	PB19	FLEXCOM11_IO0	
		60	PB20	FLEXCOM11_IO1	
FLEXCOM12	1	61	PB21	FLEXCOM12_IO0	
		62	PB22	FLEXCOM12_IO1	

11.1.2 Interfacing in UART Mode

Eleven FLEXCOM interfaces configurable in UART mode are available on the SAM9X60D1G-I/LZB.

Table 11-2. UART Interface Configurations

Interface Instance	IO Set	Pin No.	PIO	Pin Name
FLEXCOM1	1	73	PA5	FLEXCOM1_IO0
		74	PA6	FLEXCOM1_IO1
FLEXCOM2	1	32	PA7	FLEXCOM2_IO0
		33	PA8	FLEXCOM2_IO1
FLEXCOM3	1	120	PC22	FLEXCOM3_IO0
		121	PC23	FLEXCOM3_IO1
FLEXCOM4	1	145	PA12	FLEXCOM4_IO0
		144	PA11	FLEXCOM4_IO1
FLEXCOM5	1,2	35	PA22	FLEXCOM5_IO0
		36	PA21	FLEXCOM5_IO1
FLEXCOM6	1	80	PA30	FLEXCOM6_IO0
		79	PA31	FLEXCOM6_IO1
FLEXCOM7	1	92	PC0	FLEXCOM7_IO0
		93	PC1	FLEXCOM7_IO1
FLEXCOM9	1	102	PC8	FLEXCOM9_IO0
		104	PC9	FLEXCOM9_IO1
FLEXCOM10	1	111	PC16	FLEXCOM10_IO0
		112	PC17	FLEXCOM10_IO1
FLEXCOM11	1	64	PB19	FLEXCOM11_IO0
		60	PB20	FLEXCOM11_IO1
FLEXCOM12	1	61	PB21	FLEXCOM12_IO0
		62	PB22	FLEXCOM12_IO1

11.1.3 Interfacing in SPI Mode

Four FLEXCOM interfaces configured in SPI mode are available on the SAM9X60D1G-I/LZB.

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Host or Client mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPI devices. During a data transfer, one SPI system acts as the "host," which controls the data flow, while the other devices act as "clients," which have data shifted in and out by the host. Different CPUs can take turns being hosts (multiple host protocol, as opposed to single host protocol, where one CPU is always the host while all others are always clients). One host can simultaneously shift data into multiple clients. However, only one client can drive its output to write data back to the host at any given time.

A client device is selected when the host asserts its NSS signal. When multiple client devices are available, the host generates a separate client select signal (NPCS) for each.

The SPI system consists of two data lines and two control lines:

- Host Out Client In (MOSI)—This data line supplies the output data from the host shifted into the input(s) of the client(s).
- Host In Client Out (MISO)—This data line supplies the output data from a client to the input of the host. There may be no more than one client transmitting data during any particular transfer.
- Serial Clock (SPCK)—This control line is driven by the host and regulates the flow of the data bits. The host can transmit data at a variety of baud rates; there is one SPCK pulse for each bit transmitted.

- Client Select (NSS)—This control line allows clients to be turned on and off by hardware.

Table 11-3. FLEXCOM Interface Configurations in SPI Mode

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Description
FLEXCOM1	1	73	PA5	FLEXCOM1_IO0	MOSI Signal
		74	PA6	FLEXCOM1_IO1	MISO Signal
		129	PC29	FLEXCOM1_IO2	SPCK Signal
		128	PC28	FLEXCOM1_IO3	NPCS0 Signal
FLEXCOM3	1	120	PC22	FLEXCOM3_IO0	MOSI Signal
		121	PC23	FLEXCOM3_IO1	MISO Signal
		126	PC26	FLEXCOM3_IO2	SPCK Signal
		125	PC25	FLEXCOM3_IO3	NPCS0 Signal
FLEXCOM4	1	145	PA12	FLEXCOM4_IO0	MOSI Signal
		144	PA11	FLEXCOM4_IO1	MISO Signal
		146	PA13	FLEXCOM4_IO2	SPCK Signal
		147	PA14	FLEXCOM4_IO3	NPCS0 Signal
FLEXCOM4	2	145	PA12	FLEXCOM4_IO0	MOSI Signal
		144	PA11	FLEXCOM4_IO1	MISO Signal
		146	PA13	FLEXCOM4_IO2	SPCK Signal
		147	PA14	FLEXCOM4_IO3	NPCS0 Signal
FLEXCOM5	1	35	PA22	FLEXCOM5_IO0	MOSI Signal
		36	PA21	FLEXCOM5_IO1	MISO Signal
		34	PA23	FLEXCOM5_IO2	SPCK Signal
		33	PA8	FLEXCOM5_IO3	NPCS0 Signal
		80	PA31	FLEXCOM5_IO5	NPCS2 Signal
		79	PA30	FLEXCOM5_IO6	NPCS3 Signal
FLEXCOM5	2	35	PA22	FLEXCOM5_IO0	MOSI Signal
		36	PA21	FLEXCOM5_IO1	MISO Signal
		34	PA23	FLEXCOM5_IO2	SPCK Signal
		33	PA8	FLEXCOM5_IO3	NPCS0 Signal
		32	PA7	FLEXCOM5_IO4	NPCS1 Signal
		80	PA31	FLEXCOM5_IO5	NPCS2 Signal
		79	PA30	FLEXCOM5_IO6	NPCS3 Signal

11.2 Interfacing with an SD Card

The SD (Secure Digital) Card is a nonvolatile memory card format used as mass storage memory in mobile devices.

Secure Digital Multimedia Card (SDMMC) Controller

The SAM9X60D1G-I/LZB includes two Secure Digital Multimedia Card (SDMMC) interfaces that support the MultiMedia Card (e.MMC) specification V4.51, the SD Memory Card specification V3.0, and the SDIO V3.0 specification. They are compliant with the SD Host Controller Standard V3.0 specification.

The two interfaces can be connected to a standard SD Card interface.

SDMMCx Card Connector

The board features two standard MMC/SD Card connectors, connected to SDMMC0 and SDMMC1. Both interface communications are based on a 4-pin interface (clock, command, four data and power lines).

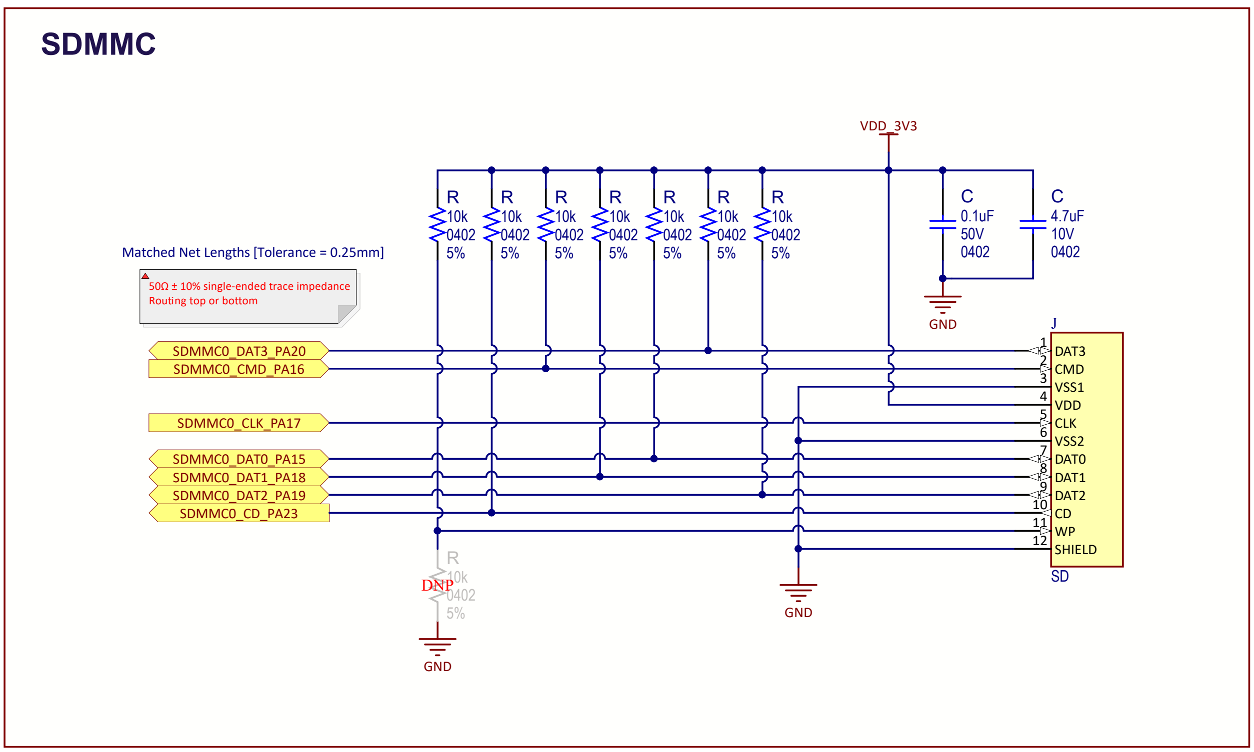
Table 11-4. SDMMCx Interface Configurations

Interface Instance	IO Set	Pin No.	PIO	Pin Name	Description
SDMMC0	1	86	PA17	SDMMC0_CK	SD Card/e.MMC clock signal
		89	PA16	SDMMC0_CMD	SD Card/e.MMC command Line
		91	PA15	SDMMC0_DAT0	SD Card/e.MMC data lines
		88	PA18	SDMMC0_DAT1	
		90	PA19	SDMMC0_DAT2	
		87	PA20	SDMMC0_DAT3	
SDMMC1	1	146	PA13	SDMMC1_CK	SD Card/e.MMC clock signal
		145	PA12	SDMMC1_CMD	SD Card/e.MMC command line
		144	PA11	SDMMC1_DAT0	SD Card/e.MMC data lines
		81	PA2	SDMMC1_DAT1	
		82	PA3	SDMMC1_DAT2	
		83	PA4	SDMMC1_DAT3	

11.2.1 Design Schematic Example

The figure below illustrates the implementation for the SDMMC0 interface for a 4-bit interface.

Figure 11-1. 4-bit SD Card Interface Example Schematic



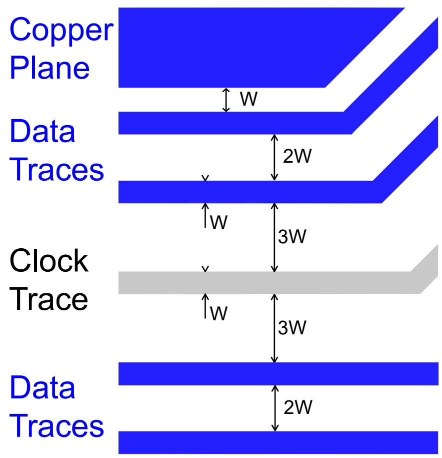
11.2.2 Design Layout Recommendations

When designing the SD Card interface, consider the following recommendations:

- Apply impedance control of 50 Ohms on the clock and data interfaces.

- Match signal lengths to within 20 mils. Affected PIOs in the example above are PA15 to PA20.
- Place the clock line (PA17) at least three times the trace width away from other signals for noise immunity.
- Place data signals at least two times the trace width away from any other data traces.
- Place data signals at least one trace width away from any copper plane.

Figure 11-2. SD Card Layout Example



11.3 Interfacing with an LCD

11.3.1 Design Schematic Example

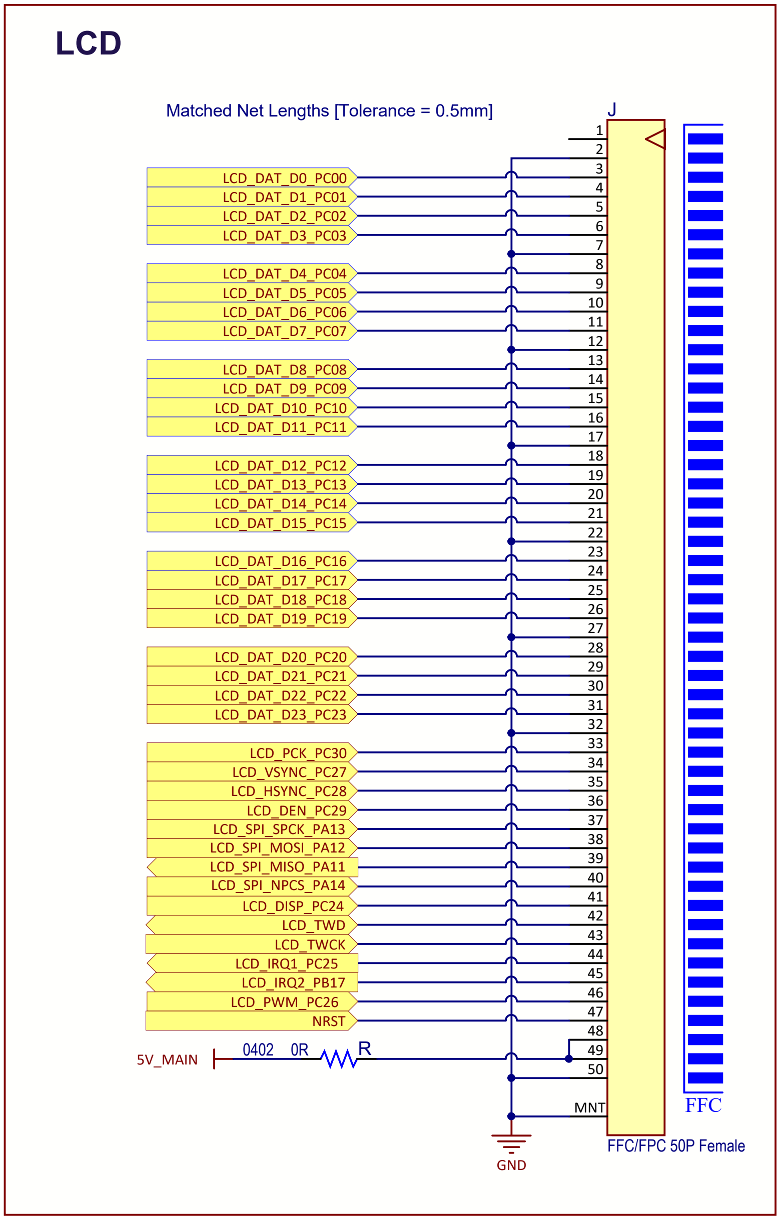
The SAM9X60D1G-I/LZB features a 24-bit RGB LCD interface.

The figure below is a schematic example at main board level illustrating the interface with the AC32005 Microchip display module (WVGA LCD display module with maXTouch® technology).

In this example, several interfaces are used:

- LCD_xxx signals for display
- One SPI interface for display configuration
- One TWI interface for maXTouch and QTouch device control
- Two IRQ I/Os for capacitive touch and buttons interruption

Figure 11-3. LCD Schematic Example



11.3.2 Design Layout Recommendations

When designing the LCD interface, consider the following recommendations:

- Match the LCD signals lengths to within 50 mils. Affected PIOs in the example above are PC0 to PC23, PC27 to PC30.
- Place the clock line (PC30) at least three times the trace width away from other signals for noise immunity.
- Place data signals at least two times the trace width away from any other data trace.
- Design data signals at least two times the trace width away from any copper plane.

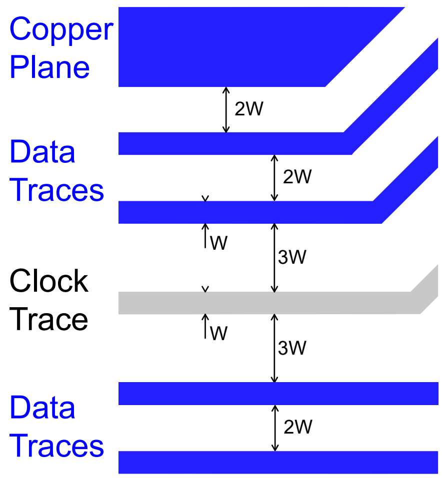


Figure 11-4. LCD Layout Example

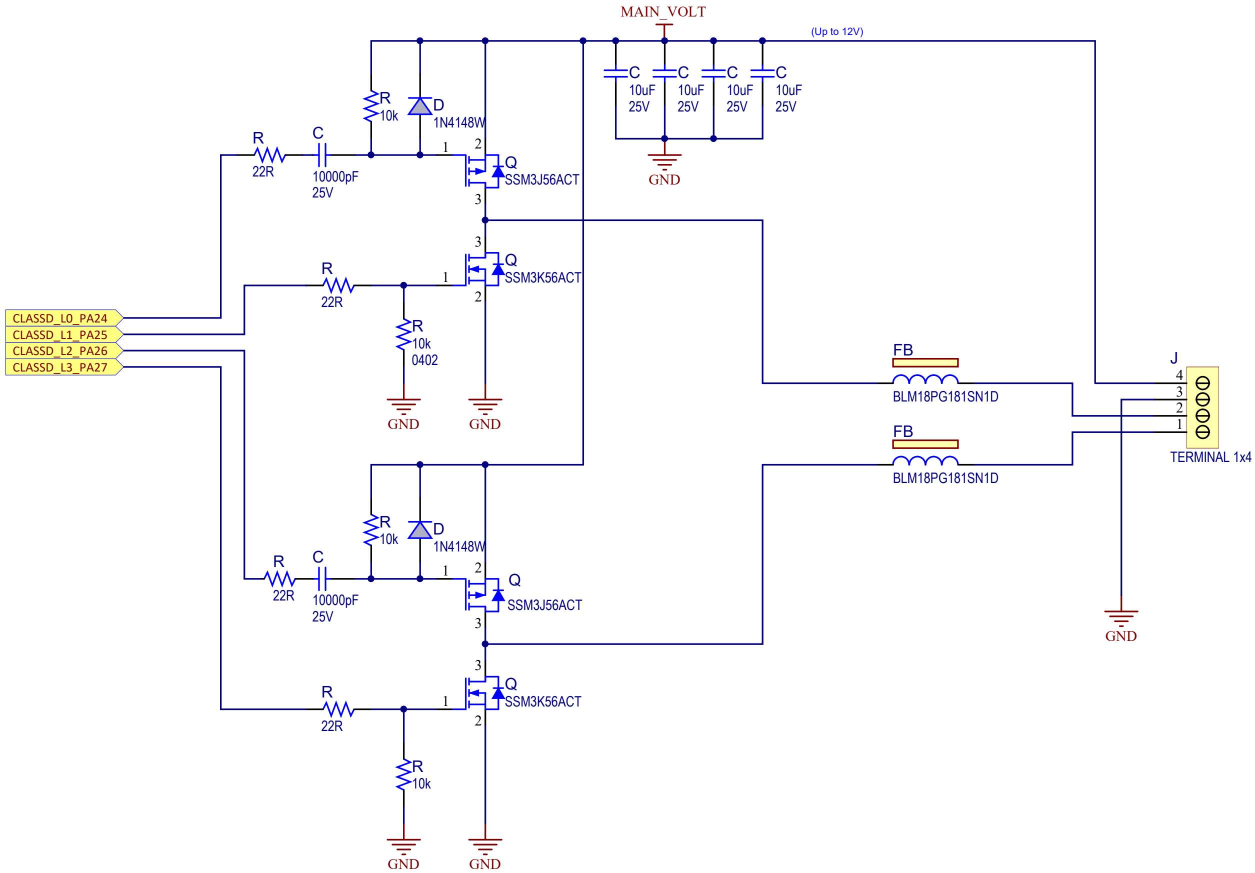
11.4 Interfacing with Class D Audio Output

The Audio Class D (CLASSD) amplifier is a digital input, Pulse Width Modulated (PWM) output mono Class D amplifier. It features a high-quality interpolation filter embedding a digitally-controlled gain, an equalizer and a de-emphasis filter.

On its input side, the CLASSD is compatible with most common audio data rates. On the output side, its PWM output can drive either:

- high-impedance single-ended or differential output loads (Audio DAC application), or
- external MOSFETs through an integrated non-overlapping circuit (Class D power amplifier application).

Figure 11-5. Class D Interface Example Schematic



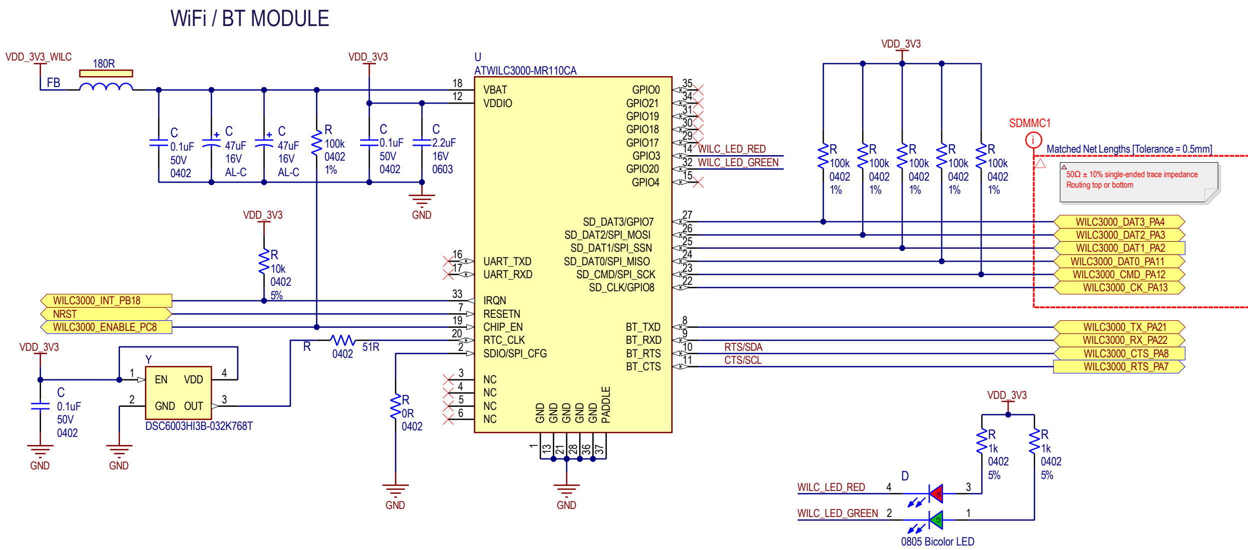
11.5 Interfacing with a Wireless Module

To interface the SAM9X60D1G-I/LZB System-On-Module with a wireless feature, several interfaces must be used, such as SDIO and USART interfaces. The example below is a Microchip ATWILC3000 wireless module.

ATWILC3000 is a single chip IEEE® 802.11 b/g/n RF/Baseband/MAC link controller with integrated Bluetooth® 5.0. The ATWILC3000 connects to Microchip AVR/SMART MCUs, SMART MPUs and other processors with minimal resource requirements using simple SPI/SDIO-to-Wi-Fi® and UART-to-Bluetooth interfaces. Any of the two ATWILC3000 variants, ATWILC3000-MR110UA (u.FL connector) and ATWILC3000-MR110CA (integrated antenna), can be used.

11.5.1 Design Schematic Example

Figure 11-6. Wireless Design Schematic Example



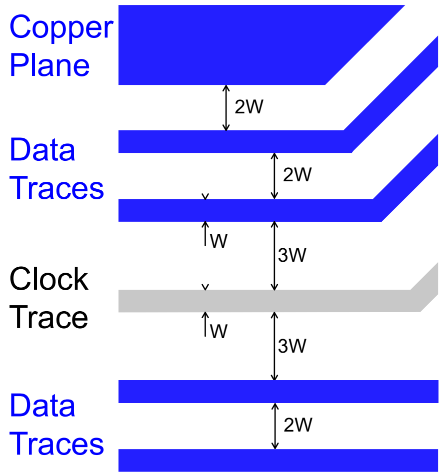
11.5.2 Design Layout Recommendations

No particular layout recommendation about the wireless module is provided in this chapter. All modules have their own recommendations described in their data sheet or application note. Refer to the appropriate document.

When designing the SDIO interface for the wireless solution, consider the following recommendations:

- Apply impedance control of 50 Ohms on the clock and data interfaces.
- Match the SDIO signal lengths to within 20 mils. Affected PIOs in the above example are PA2 to PA4, PA11 to PA13.
- Place the clock line (PA13) at least three times the trace width away from other signals for noise immunity.
- Place data signals at least two times the trace width away from any other data trace.
- Design data signals at least two times the trace width away from any copper plane.

Figure 11-7. SDIO Wireless Interface Layout Example



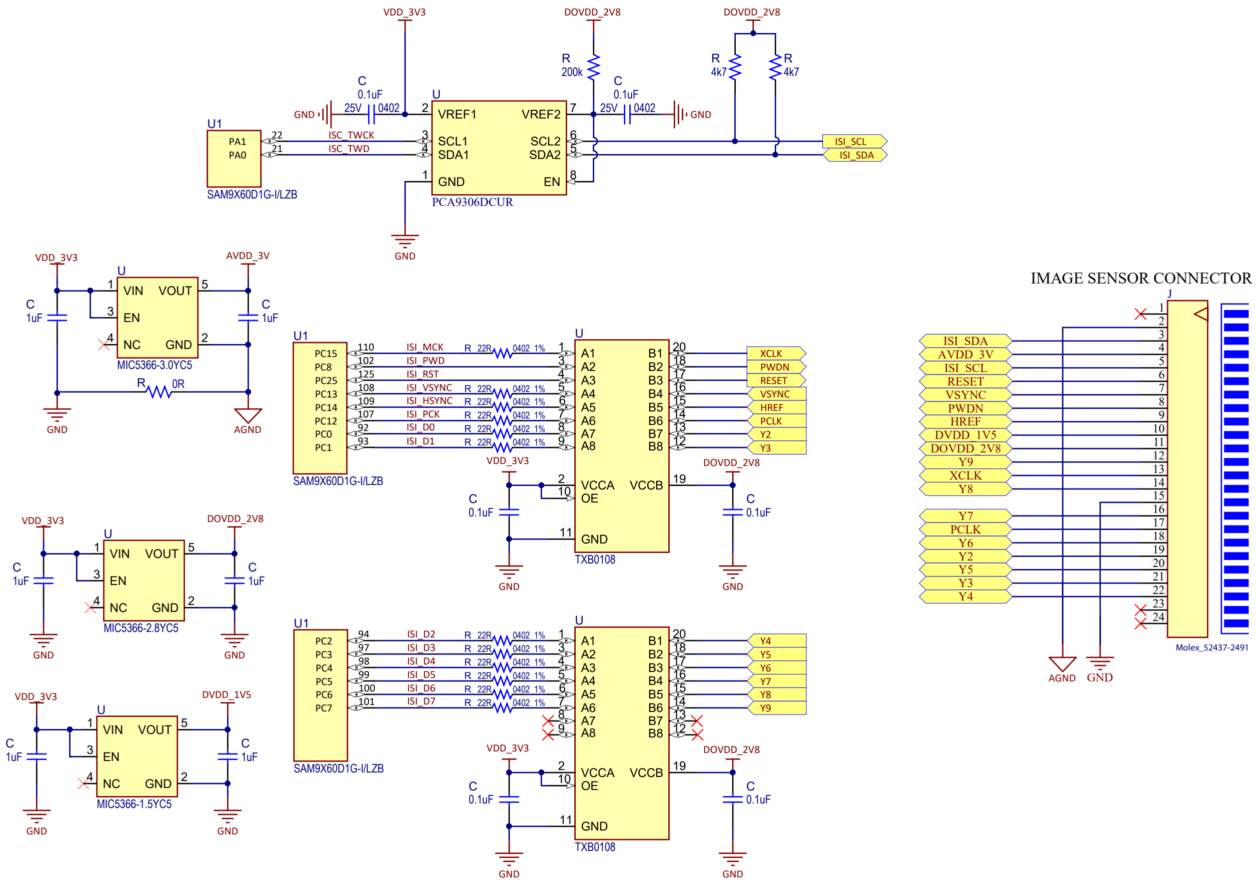
11.6 Interfacing with an Image Sensor

The Image Sensor Interface (ISI) system (or "camera interface") manages incoming data from a parallel sensor. It supports a single active interface. The parallel interface protocol can use a free-running clock or a gated clock strategy. It supports several protocols with an 8-bit or 10-bit data width, and raw Bayer format.

For more information about the ISI Interface, see Reference Documents.

11.6.1 Design Schematic Example

Figure 11-8. Camera Interface Example Schematic

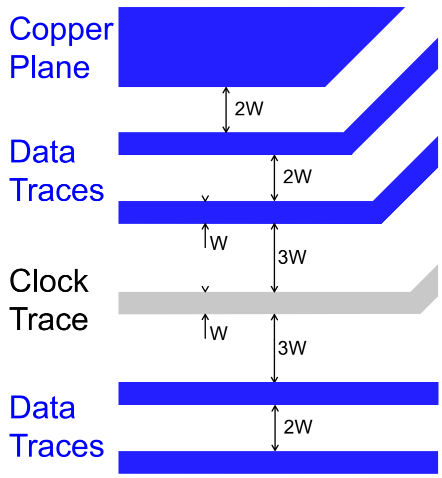


11.6.2 Design Layout Recommendations

When designing the ISI interface, consider the following recommendations:

- Match signal lengths to within 20 mils. Affected PIOs in the example above are PC0 to PC7 and PC12 to PC15.
- Place the clock lines (PC12 and PC15) at least three times the trace width away from other signals for noise immunity.
- Place data signals at least two times the trace width away from any other data traces.
- Place data signals at least two times the trace width away from any copper plane.

Figure 11-9. ISC Layout Example



11.7 Interfacing with a QSPI Memory

The Quad Serial Peripheral Interface (QSPI) is a synchronous serial data link that provides communication with external devices in Host mode.

The QSPI can be used in SPI mode to interface to serial peripherals such as ADCs, DACs, LCD controllers, CAN controllers and sensors, or in Serial Memory mode to interface to serial Flash memories.

The QSPI enables the system to execute code directly from a serial Flash memory (eXecute In Place (XIP)) without code shadowing to RAM.

The serial Flash memory mapping is seen in the system as other memories such as ROM, SRAM, DRAM, embedded Flash memory, etc.

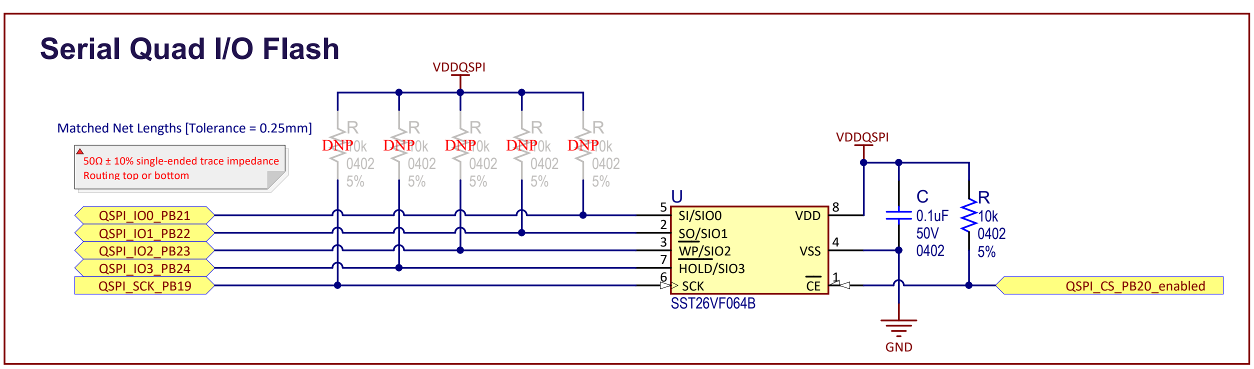
With the support of the Quad SPI protocol, the QSPI enables the system to use high-performance serial Flash memories which are small and inexpensive, instead of larger and more expensive parallel Flash memories.

For more information about the QSPI Interface, see Reference Documents.

Note: Stacked devices with a rollover in the memory address space at each die boundary are not supported.

11.7.1 Design Schematic Example

Figure 11-10. QSPI Interface Example Schematic

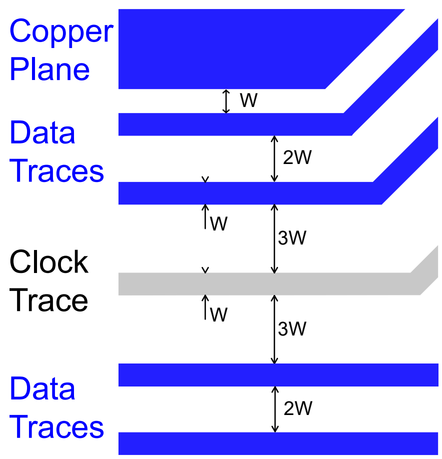


11.7.2 Design Layout Recommendations

When designing the QSPI interface, consider the following recommendations:

- Apply impedance control of 50 Ohms on the clock and data interfaces.
- Match signal lengths to within 10 mils. Affected PIOs in the example above are PB19 to PB24.
- Place the clock line (PB19) at least three times the trace width away from other signals for noise immunity.
- Place data signals at least two times the trace width away from any other data traces.
- Place data signals at least one trace width away from any copper plane.

Figure 11-11. QSPI Layout Example



12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Table 12-1. Absolute Maximum Ratings

I/O Supply Voltage	All GPIO	-0.3V to 4.0V	**Note:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. **Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**
QSPI Supply Voltage	VDDQSPI	-0.3V to 4.0V	
Main Supply Voltage	5V_MAIN	-0.3V to 6.0V	
Backup Supply Voltage	VDDBU	-0.3V to 4.0V	
Storage Temperature	$T_{STORAGE}$	-55 to +150°C	
Maximum Input Current	VDD_MAIN	2A	

12.2 Recommended Operating Conditions

The following table provides the operating conditions for the SAM9X60D1G-I/LZB.

Table 12-2. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
All GPIO	I/O supply voltage	3.23	3.36	V
VDDQSPI	QSPI supply voltage	1.6	3.6	V
5V_MAIN	Main supply voltage	3.0	5.5	V
VDDBU	Backup supply voltage	1.65	3.6	V
T_A	Module operating ambient temperature	–40	85	°C

12.3 DC Characteristics

The following characteristics are applicable to the T_A = -40°C to +85°C operating temperature range, unless otherwise specified.

Table 12-3. DC Electrical Characteristics for GPIO Inputs

Pad	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	All GPIO @ 3.3V	-0.3	–	0.4	V
V_{IH}	High-level input voltage	All GPIO @ 3.3V	2.3	–	3.6	V
V_{OL}	Low-level output voltage	IO max.	–	–	0.41	V
V_{OH}	High-level output voltage	IO max.	2.9	–	–	V
I_{IL}	Low-level input current	All GPIO @ 3.3V	-1	–	1	µA
I_{IH}	High-level input current	All GPIO @ 3.3V	-1	–	1	µA
I_{OL}	Low-level output current	All GPIO @ 3.3V / Low	-2	–	–	mA
		All GPIO @ 3.3V / High	-32	–	–	mA
I_{OH}	High-level output current	All GPIO @ 3.3V / Low	–	–	2	mA
		All GPIO @ 3.3V / High	–	–	32	mA

12.4 Power Consumption

The following current consumption values are provided for information only.

Current consumption can vary according to temperature, MPU and GPU activities and customer application implementation (hardware interface uses, clock speed setup and embedded software solutions).

Table 12-4. Power Consumption

Node	Measurement	Conditions	Min	Typ	Max	Unit
5V_MAIN	Current consumption	Linux and Ethernet transfer. 5V_MAIN = 5.00V	–	115	130	mA
5V_MAIN	Current consumption	Linux in Idle[1] 5V_MAIN = 5.00V	–	90	105	mA
5V_MAIN	Current consumption	System off, all supplies off. 5V_MAIN = 5.00V	–	10	25	µA
VDDBU	Current consumption	VDDBU = 3.3V @ 25°C	–	2.43	–	µA
VDDBU	Current consumption	1.6V < VDDBU < 3.6V. All temperature ranges, all modes	1.4	–	5	µA

Note:

1. "Linux in Idle" means that Linux is loaded and that the prompt is shown on the console, waiting for instructions.

13. Mechanical Characteristics

13.1 SAM9X60D1G-I/LZB Dimensions

Figure 13-1. SAM9X60D1G-I/LZB Dimensions

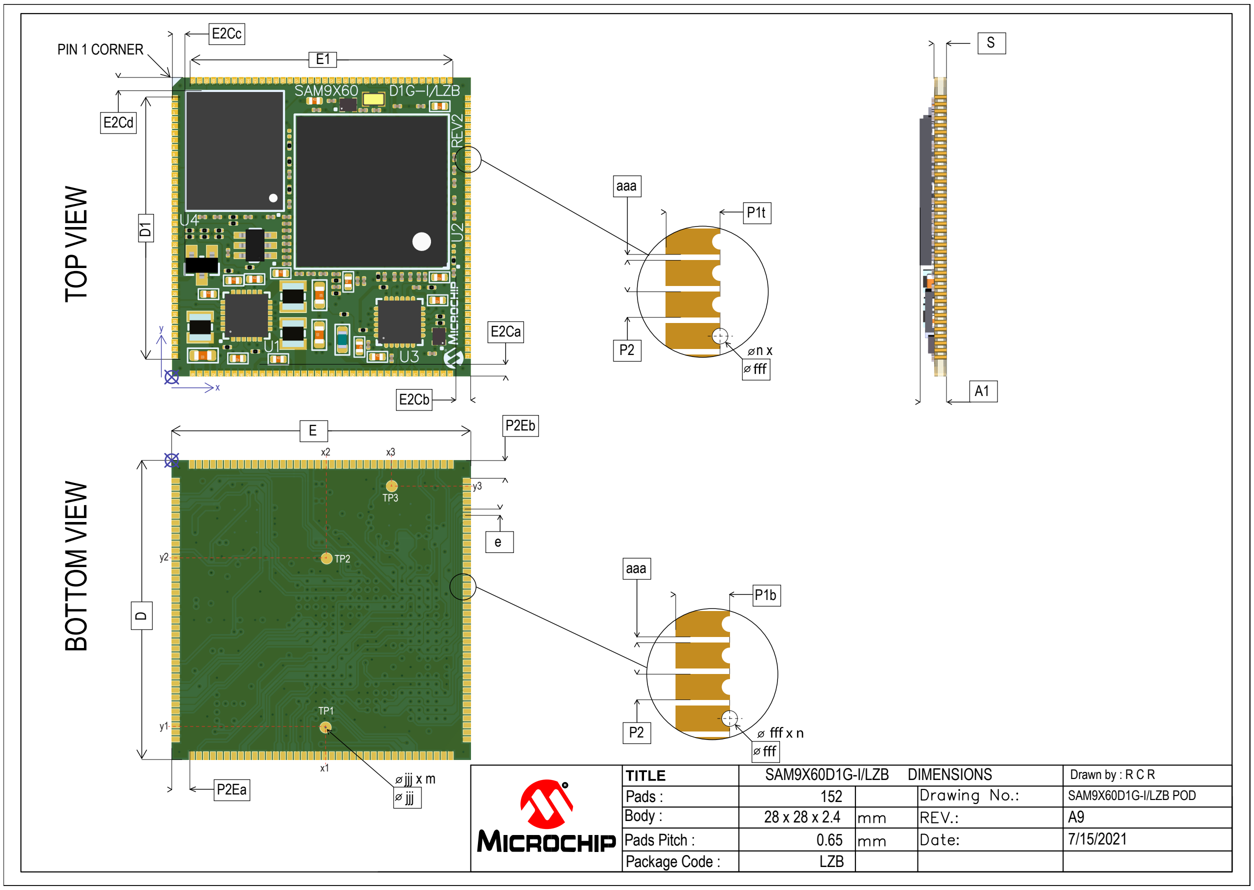


Table 13-1. SAM9X60D1G-I/LZB Dimensions (in mm)

Parameter		Symbol	Common Dimensions			Comments
			Min	Typ	Max	
Body overall dimensions	X	E	27.800	28.000	28.200	
	Y	D	27.800	28.000	28.200	
Pad pitch		e	–	0.650	–	
PCB thickness		S	1.150	1.200	1.250	
SOM total thickness		A1	–	2.400	2.450	
Pad length[1]	Top side	P1t	–	0.550	–	
	Bottom side	P1b	–	0.800	–	
Pad width[1]		P2	–	0.450	–	
Pad gap[1]		aaa	–	0.200	–	
Opening drill diameter		fff	–	0.300	–	0.300 typical minus metallization
Pad count		n	–	152	–	
Test point diameter		jjj	–	1.000	–	
Test point count		m	–	3	–	

...........continued

Parameter		Symbol	Common Dimensions			Comments
			Min	Typ	Max	
Pad edge to SOM edge[1]	X	P2Ea	–	1.750	–	
	Y	P2Eb	–	1.750	–	
SOM edge to first component edge		E2Ca	–	1.150	–	
		E2Cb	–	1.425	–	
		E2Cc	–	1.225	–	
		E2Cd	–	1.225	–	

Notes:

1. Tolerances are defined as per standards:
   - IPC A600 – Class2
   - IPC 2615
2. Test points placed under the SAM9X60D1G-I/LZB are for production purposes only. No connection to these points is allowed. To avoid any contact with the main board vias or copper areas, see the following table.

13.2 Other Characteristics

Table 13-2. SAM9X60D1G-I/LZB Weight

Parameter	Measurement	
	Value	Unit
Weight	3.6	g

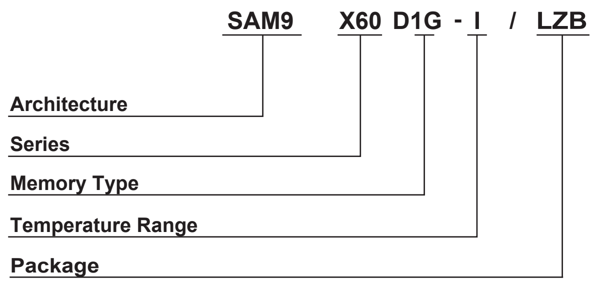
14. Ordering Information

For details on ordering codes, see Product Identification System.

Ordering Code	SiP Device Revision	DDR Memory Configuration	NAND Memory Configuration	Package	Carrier Type	Module Ambient Temperature Range
SAM9X60D1G-I/LZB	A2	1-Gbit DDR2 SDRAM	4 Gbits	152-pin 28x28 mm module	Tray	-40°C to +85°C

15. Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture:	SAM9	= ARM926EJ-S Arm Thumb microprocessor
Series:	X60	= General purpose microprocessor
Memory Type and Size	D1G	= 1-Gbit DDR2 SDRAM
Ambient Temperature Range:	I	= -40°C to +85°C (industrial)
Package:	LZB	= System-On-Module package code

Example:

- SAM9X60D1G-I/LZB = System-On-Module (SOM) based on the SAM9X60 1-Gbit SiP device

16. Revision History

16.1 DS60001747C - 01/2025

Changes
Updated Ordering Information, Figure 7-1, NAND Flash Memory, Ethernet PHY, Table 8-1
Added sections Design Resources, Particular Considerations
Corrected number of FLEXCOMs in Interfacing in I²C/TWI Mode, Interfacing in UART Mode
Corrected body overall dimensions in Table 13-1

16.2 DS60001747B - 02/2024

Changes
Introduction: updated picture.
Features: updated. Added information on package.
Reference Documents: updated.
Pinout Overview: updated pin assignment image.
Pin List: updated.
PIOA Pin List: added Note 3.
System Pin List: added notes.
SAM9X60D1G-I/LZB Power Supplies: updated table. Added note.
Power Management Unit: updated.
SAM9X60 System-in-Package (SiP): removed schematics.
MPU Clocks: removed schematics.
NAND Flash Memory: updated.
EEPROM: updated.
Ethernet PHY: updated.
SAM9X60D1G-I/LZB Land Pattern (Host Board PCB Footprint): deleted.
Assembly and Storage Information: deleted.

16.3 DS60001747A - 01/2022

Changes
First issue.

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