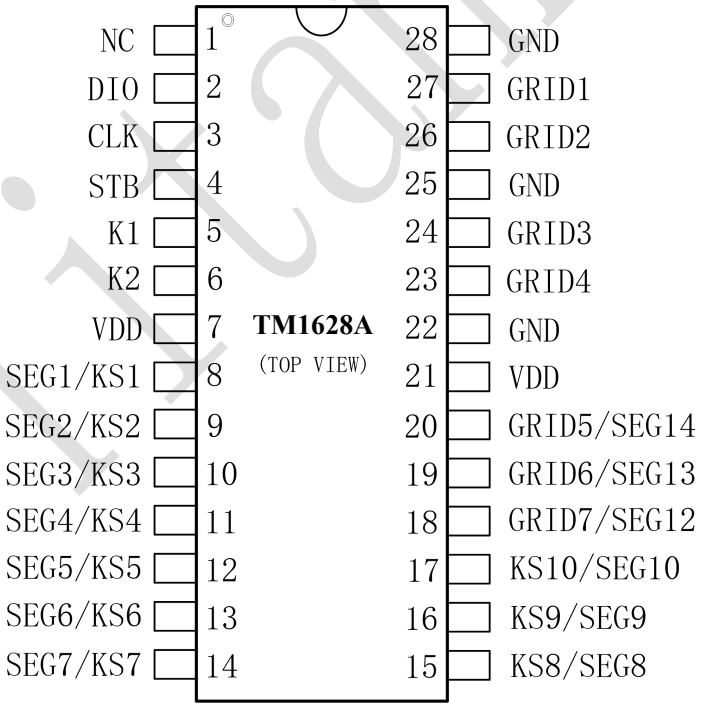
Ⅰ、Overview

TM1628A is a special circuit for LED (light-emitting diode) driver control. It integrates with different circuits such as MCU digital port, data latch, LED high-voltage drive, etc. The product has good performance and reliable quality, and is mainly applied in display drive of VCR, VCD, DVD, home theater and other similar products.

Ⅱ、 Features

- Low power consumption CMOS workmanship
- Multiple display mode(10 Segments x 7 Grids ～13 Segments x 4 Grids)
- Key Scanning (10 x 2 Matrix)
- Luminance adjustment circuit (8-level adjustable duty cycle)
- Serial port (DIO,CLK,STB)
- Oscillation mode: built-in RC oscillation
- Built-in power-on reset circuit
- Data latch circuit in internal design
- Strong anti-interference ability
- Packaging:SOP28、SSOP28

Ⅲ、 Pin definitions



Figure（1）

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Ⅳ、Pin description

Sign	I/O	Pin	Description
NC	NC	1	NC
DIO	I/O	2	Input serial data at the rising edge of clock from low bit and output serial data at the falling edge of the clock from low bit. NMOS open drain output. Built-in 13.3KΩ pull-up resistor
CLK	I	3	Reads serial data at the rising edge and outputs data at the falling edge. Built-in 13.3KΩ pull-up resistor
STB	I	4	Initialize serial interface on the rising or falling edge and wait for the command of reception. STB is set as low, the first byte is used as command, When processing command, current other processing is terminated. When STB is set as high, CLK is ignored. Built-in 13.3KΩ pull-up resistor
K1～K2	I	5～6	The data send to these pins are latched at the end of the display cycle.
SGE1/KS1～ SEG10/KS10	O	8～17	Segment output(Key scan), PMOS open drain output with a 7.2KΩ pull-down resistor
GRID1～GRID4	O	27～26 24～23	Grid output, NMOS open drain output with a 2.7KΩ pull-up resistor
SEG12/DRID7 ～ SEG14/GRID5	O	20～18	Segment/Grid multiplex output, only choose one of both.
VDD	--	7、21	Power Supply
GND	--	28、25、22	Ground system

Integrated circuit is an electrostatic sensitive device, which is easy to generate a large amount of static electricity in the dry season or dry environments. Electrostatic may damage integrated circuits. Titan Micro Electronics suggests that all preventive measures of appropriate integrated circuit shall be taken. Improper handing and welding may result is ESD damaged, or performance degradation. In addition, the chip fails to work.

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Ⅴ、Commands description

Commands are used to set display mode and state of LED driver.
The first byte input by DIO at the falling edge of STB is taken as the first command. Through decoding, take the highest two bits B7 and B6 to distinguish different commands.

B7	B6	Command
0	0	Display mode setting command
0	1	Data setting command
1	0	Display control command
1	1	Address setting command

If STB is set to high level during command or data transmission, the serial communication will be initialized, and the command or data being transmitted are invalid (previously transmitted commands or data are still valid).

(1) Display Mode Setting Commands

The command is used to set the number of the segments and bits (4~7 Grids, 10~13 Segments). When execute instructions, the display is forced off. If transmit display control command to turn on the display, the original displayed data will not be changed, However, above situation does not happen while setting same mode. When power is turned ON, the 7-grid, 10-segment default modes is selected.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display mode
0	0	Fill in 0 for the irrelevant.				0	0	4 grids 13 segments
0	0					0	1	5 grids 12 segments
0	0					1	0	6 grids 11 segments
0	0					1	1	7 grids 10 segments

(2) Data command setting

The command is used to set the writing and reading of data. B1 and B0 bit is set to 01 or 11 is not allowed.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	1	Fill in 0 for the irrelevant.				0	0	Data Reading and writing mode setting	Write data to display register
0	1					1	0		Read key scan data
0	1				0			Address mode setting	Auto increase of address
0	1				1				Fixed address
0	1			0				Test mode setting （Internal use）	Normal mode
0	1			1					Test mode

(3) Display control command setting

The command is used to set the display brightness and on/off. There are 8 levels of brightness.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
1	0	Fill in 0 for the irrelevant.			0	0	0	Extinction Number setting	Set pulse width to 1/16
1	0				0	0	1		Set pulse width to 2/16
1	0				0	1	0		Set pulse width to 4/16
1	0				0	1	1		Set pulse width to 10/16
1	0				1	0	0		Set pulse width to 11/16
1	0				1	0	1		Set pulse width to 12/16
1	0				1	1	0		Set pulse width to 13/16
1	0				1	1	1		Set pulse width to 14/16
1	0			0				Display switch setting	Display off
1	0			1					Display on

(4) Address command setting

The command is used to set the address of display register. The maximum valid address is 14 grids (C0H-CDH). When the address is set as CEH or higher, the data is ignored until a valid address is set. When powered, the default address is set as C0H.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display address
1	1	Fill in 0 for the irrelevant		0	0	0	0	C0H
1	1			0	0	0	1	C1H
1	1			0	0	1	0	C2H
1	1			0	0	1	1	C3H
1	1			0	1	0	0	C4H
1	1			0	1	0	1	C5H
1	1			0	1	1	0	C6H
1	1			0	1	1	1	C7H
1	1			1	0	0	0	C8H
1	1			1	0	0	1	C9H
1	1			1	0	1	0	CAH
1	1			1	0	1	1	CBH
1	1			1	1	0	0	CCH
1	1			1	1	0	1	CDH

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Ⅵ、 Display register address

The register stores data that is transmitted to TM1628A from external device through serial interface, there are total 14 bytes locations from address C0H-CDH, which correspond with the LED lamps connected with the pins of chip SGE and GRID respectively. Distribution is shown as following chart.

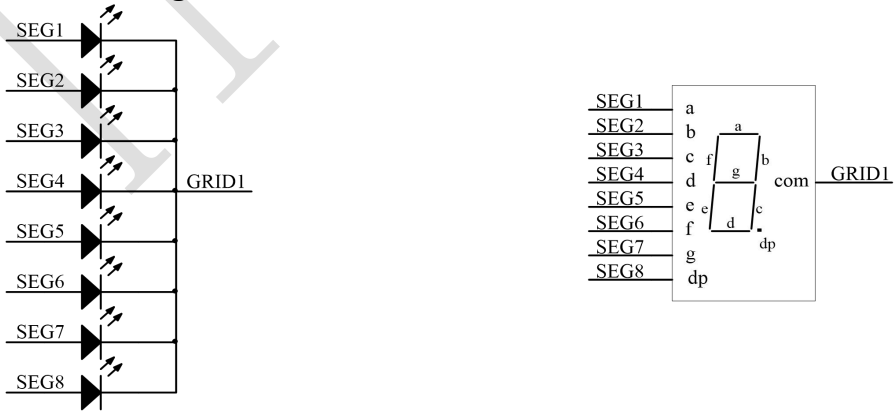
When writing LED display data, operation according to display address from low to high and data byte from low bit to high bit.

SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	X	SEG12	SEG13	SEG14	X	X	
xxHL(four low bits)				xxHU(four high bits)				xxHL(four low bits)				xxHU(four high bits)				
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
00HL				00HU				01HL				01HU				GRID1
02HL				02HU				03HL				03HU				GRID2
04HL				04HU				05HL				05HU				GRID3
06HL				06HU				07HL				07HU				GRID4
08HL				08HU				09HL				09HU				GRID5
0AHL				0AHU				0BHL				0BHU				GRID6
0CHL				0CHU				0DHL				0DHU				GRID7

▲**Note**: Maybe the display random when power on, Suggest to send 14 bytes of 0x00 to the display register address(C0H-CDH) before send the display on command.

Ⅶ、 Display

(1) Drive common cathode digital tube



Figure（2）

The figure（2）shows the connection diagram of common cathode digital tube, to make the digital tube display “0”, need to write data 0x3FH in C0H（GRID1） address unit from low bit to high bit. the detail address table shown as below：

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	1	1	1	1	1	1	**GRID1(C0H)**
B7	B6	B5	B4	B3	B2	B1	B0	

(2) Drive common anode digital tube

Figure（3）

The figure 3 shows the connection diagram of common anode digital tube, to make the digital tube display "0", need to write data 01H to address unit C0H(GRID1)、C2H(GRID2)、C4H(GRID3)、C6H(GRID4)、C8H(GRID5)and CAH(GRID6) , and write data 00H to other address unit(CCH/GRID7), the detail address table shown as below:

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	0	0	0	0	0	1	**GRID1(C0H)**
0	0	0	0	0	0	0	1	**GRID2(C2H)**
0	0	0	0	0	0	0	1	**GRID3(C4H)**
0	0	0	0	0	0	0	1	**GRID4(C6H)**
0	0	0	0	0	0	0	1	**GRID5(C8H)**
0	0	0	0	0	0	0	1	**GRID6(CAH)**
0	0	0	0	0	0	0	0	**GRID7(CCH)**
B7	B6	B5	B4	B3	B2	B1	B0	

▲ **Note**: When use them, SEG can be connect with LED anode only, and GRID for cathode only. Reversed connection is not allowed.

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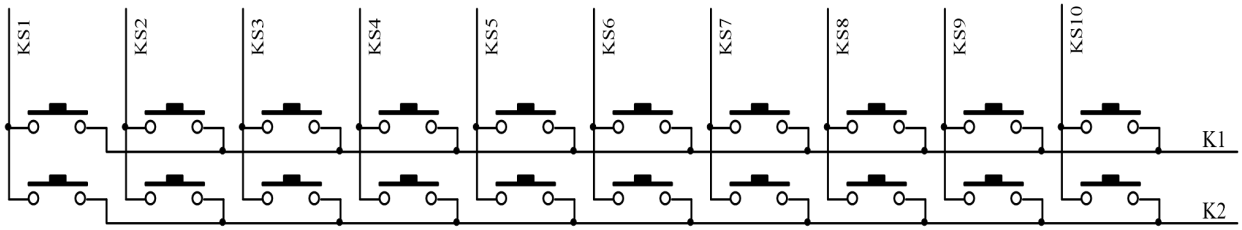
Ⅷ、 Keyboard scan and data register

Keyboard scan matrix is 10×2bit，as follows：



Figure（4）

The storage address of keyboard scan is shown as following chart, after send the reading key command, start reading Byte 1~ Byte 5 of key data which output from low bit. B6 and B7 are invalid bits which output is 0 at this time. When press the keys correspond with the pins of chip K and KS, corresponding bit within the byte is 1.

B0	B1	B2	B3	B4	B5	B6	B7	
K1	K2	X	K1	K2	X	X	X	
KS1			KS2			0	0	**BYTE1**
KS3			KS4			0	0	**BYTE2**
KS5			KS6			0	0	**BYTE3**
KS7			KS8			0	0	**BYTE4**
KS9			KS10			0	0	**BYTE5**

▲ **Note:** 1. TM1628A read 5 bytes maximum, more reading is not allowed.

2. Data byte can be read only from Byte 1~ Byte 5 in sequence, it can not be read across the byte. For example, when press the key correspond with the K2 and KS10, if need read data of this key, must read till the fifth bit of Byte 5.

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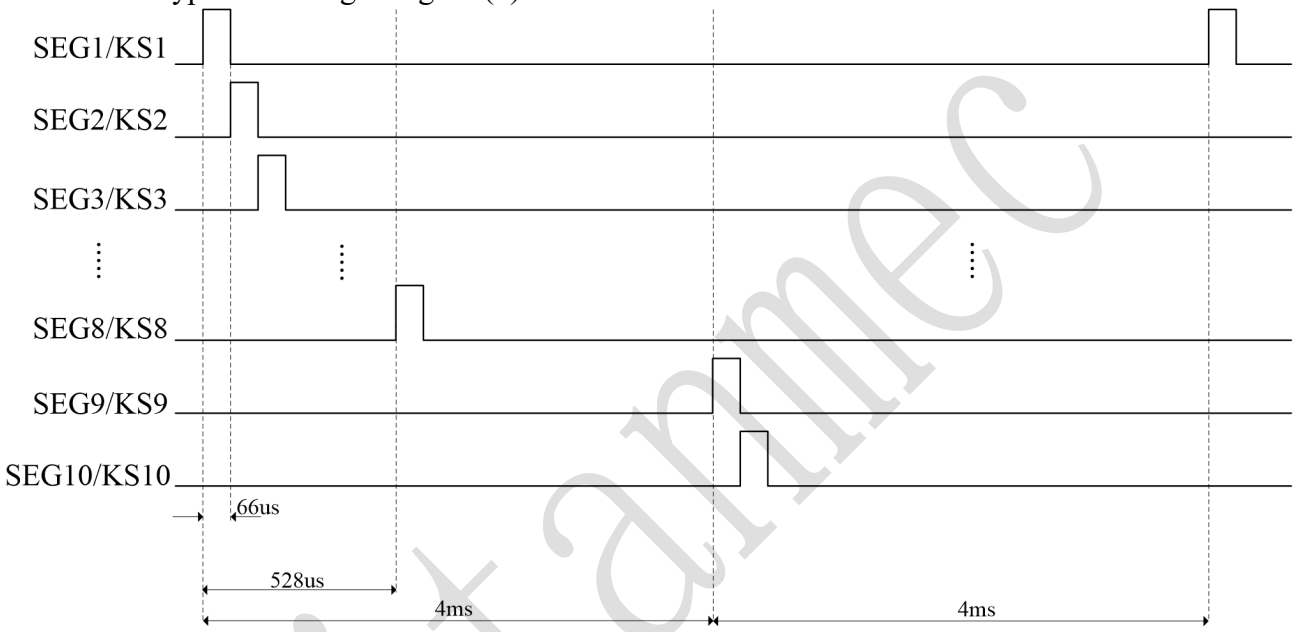
Ⅸ、Keyboard

(1) Keyboard scan

Keyboard scanning is automatically done by TM1628A without user control. Users only need to read key codes according to time sequence. It takes two display cycle to complete one time keypad scanning, a display cycle takes about T=4ms. During this 8ms, if two different keys are pressed, the key code read in both times is the one of the key pressed first. At 7Grids11Segs mode, the SEG1/KS1～SEG10/KS10 waveform of keypad scanning as figure (5):



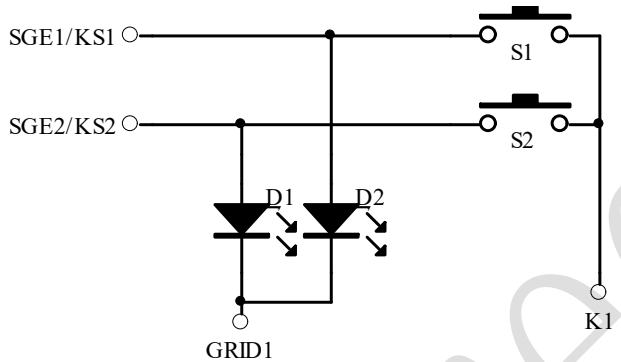
Figure（5）

As the figure (5), the principle of chip keyboard scanning as below:
Scanning start from SEG1/KS1 to SEG10/KS10, SEG1/KS1-SEG8/KS8 finish at the same cycle and SEG9/KS9-SEG10/KS10 at the next cycle. When send the reading key command, if the key scanning high level of the SEG1/KS1-SEG10/KS10 input to the K1/K2/K3 by pressing the keyboard, the chip will output high level data at the corresponding bit.

▲**Note:** Display cycle is related on the oscillation frequency of IC, the oscillation frequency is not exactly the same, please to respect the actual measurement.

(2) Combination keys

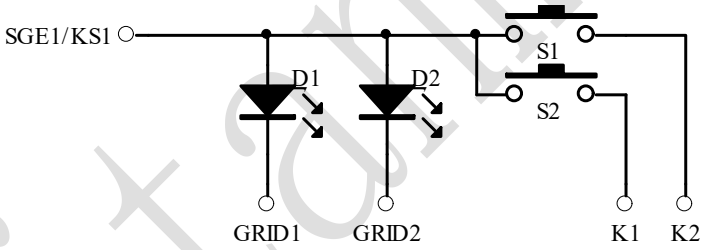
Unusual problems with combination keys: SEG1/KS1-SEG10/KS10 are for combined use for display and key scanning. Take figure (6) for example, to turn D1 on and D2 off, we have make sure SEG1 is in the status of "0"and SEG2 is in the status of "1". If S1 and S2 are pressed simultaneously, it is to the effect that SEG1 and SEG2 are short-circuited, and then D1 and D2 are turn on.



Figure（6）

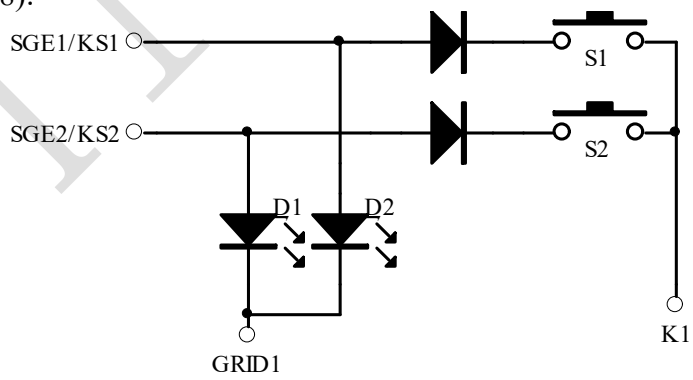
Solution:

1. In terms of hardware, it is advisable to arrange the keys to be pressed at the same time on different K line, as figure (7):



Figure（7）

2. Series diodes as figure (8):



Figure（8）

▲**Note:** It is recommend to use combination keys on the same KS but different K pin.

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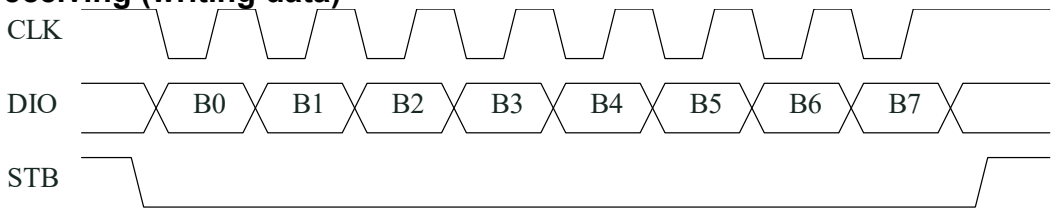
X、Serial data transmission format

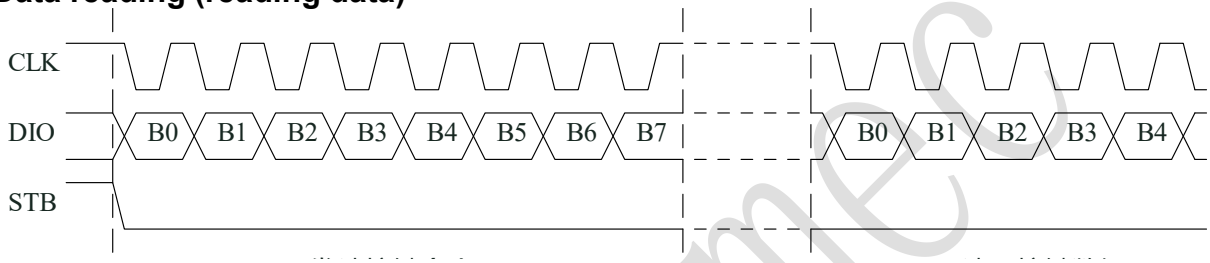
The operation of reading and receiving 1 Bit is on the clock rising edge.

Data receiving (writing data)



Figure（9）

Data reading (reading data)



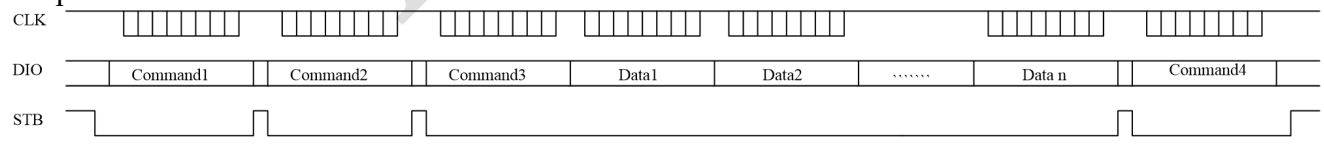
Figure（10）

▲ **Note**: When reading data, it takes a waiting time Twait (minimum 2us) from instruction setting at the eighth rising edge of CLK to data reading at falling edge of the CLK. See the Time Characteristics table for specific parameters.

XI、 Transmission of serial data in application

(1) Address increase mode

In the address auto +1 mode, to set an address actually means to set the initial address stored in the transferred data flow. When the initial address command is completely sent, send the data (14 bytes at most) immediately without having to set "STB" to high level, and only do it when data sending completes.

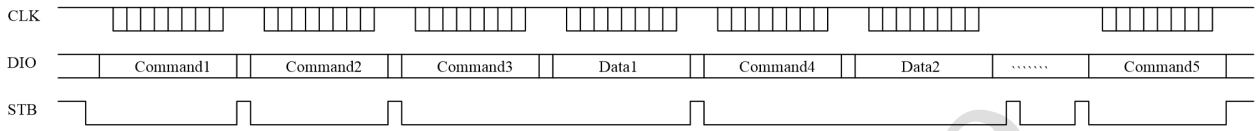


Figure（11）

Command1: display mode setting command
Command2: data setting command
Command3: display address setting command
Data1~ n: Transmit display data or content to command3 address and following address (no more than 14 bytes)
Command4: display control setting command

(2) Fixed address mode

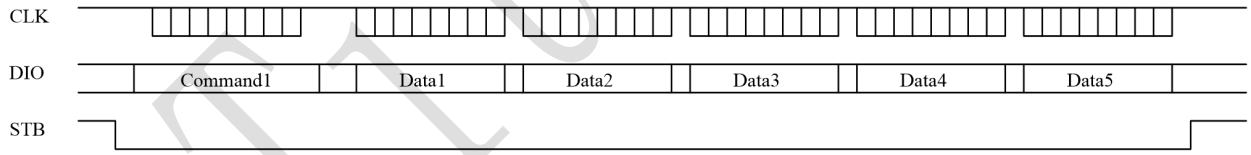
In the fixed address mode, to set the address actually means to set the address stored in the to-be-transferred 1 byte data. When the address is sent completely, send the 1 byte data immediately without having to set "STB" to high level (only do it when data sending completes); then, set the address to be stored in the second data, and when the data (14 bytes at most) sending completes, set “STB” to high level.



Figure（12）

Command1: display mode setting command
Command2: data setting command
Command3: display address setting command
Data1: send the first display data to the Command3 address
Command4: second display address setting command
Data2: send the second display data to the Command3 address
……
Command5: display control setting command

(3) Read time sequence of the key



Figure（13）

Command1: Set display mode
Data1～5: Read key data

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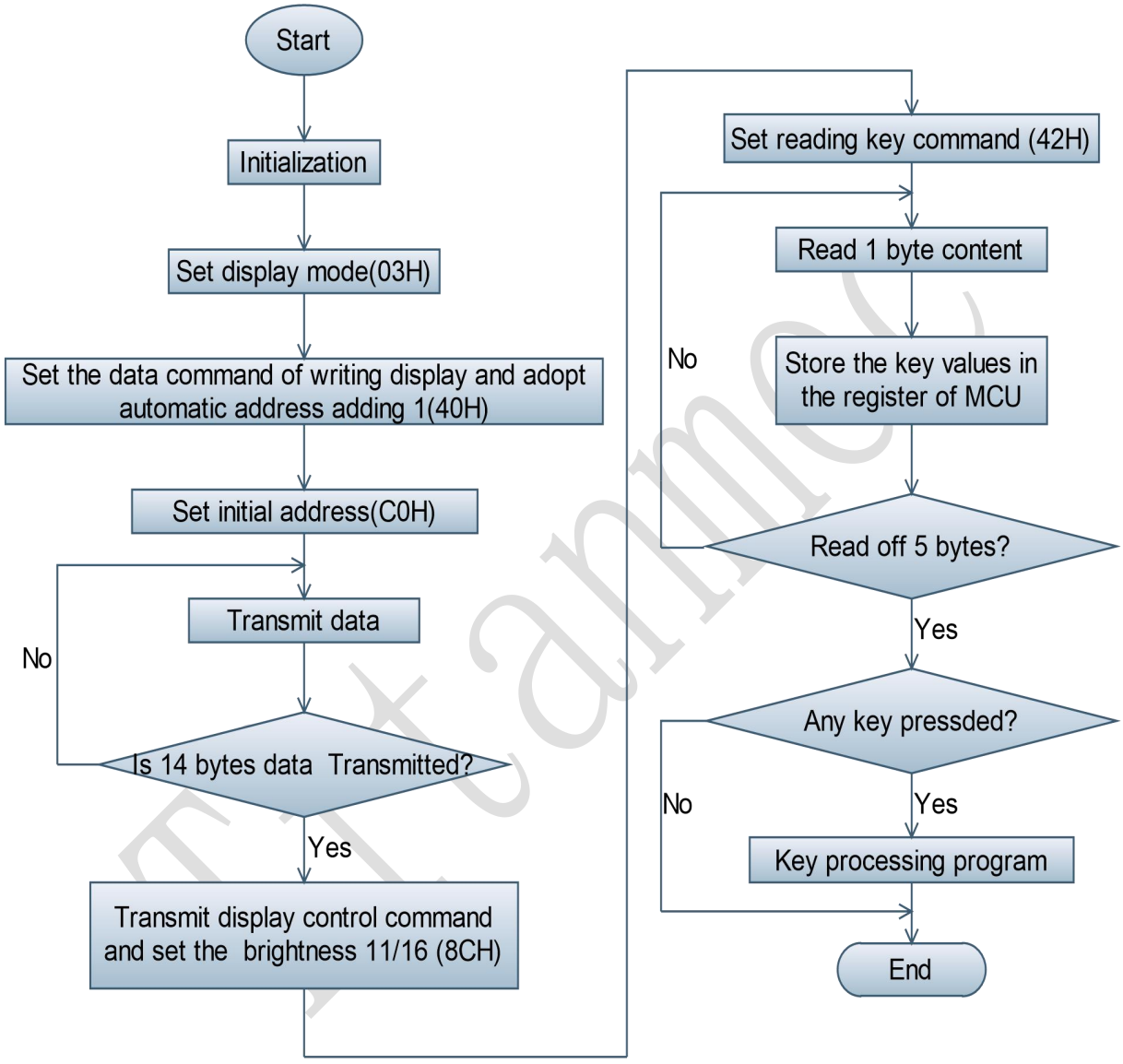
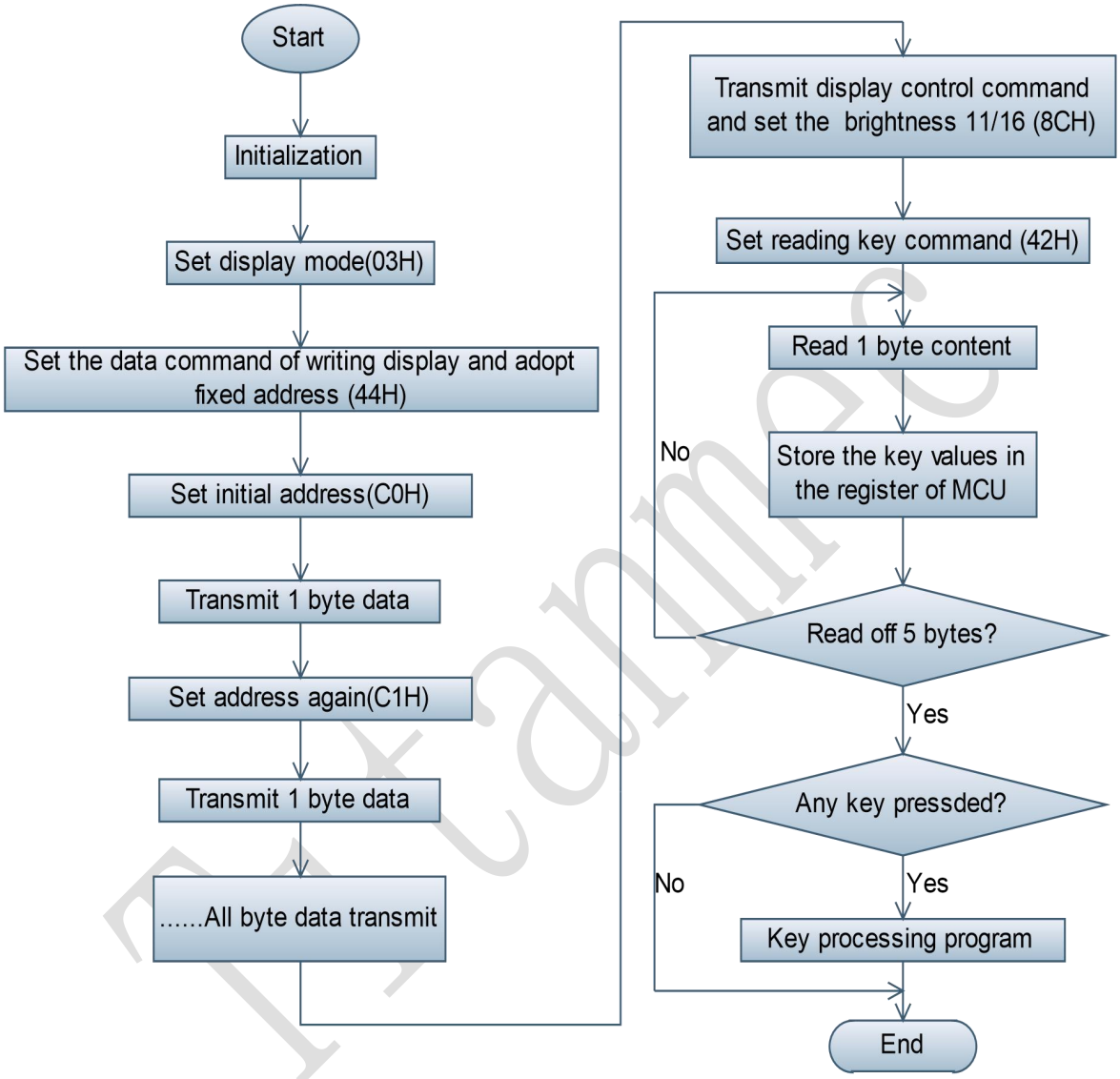
Program flow chart

(1) The program flow chart adopts the mode of automatic address adding 1:



Figure（14）

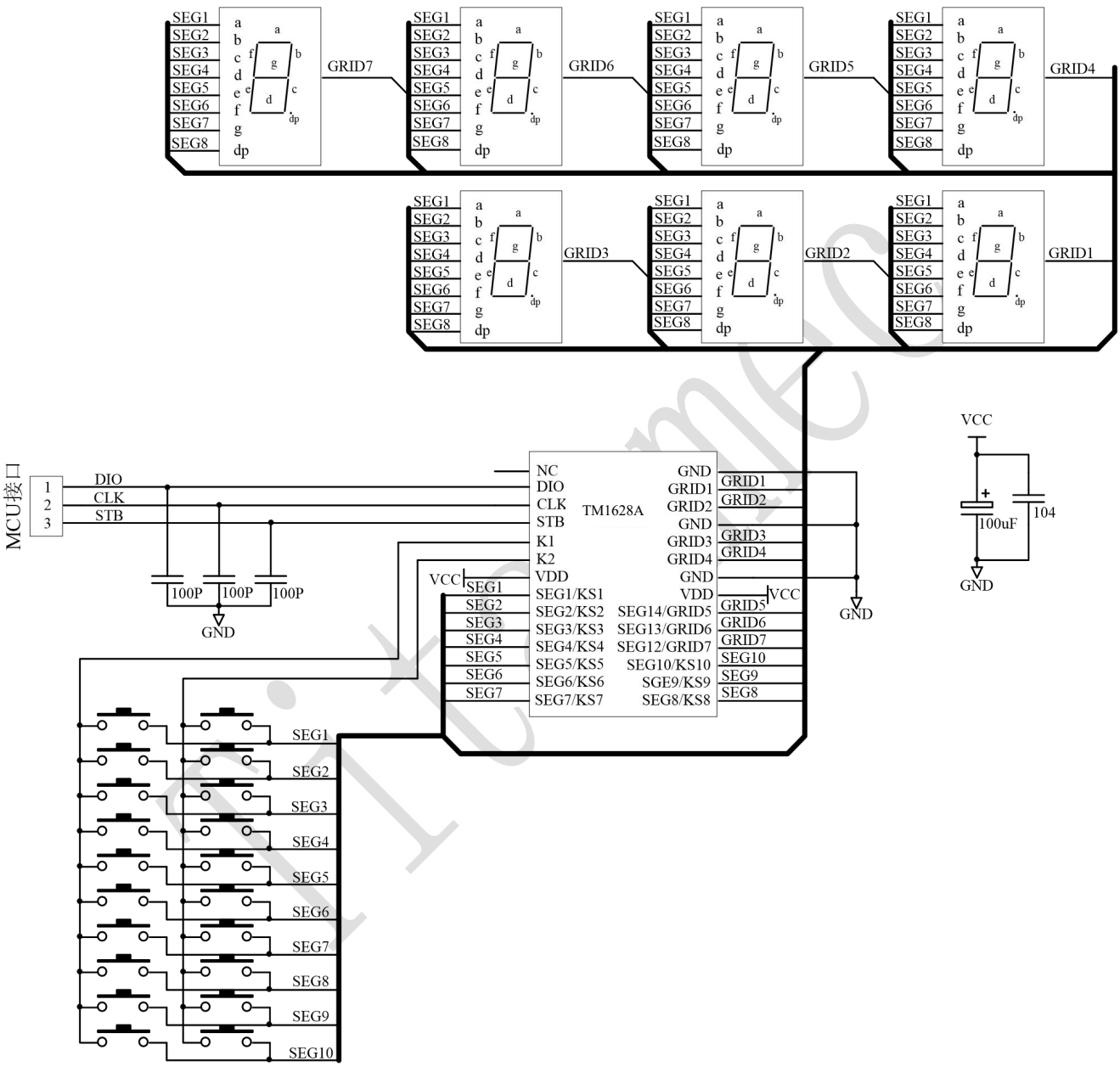
(2)The program chart adopt fixed address mode：



Figure（15）

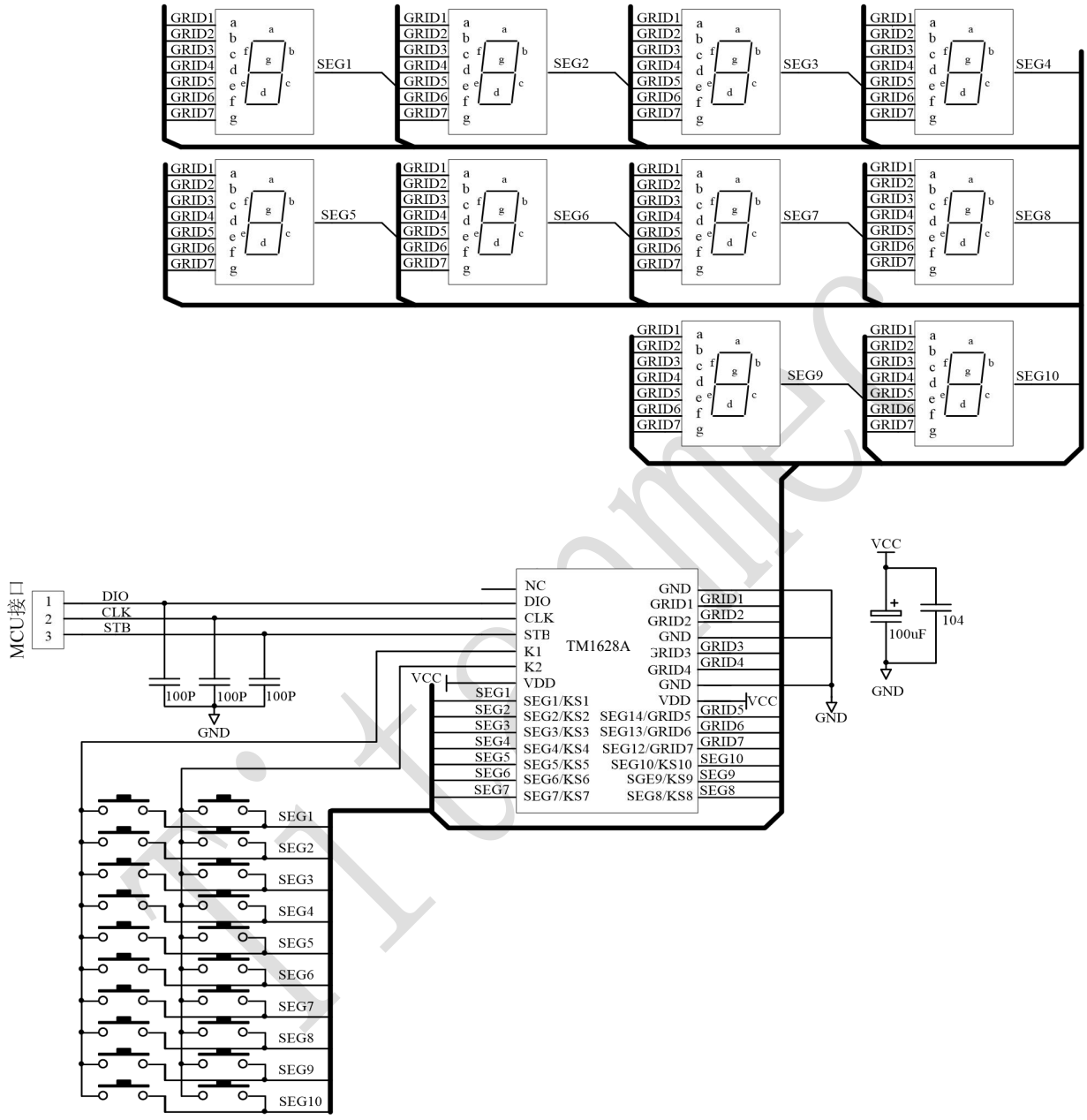
XII、Application circuit

Connecting circuit of TM1628A drive common cathode digital tube is shown as below:



Figure（16）

Connecting circuit of TM1628A drive common anode digital tube is shown as below:



Figure（17）

▲Note:

1. The wiring of the filter capacitor between VDD and GND on PCB should be close to the chip of TM1628A to enhance filtering effect.
2. The three 100pF capacitors connecting to DIO, CLK and STB communication ports can reduce interferences to such ports.
3. Since the conduction pressure drop of blue or white light digital tube is 3V, the power supply of TM1628A is 5V.

XIII、 Electrical parameters

Limit parameters（Ta = 25℃, Vss = 0V）

Parameter	Sign	Range	Unit
Logic supply voltage	VDD	-0.5 ～+7.0	V
Logic input voltage	VI1	-0.5 ～ VDD + 0.5	V
LED SEG driver output current	IO1	-50	mA
LED GRID driver output current	IO2	+200	mA
Power consumption	PD	400	mW
Operating temperature	Topt	-40 ～ +85	℃
Storage temperature	Tstg	-65 ～+150	℃

▲Note:

(1) For these levels in the above table, it may cause permanent damage to the device and reduce device reliability under the condition of prolonged using of the chip. We do not suggest that chips operate beyond these limit parameters under any other conditions.

(2) All voltage values are tested systematically.

normal operating range（Vss = 0V）

Parameter	Sign	Min.	Typical	Max.	Unit	Testing condition
Logic supply voltage	VDD		5		V	-
High level input voltage	VIH	0.7 VDD	-	VDD	V	-
Low level input voltage	VIL	0	-	0.3 VDD	V	-

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Electrical characteristics (VDD = 5V, V_{SS} = 0V)

Parameter	Sign	Min.	Typical	Max.	Unit	Testing condition
High level output current	Ioh1	20	35	60	mA	SEG1～SEG10, Vo = VDD -3V
Low level input current	I_{OL}	80	120	-	mA	GRID1～GRID7 Vo=0.3V
Low level output current	Idout	3	-	-	mA	Vo = 0.4V, Dout
High level output current tolerance	Itolsg	-	-	5	%	Vo = VDD - 3V, SEG1～SEG10
High level input voltage	VIH	0.7 VDD	-		V	CLK, DIO, STB
Low level input voltage	VIL	-	-	0.3 VDD	V	CLK, DIO, STB

Switching characteristics (VDD = 5V)

Parameter	Sign	Min.	Typical	Max.	Unit	Testing condition	
Transmission delay time	t_{PLZ}	-	-	300	ns	CLK → DOUT	
	t_{PZL}	-	-	100	ns	CL = 15pF, RL = 10K Ω	
Rising time	t_{TZH} 1	-	-	2	μs	CL = 300pF	SEG1～SEG10
	t_{TZH} 2	-	-	0.5	μs		GRID1～GRID4 SEG12/GRID7～SEG14/GRID5
Falling time	t_{THZ}	-	-	1.5	μs	CL = 300pF, SEGn, GRIDn	
Maximum clock frequency	Fmax	-	-	1	MHz	Duty cycle 50%	
Input capacitance	CI	-	-	15	pF	-	

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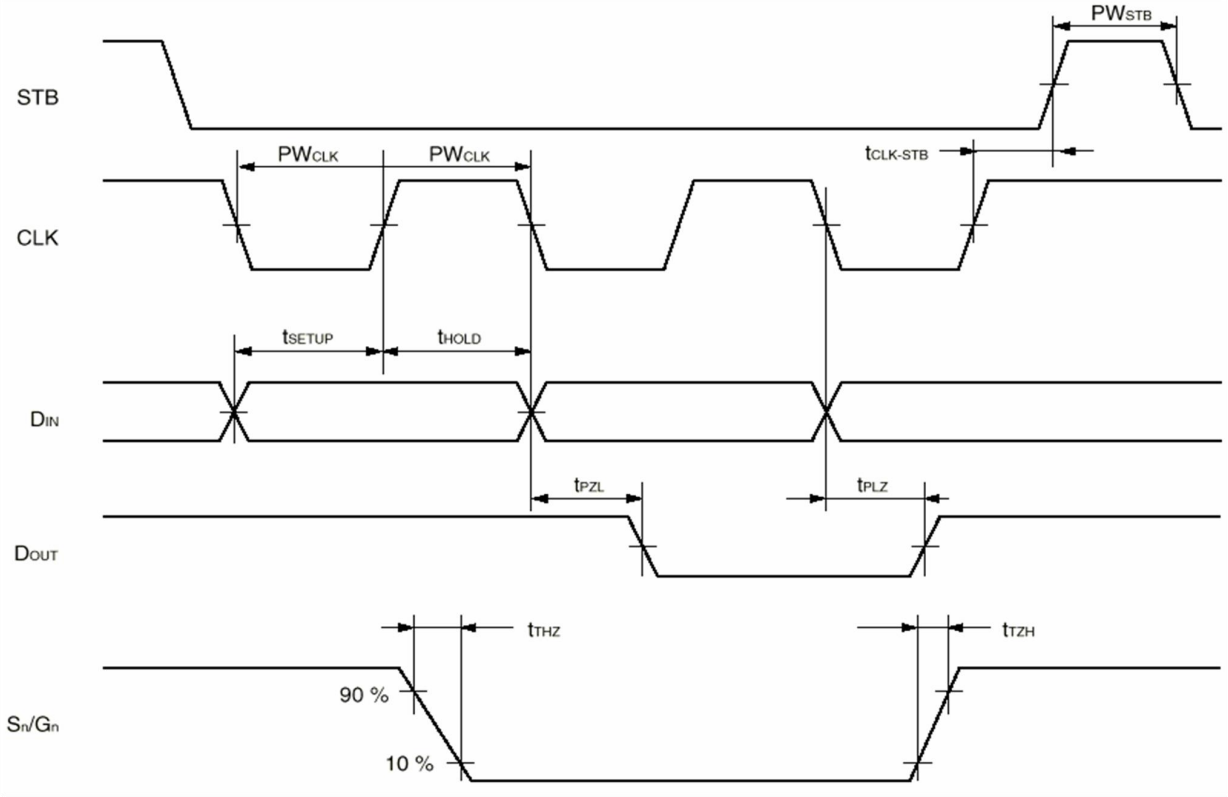
Timing characteristics（VDD = 5V）

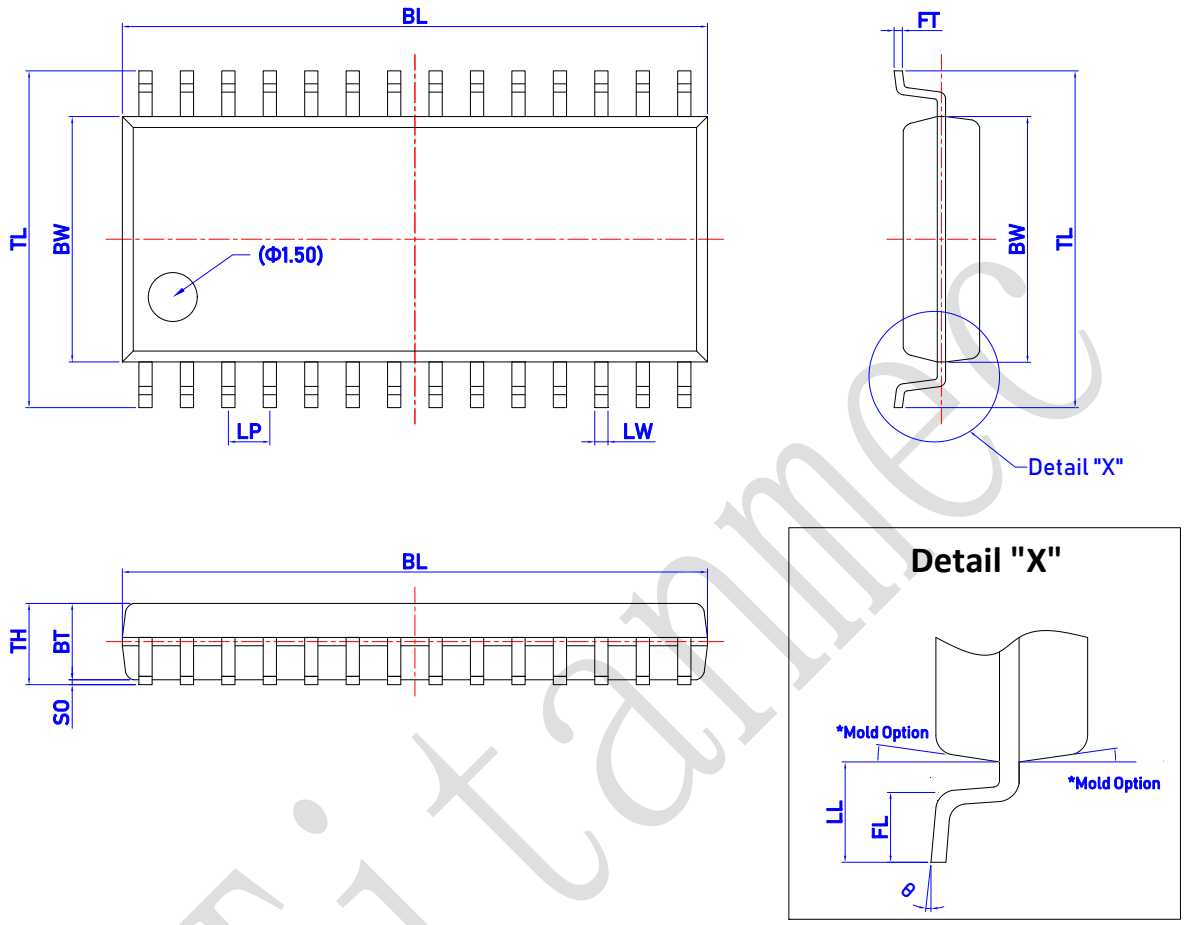
Parameter	Sign	Min.	Typical	Max.	Unit	Testing condition
Clock pulse width	PW_{CLK}	500	-	-	ns	-
Gating Pulse width	PW_{STB}	1	-	-	μs	-
Data setup time	t_{SETUP}	100	-	-	ns	-
Data hold time	t_{HOLD}	100	-	-	ns	-
CLK →STB time	$t_{CLK-STB}$	1	-	-	μs	CLK↑→STB↑

Timing waveform



Figure（18）

XIV、IC packing size (SOP28-300)



Dimensions

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
表示	总长	胶体宽度	跨度	脚宽	脚间距	脚厚	胶体厚度	站高	胶体高度	单边长	脚长	脚角度
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	?
Spec	18.03 (17.93) 17.83	7.62 (7.52) 7.42	10.56 (10.37) 10.21	0.406 TYP	1.270 TYP	0.300 (0.250) 0.200	2.44 (2.34) 2.24	0.250 (0.150) 0.100	2.590 Max.	1.50 (1.40) 1.30	0.90 (0.80) 0.70	8 (4) 0

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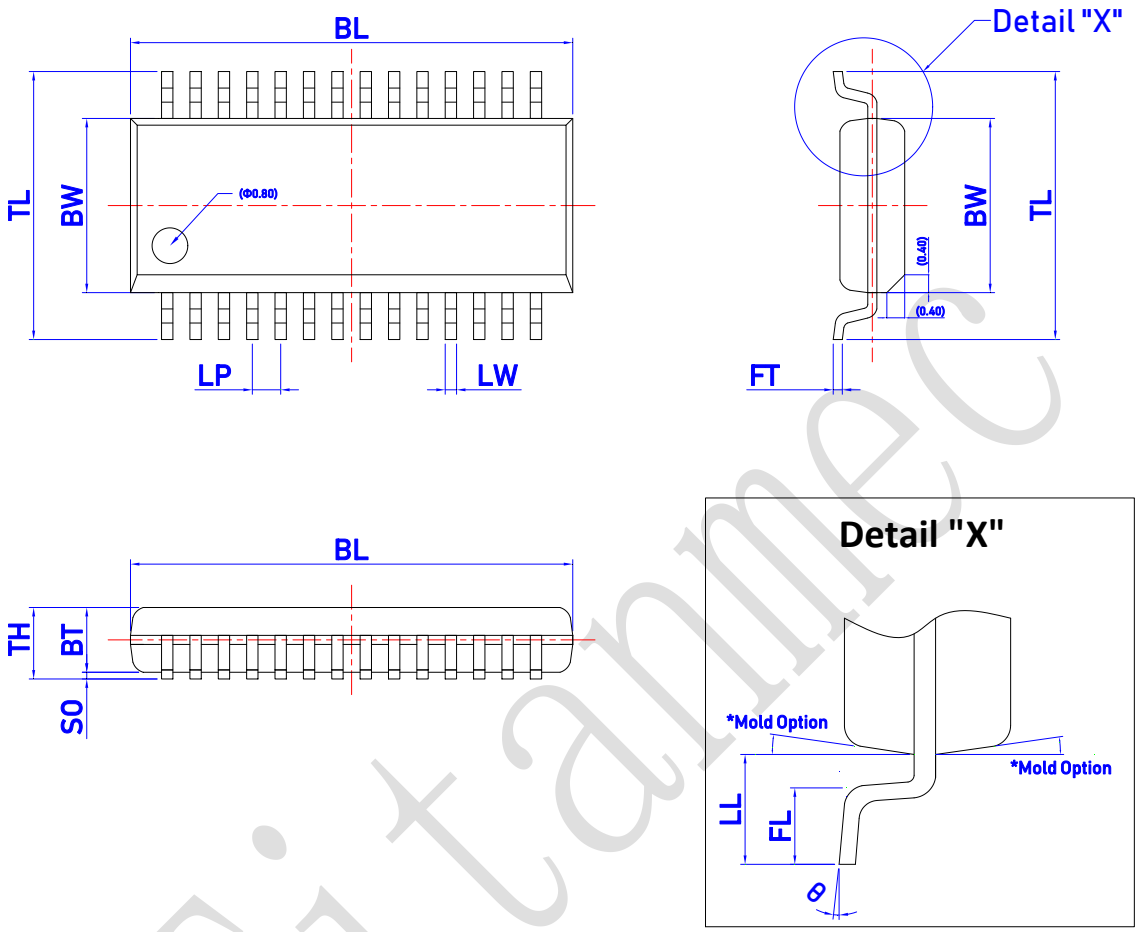
IC packing size (SSOP28-150)



Dimensions

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
表示	总长	胶体宽度	跨度	脚宽	脚间距	脚厚	胶体厚度	站高	胶体高度	单边长	脚长	脚角度
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	?
Spec	10.00 (9.90) 9.80	4.00 (3.90) 3.80	6.20 (6.00) 5.80	0.254 TYP	0.635 TYP	0.250 (0.200) 0.150	1.55 (1.45) 1.25	0.200 (0.150) 0.100	1.650 Max.	1.20 (1.10) 1.00	0.80 (0.60) 0.45	8 (4) 0

All specs and applications shown above subject to change without prior notice.

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