SAM9X75-Curiosity

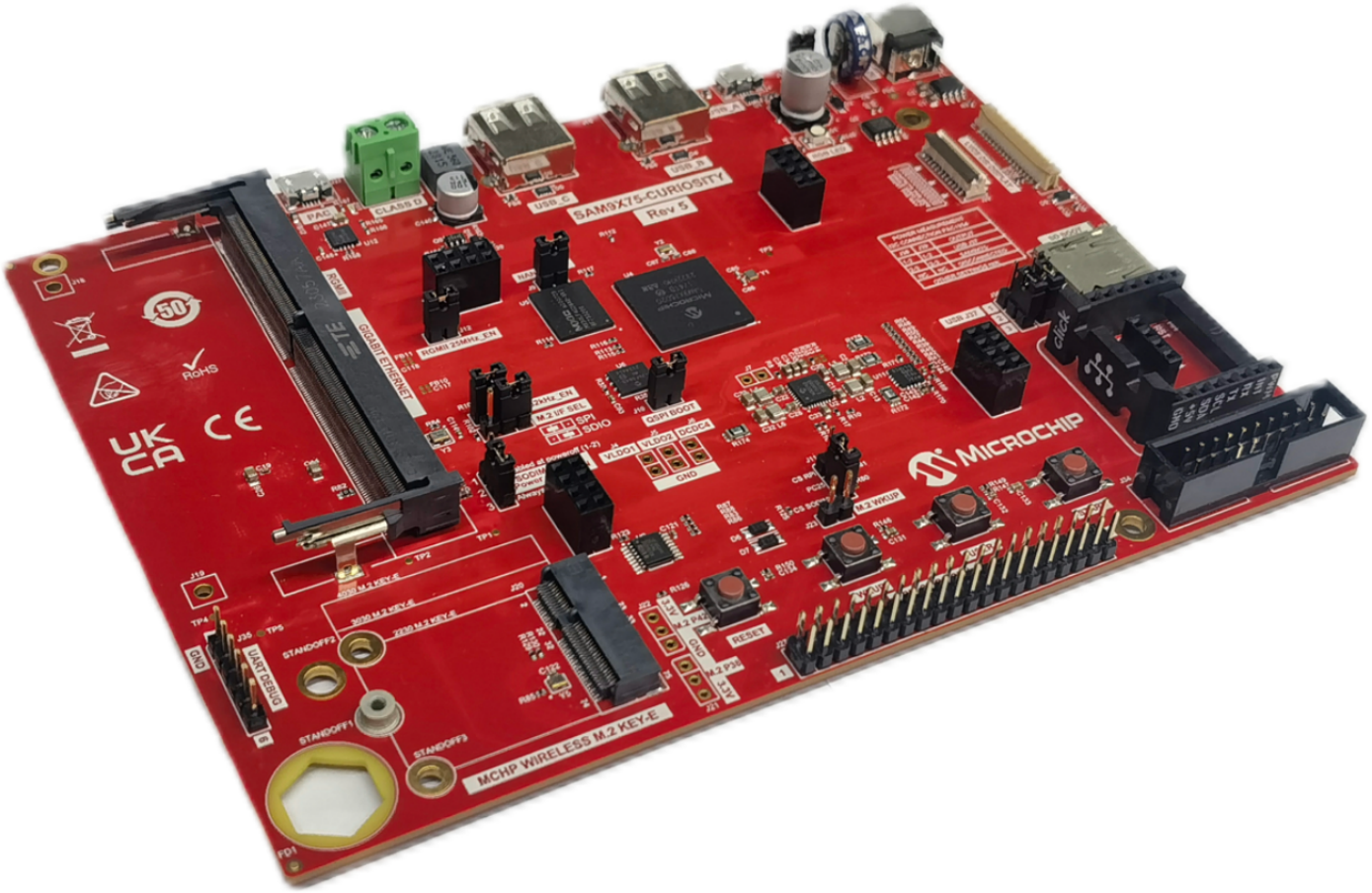
User Guide

Product Page Links

Scope

This user guide introduces the SAM9X75-Curiosity board and describes the development and debugging capabilities running on SAM9 Arm®-based embedded MPUs. The board features a SAM9X75D2G MPU and is the evaluation platform for the SAM9X7 Series MPU devices.

Figure 1. SAM9X75-Curiosity Overview



1. Introduction

1.1. Document Layout

The document is organized as follows:

- Introduction
- Product Overview – Important information about the SAM9X75-Curiosity board
- Function Blocks – Specifications of the SAM9X75-Curiosity and high-level description of the major components and interfaces
- Installation and Operation – Instructions on how to get started with the SAM9X75-Curiosity board
- Errata
- Appendix. Schematics and Layouts – SAM9X75-Curiosity schematics and layout diagrams

1.2. Recommended Reading

The following Microchip documents are available on www.microchip.com and are recommended as supplemental reference resources:

- SAM9X7 Series Data Sheet. Lit. Number DS60001813
- SAM9X7 Series Silicon Errata and Data Sheet Clarifications. Lit. Number DS80001082
- SAM9X75 SiP Data Sheet. Lit. Number DS60001827

2. Product Overview

To simplify your design, Microchip offers a complete embedded solution. The SAM9X75-Curiosity board delivers the needed performance, from power management and timing to storage and communication interfacing. SAM9X75-Curiosity follows the Microchip MPU strategy for versatile evaluation kits, showcasing all the features that the SAM9X75D2G MPU can offer. This differentiated offering allows designers to immediately focus on delivering their design.

2.1. SAM9X75-Curiosity Features

Table 2-1. SAM9X75-Curiosity Features

Characteristic	Specification	Featured Components
Processor	243-ball TFBGA, 16x16mm body, pitch 0.8mm	Microchip SAM9X75D2G-I/4TB
External clock	24 MHz oscillator MEMS 32.768 kHz crystal 125 MHz reference clock generator for GMAC 25 MHz clock generator for ETH PHY 32.768 kHz clock generator for wireless M.2 Key E	ABM11AIG-24.000MHZ-4Z-T3 FC-12M 32.7680KA-A3 Microchip DSC1502MI2A-125M0000 Microchip VC-840-EAE-KAAN-25M0000000 ASAK-32.768KHZ-LRS-T
Memory	2 Gb DDR3L One 4 Gb NAND Flash One 64 Mb QSPI NOR Flash	Internal memory Macronix MX30LF4G28AD-XKI Microchip SST26VF064BEUIT-104I/MF
SD/MMC	One microSD card interface One M.2 Key E connector/radio module interface	– –
USB	One Micro-B USB device Two USB Type-A connectors	– Microchip MIC2026-1YM
Ethernet	One Gigabit Ethernet interface through SODIMM 260-pin connector	–
Audio	Mono single CLASS D amplifier	–
CAN	Through mikroBUS™ connector	MIKROE-2299 (Microchip MCP2542WFD, not included in the box)
Video	One LVDS connector One MIPI camera connector	– –
Debug port	One UART debug connector One JTAG interface	– –
Board monitor	One RGB (Red, Green, Blue) LED Four push button switches	– –
Expansion	Raspberry Pi® 40-pin GPIO connector(1) One mikroBUS connector with PTA	– Hundreds of possible Click™ extensions featuring Microchip functions inside
Power measurement	Current sense	Microchip PAC1934T-I/JQ
Power management	Power supply unit	Microchip MCP16502TAB-E/S8B
Board supply	System $5V_{DC}$ from jack or USB A	–

Note:

1. Raspberry Pi is a trademark of Raspberry Pi Trading.

2.2. Evaluation Kit Specifications

Table 2-2. Evaluation Kit Specifications

Characteristic	Specification
Board identification	SAM9X75-Curiosity
Board supply voltage	Jack or USB powered
Temperature	Operating: 0°C to +70°C
Relative humidity	0 to 90% (non-condensing)
Main board dimensions	165 mm x 120 mm
RoHS status	RoHS 3 compliant
China RoHS status	EFUP50
REACH Status	REACH compliant

2.3. Power Sources

Two options are available to power up the SAM9X75-Curiosity board:

- Powering through the jack connector (J1)
- Powering through the USB Micro-B connector on the USBA port (J2)

The selection of the input supply is automatic with a priority given to the jack connector.

Table 2-3. Electrical Characteristics

Characteristic	Specification
Input voltage	5 V_{DC}
Maximum input voltage (limits)	6 V_{DC}
Input current	Up to 6 A when using DC jack Up to 500 mA when using USB

CAUTION The SAM9X75-Curiosity board runs at a 3.3V voltage level logic. The maximum voltage that the I/O pins can tolerate is 3.3V. Providing higher voltages (e.g., 5V) to an I/O pin could damage the board.

2.4. Connectors on Board

The fully featured SAM9X75-Curiosity board integrates multiple peripherals and interface connectors, as shown in the following figure.

Figure 2-1. SAM9X75-Curiosity Top Board Interface Connectors

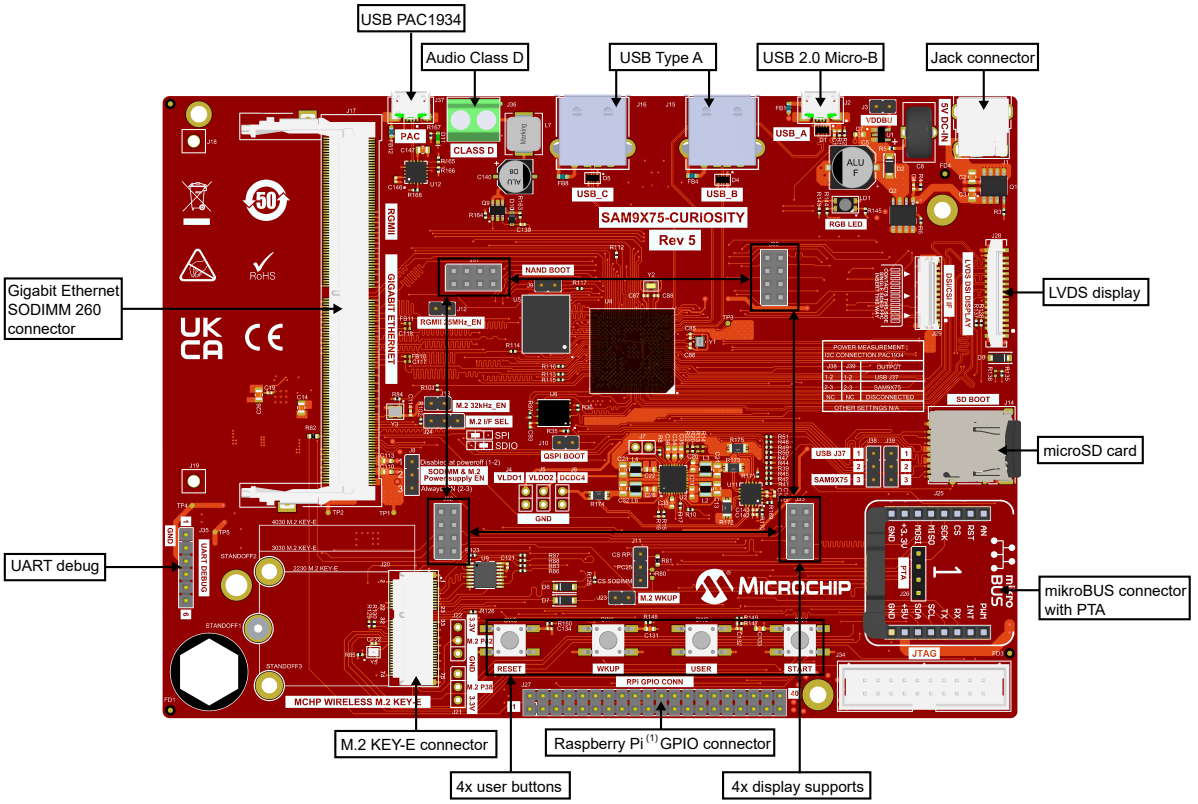


Table 2-4. SAM9X75-Curiosity Top Board Interface Connectors

Connector	Interfaces to
J1	DC jack (internal 2.1mm, external 5.5mm) connector, positive terminal on central pin
J2	USB 2.0 Micro-B (USB-A)
J14	microSD card connector
J15	USB Type-A (USB-B)
J16	USB Type-A (USB-C)
J17	Gigabit Ethernet SODIMM 260-pin connector
J20	M.2 KEY-E connector for radio modules interface
J25 and J26	mikroBUS with PTA connector
J27	Raspberry Pi(1) GPIO connector
J29	MIPI connector
J28	LVDS connector
J30, J31, J32 and J33	Display module support
J34	JTAG connector
J35	FTDI connector (UART debugger)
J36	Audio Class D connector
J37	USB Micro-B PAC1934 power measure connector

Note:

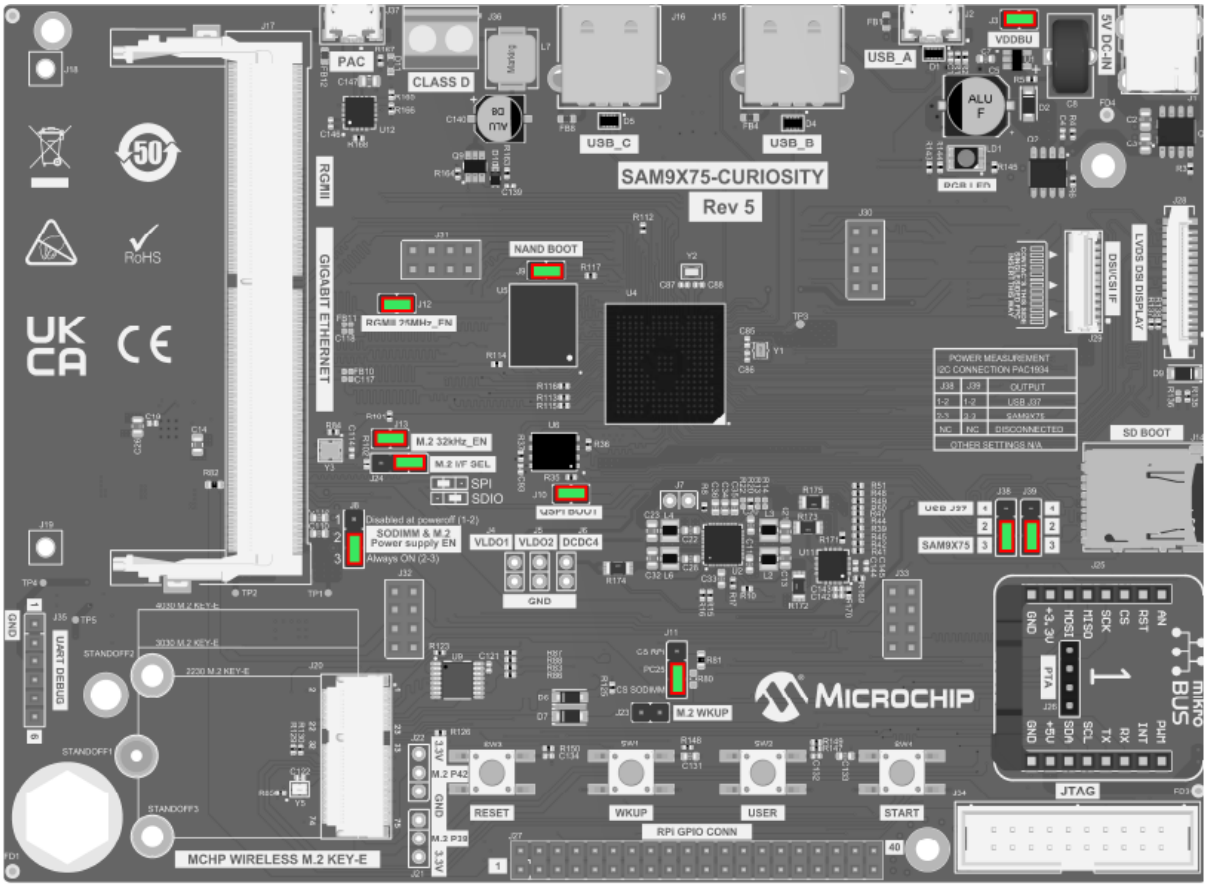
1. Raspberry Pi is a trademark of Raspberry Pi Trading.

2.5. Default Jumper Settings

Table 2-5. SAM9X75D2G Default Jumper Settings

Header	Default Setting	Function
J3	Closed	VDDBU current measurement
J8	2-3 (always on)	Enable extra 3.3V and 2.5V power supply: • 1-2 Enable with VDD_3V3 • 2-3 Enable with 5V_MAIN
J9	Closed	NAND boot: • Open: disabled • Closed: enabled
J10	Closed	QSPI CS: • Open: disabled • Closed: enabled
J11	2-3 (CS SODIMM)	SODIMM/RPi CS: • 1-2: RPi SPI CS selected • 2-3: SODIMM SPI CS selected
J12	Closed	25 MHz (Gigabit Ethernet J17): • Open: disabled • Closed: enabled
J13	Closed	32.768 kHz (M.2 KEY E connector J20) • Open: disabled • Closed: enabled
J24	1-2 (SDIO)	M.2 KEY E host interface: • 1-2: SDIO interface • 2-3: SPI interface
J38 and J39	Both 2-3	I2C PAC1934: • Both 1-2 connected to USB J34 • Both 2-3 connected to SAM9X75 I2C (PC0 and PC1) • Both open: disconnected • Other settings: not allowed

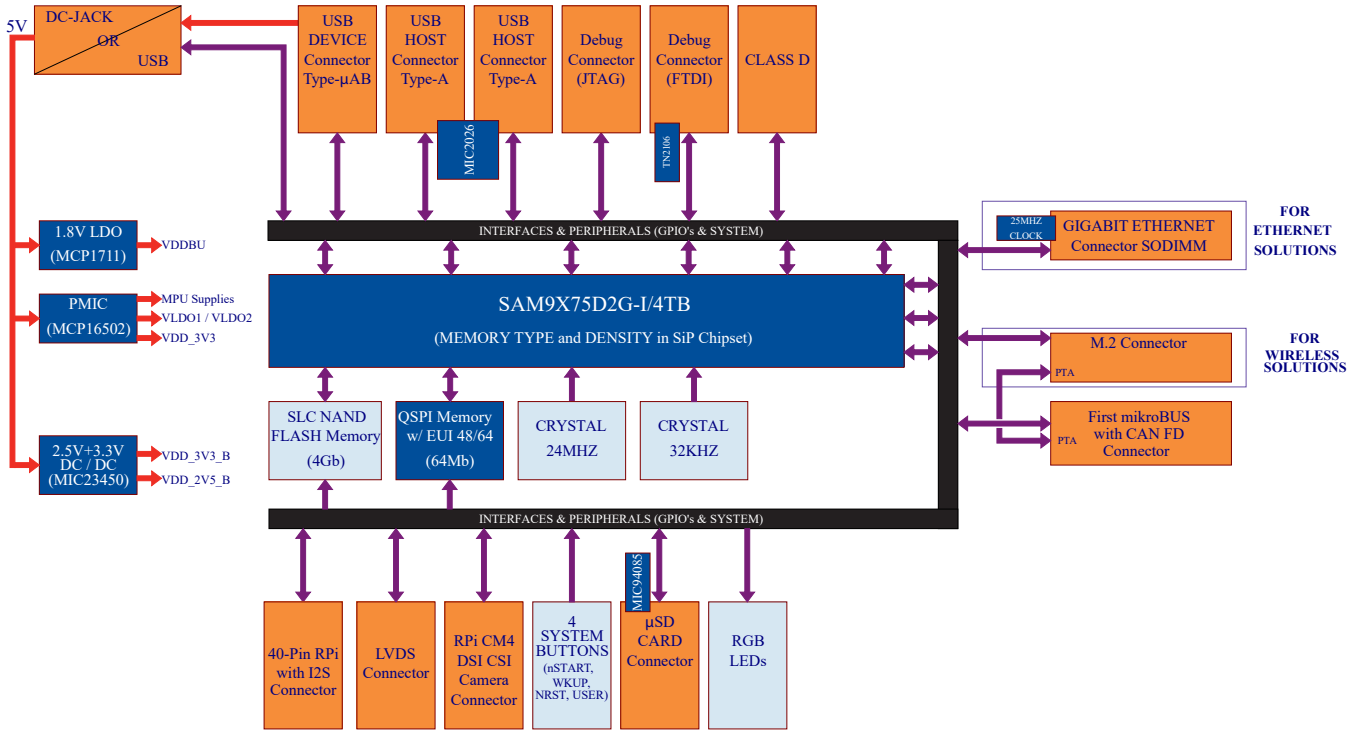
Figure 2-2. SAM9X75-Curiosity Default Jumper Settings



3. Function Blocks

This section covers the specifications of the SAM9X75-Curiosity and provides a high-level description of the board's major components and interfaces. This document is not intended to provide detailed documentation about the processor or about any other component used on the board. It is expected that the user will refer to the appropriate documents of these devices to access detailed information.

Figure 3-1. SAM9X75-Curiosity Block Diagram



3.1. Power Supply Topology and Power Distribution

This section describes the implementation and the circuitry that ensures adequate voltage stability and current budget for all the devices on the board and a correct power-up sequence for the MPU.

The power-up and power-down sequences indicated in the SAM9X7 Series data sheet must be respected for a reliable operation of the device.

3.1.1. Input Power Options

The SAM9X75-Curiosity board can be powered through:

- DC jack (J1)
- USB port A (J2)

The selection of the input supply is automatic with a priority given to the DC jack.

3.1.1.1. DC-Jack Connection (J1)

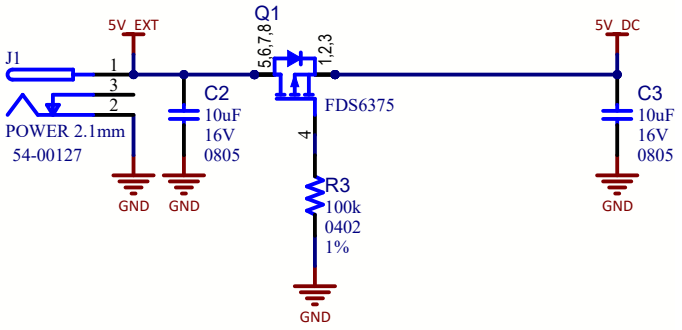
The SAM9X75-Curiosity board can be supplied by an external 5V wall adapter with the following absolute maximum ratings:

- V_{IN} max: 6V
- I_{IN} max: 6A

- DC-jack internal diameter: 2.10 mm (0.083 inch)
- DC-jack external diameter: 5.50 mm (0.217 inch)

The following figure shows the input power DC-jack supply.

Figure 3-2. DC-Jack Power Input Connection



3.1.1.2. USB Type Micro-B Connection (J2)

The SAM9X75-Curiosity board can be supplied by an external USB Micro-B cable with the following absolute maximum ratings:

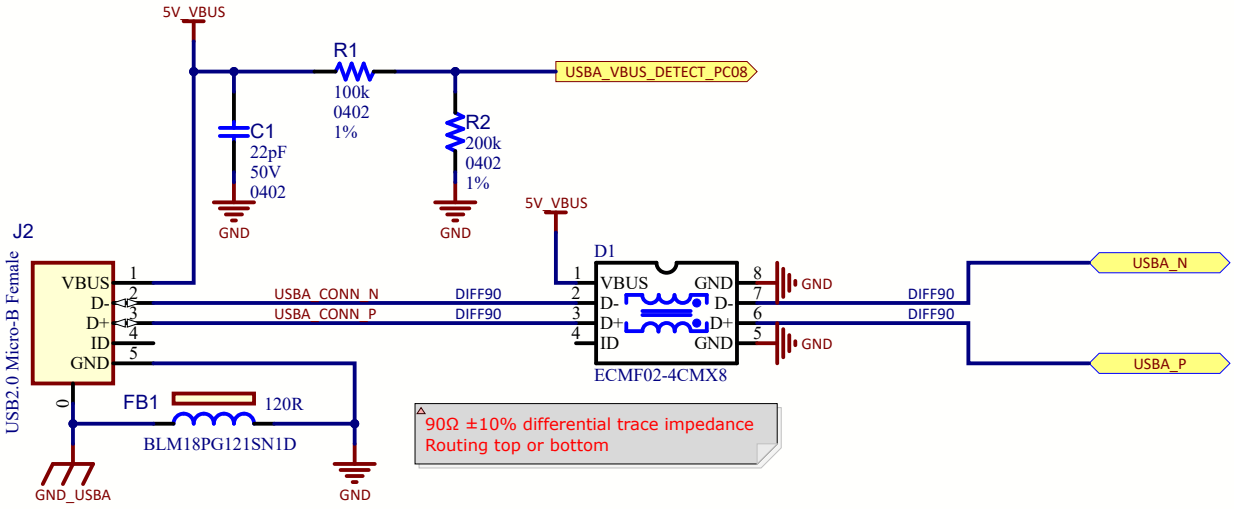
- V_{IN} max: 5.75V
- I_{IN} max: 500 mA in USB 2.0
- USB connector: USB Type Micro-B

The USB-powered operation comes from the USB device port connected to a PC or a 5 VDC supply.

The USB supply is enough to power the board in most applications. It is important to note that when the USB supply is used, the USB port has limited power.

The following figure shows the input power USB supply.

Figure 3-3. USB Power Input Connection

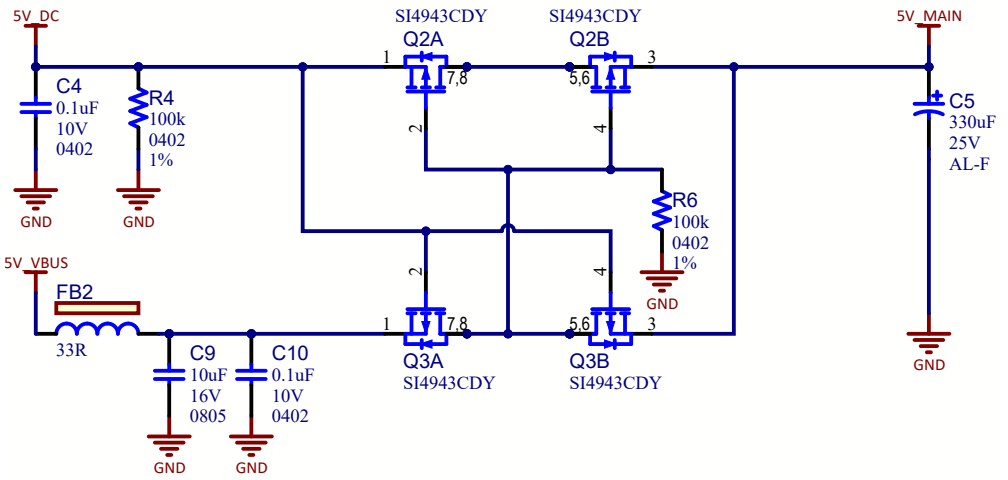


Note: USB-powered operation eliminates the need for additional wires and batteries. It is the preferred mode of operation for any project that requires only a 5V source at up to 500 mA.

3.1.1.3. Automatic Power Switch

The following figure depicts the automatic power switch between the USB and DC jack inputs.

Figure 3-4. Automatic Power Switch



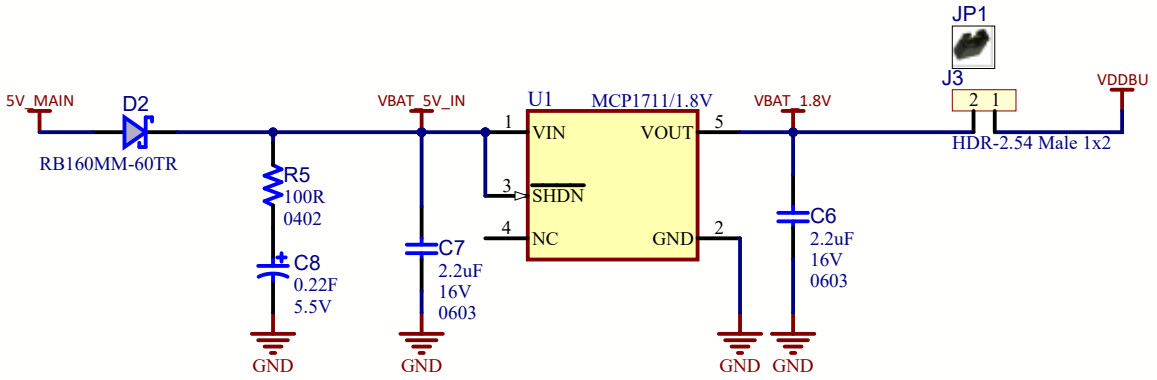
3.1.2. Backup Supply

The SAM9X75-Curiosity board embeds a backup voltage storage energy system to allow Low-Power mode tests.

J3 is used to measure the current on the backup rail.

The following figure shows the backup supply topology.

Figure 3-5. Backup Supply



3.1.3. Power Management Integrated Circuit (PMIC)

The MCP16502 is a high-performance power management IC providing four output voltages with maximum efficiency, compatible with Microchip's eMPUs (Embedded Microprocessor Units) and associated DRAM memories. It is compatible with SAM9X7.

The MCP16502 integrates four DC-DC buck regulators and two auxiliary LDOs and provides a comprehensive interface to the MPU.

All buck channels can support loads up to 1A and are 100% duty-cycle capable.

Two 300 mA LDOs are provided so that sensitive analog loads can be supported.

For more information about the MCP16502, refer to the product web page.

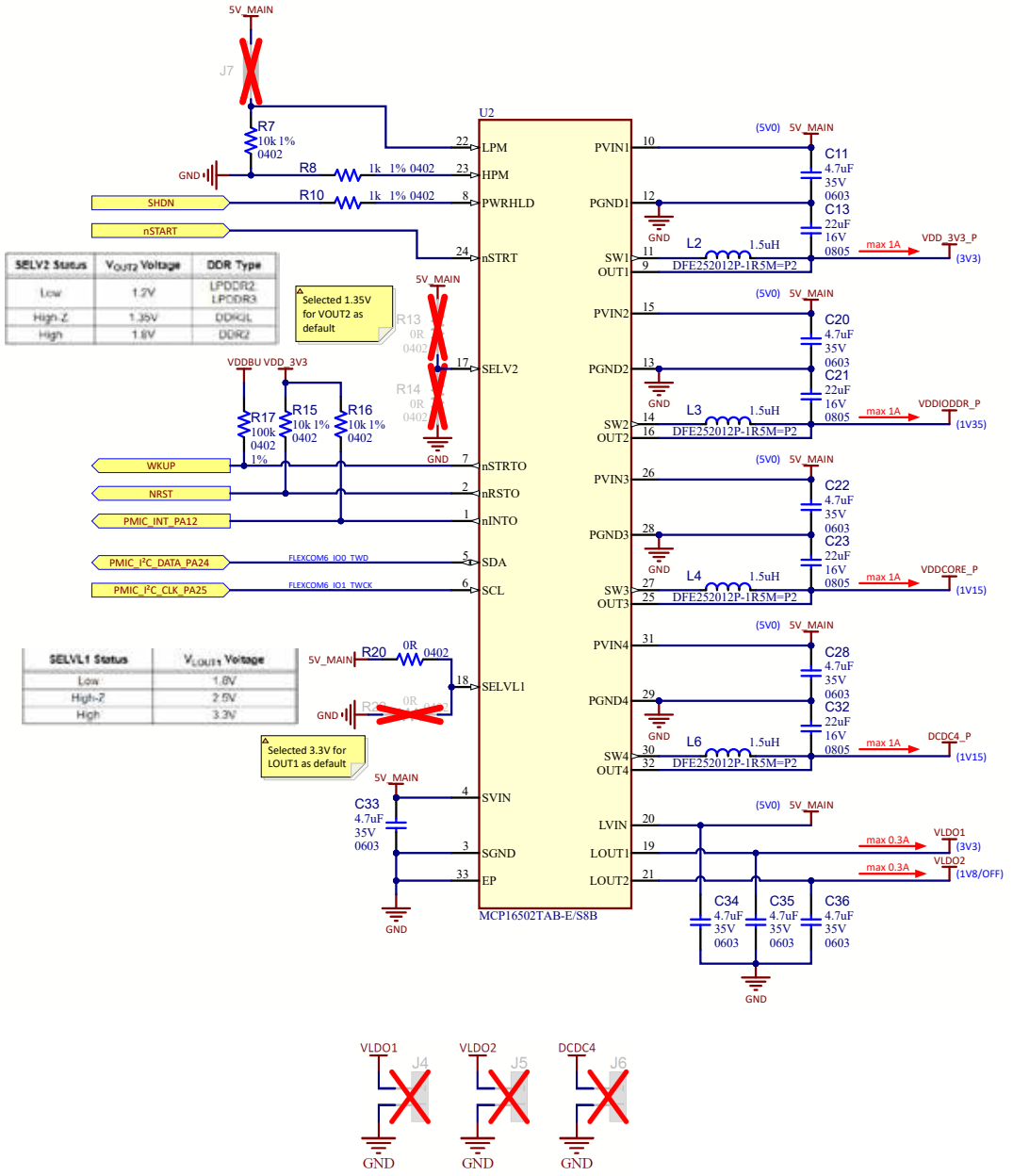
Detailed information on the SAM9X75D2G MPU power supplies and power-up/down considerations are described in section "Electrical Characteristics" in the SAM9X7 Series Data Sheet.

The MCP16502 comes preset to supply all the voltage rails needed by the system:

- OUT1: 3.3V supplies SAM9X75D2G I/O pads.
- OUT2: 1.35V supplies SAM9X75D2G DDR3L pads (VDDIODDR).
- OUT3: 1.15V supplies SAM9X75D2G Core (VDDCORE).
- OUT4: available in J6.
- LOUT1: available in J4.
- LOUT2: available in J5.

The following figure shows the power management scheme.

Figure 3-6. Power Management Integrated Circuit



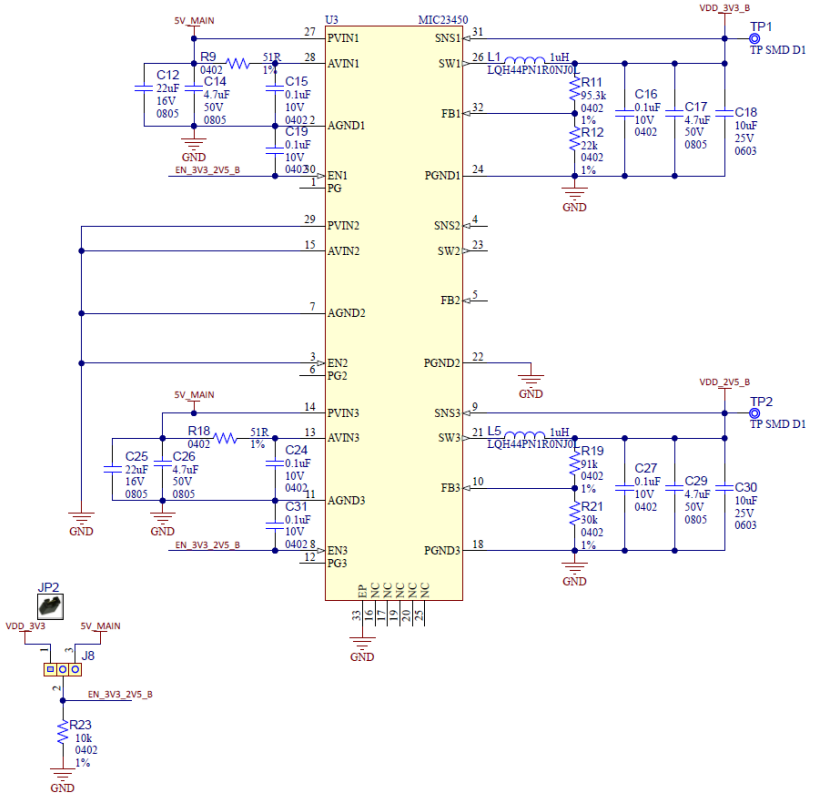
3.1.4. Add-On Board Supplies

The SAM9X75-Curiosity board embeds one extra DC/DC converter to supply interfaces such as the Gigabit Ethernet interface and the Wireless M.2 interface.

The extra power supply source embedded in the SAM9X75-Curiosity board generates a 3.3V supply dedicated for both the Gigabit Ethernet and the Wireless M.2 interfaces, and a 2.5V supply dedicated only for the Gigabit Ethernet interface. The feature is ensured by a MIC23450 DC/DC converter delivering up to 2A.

The following figure shows the extra 3.3V and 2.5V power supply schematics.

Figure 3-7. Extra 3.3V Power Supply Schematic



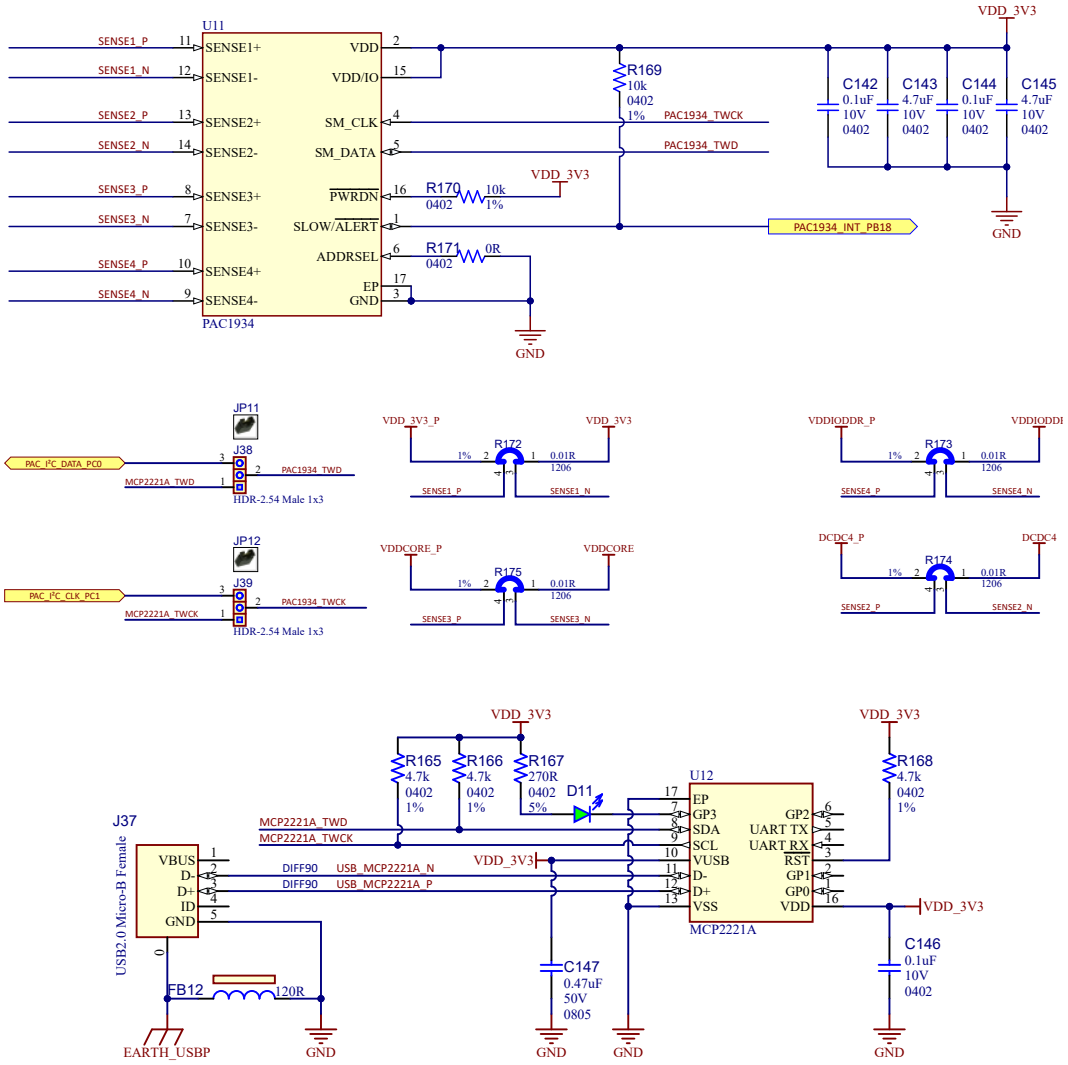
3.1.5. DC Power Monitoring

The SAM9X75-Curiosity board embeds a DC Power Monitor device performing power calculations and energy accumulations on the three main SAM9X75D2G power rails. This function is ensured by the PAC1934 Current and Power Measurement IC.

Data can be retrieved through an I²C interface connected either on SAM9X75D2G or on a computer through a USB Micro-B connector. The protocol conversion from I²C to USB interfaces is ensured by a Microchip Serial Converter Chipset MCP2221A.

The following figure shows the DC power monitoring schematic.

Figure 3-8. DC Power Monitoring Schematic



The following table shows the DC power monitoring configuration signal selection.

Table 3-1. DC Power Monitoring Configuration Signal Selection

J38	J39	Interface	PIO	Signal Name	Signal Description
Jumper 3-2	Jumper 3-2	SAM9X75D2G	PC0	PAC_I²C_DATA	TWI interface connected to SAM9X75D2G (PAC1934 driven onboard by the MPU)
			PC1	PAC_I²C_CLK	
Jumper 2-1	Jumper 2-1	USB Micro-B connector (37)	–	–	TWI interface connected to MCP2221A (PAC1934 driven externally through USB)
NC	NC	Disconnected	–	–	–
–	–	Other settings N/A	–	–	–

3.2. Processor

The SAM9X75D2G is a high-performance, ultra-low power ARM926EJ-S CPU-based embedded microprocessor (MPU) running up to 800 MHz, with an integrated 2 Gbit DDR3L memory. The device integrates powerful peripherals for connectivity and user interface applications, including MIPI DSI®, LVDS, RGB and 2D graphics, MIPI-CSI-2, Gigabit Ethernet with TSN and CAN-FD. Advanced security

functions are offered, such as tamper detection, secure boot, secure key storage, TRNG, PUF as well as high-performance crypto accelerators for AES and SHA.

Refer to the SAM9X7 Series data sheet for more information. See Recommended Reading.

3.2.1. Power Supply

The PMIC (main regulator) provides all power supplies required by the SAM9X75D2G device:

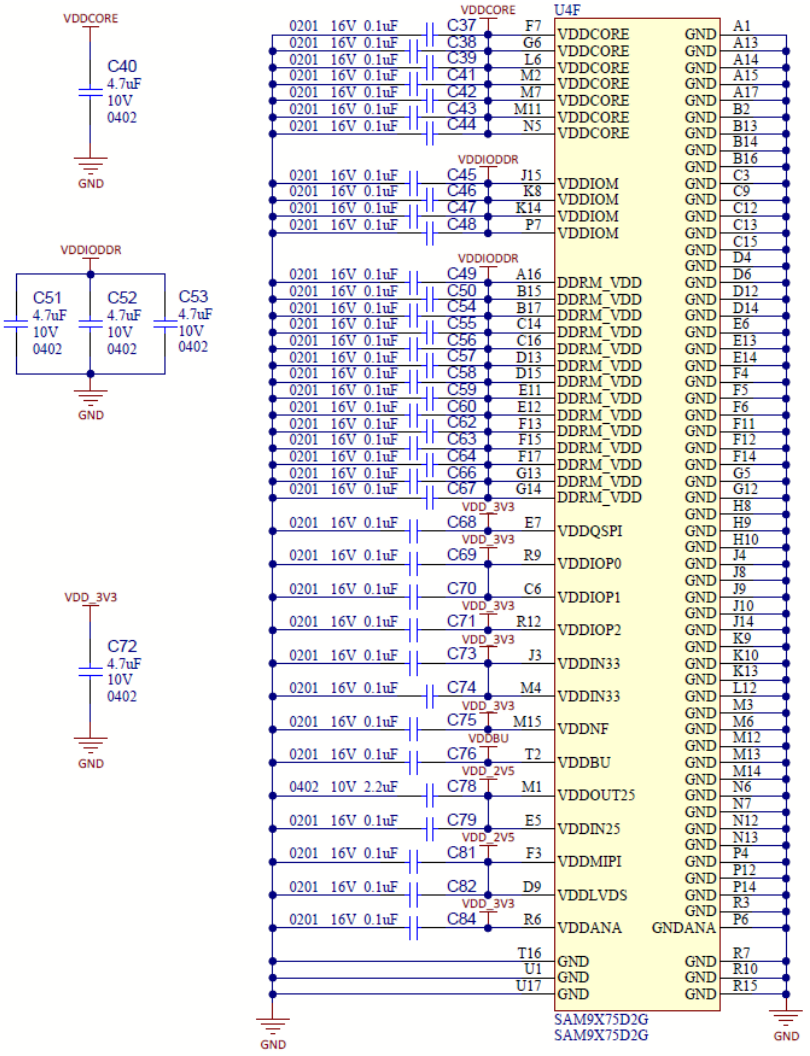
- 1.15V for VDDCORE
- 1.35V for VDDIODDR
- 3.3V for VDD3V3

A 1.8V backup supply is also available for VDDBU.

Decoupling capacitors are placed close to the MPU power pins to stabilize the voltage rails.

The following figure shows the processor power supplies.

Figure 3-9. Processor Power Supplies



3.2.2. Main Configurations and Control

The following figure shows the power main configuration and control.

Figure 3-10. Processor Main Configuration and Control

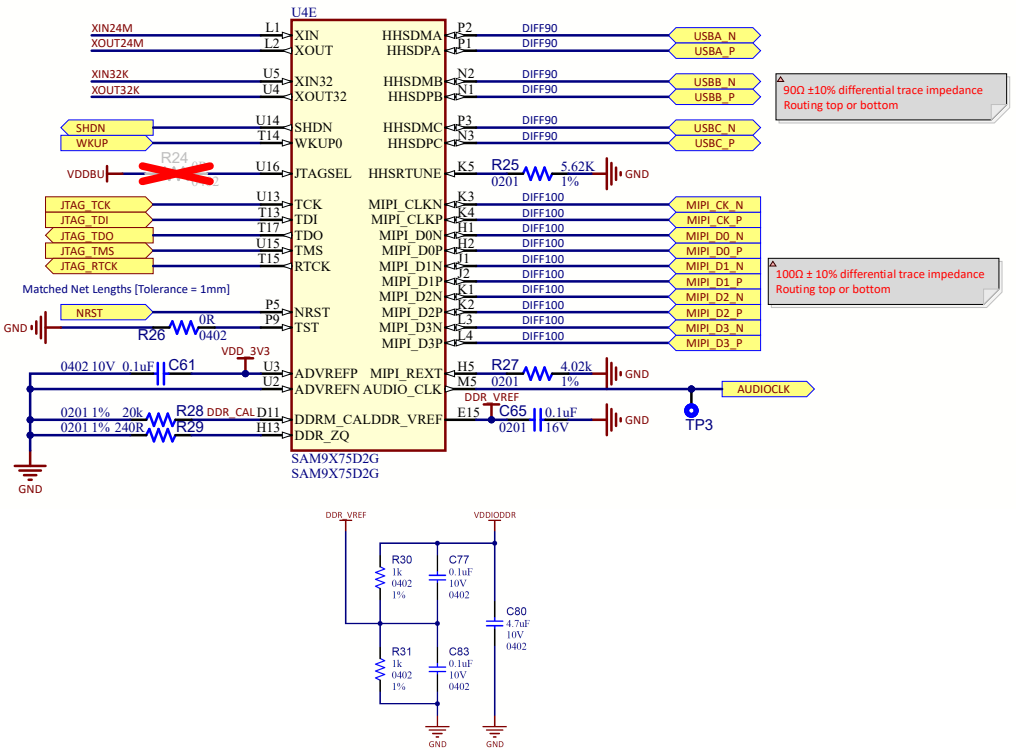


Table 3-2. Processor Main Configuration and Control Signals

Pin Name	Type	Signal Description
XIN	Input	Main Clock Oscillator input
XOUT	Output	Main Clock Oscillator output
XIN32	Input	Slow Clock Oscillator input
XOUT32	Output	Slow Clock Oscillator output
SHDN	Output	Enable or disable an external power supply circuit in Low-Power modes
WKUP0	Input	Event detection used to wake up the processor from Shutdown state
JTAGSEL	Input	JTAG boundary scan (1L) or Embedded ICE (0L) selection pin
TCK	Input	ICE and JTAG Test Clock
TDI	Input	ICE and JTAG Test Data In
TDO	Output	ICE and JTAG Test Data Out
TMS	Input	ICE and JTAG Test Mode Select
RTCK	Output	ICE and JTAG Return Test Clock
NRST	Input	External Reset Input
TST	Input	Test Mode Select
ADVREFP	Analog Input	Positive reference voltage
ADREFN	Analog Input	Negative reference voltage
DDRM_CAL	Analog Input	SDRAM Controller Calibration Input
DDR_ZQ	Analog	Calibration for DQ drive and ODT
HHSDMA	Analog	USB Host Port A High Speed Data -
HHSDPA	Analog	USB Host Port A High Speed Data +
HHSDMB	Analog	USB Host Port B High Speed Data -

Table 3-2. Processor Main Configuration and Control Signals (continued)

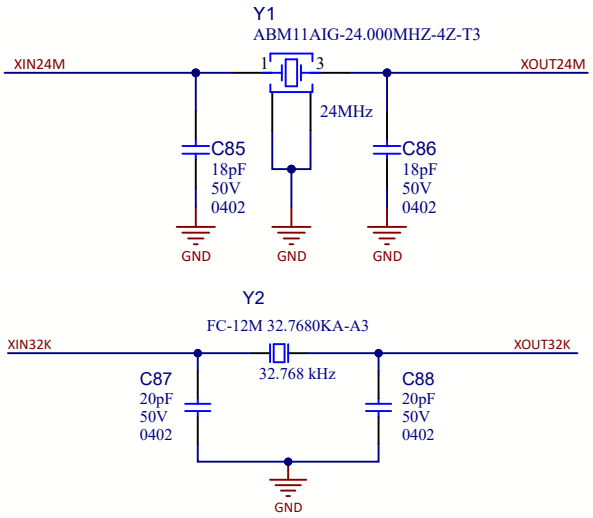
Pin Name	Type	Signal Description
HHSDPB	Analog	USB Host Port B High Speed Data +
HHSDMC	Analog	USB Host Port C High Speed Data -
HHSDPC	Analog	USB Host Port C High Speed Data +
HHSRTUNE	Input	USB external tunning
MIPI_CLKP	O	MIPI D-PHY Differential Output Clock Lane +
MIPI_CLKN	O	MIPI D-PHY Differential Output Clock Lane -
MIPI_DPx	I/O	MIPI D-PHY Differential Output Data Lane + [3:0]
MIPI_DNx	I/O	MIPI D-PHY Differential Output Data Lane - [3:0]
MIPI_REXT	Analog Input	Calibration Reference Resistor
AUDIO_CLK	Output	Audio Programmable Clock Output
DDR_VREF	Analog Input	I/O Reference Voltage

3.2.3. Clock Circuitry

The embedded MPU generates its necessary clocks based on two external oscillators: one slow clock (SLCK) oscillator running at 32.768 kHz and one main clock oscillator running at 24 MHz.

The following figure shows the processor clock circuitry.

Figure 3-11. Processor Clock Circuitry



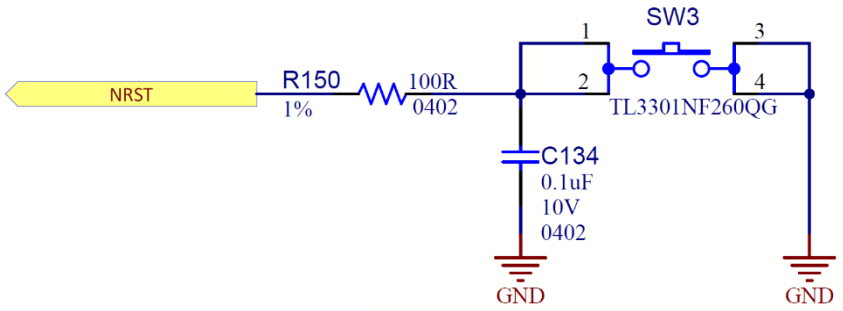
3.2.4. Reset Circuitry

The board features the following reset sources for the MPU:

- Power-on Reset from the power management unit MCP16502
- User push button reset
- External JTAG

The following figure shows the user push button reset.

Figure 3-12. User Push Button Reset



3.2.5. GPIOs

The following sections depict all the signals connected to the SAM9X75D2G MPU ports.

The following figure shows the processor PIOs connections.

Figure 3-13. Processor PIOs PA and PB

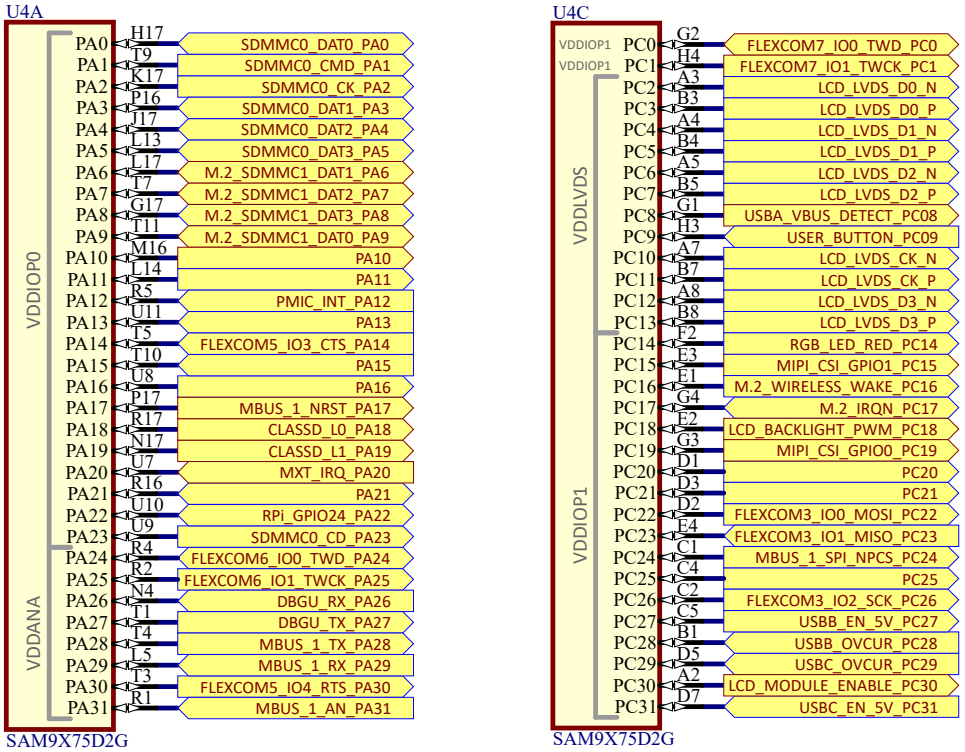
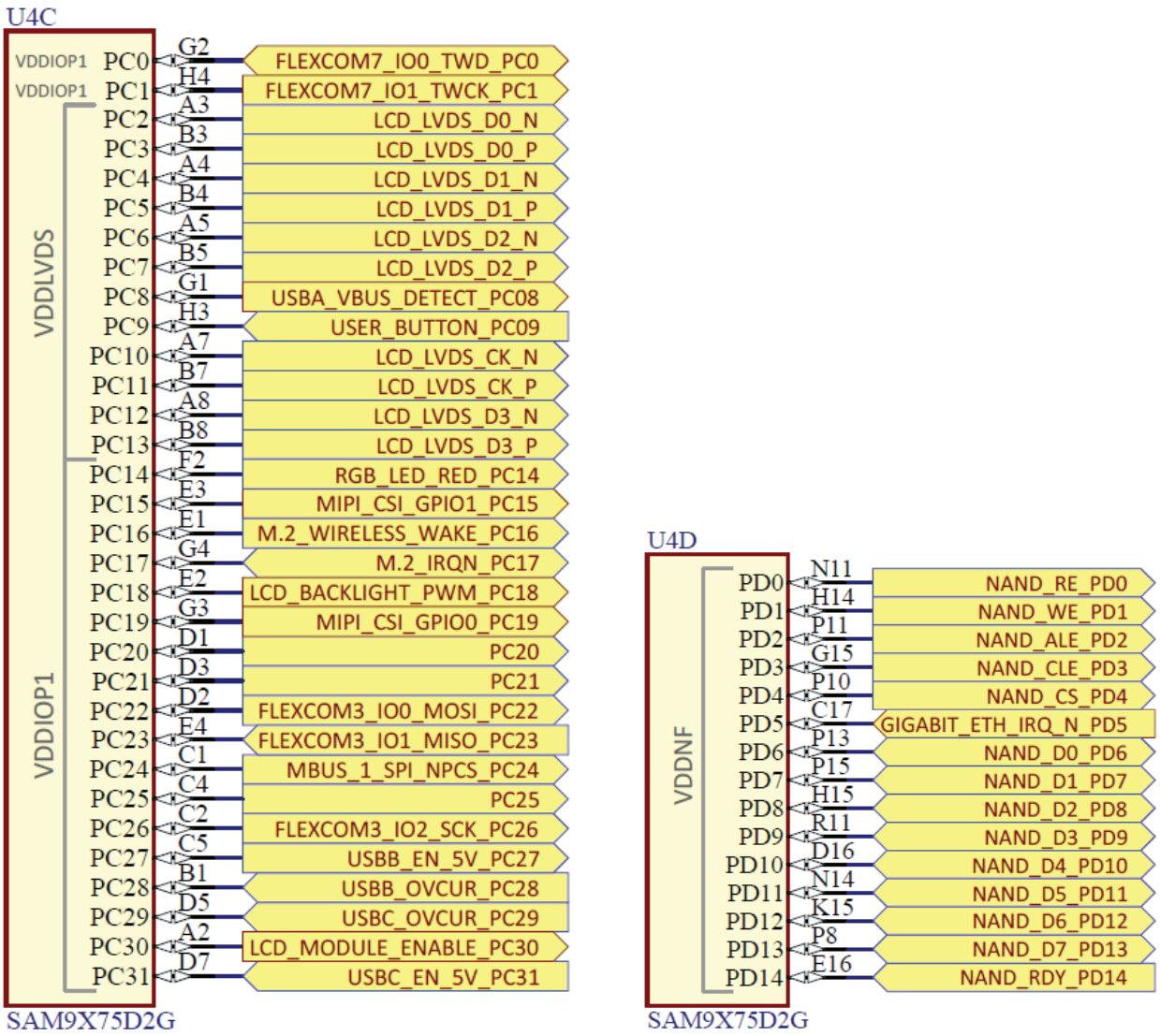


Figure 3-14. Processor PIOs PC and PD

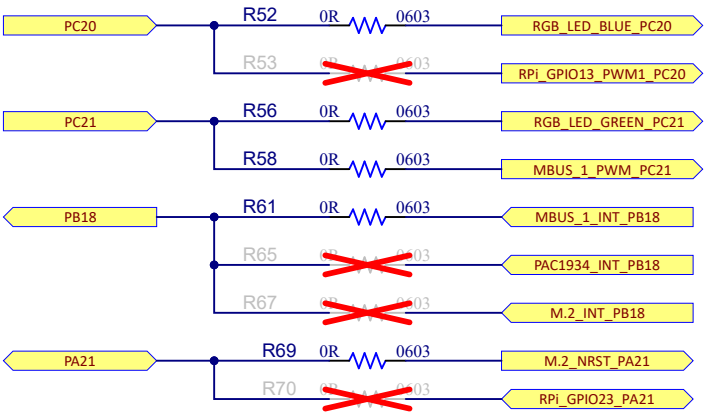


Some of the ports are multiplexed to accommodate more devices on the evaluation kit and to showcase all the functions the SAM9X75D2G MPU can address off a single PIO wire.

Most of the lines that share multiple functions are split through passive resistors. In order to access them, the user can opt for moving the selection resistors using the text searchable assembly drawing from the appendix of this user guide. In some cases, the user can use only one of the functions at a time, or can develop a composite driver enabling the use of multiple functions at the same time.

The following figure shows an example of the processor PIO muxing.

Figure 3-15. GPIO Distribution



3.2.6. Standard Serial Communication Interfaces Distribution

SAM9X75-Curiosity features several devices and interfaces that use UART, SPI and TWI interfaces. These are multiplexed in order to minimize the number of pins used and maximize the number of addressable devices.

The following table shows the PIOs assignment and signal description.

Table 3-3. Processor PIOs Pin Assignment and Signal Description

Pad	Power Rail	Function	I/O Type
PA0	VDDIOP0	SDMMC0_DAT0	Data 0 bidirectional line going to the microSD card connector (J14)
PA1	VDDIOP0	SDMMC0_CMD	Command (CMD) bidirectional line going to the microSD card connector (J14)
PA2	VDDIOP0	SDMMC0_CK	Clock (CLK) output line going to the microSD card connector (J14)
PA3	VDDIOP0	SDMMC0_DAT1	Data 1 bidirectional line going to the microSD card connector (J14)
PA4	VDDIOP0	SDMMC0_DAT2	Data 2 bidirectional line going to the microSD card connector (J14)
PA5	VDDIOP0	SDMMC0_DAT3	Data 3 bidirectional line going to the microSD card connector (J14)
PA6	VDDIOP0	SDMMC1_DAT1	Data 1 bidirectional line going to the M.2 KEYE connector (J20)
PA7	VDDIOP0	SDMMC1_DAT2	Data 2 bidirectional line going to the M.2 KEYE connector (J20)
PA8	VDDIOP0	SDMMC1_DAT3	Data 3 bidirectional line going to the M.2 KEYE connector (J20)
PA9	VDDIOP0	SDMMC1_DAT0	Data 0 bidirectional line going to the M.2 KEYE connector (J20)
			SPI Host Input Client Output (MISO) input line going to the M.2 KEYE connector (J20)
PA10	VDDIOP0	SDMMC1_CMD	Command (CMD) bidirectional line going to the M.2 KEYE connector (J20)
		FLEXCOM4_IO0_SPI_MOSI	SPI Host Output Client Input (MOSI) output line going to the M.2 KEYE connector (J20)
PA11	VDDIOP0	SDMMC1_CK	Clock (CLK) output line going to the M.2 KEYE connector (J20)
		FLEXCOM4_IO2_SPI_CLK	SPI Clock (SCK) output line going to the M.2 KEYE connector (J20)
PA12	VDDIOP0	PMIC_INT	PMIC Interrupt line for other I²C devices
PA13	VDDIOP0	SDMMC1_CD	Card Detect input line going to the M.2 KEYE connector (J20)
		FLEXCOM4_IO4_SPI_CS	SPI Chip Select (CS) output line going to the M.2 KEYE connector (J20)
PA14	VDDIOP0	FLEXCOM5_IO3_CTS	UART Clear to Send (CTS) input line going to the M.2 KEYE connector (J20)
PA15	VDDIOP0	FLEXCOM5_IO1_RXD	UART Receive (RXD) input line going to the M.2 KEYE connector (J20)
		RPi_GPIO15_MPU32_RXD	UART Receive (RX) input line going to the external 40-pin connector (J27)
PA16	VDDIOP0	FLEXCOM5_IO0_TXD	UART Transmit (TXD) output line going to the M.2 KEYE connector (J20)
		RPi_GPIO14_MPU32_TXD	UART Transmit (TX) output line going to the external 40-pin connector (J27)
PA17	VDDIOP0	MBUS_1_NRST	Reset signal going to the mikroBUS connector (J25)
PA18	VDDIOP0	CLASSD_L0	Class D controller Left Output 0 to Class D connector (J36)
PA19	VDDIOP0	CLASSD_L1	Class D controller Left Output 1 to Class D connector (J36)
PA20	VDDIOP0	MXT_IRQ	LCD Interrupt line for other I²C devices input signal going to Video LVDS connector (J28)
PA21	VDDIOP0	RPi_GPIO23	GPIO going to the external 40-pin connector (J27)
		M.2_NRST	Reset line output going to M.2 KEYE connector (J20)
PA22	VDDIOP0	RPi_GPIO24	GPIO going to the external 40-pin connector (J27)
PA23	VDDIOP0	SDMMC0_CD	Card Detect input line going to the microSD card connector (J14)

Table 3-3. Processor PIOs Pin Assignment and Signal Description (continued)

Pad	Power Rail	Function	I/O Type
PA24	VDDIOP0	M.2_I²C_DATA	TWI Data (TWD) bidirectional line shared between the M.2 KEYE connector (J20), PMIC, Camera MIPI connector (J29) and Video LVDS connector (J28)
		PMIC_ I²C_DATA	
		CAM_I²C_DATA	
		LCD_I²C_DATA	
PA25	VDDANA	M.2_I²C_CLK	TWI Clock (TWCK) output line shared between the M.2 KEYE connector (J20), PMIC, Camera MIPI connector (J29) and Video LVDS connector (J28)
		PMIC_ I²C_ CLK	
		CAM_I²C_ CLK	
		LCD_I²C_ CLK	
PA26	VDDANA	DBGU_RX	Debug UART Receive (DRX) input line going to Debug connector (J35)
PA27	VDDANA	DBGU_TX	Debug UART Transmit (DTX) output line going to Debug connector (J35)
PA28	VDDANA	MBUS_1_TX	UART Transmit (TX) output line going to the mikroBUS connector (J25)
PA29	VDDANA	MBUS_1_RX	UART Receive (RX) input line going to the mikroBUS connector (J25)
PA30	VDDANA	FLEXCOM5_IO4_RTS	UART Request to Send (RTS) output line going to the M.2 KEYE connector (J20)
PA31	VDDANA	MBUS_1_AN	Analog input from the mikroBUS connector (J25)
PB0	VDDIOP2	RGMII_RXD2/GMII_RXD2	MII Ethernet Receive Data 2 signal going to SODIMM connector (J17)
PB1	VDDIOP2	RGMII_RXD3/GMII_RXD3	MII Ethernet Receive Data 3 signal going to SODIMM connector (J17)
PB2	VDDIOP2	GIGABIT_ETH_125CK	Gigabit Ethernet 125CK signal going to SODIMM connector (J17)
PB3	VDDIOP2	RGMII_RXCTL/GMII_RXDV	MII Ethernet Receive Data Valid signal going to SODIMM connector (J17)
PB4	VDDIOP2	RGMII_TXD2/GMII_TXD2	MII Ethernet Transmit Data 2 signal going to SODIMM connector (J17)
PB5	VDDIOP2	RGMII_TXD3/GMII_TXD3	MII Ethernet Transmit Data 3 signal going to SODIMM connector (J17)
PB6	VDDIOP2	RGMII_TXC-TXCK/GMII_TXCLK	MII Ethernet Transmit Clock signal going to SODIMM connector (J17)
PB7	VDDIOP2	RGMII_TXCTL/GMII_TXEN	MII Ethernet Transmit Enable signal going to SODIMM connector (J17)
PB8	VDDIOP2	RGMII_RXC-RXCK/GMII_RXCLK	MII Ethernet Receive Clock signal going to SODIMM connector (J17)
PB9	VDDIOP2	GIGABIT_ETH_MDIO	MII Ethernet Management Data I/O signal going to SODIMM connector (J17)
PB10	VDDIOP2	GIGABIT_ETH_MDC	MII Ethernet Management Data Clock signal going to SODIMM connector (J17)
PB11	VDDIOP2	RGMII_RXD0/GMII_RXD0	MII Ethernet Receive Data 0 signal going to SODIMM connector (J17)
PB12	VDDIOP2	RGMII_RXD1/GMII_RXD1	MII Ethernet Receive Data 1 signal going to SODIMM connector (J17)
PB13	VDDIOP2	RGMII_TXD0/GMII_TXD0	MII Ethernet Transmit Data 0 signal going to SODIMM connector (J17)
PB14	VDDIOP2	RGMII_TXD1/GMII_TXD1	MII Ethernet Transmit Data 1 signal going to SODIMM connector (J17)
PB15	VDDQSPI	RPi_GPIO19_I²S_WS	I²S Word Select (WS) signal going to the external 40-pin connector (J27)
PB16	VDDQSPI	RPi_GPIO20_I²S_DIN	I²S Data IN (DIN) signal going to the external 40-pin connector (J27)
PB17	VDDQSPI	RPi_GPIO21_I²S_DOUT	I²S Data OUT (DOUT) signal going to the external 40-pin connector (J27)
PB18	VDDQSPI	MBUS_1_INT	Interrupt line input shared between the mikroBUS 1 connector (J25), PAC1934 and M.2 KEYE connector (J20)
		PAC1934_INT	
		M.2_INT	
PB19	VDDQSPI	QSPI_SCK	QSPI Clock signal going to SST26VF064BEUIT-104I/MF
PB20	VDDQSPI	QSPI_CS	QSPI Chip Select signal going to SST26VF064BEUIT-104I/MF
PB21	VDDQSPI	QSPI_IO0	QSPI Data 0 signal going to SST26VF064BEUIT-104I/MF
PB22	VDDQSPI	QSPI_IO1	QSPI Data 1 signal going to SST26VF064BEUIT-104I/MF
PB23	VDDQSPI	QSPI_IO2	QSPI Data 2 signal going to SST26VF064BEUIT-104I/MF
PB24	VDDQSPI	QSPI_IO3	QSPI Data 3 signal going to SST26VF064BEUIT-104I/MF
PB25	VDDQSPI	RPi_GPIO4_I²S_MCK/GPCLK0	I²S Host Clock (MCK) signal going to the external 40-pin connector (J27)
PB26	VDDQSPI	RPi_GPIO18_I²S_BCLK	I²S Clock (CK) signal going to the external 40-pin connector (J27)
PC0	VDDIOP1	PAC_I²C_DATA	TWI Data (TWD) bidirectional line shared between the PAC1934, SODIMM connector (J15), mikroBUS connector (J22) and external 40-pin connector (J27)
		GIGABIT_ETH_ I²C_DATA	
		MBUS_1_I²C_DATA	
		RPi_GPIO2_I²C_SDA	
PC1	VDDIOP1	PAC_I²C_CLK	TWI Clock (TWCK) output line shared between the PAC1934, SODIMM connector (J15), mikroBUS connector (J22) and external 40-pin connector (J27)
		GIGABIT_ETH_ I²C_ CLK	
		MBUS_1_I²C_ CLK	
		RPi_GPIO3_I²C_SCL	
PC2	VDDLVDS	LCD_LVDS_D0_N	LVDS Data 0 N signal going to Video LVDS connector (J28)
PC3	VDDLVDS	LCD_LVDS_D0_P	LVDS Data 0 P signal going to Video LVDS connector (J28)
PC4	VDDLVDS	LCD_LVDS_D1_N	LVDS Data 1 N signal going to Video LVDS connector (J28)
PC5	VDDLVDS	LCD_LVDS_D1_P	LVDS Data 1 P signal going to Video LVDS connector (J28)

Table 3-3. Processor PIOs Pin Assignment and Signal Description (continued)

Pad	Power Rail	Function	I/O Type
PC6	VDDLVDS	LCD_LVDS_D2_N	LVDS Data 2 N signal going to Video LVDS connector (J28)
PC7	VDDLVDS	LCD_LVDS_D2_P	LVDS Data 2 P signal going to Video LVDS connector (J28)
PC8	VDDIOP1	USBA_VBUS_DETECT	USBA VBUS detect input
PC9	VDDIOP1	USER_BUTTON	GPIO used as input to probe the changes of the user button
PC10	VDDLVDS	LCD_LVDS_CK_N	LVDS Clock N signal going to Video LVDS connector (J28)
PC11	VDDLVDS	LCD_LVDS_CK_P	LVDS Clock P signal going to Video LVDS connector (J28)
PC12	VDDLVDS	LCD_LVDS_D3_N	LVDS Data 3 N signal going to Video LVDS connector (J26)
PC13	VDDLVDS	LCD_LVDS_D3_P	LVDS Data 3 P signal going to Video LVDS connector (J28)
PC14	VDDIOP1	RGB_LED_RED	LD1 red LED
PC15	VDDIOP1	MIPI_CSI_GPIO1	GPIO going to the Camera MIPI connector (J29)
PC16	VDDIOP1	WIRELESS_WAKE	GPIO used as wireless wake up going to the M.2 KEYE connector (J20)
PC17	VDDIOP1	IRQN	GPIO used as IRQ going to the M.2 KEYE connector (J20)
PC18	VDDIOP1	LCD_BACKLIGHT_PWM	LCD PWM for Contrast Control output signal going to Video LVDS connector (J28)
PC19	VDDIOP1	MIPI_CSI_GPIO0	GPIO going to the Camera MIPI connector (J29)
PC20	VDDIOP1	RGB_LED_BLUE	LD1 blue LED
		RPi_GPIO13_PWM1	PWM1 signal output line going to the external 40-pin connector (J27)
PC21	VDDIOP1	RGB_LED_GREEN	LD1 green LED
		MBUS_1_PWM	PWM signal output line going to the mikroBUS connector (J22)
PC22	VDDIOP1	MBUS_1_SPI_MOSI	SPI Host Output Client Input (MOSI) output line shared between the mikroBUS connector (J22), the external 40-pin connector (J27) and the SODIMM connector (J17)
		RPi_GPIO10_SPI_MOSI	
		GIGABIT_SPI_MOSI	
PC23	VDDIOP1	MBUS_1_SPI _MISO	SPI Host Input Client Output (MISO) input line shared between the mikroBUS connector (J22), the external 40-pin connector (J27) and the SODIMM connector (J17)
		RPi_GPIO9_SPI_ MISO	
		GIGABIT_SPI_MISO	
PC24	VDDIOP1	MBUS_1_SPI_NPCS	SPI Chip Select (CS) output line for the mikroBUS connector (J22)
PC25	VDDIOP1	NRST_OUT	Output signal used to reset all the devices on the board
		RPi_GPIO8_SPI_ NPCS0/ GIGABIT_SPI_NPCS0	SPI Chip Select 0 (CS) output line for external 40-pin connector (J27) or the SODIMM connector (J17)
PC26	VDDIOP1	MBUS_1_SPI _SCK	SPI Clock (SCK) output line shared between the mikroBUS connector (J22), the external 40-pin connector (J27) and the SODIMM connector (J17)
		RPi_GPIO11_SPI _ SCK	
		GIGABIT_SPI_SCK	
PC27	VDDIOP1	USBB_EN_5V	Power Delivery Enable signal for USBB host interface
PC28	VDDIOP1	USBB_OVCUR	USBB overcurrent flag input
PC29	VDDIOP1	USBC_OVCUR	USBC overcurrent flag input
PC30	VDDIOP1	LCD_MODULE_ENABLE	LCD Enable output signal going to Video LVDS connector (J28)
PC31	VDDIOP1	USBC_EN_5V	Power Delivery Enable signal for USBC host interface
PD0	VDDNF	NAND_RE	NAND Flash Read Enable (RE) output signal going to MX30LF4G28ADXKI
PD1	VDDNF	NAND_WE	NAND Flash Write Enable (OE) output signal going to MX30LF4G28ADXKI
PD2	VDDNF	NAND_ALE	NAND Flash Address Latch Enable (ALE) output signal going to MX30LF4G28AD-XKI
PD3	VDDNF	NAND_CLE	NAND Flash Command Latch Enable (CLE) output signal going to MX30LF4G28AD-XKI
PD4	VDDNF	NAND_CS	NAND Flash Chip Select (CS) output signal going to MX30LF4G28AD-XKI
PD5	VDDNF	GIGABIT_ETH_IRQ_N	Gigabit Ethernet IRQ_N signal going to SODIMM connector (J17)
PD6	VDDNF	NAND_D0	NAND Flash Data 0 (D0) bidirectional signal going to MX30LF4G28ADXKI
PD7	VDDNF	NAND_D1	NAND Flash Data 1 (D1) bidirectional signal going to MX30LF4G28ADXKI
PD8	VDDNF	NAND_D2	NAND Flash Data 2 (D2) bidirectional signal going to MX30LF4G28ADXKI
PD9	VDDNF	NAND_D3	NAND Flash Data 3 (D3) bidirectional signal going to MX30LF4G28ADXKI
PD10	VDDNF	NAND_D4	NAND Flash Data 4 (D4) bidirectional signal going to MX30LF4G28ADXKI
PD11	VDDNF	NAND_D5	NAND Flash Data 5 (D5) bidirectional signal going to MX30LF4G28ADXKI
PD12	VDDNF	NAND_D6	NAND Flash Data 6 (D6) bidirectional signal going to MX30LF4G28ADXKI

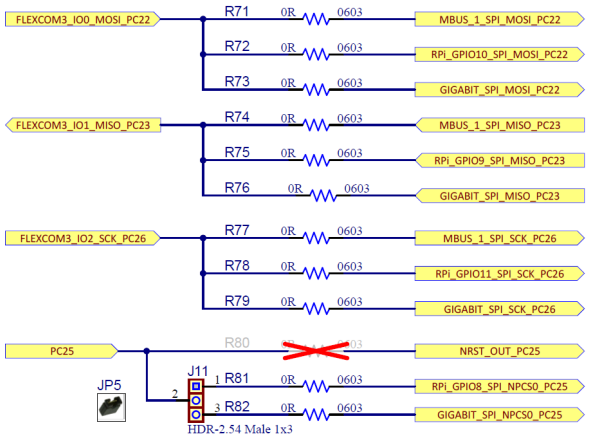
Table 3-3. Processor PIOs Pin Assignment and Signal Description (continued)

Pad	Power Rail	Function	I/O Type
PD13	VDDNF	NAND_D7	NAND Flash Data 7 (D7) bidirectional signal going to MX30LF4G28ADXKI
PD14	VDDNF	NAND_RDY	NAND Flash Ready/Busy (R/B#) input signal coming from MX30LF4G28AD-XKI

3.2.6.1. SPI Interface Distribution

A single SPI bus provided by FLEXCOM3 connects the MPU to three extension slots, providing access to multiple options of extension devices. The three interfaces are mikroBUS, RPi compatible header and SODIMM connector.

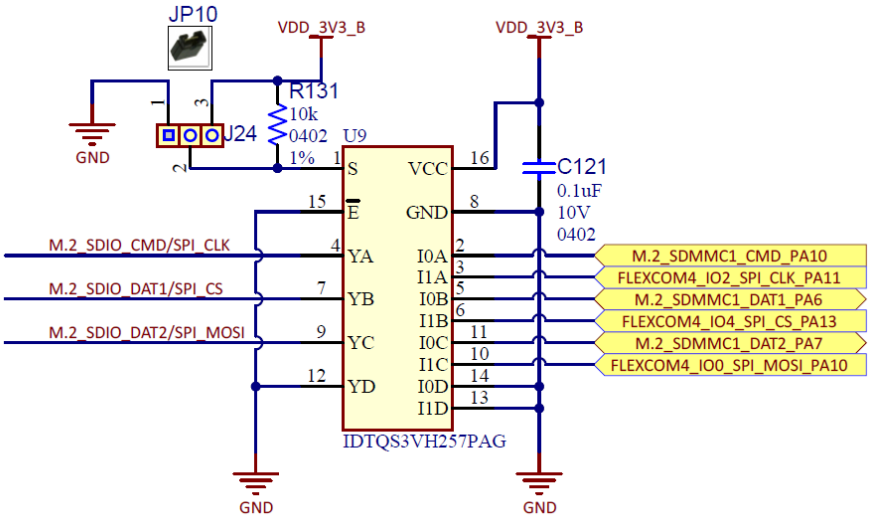
Figure 3-16. SPI Interface Distribution



Two chip select lines are available on FLEXCOM3 and one of them is shared between NPCS0 of the RPi connector interface and the SODIMM interface. To use the SPI of the RPI connector interface, JP5 must connect positions 1 and 2 of J11 header. Using the SPI of the SODIMM interface requires mounting JP5 on positions 2 and 3 of J11.

One extra SPI interface is implemented for the M.2 interface and it is multiplexed with the SDIO interface. In order to activate the SPI communication, the user must move jumper JP10 from its default 1-2 position on J11, which enables the SDIO communication, to 2-3 position on J11.

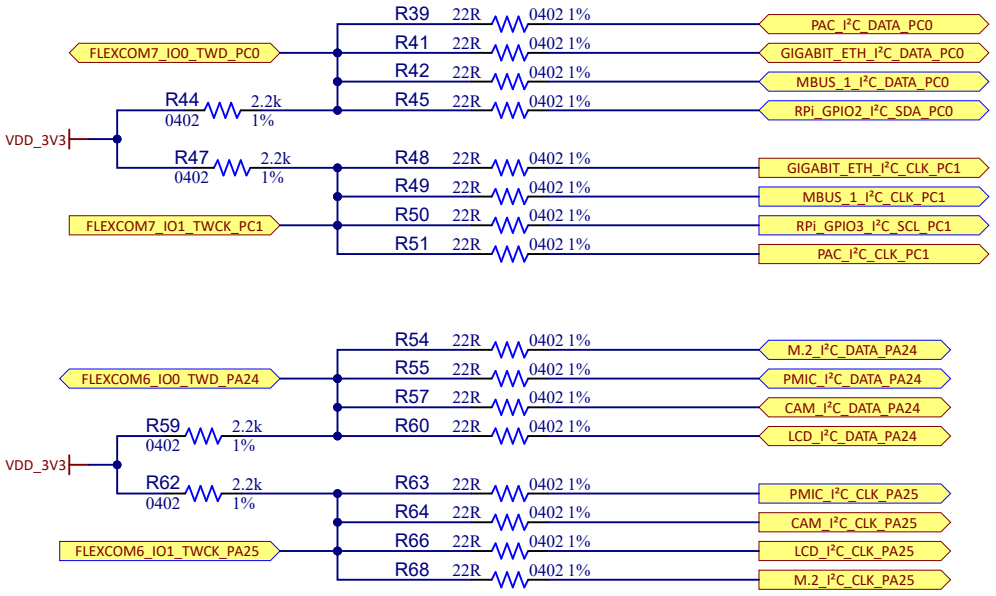
Figure 3-17. M.2 SPI Interface Multiplexed with SDIO



3.2.6.2. TWI Interface Distribution

Two TWI interfaces on FLEXCOM6 and FLEXCOM7 connect the MPU to several on-board devices and extension slots. The reason to split the devices on a multiple BUS configuration is to balance the data traffic because some devices may require continuous communication.

Figure 3-18. TWI Interface Distribution



3.2.6.3. UART Interface Distribution

A UART interface is split between the RPi compatible header and the M.2 interface. The M.2 interface is prioritized, because it is used for the DFU (Device Firmware Update) of the compatible Microchip devices.

In order to use the UART interface on the RPi compatible header, the user must solder resistors R40 and R46 on the board. In this case, if a device is connected to the M.2 interface, the user must also unsolder resistors R38 and R43.

Figure 3-19. UART Interface Distribution

3.3. On-Board Memories

The SAM9X75D2G features an internal DDR3(L) memory and an External Bus Interface (EBI) to enable interfacing to a wide range of external memories and to almost any type of parallel peripheral.

This section describes the memory devices mounted on the SAM9X75-Curiosity board.

- One DDR3L SDRAM embedded in the SiP
- One NAND Flash
- One NOR QSPI

Additional memory can be added to the board by:

- Installing an SPI and I^2C memory Clickboard on the mikroBUS connector (J25)
- Installing a microSD card in the connector (J14)
- Installing an SD or MMC card with an adapter in the M.2 Key E connector (J20)
- Using the USB ports

Support is dependent upon driver support in the OS.

3.3.1. DDR3L/SDRAM

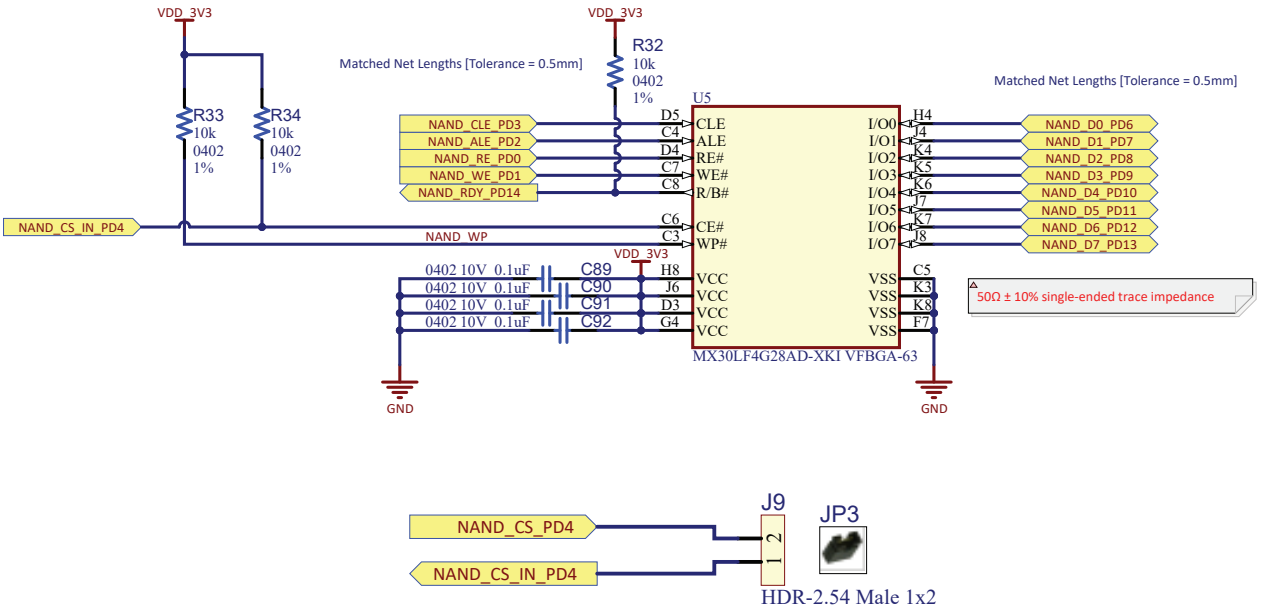
The SAM9X75D2G-I/4TB features an internal 2-Gbit DDR3L SDRAM memory from Winbond, with a 16-bit data bus.

3.3.2. NAND Flash

The SAM9X75-Curiosity board has native support for NAND Flash memory through its NAND Flash controller. The board implements one MX30LF4G28AD 4 Gb (512M x 8) NAND Flash connected to the Chip Select of the microprocessor.

The following figure shows the NAND Flash.

Figure 3-20. NAND Flash



The following table shows the NAND Flash PIO signal description.

Table 3-4. NAND Flash PIO Signal Description

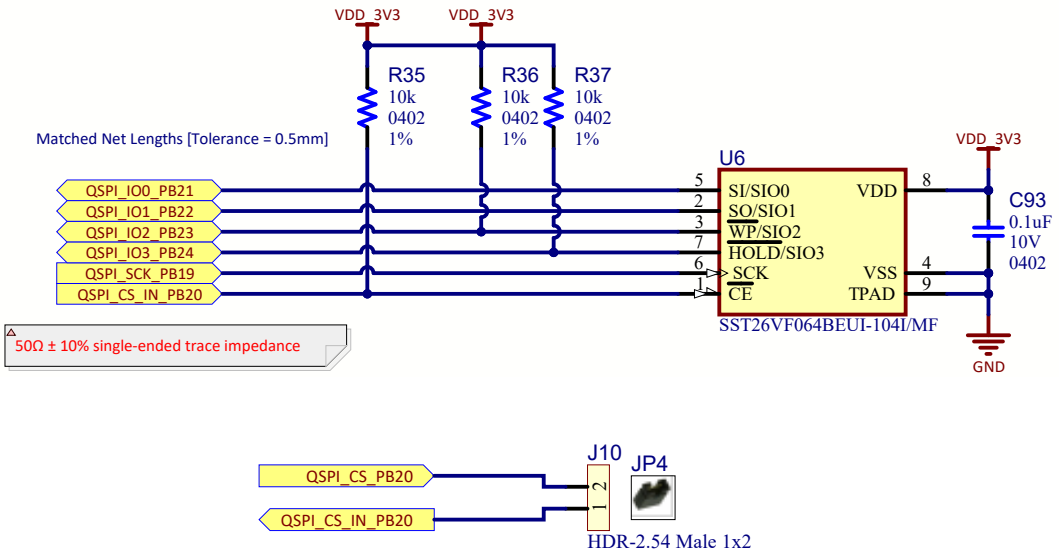
PIO	Signal Name	Signal Description
PD6	NAND_D0_PD6	Data 0
PD7	NAND_D1_PD7	Data 1
PD8	NAND_D2_PD8	Data 2
PD9	NAND_D3_PD9	Data 3
PD10	NAND_D4_PD10	Data 4
PD11	NAND_D5_PD11	Data 5
PD12	NAND_D6_PD12	Data 6
PD13	NAND_D7_PD13	Data 7
PD3	NAND_CLE_PD3	Command Latch Enable
PD2	NAND_ALE_PD2	Address Latch Enable
PD0	NAND_RE_PD0	Read Enable
PD1	NAND_WE_PD1	Write Enable
PD14	NAND_RDY_PD14	Ready/Busy#
PD4	NAND_CS_IN_PD4	Chip Select

3.3.3. QSPI Flash Memory

The SAM9X75-Curiosity board has native support for QSPI Flash memory through its Quad Serial Peripheral Interface. The board implements one SST26VF064BEUIT 64 Mbit Serial Quad I/O (SQI) Flash Memory with EUI-48™ and EUI-64™ identifiers. For more information about the SST26VF064BEUI, refer to the product web page.

The following figure shows the QSPI Flash Memory.

Figure 3-21. SST26VF064BEUI QSPI Flash Memory



The following table shows the QSPI Flash Memory PIO signal description.

Table 3-5. QSPI Flash Memory PIO Signal Description

PIO	Signal Name	Signal Description
PB21	QSPI_IO0_ PB21	Data 0
PB22	QSPI_IO1_ PB22	Data 1
PB23	QSPI_IO2_ PB23	Data 2
PB24	QSPI_IO3_ PB24	Data 3
PB19	QSPI_SCK_ PB19	Clock
PB20	QSPI_CS_ PB20	Chip Select

3.4. Peripherals

Several interfaces and connectors are implemented in the SAM9X75-Curiosity board with the purpose of enabling the user to exploit all the features that the MPU can offer and to facilitate a reference design for future customer applications.

This section describes the following peripherals mounted on the SAM9X75-Curiosity board:

- USB host/device
- mikroBUS interface
- Controller Area Network (CAN) interface
- GPIO interface
- Inter-IC Sound Multi-Channel Controller (I2SMCC) interface
- Gigabit Ethernet interface
- microSD card (Secure Digital Multimedia Card, SDMMC)
- Wireless M.2 interface
- Video LVDS interface
- MIPI camera interface
- LCD module positioning over motherboard

- Audio Class D

3.4.1. USB Host/Device

The USB (Universal Serial Bus) is a hot-pluggable general-purpose high-speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High Speed USB). A USB host bus connector uses four pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin.

The SAM9X75-Curiosity board features three USB communication ports named USB-A to USB-C™.

The USB-A port implementation on SAM9X75-Curiosity can act only as a USB device interface and can be accessed via the USB Micro-B connector (J2).

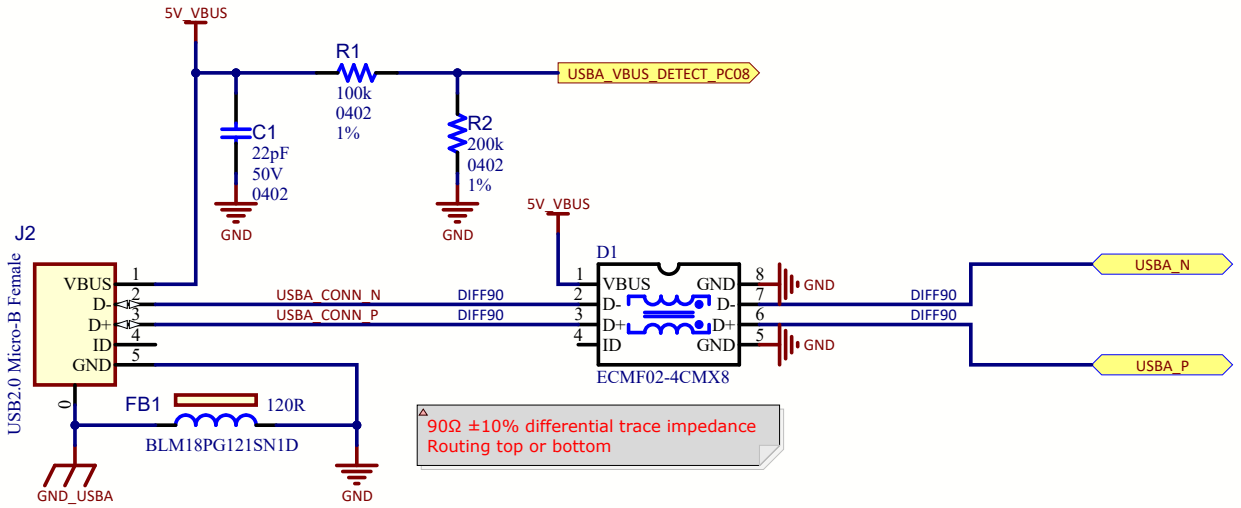
Two resistors (R1 and R2) are placed on its power rail to form a voltage divider, converting 5V into 3.3V that is then used to signal the presence of a USB host to the MPU.

The USB-A port is used as a power source, as mentioned in Power Supply Topology and Power Distribution. In most cases, this port is limited to 500 mA.

In the case of board bring-up, USB-A is the default port used to connect to the MPU over SAM-BA (SAM Boot Assistance). For more information, refer to the product web page.

The following figure shows the USB-A Port.

Figure 3-22. USB-A Port



The following table shows the USB-A connector signal description.

Table 3-6. USB-A Connector Signal Description

Pin No.	Signal Name	Signal Description
0	GND_USBA	Connector chassis connected to ground
1	5V_VBUS	First port 5V power
2	USBA_N	First port data minus
3	USBA_P	First port data plus
4	ID	- (Not used)
5	GND	First port ground

The following table shows the USB-A PIO signal description.

Table 3-7. USB-A PIO Signal Description

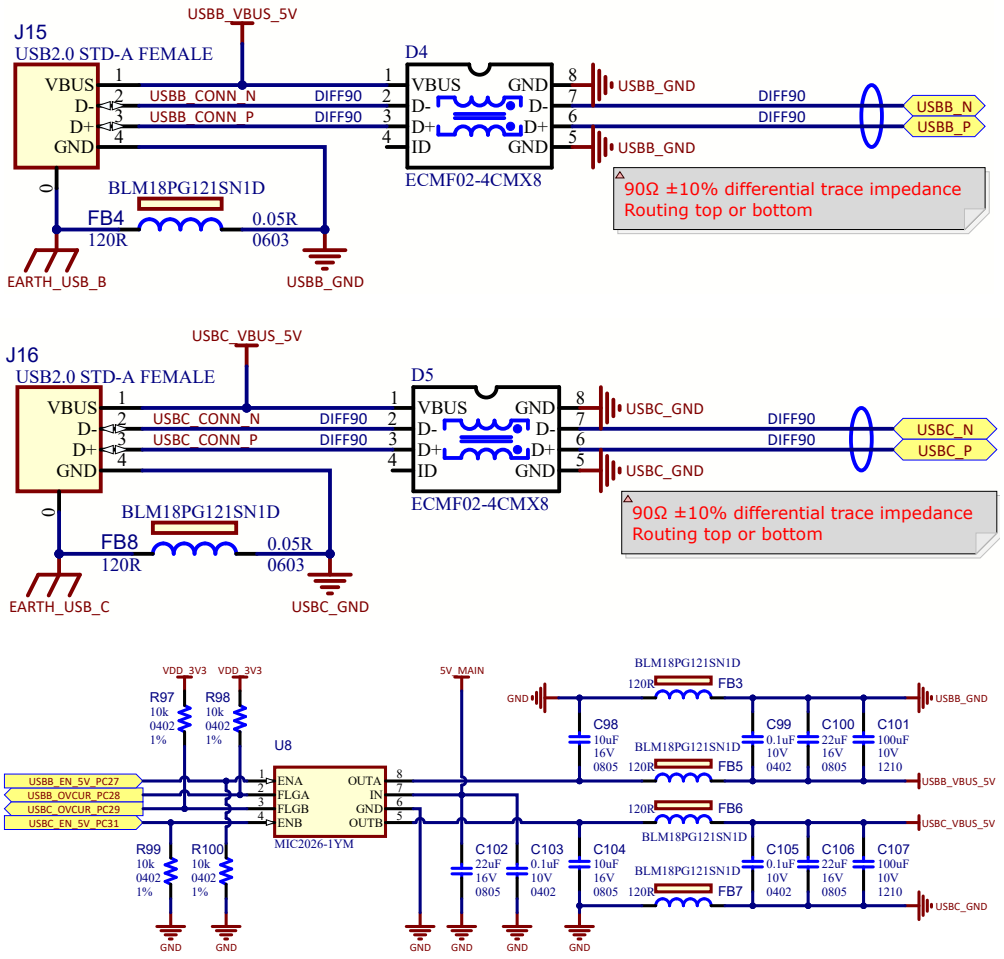
PIO	Signal Name	Signal Description
PC08	USBA_VBUS_DETECT_PC08	VBUS detection

The USB-B and USB-C ports are connected to both USB Type-A connectors (J15 and J16) and can act as hosts.

USB Host ports B and C are equipped with 500 mA high-side power switches to enable self-powered and bus-powered applications. The USBB_EN_5V_PC27 and USBC_EN_5V_PB18 signals control the current limiting power switch, MIC2026, which in turn supplies power to a client device. Per the USB specification, bus-powered USB 2.0 devices are limited to a maximum of 500 mA, therefore the MIC2026 limits the current and indicates an overcurrent with the USBB_OVCUR_PC28 and USBC_OVCUR_PC29 signals. For more information about the MIC2026, refer to the product web page.

The following figure shows the USB-B and USB-C ports.

Figure 3-23. USB-B and USB-C Ports



The following table shows the USB-B and USB-C connectors signal description.

Table 3-8. USB-B and USB-C Connectors Signal Description

Pin No.	Signal Name	Signal Description
(J15) 0	EARTH_USB_B	Connector chassis connected to ground
(J15) 1	USBB_VBUS_5V	Second port 5V power
(J15) 2	USBB_N	Second port data minus
(J15) 3	USBB_P	Second port data plus
(J15) 5	GND	Second port ground
(J16) 0	EARTH_USB_C	Connector chassis connected to ground
(J16) 1	USBC_VBUS_5V	Third port 5V power
(J16) 2	USBC_N	Third port data minus
(J16) 3	USBC_P	Third port data plus
(J16) 5	GND	Third port ground

The following table shows the USB-B and USB-C Power Switch PIO signal description.

Table 3-9. USB-B and USB-C Power Switch PIO Signal Description

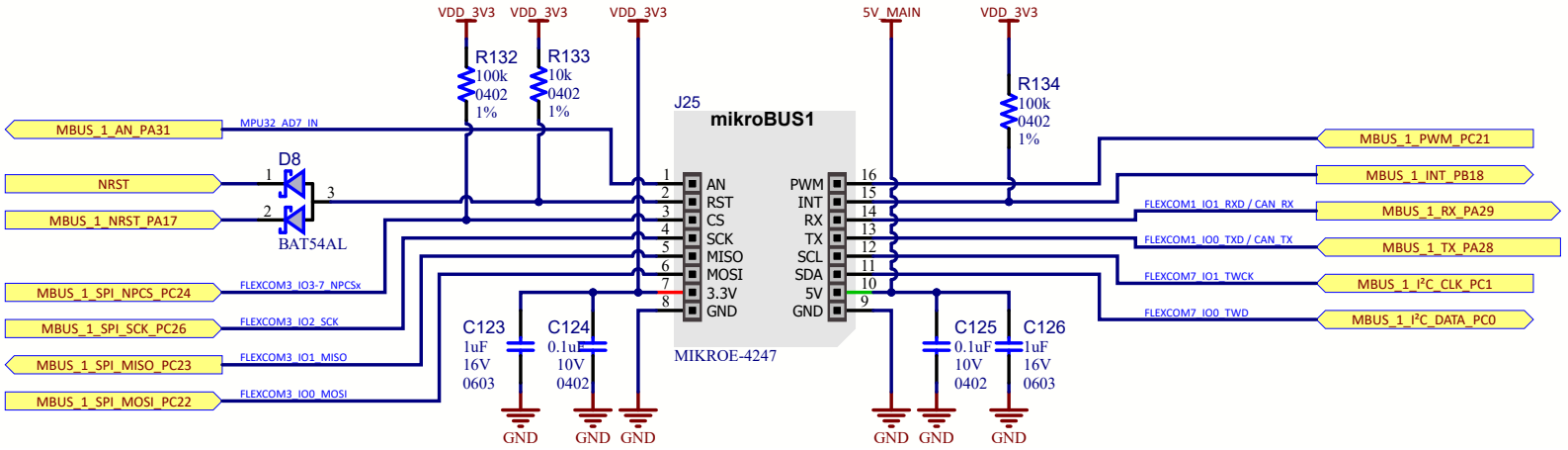
PIO	Signal Name	Signal Description
PC27	USBB_EN_ 5V_PC27	Power switch USBB enable (active high)
PC28	USBB_OVCUR_PC28	Indicates overcurrent USBB (open drain)
PC29	USBC_OVCUR_PC29	Indicates overcurrent USBC (open drain)
PC31	USBC_EN_ 5V_PC31	Power switch USBC enable (active high)

3.4.2. mikroBUS Interface

The SAM9X75-Curiosity board hosts a mikroBUS socket (J25) with PTA (Packet Traffic Arbitration) connector for wireless communications (J26). The mikroBUS standard defines the main board sockets and add-on boards used for interfacing the microprocessor with integrated modules having a proprietary pin configuration. For details, refer to the mikroBUS documentation on www.mikroe.com/mikrobus.

The following figure shows the mikroBUS interface.

Figure 3-24. mikroBUS Interface



The following table shows the mikroBUS connector signal description.

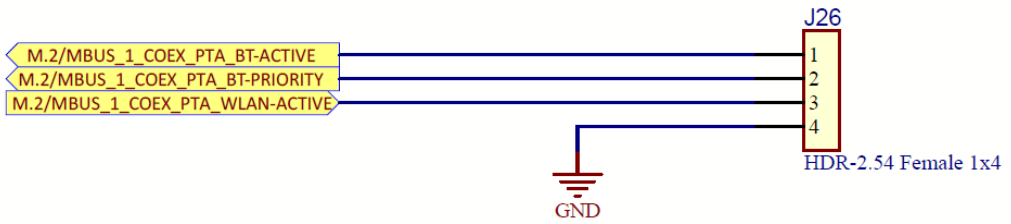
Table 3-10. mikroBUS Connector Signal Description

Pin No.	PIO	Signal Name	Signal Description
1	PA31	MBUS_1_AN_PA31	Analog
2	NRST or PA17	NRST or NRST_OUT_PC25	Reset
3	PC24	MBUS_1_SPI_NPCS_PC24	SPI Chip Select
4	PC26	MBUS_1_SPI_SCK_PC26	SPI Clock
5	PC23	MBUS_1_SPI_MISO_PC23	SPI MISO
6	PC22	MBUS_1_SPI_MOSI_PC22	SPI MOSI
7	–	VDD_3V3	3.3V
8	–	GND	GND
9	–	GND	GND
10	–	5V_MAIN	5V
11	PC0	MBUS_1_I^{2}C_DATA_PC0	TWI Data
12	PC1	MBUS_1_I^{2}C_CLK_PC1	TWI Clock
13	PA28	MBUS_1_TX_PA28	UART Transmit
14	PA29	MBUS_1_RX_PA29	UART Receive
15	PB18	MBUS_1_INT_PB18	Interrupt
16	PC21	MBUS_1_PWM_PC21	Pulse Width Modulated

The SAM9X75-Curiosity board can embed several radio solutions using the 2.4 GHz radio bandwidth with Wi-Fi and Bluetooth solutions. The coexistence between the radio modules is necessary to ensure a good packet transfer rate and pass RED and FCC certifications. The PTA interface between the modules consists of a set of 3-wire signals and organizes wireless packet traffic for communication protocols operating in the same frequency band without affecting RF performance by intelligently sharing the frequency band.

The following figure shows the mikroBUS PTA interface for Wireless.

Figure 3-25. mikroBUS PTA for Wireless Connector



The following table shows the mikroBUS PTA for Wireless connector signal description.

Table 3-11. mikroBUS PTA for Wireless Connector Signal Description

Pin No.	PIO	Signal Name	Signal Description
1	–	MBUS_1_COEX_PTA_BT-ACTIVE	PTA Bluetooth Active Input
2	–	MBUS_1_COEX_PTA_BT-PRIORITY	PTA Bluetooth Priority Input
3	–	MBUS_1_COEX_PTA_BT-WLAN-ACTIVE	PTA Wireless LAN Active Output
4	–	GND	Ground

3.4.3. Controller Area Network (CAN) Interface

The SAM9X75D2G has native support for Controller Area Network (CAN). The SAM9X75-Curiosity board shares the CAN interface with the UART signals of the mikroBUS connector (J25). Use the mikroBUS Click MIKROE-2299 that embeds a Microchip MCP2542WFD to connect the SAM9X75-Curiosity to a CAN network.

The MCP2542 is a high-speed CAN transceiver that provides the interface between the CAN protocol controller and the physical two-wire bus. For more information about the MCP2542, refer to the product web page.

The following table shows the CAN interface in mikroBUS connector signal description.

Table 3-12. CAN Interface in mikroBUS Connector Signal Description

Pin No.	PIO	Signal Name	Signal Description
13	PA28	MBUS_1_TX_PA28	CAN Transmit
14	PA29	MBUS_1_RX_PA29	CAN Receive

3.4.4. GPIO Interface

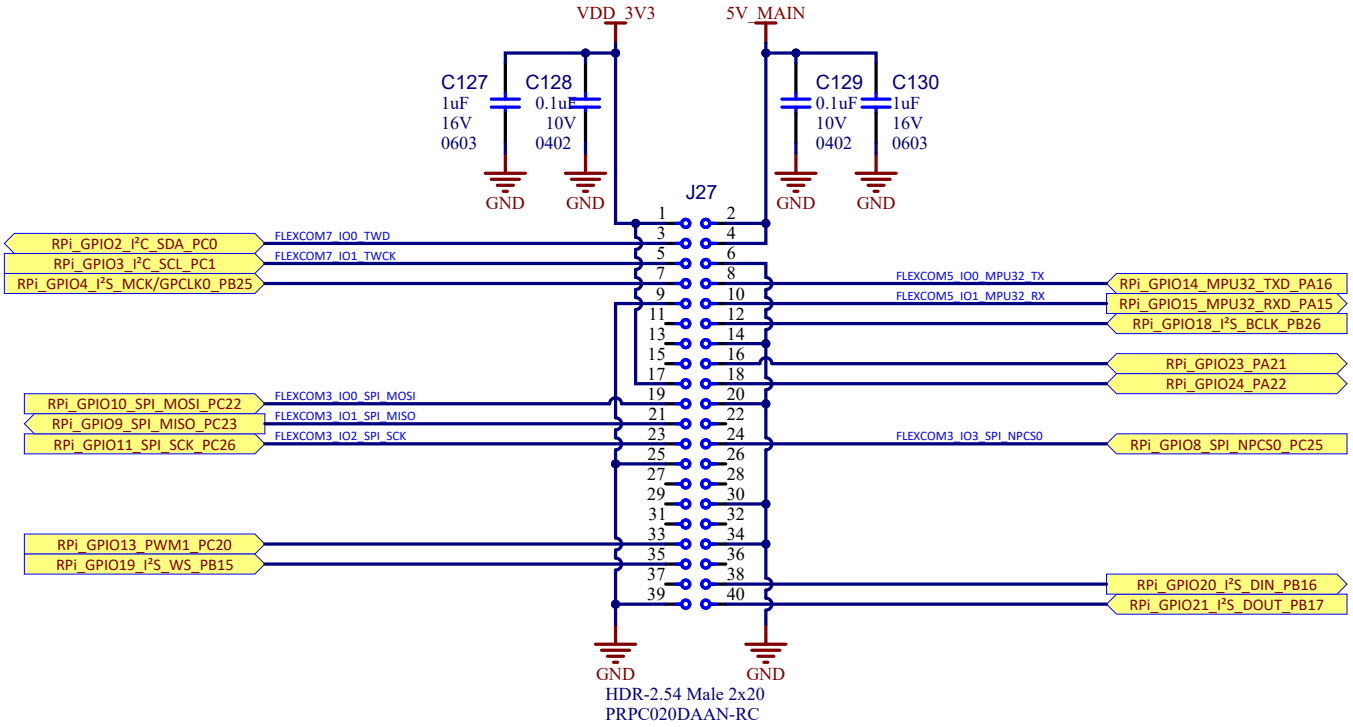
The SAM9X75-Curiosity board features a 40-pin connector (J27) (Raspberry Pi compatible[1]) for free use.

Note:

1. Raspberry Pi is a trademark of Raspberry Pi Trading.

The following figure shows the 40-pin connector interface.

Figure 3-26. 40-pin Connector Interface



The following table shows the 40-pin connector the signal description.

Table 3-13. 40-pin Connector Signal Description

Pin No.	PIO	Signal Name	Signal Description
1	–	VDD_3V3	3.3V
2	–	5V_MAIN	5V
3	PC0	RPi_GPIO2_I²C_SDA_PC0	TWI Data
4	–	5V_MAIN	5V
5	PC1	RPi_GPIO3_I²C_SCL_PC1	TWI Clock

Table 3-13. 40-pin Connector Signal Description (continued)

Pin No.	PIO	Signal Name	Signal Description
6	–	GND	GND
7	PB25	RPi_GPIO4_I²S_MCK/GPCLK0_PB25	I²S Host Clock
8	PA16	RPi_GPIO14_MPU32_TXD_PA16	UART Transmit
9	–	GND	GND
10	PA15	RPi_GPIO15_MPU32_RXD_PA15	UART Receive
11	–	NC	Not Connected
12	PB26	RPi_GPIO18_I²S_BCLK_PB26	I²S Clock
13	–	NC	Not Connected
14	–	GND	GND
15	–	NC	Not Connected
16	PA21	RPi_GPIO23_PA21	General Purpose I/O
17	–	VDD_3V3	3.3V
18	PA22	RPi_GPIO24_PA22	General Purpose I/O
19	PC22	RPi_GPIO10_SPI_MOSI_PC22	SPI MOSI
20	–	GND	GND
21	PC23	RPi_GPIO9_SPI_MISO_PC23	SPI MISO
22	–	NC	Not Connected
23	PC26	RPi_GPIO11_SPI_SCK_PC26	SPI Clock
24	PC25	RPi_GPIO8_SPI_NPCS0_PC25	SPI Chip Select
25	–	GND	GND
26	–	NC	Not Connected
27	–	NC	Not Connected
28	–	NC	Not Connected
29	–	NC	Not Connected
30	–	GND	GND
31	–	NC	Not Connected
32	–	NC	Not Connected
33	PC20	RPi_GPIO13_PWM1_PC20	Pulse Width Modulated
34	–	GND	GND
35	PB15	RPi_GPIO19_I²S_WS_PB15	I²S Word Select
36	–	NC	Not Connected
37	–	NC	Not Connected
38	PB16	RPi_GPIO20_I²S_DIN_PB16	I²S Data IN
39	–	GND	GND
40	PB17	RPi_GPIO21_I²S_DOUT_PB17	I²S Data OUT

3.4.5. Inter-IC Sound Multi-Channel Controller (I2SMCC) Interface

The SAM9X75D2G has native support for Inter-IC Sound Controller (I2SMCC) and provides a 5-wire, bidirectional, synchronous, digital audio link to external audio devices.

With the purpose of enabling the user to test this feature, the SAM9X75-Curiosity board has the I²S signals in the 40-pin connector (J27). Many Raspberry Pi(1) Hats with I2S are available.

Note:

1. Raspberry Pi is a trademark of Raspberry Pi Trading.

The following table shows the I²S interface in 40-pin connector signal description.

Table 3-14. I²S Interface in 40-pin Connector Signal Description

Pin No.	PIO	Signal Name	Signal Description
7	PB25	RPi_GPIO4_I²S_MCK/GPCLK0_PB25	I²S Host Clock
12	PB26	RPi_GPIO18_I²S_BCLK_PB26	I²S Clock
35	PB15	RPi_GPIO19_I²S_WS_PB15	I²S Word Select
38	PB16	RPi_GPIO20_I²S_DIN_PB16	I²S Data IN
40	PB17	RPi_GPIO21_I²S_DOUT_PB17	I²S Data OUT

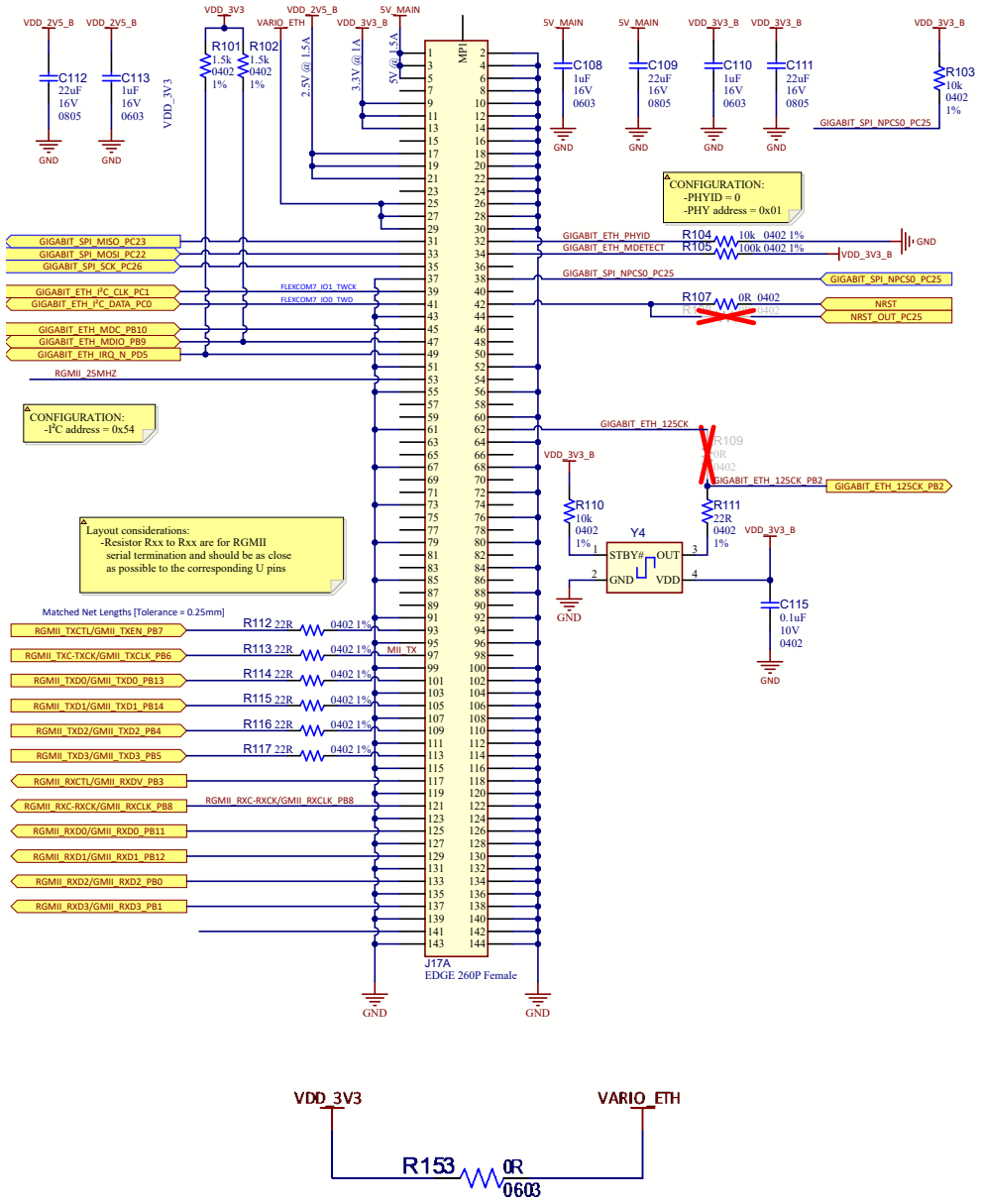
3.4.6. Gigabit Ethernet Interface

The SAM9X75-Curiosity board embeds a modular Ethernet PHY system (Gigabit Ethernet Interface through SODIMM connector) that enables different PHYs and switches to be plugged into the board. This interface is set up to use one Reduced Gigabit Media-Independent Interface (RGMII), a PTP interface, SERDES interfaces and an I²C bus interface with GPIO.

The same connector also provides an SPI communication bus for compatible daughter boards. In order to enable the SPI communication, jumper JP5 needs to be connected between positions two and three of the J11 header.

The following figure shows the Gigabit Ethernet interface.

Figure 3-27. Gigabit Ethernet Interface



The following table shows the Gigabit Ethernet interface signal description.

Table 3-15. Gigabit Ethernet Interface Signal Description

Pin No.	PIO	Signal Name	Signal Description
1, 3, 5	–	5V_MAIN	5V

Table 3-15. Gigabit Ethernet Interface Signal Description (continued)

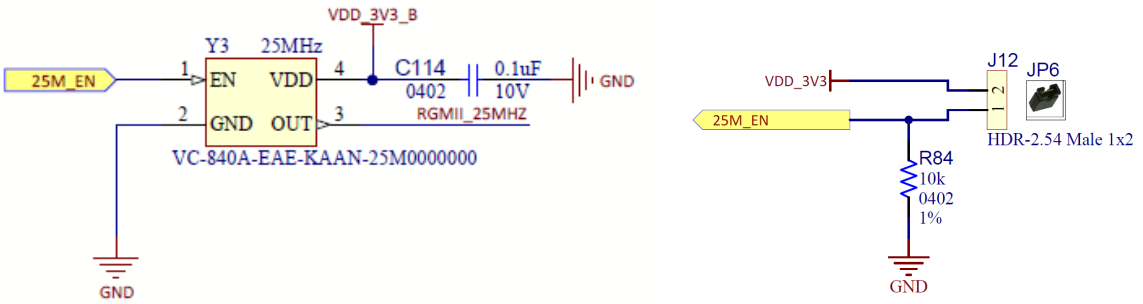
Pin No.	PIO	Signal Name	Signal Description
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 37, 43, 51, 52, 55, 56, 60, 61, 67, 68, 72, 73, 76, 79, 80, 84, 85, 91, 92, 95, 96, 99, 100, 103, 104, 106, 107, 108, 110, 111, 112, 114, 115, 116, 118, 119, 120, 122, 123, 124, 126, 127, 128, 130, 131, 132, 134, 135, 136, 138, 139, 140, 142, 143, 144, 145, 146, 149, 151, 155, 159, 163, 167, 171, 175, 179, 183, 187, 191, 195, 199, 203	–	GND	Ground
9, 11, 13	–	VDD_3V3_B	3.3V
17, 19, 21	–	VDD_2V5_B	2.5V
25, 27, 29	–	VARIO_ETH	3.3V
31	PC23	GIGABIT_SPI_MISO	SPI Host Input Signal
32	–	GIGABIT_ETH_ PHYID	Pull-Down
33	PC22	GIGABIT_SPI_MOSI	SPI Host Output Signal
34	–	GIGABIT_ETH_MDETECT	Pull-Up
35	PC26	GIGABIT_SPI_SCK	SPI Clock Signal
38	PC25	GIGABIT_SPI_NPCS0	SPI Chip Select signal
39	PC1	GIGABIT_ETH_I^{2}C_CLK_PC1	TWI Clock
41	PC0	GIGABIT_ETH _I^{2}C_DATA_PC0	TWI Data
42	NRST or PC25	NRST or NRST_OUT	Reset
45	PB10	GIGABIT_ETH_MDC	Management Data Clock
47	PB9	GIGABIT_ETH_MDIO	Management Data Input/Output
49	PD5	GIGABIT_ETH_IRQ_N	Interrupt
53	–	RGMII_25MHZ	Clock 25 MHz
62	PB2	GIGABIT_ETH_125CK	125 MHz Clock
93	PB7	RGMII_TXCTL/GMII_TXEN	Transmit Enable or Transmit Control
97	PB6	RGMII_TXC-TXCK/GMII_TXCLK	Transmit Clock
101	PB13	RGMII_TXD0/GMII_TXD0	Transmit Data 0
105	PB14	RGMII_TXD1/GMII_TXD1	Transmit Data 1
109	PB4	RGMII_TXD2/GMII_TXD2	Transmit Data 2
113	PB5	RGMII_TXD3/GMII_TXD3	Transmit Data 3
117	PB3	RGMII_RXCTL/GMII_RXDV	Receive Control or Receive Data Valid
121	PB8	RGMII_RXC-RXCK/GMII_RXCLK	Receive Clock
125	PB11	RGMII_RXD0/GMII_RXD0	Receive Data 0
129	PB12	RGMII_RXD1/GMII_RXD1	Receive Data 1
133	PB0	RGMII_RXD2/GMII_RXD2	Receive Data 2
137	PB1	RGMII_RXD3/GMII_RXD3	Receive Data 3

3.4.6.1. Clock for Gigabit Ethernet interface

The Gigabit Ethernet modules need to be clocked by an external clock source available on the SAM9X75-Curiosity board.

The following figure shows the clock for the Gigabit Ethernet interface.

Figure 3-28. Gigabit Ethernet Interface Clock



3.4.6.2. Provision for EMI Filtering

In the event that CE RED or FCC certification is required, the board can be fine-tuned using LC filtering positions on various clock lines near connectors and devices. These positions are available but not populated by default.

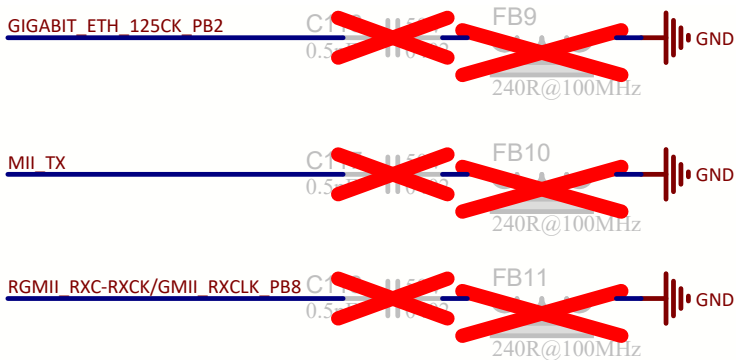
Mounting the components will help reduce EMI during the test.

The following filter (with components not populated) is available and placed on the following nodes:

- GIGABIT_ETH_125CK
- MII_TX
- MII_RX

The following figure shows the EMI filtering.

Figure 3-29. EMI Filtering

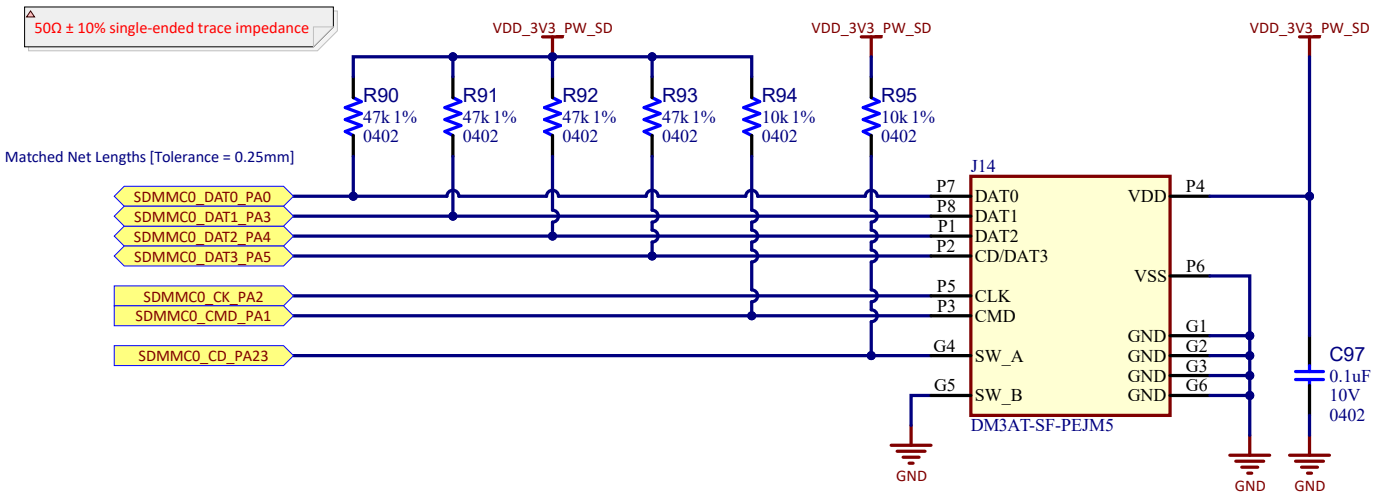


3.4.7. Micro Secure Digital Multimedia Cards (SDMMC)

The SAM9X75-Curiosity board embeds a standard microSD card connector, connected to the SDMMC interface, also mounted on the top side of the board. The SDMMC0 communication is based on an 8-pin interface (clock, command, four data and power lines). It includes a card detection switch. This connector gives access to the boot environment.

The following figure shows the microSD card connector.

Figure 3-30. microSD Card Connector



The following table shows the SD card connector signal description.

Table 3-16. microSD Card Signal Description

Pin No.	PIO	Signal Name	Signal Description
P1	PA4	SDMMC0_DAT2	Data 2
P2	PA5	SDMMC0_DAT3	Data 3
P3	PA1	SDMMC0_CMD	Card command
P4	–	VDD_3V3_PW_SD	3.3V
P5	PA2	SDMMC0_CK	Clock
P6, G5	–	GND	GND
P7	PA0	SDMMC0_DAT0	Data 0
P8	PA3	SDMMC0_DAT1	Data 1
G4	PA23	SDMMC0_CD	Card detect
G1, G2, G3, G6	–	-	Connected to GND

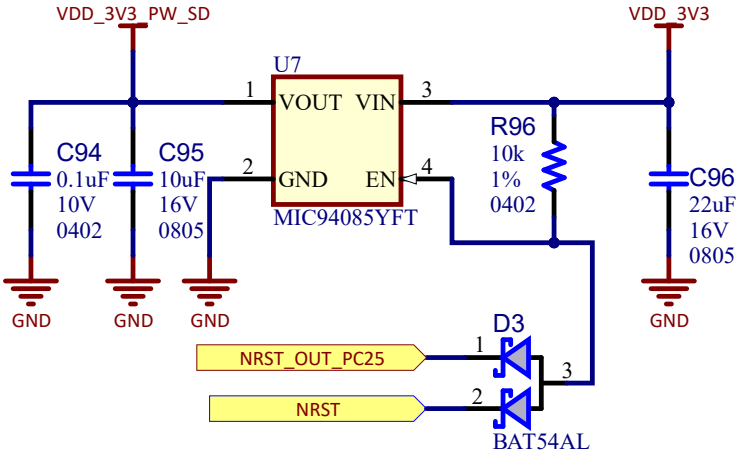
3.4.7.1. microSD Card Reset

The user can perform a hard reset of the SD card by using the processor reset line "NRST_OUT" signal (disabled by default) or the “NRST” reset system.

This action disables the MIC94085YFT power switch and forces VDD_SDCARD to ground. For more details about the MIC94085YFT power switch, refer to the product web page.

The following figure shows the microSD Card Reset schematic.

Figure 3-31. microSD Card Reset



3.4.8. Wireless M.2 Interface

The SAM9X75-Curiosity board embeds an M.2 connector to interconnect with Wireless modules.

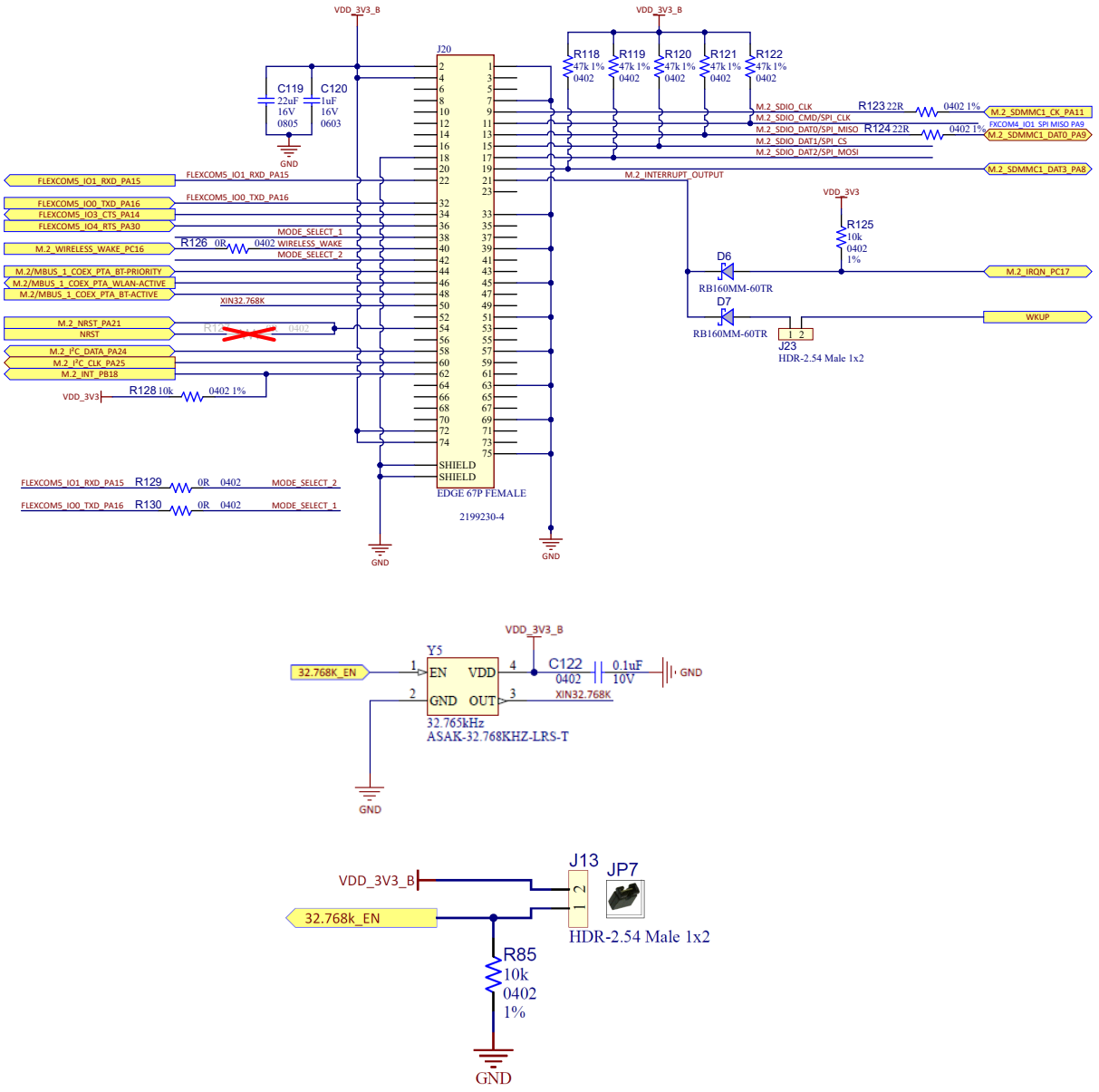
M.2 (formerly known as NGFF) is a small form factor card and connector that supports applications such as Wi-Fi, WLAN, USB, PCIe and SATA, as defined in the PCI-SIG M.2 Specification.

The default interface used with the Wireless Module solution is the SDIO. However, the Wireless module can be controlled in SPI mode and configuration can be performed manually by the end user.

The interface is based on a 67-pin connector and includes clock, SDIO/SPI interface, USART Interface, wake-up/interrupt, reset and power lines.

The following figure shows the M.2 Wireless module interface.

Figure 3-32. M.2 Wireless Module Interface



The following table shows the M.2 Wireless module interface signal description.

Table 3-17. M.2 Wireless Module Interface Signal Description

Pin No.	PIO	Signal Name	Signal Description
1, 7, 18, 33, 39, 45, 51, 57, 63, 69, 75	–	GND	Ground
2, 4, 72, 74	–	VDD_3V3_B	3.3V
9	PA11	SDMMC1_CK	SDIO Clock Input
11	PA10 or PA11	SDMMC1_CMD or FXCOM4_IO2 SPI CLK	SDIO Command or SPI Clock Input
13	PA9	SDMMC1_DAT0	SDIO Data 0 or SPI MISO
15	PA6 or PA13	SDMMC1_DAT1 or FXCOM4_IO4 SPI CS	SDIO Data 1 or SPI Chip Select (CS)
17	PA7 or PA10	SDMMC1_DAT2 or FXCOM4_IO0 SPI MOSI	SDIO Data 2 or SPI MOSI

Table 3-17. M.2 Wireless Module Interface Signal Description (continued)

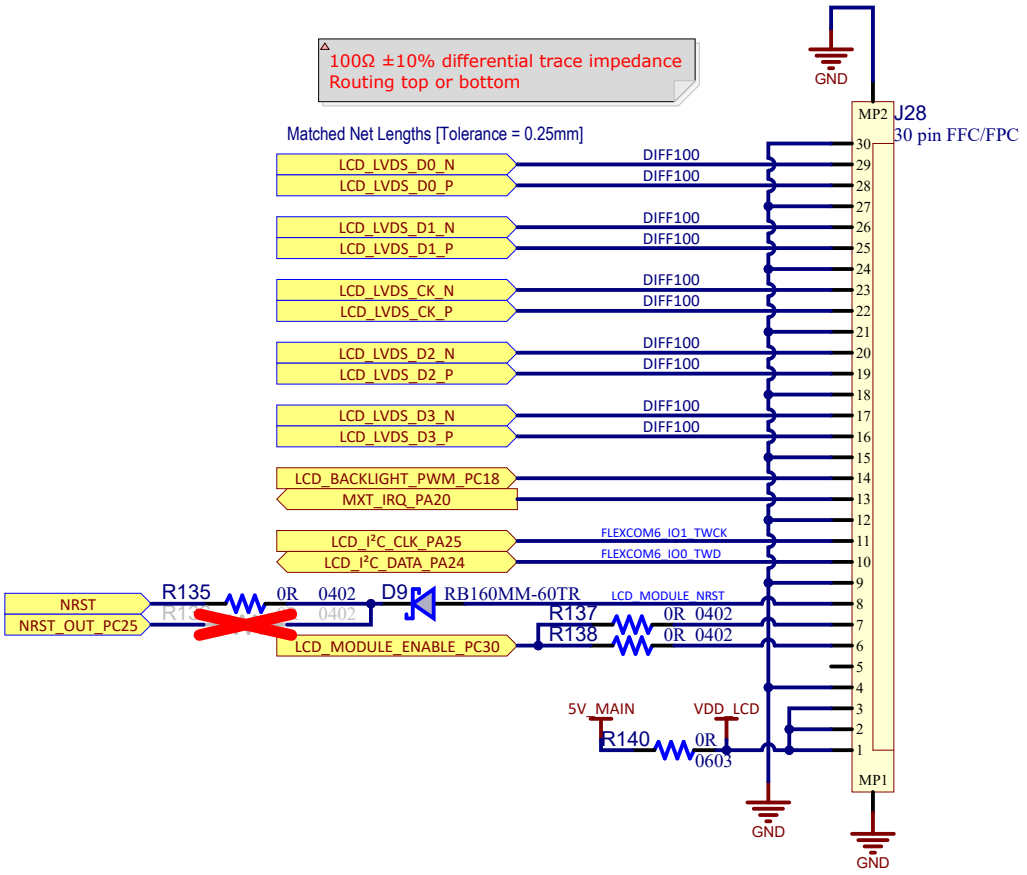
Pin No.	PIO	Signal Name	Signal Description
19	PA8	SDMMC1_DAT3	SDIO Data 3
21	WKUP0 or PC17	WKUP or IRQN	Wake host (interrupt) or Output (UART/SPI/SDIO)
22	PA15	FLEXCOM5_IO1_RXD	UART Rx connected to Bluetooth UART TxD Output
32	PA16	FLEXCOM5_IO0_TXD	UART Tx connected to Bluetooth UART RxD Input
34	PA14	FLEXCOM5_IO3_CTS	UART CTS connected to Bluetooth UART RTS Output
36	PA30	FLEXCOM5_IO4_RTS	UART RTS connected to Bluetooth UART CTS Input
38	–	MODE_SELECT_1/DFU_RX	Mode Select Input 1 of the M.2 Interface configuration
40	PC16	WIRELESS_WAKE	Wake Wireless Device Input
42	–	MODE_SELECT_2/DFU_TX	Mode Select Input 2 of the M.2 Interface configuration
44	–	MBUS_1_COEX_PTA_BT-PRIORITY	PTA Bluetooth Priority Input
46	–	MBUS_1_COEX_PTA_WLAN-ACTIVE	PTA Wireless LAN Active Output
48	–	MBUS_1_COEX_PTA_BT-ACTIVE	PTA Bluetooth Priority Input
50	–	XIN32.768K	32.768 kHz clock module input
54	NRST or PC25	NRST or NRST_OUT	Reset
58	PA24	M.2_I²C_DATA	TWI Data
60	PA25	M.2_I²C_CLK	TWI Clock
62	PC31	M.2_INT	TWI interrupt

3.4.9. Video LVDS Interface

The SAM9X75-Curiosity board embeds a 4-lane LVDS interface to be used with LVDS compatible displays.

The following figure shows the video LVDS interface.

Figure 3-33. Video LVDS Interface



The following table shows the video LVDS interface signal description.

Table 3-18. Video LVDS Interface Signal Description

Pin No.	PIO	Signal Name	Signal Description
1, 2, 3	–	VDD_LCD	5V
4, 9, 12, 15, 18, 21, 24, 27, 30	–	GND	Ground
6	PC30	LCD_MODULE_ENABLE	Data enable
7	PC30	LCD_DISP	Display enable signal
8	NRTS or PC25	NRTS or NRTS_OUT	Reset
10	PA24	LCD_I²C_DATA	TWI Data
11	PA25	LCD_I²C_CLK	TWI Clock
13	PA20	MXT_IRQ	Interruption
14	PC18	LCD_BACKLIGHT_PWM	Backlight control
16	PC13	LCD_LVDS_D3_P	LVDS positive differential data 3
17	PC12	LCD_LVDS_D3_N	LVDS negative differential data 3
19	PC7	LCD_LVDS_D2_P	LVDS positive differential data 2
20	PC6	LCD_LVDS_D2_N	LVDS negative differential data 2
22	PC11	LCD_LVDS_CK_P	LVDS positive differential clock
23	PC10	LCD_LVDS_CK_N	LVDS negative differential clock
25	PC5	LCD_LVDS_D1_P	LVDS positive differential data 1
26	PC4	LCD_LVDS_D1_N	LVDS negative differential data 1
28	PC3	LCD_LVDS_D0_P	LVDS positive differential data 0

Table 3-18. Video LVDS Interface Signal Description (continued)			
Pin No.	**PIO**	**Signal Name**	**Signal Description**
29	PC2	LCD_LVDS_D0_N	LVDS negative differential data 0

3.4.10. MIPI CSI/DSI Interface

The SAM9X75-Curiosity board embeds a 4-lane MIPI D-PHY for interfacing with CSI compatible cameras and DSI compatible displays.

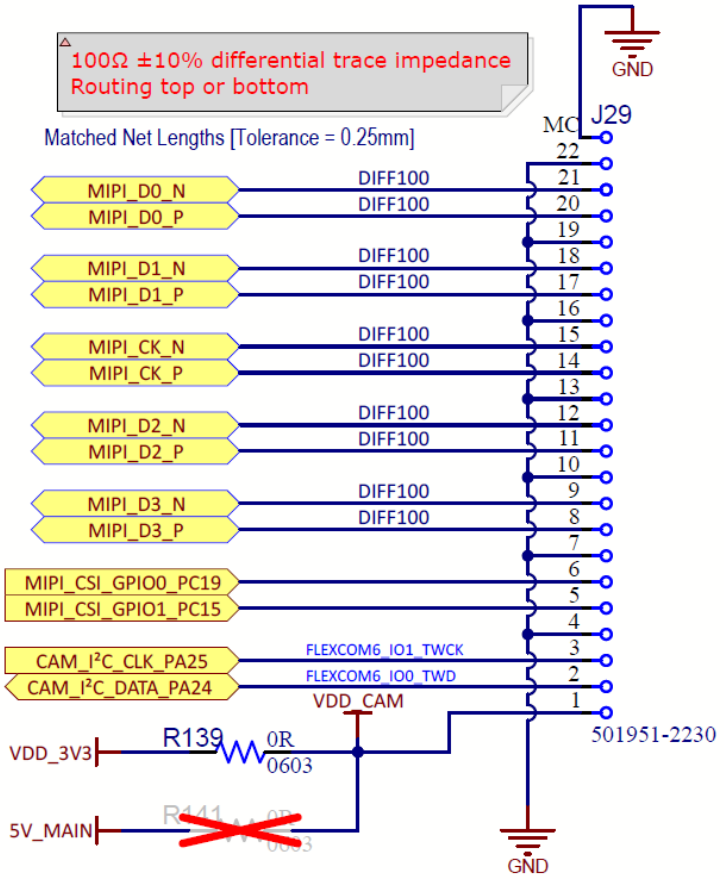
The board features a 22-pin FPC/FFC connector (J29) with 0.5 mm pitch, similar to the one used for the Raspberry Pi Compute Module boards. 4-lane MIPI cameras can connect to the board directly, while 2-lane cameras and displays provided by Raspberry Pi[(1)] require a 22-pin to 15-pin FPC adapter. For 4-lane MIPI displays, an adapter is necessary due to various non-standard connector pinout across different manufacturers. Additional GPIOs and TWI interface are provided for camera/display control.

Note:

1. Raspberry Pi is a trademark of Raspberry Pi Trading.

The following figure shows the MIPI CSI camera interface.

Figure 3-34. MIPI CSI Camera Interface



The following table shows the MIPI CSI/DSI interface signal description.

Table 3-19. MIPI CSI/DSI Interface Signal Description

Pin No.	PIO	Signal Name	Signal Description
1, 4, 7, 10, 13, 16, 19	–	GND	Ground

Table 3-19. MIPI CSI/DSI Interface Signal Description (continued)

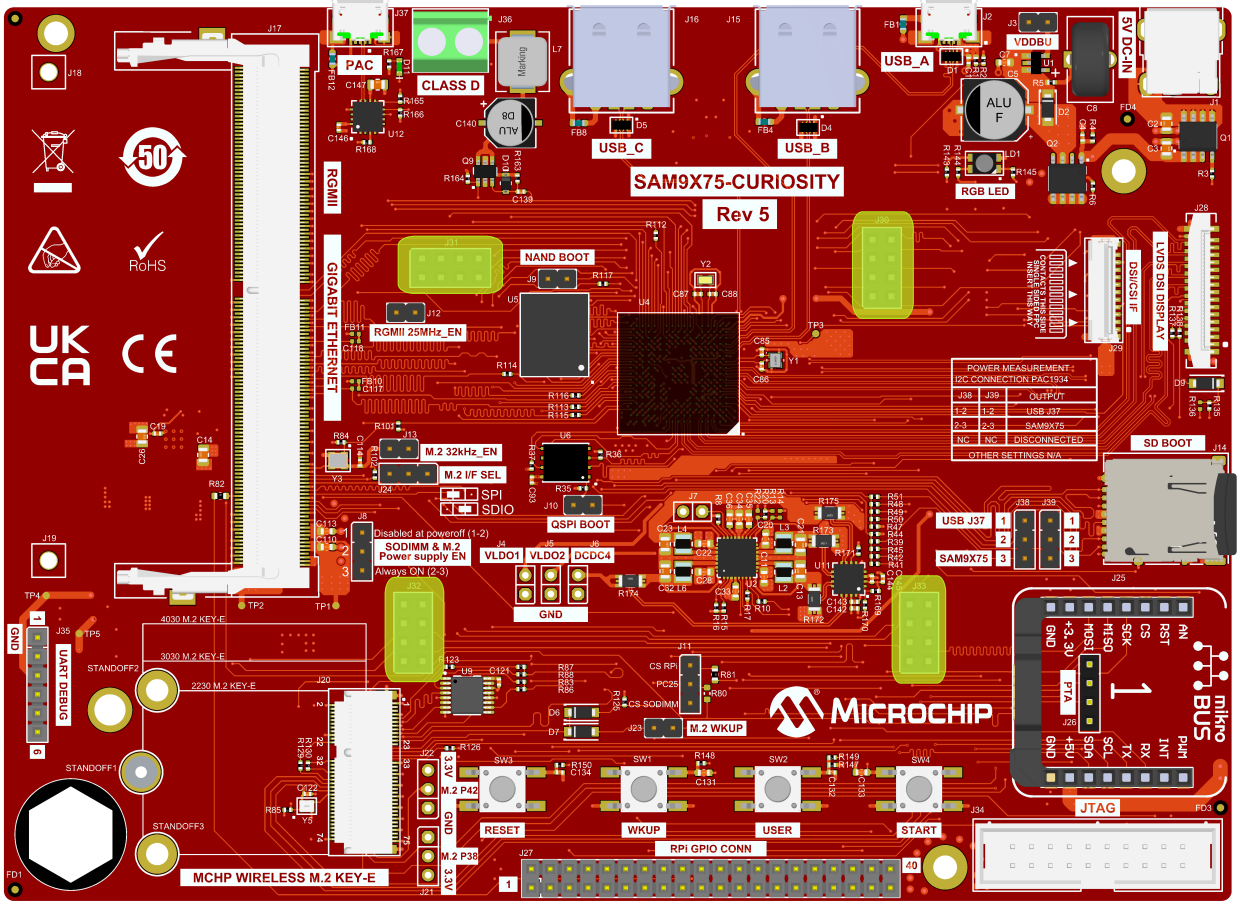
Pin No.	PIO	Signal Name	Signal Description
2	–	MIPI_D0_N	MIPI D-PHY negative differential input data 0
3	–	MIPI_D0_P	MIPI D-PHY positive differential input data 0
5	–	MIPI_D1_N	MIPI D-PHY negative differential input data 1
6	–	MIPI_D1_P	MIPI D-PHY positive differential input data 1
8	–	MIPI_CK_N	MIPI D-PHY negative differential input clock
9	–	MIPI_CK_P	MIPI D-PHY positive differential input clock
11	–	MIPI_D2_N	MIPI D-PHY negative differential input data 2
12	–	MIPI_D2_P	MIPI D-PHY positive differential input data 2
14	–	MIPI_D3_N	MIPI D-PHY negative differential input data 3
15	–	MIPI_D3_P	MIPI D-PHY positive differential input data 3
17	PC19	MIPI_CSI_GPIO0	General Purpose I/O
18	PC15	MIPI_CSI_GPIO1	General Purpose I/O
20	PA25	CAM_I²C_CLK_	TWI Clock
21	PA24	CAM_I²C_DATA	TWI Data
22	–	VDD_3V3 or 5V_MAIN	3.3V or 5V

3.4.11. LCD Module Positioning over Motherboard

Compatible Microchip LCD modules (LVDS and MIPI DSI) can be connected to the SAM9X75-Curiosity board. To ensure mechanical stability, four connectors (J30, J31, J32 and J33) are placed around the core system with specific orientation to maintain proper connection.

The following figure shows the four connectors for LCD module positioning.

Figure 3-35. Four Connectors for LCD Module Positioning



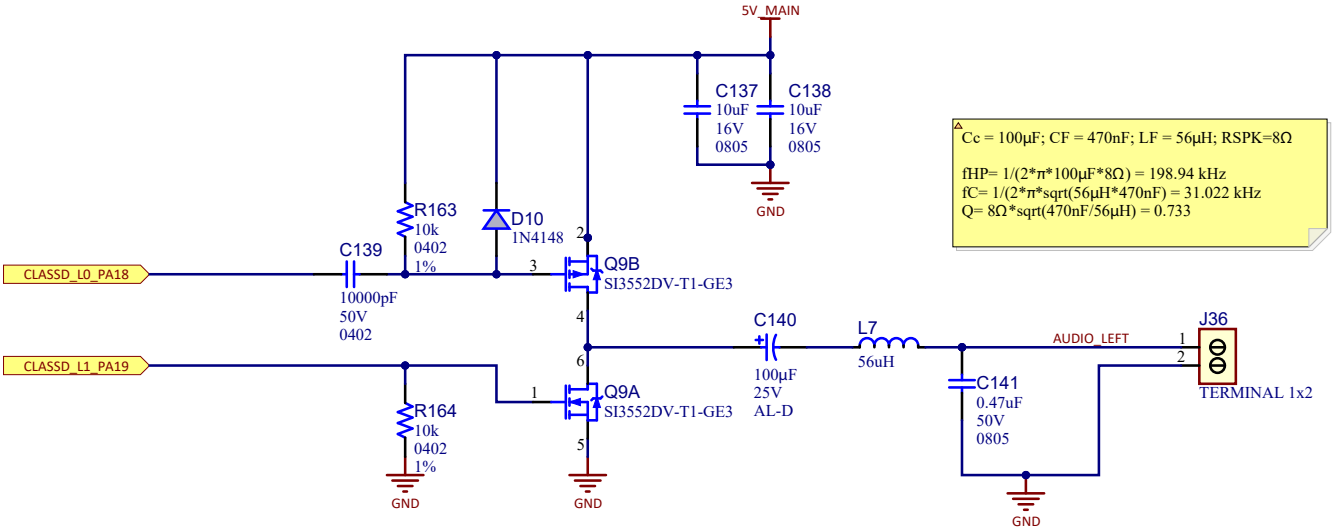
3.4.12. Audio Class D

The SAM9X75-Curiosity board embeds a mono/single-ended channel Class D audio output.

The following figure shows the Audio Class D schematic.

⚠ WARNING The threshold of the featured transistor bridge Q9 (SI3552DV-T1-GE3) implemented on the audio output is too high, which results in a signal distortion. For best audio quality, we recommend replacing Q9 with either of these footprint-compatible alternates: FDC6327C (Fairchild/Onsemi) or BSL215CH (Infineon).

Figure 3-36. Audio Class D Schematic



The following table shows the Audio Class D signal description.

Table 3-20. Audio Class D Signal Description

PIO	Signal Name	Signal Description
PA18	CLASSD_L0	High side PMOS control
PA19	CLASSD_L1	Low side NMOS control

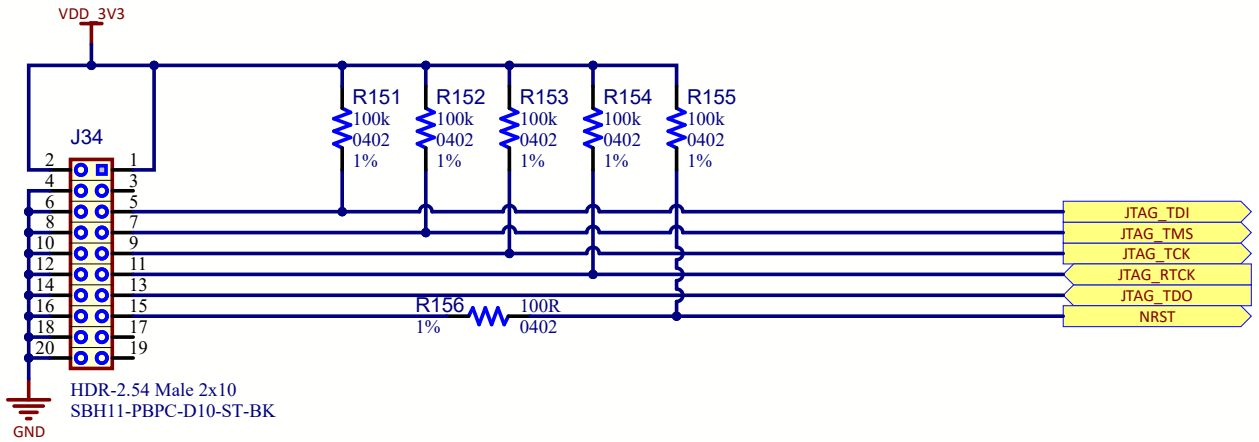
3.5. User Interaction and Debugging

3.5.1. Debug JTAG

The SAM9X75-Curiosity board includes a 20-pin JTAG header (J34) to facilitate software development and debugging using various JTAG emulators. The interface signals have a voltage level of 3.3V.

The following figure shows the Debug JTAG.

Figure 3-37. Debug JTAG



The following table shows the Debug JTAG connector signal description.

Table 3-21. Debug JTAG Connector Signal Description

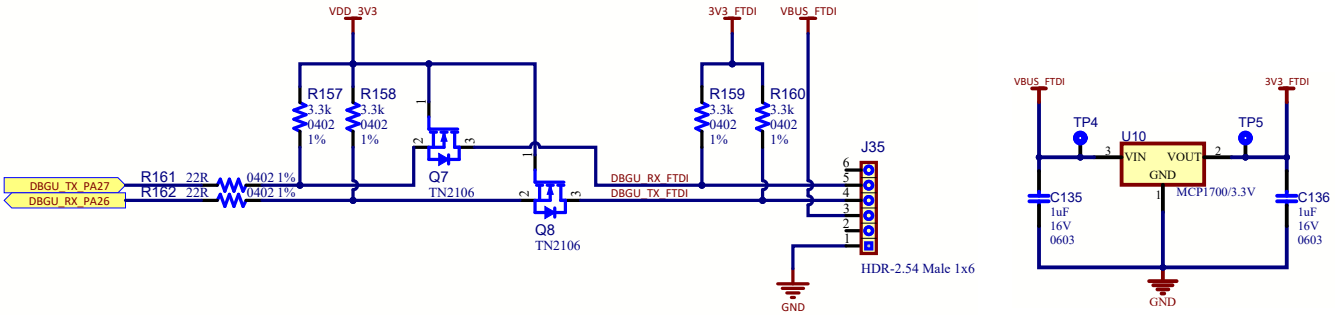
Pin No.	Signal Name	Signal Description
1, 2	VDD_3V3	3.3V
3, 17, 19	NC	Not connected
4, 6, 8, 10, 12, 14, 16, 18, 20	GND	Ground
5	JTAG_TDI	Test data in
7	JTAG_TMS	Test mode select
9	JTAG_TCK	Test clock
11	JTAG_RTCK	Return test clock
13	JTAG_TDO	Test data out
15	NRST	Reset

3.5.2. Serial Debug COM Port (FTDI)

The SAM9X75-Curiosity board features a dedicated serial port for debugging, accessible through header J35. Various interfaces can be used as a USB/Serial DBGU port bridge, such as the FTDI TTL-232R USB-to-TTL serial cable.

The following figure shows the serial debug COM port.

Figure 3-38. Serial Debug COM Port



Only Compatible with :
- TTL-232R-3V3
- TTL-232R-5V

The following table shows the serial debug COM port signal description.

Table 3-22. Serial Debug COM Port Signal Description

PIO	Signal Name	Signal Description
PA26	DBGU_RX	UART receive data
PA27	DBGU_TX	UART transmit data

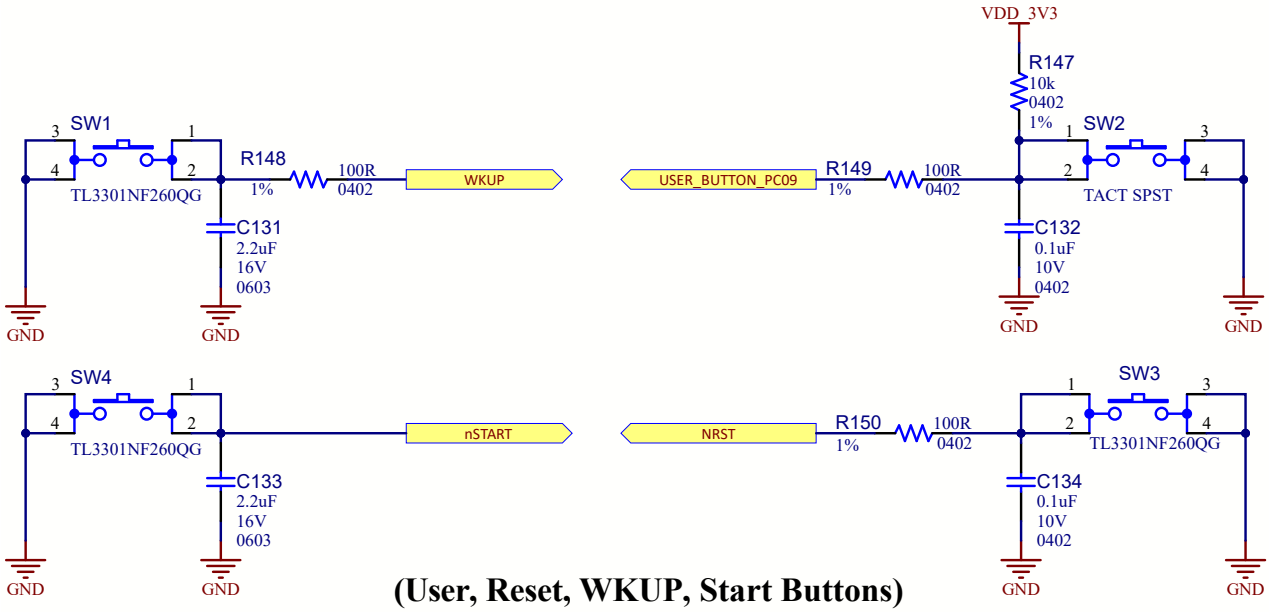
3.5.3. Push Button Switches

The SAM9X75-Curiosity board features four push buttons:

- One general purpose button (SW1) connected to GPIO PC09. This is free for user application usage.
- One wake-up button (SW2) connected to WKUP0. When pressed, the processor exits from Shutdown state.
- One board reset button (SW3). When pressed, the processor is reset.
- One Start push button (SW4) connected to the MCP16502 pin. When pressed, the PMIC start-up sequence is initiated if the buck converters are off.

The following figure shows the push buttons implementation.

Equation 3-1. Push Buttons



The following table shows the user push button signal description.

Table 3-23. User Push Button Signal Description

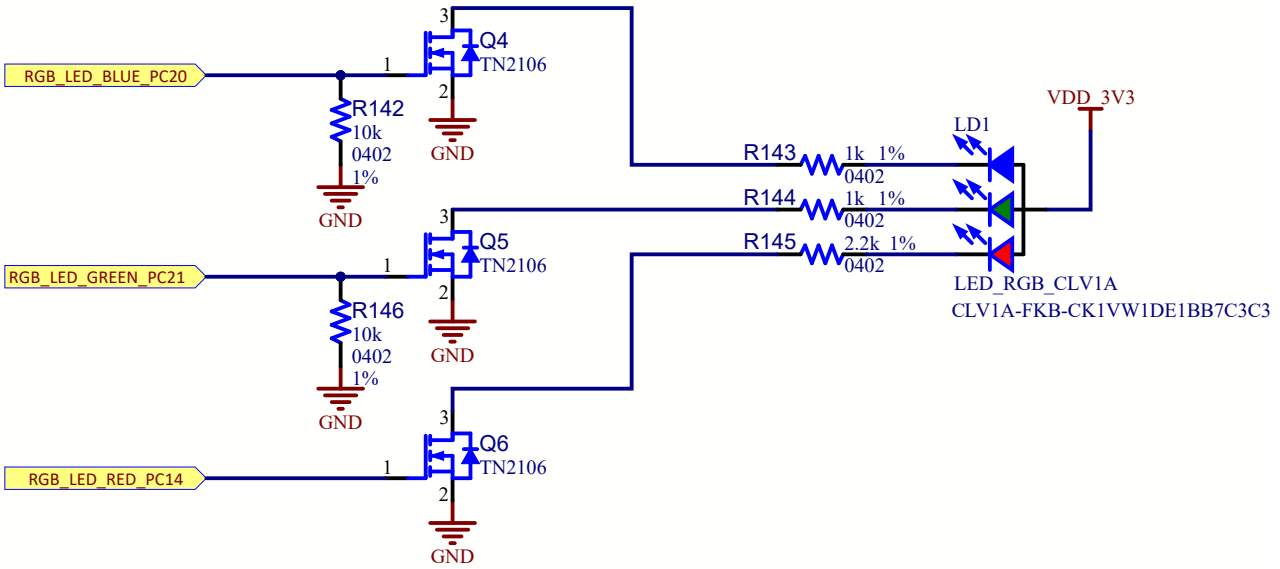
PIO	Signal Name	Signal Description
PC09	USER_BUTTON	General purpose input

3.5.4. RGB LED

The SAM9X75-Curiosity board features one RGB LED. The three LED cathodes are controlled via GPIO PWM pins.

The following figure shows the user LED.

Figure 3-39. User LED



The following table shows the user LED signal description.

Table 3-24. User LED Signal Description

PIO	Signal Name	Signal Description
PC14	RGB_LED_RED	Red LED
PC20	RGB_LED_BLUE	Blue LED
PC21	RGB_LED_GREEN	Green LED

4. Installation and Operation

4.1. System and Configuration Requirements

The SAM9X75-Curiosity board requires the following:

- Personal computer
- USB cable (provided in the kit box)
- 5V AC/DC wall adapter (not provided in the kit box) in case of high-power consumption system

4.2. Board Setup

Follow these steps before using the SAM9X75-Curiosity board:

1. Unpack the board, taking care to avoid electrostatic discharge.
2. Check the default jumper settings (see Default Jumper Settings).
3. Connect the Micro-USB cable to connector J2 (USB-A port).
4. Connect the other end of the cable to a free port on your PC.
5. Connect a USB-UART converter to J35, making sure to also connect the VBUS_FTDI power source.
6. Open a terminal (console 115200, N, 8, 1) on your PC for the USB-UART converter.
7. Reset the board. A “ROMCode” startup message appears on the console.

5. Errata

5.1. microSD Card Settings

Some microSD cards work only with slew rate on and drive strength high settings. To address this issue, the PIO I/O Slewrate Control register and the PIO I/O Drive register 1 need to be set as follows.

PIO I/O Slewrate Control Register

- Name: PIO_SLEWR
- PIOA Slewrate Address: 0xFFFFF510 (0xFFFFF400 PIOA Base Address + 0x0110 Slewrate Offset)
- Value to be bitwise OR-ed: 0x0000003F

PIO I/O Drive Register 1

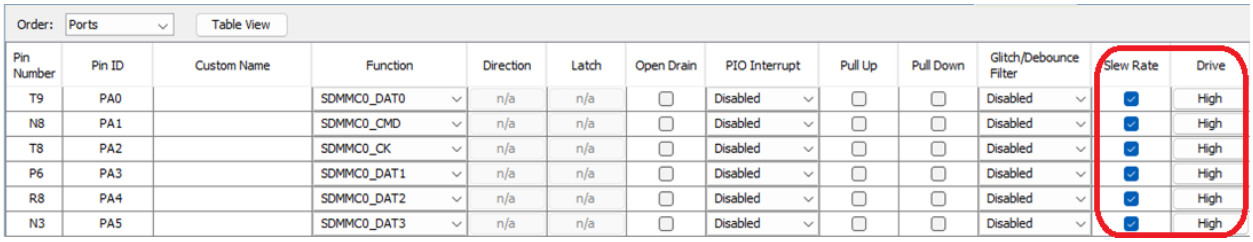
- Name: PIO_DRIVER1
- PIOA Drive Strength Address: 0xFFFFF518 (0xFFFFF400 PIOA Base Address + 0x0118 Drive Strength Offset)
- Value to be bitwise OR-ed: 0x0000003F

For Linux applications, the SAM9X75-Curiosity board device tree initiates the pin control settings accordingly.

For bare metal applications, the bootstrap is configured with drive high and slew rate on settings.

When using MPLAB X, these settings can be configured in the Pin Settings section of Harmony 3 Configurator as shown below.

Figure 5-1. Harmony 3 Configurator 'Pin Settings' Section



Affected Curiosity Kit:

SAM9X75-Curiosity

6. Appendix. Schematics and Layouts

This section contains the following schematics:

- SAM9X75-Curiosity Block Diagram
- Power Inputs
- Power Supplies
- MPU System
- MPU Memories
- PIO Assignment
- MPU Interfaces Distribution
- microSD Card Interface
- USB Interfaces
- 10/100/1000 SODIMM Ethernet Interface
- Wireless M.2 Interface
- mikroBUS Interface
- RPi 40-Pin Interface
- Video Interfaces
- User Interface
- Debug Interface
- Audio Class D
- Power Measurement
- Mechanicals and Accessories
- Top Assembly
- Bottom Assembly

Figure 6-1. SAM9X75-Curiosity Block Diagram

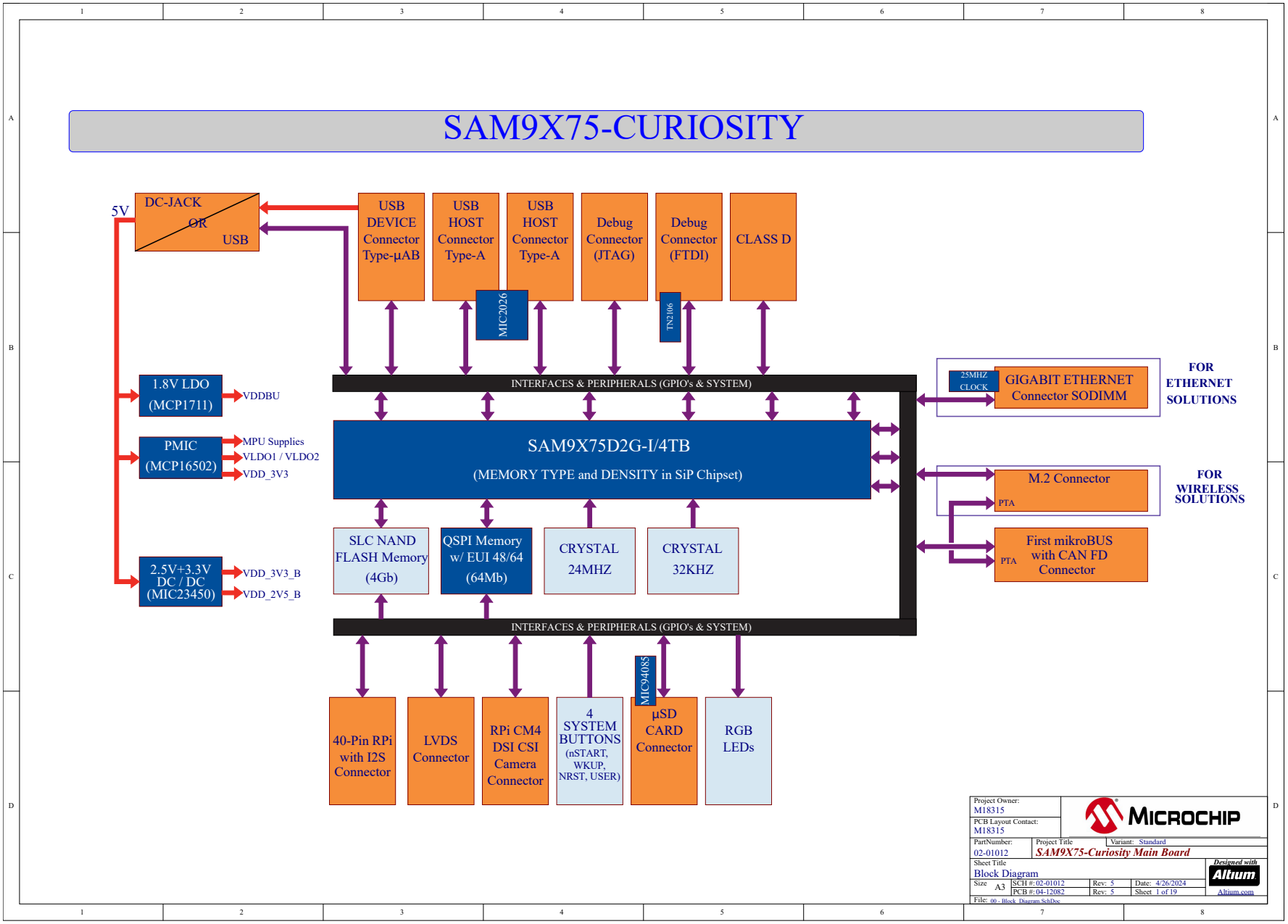


Figure 6-2. Power Inputs

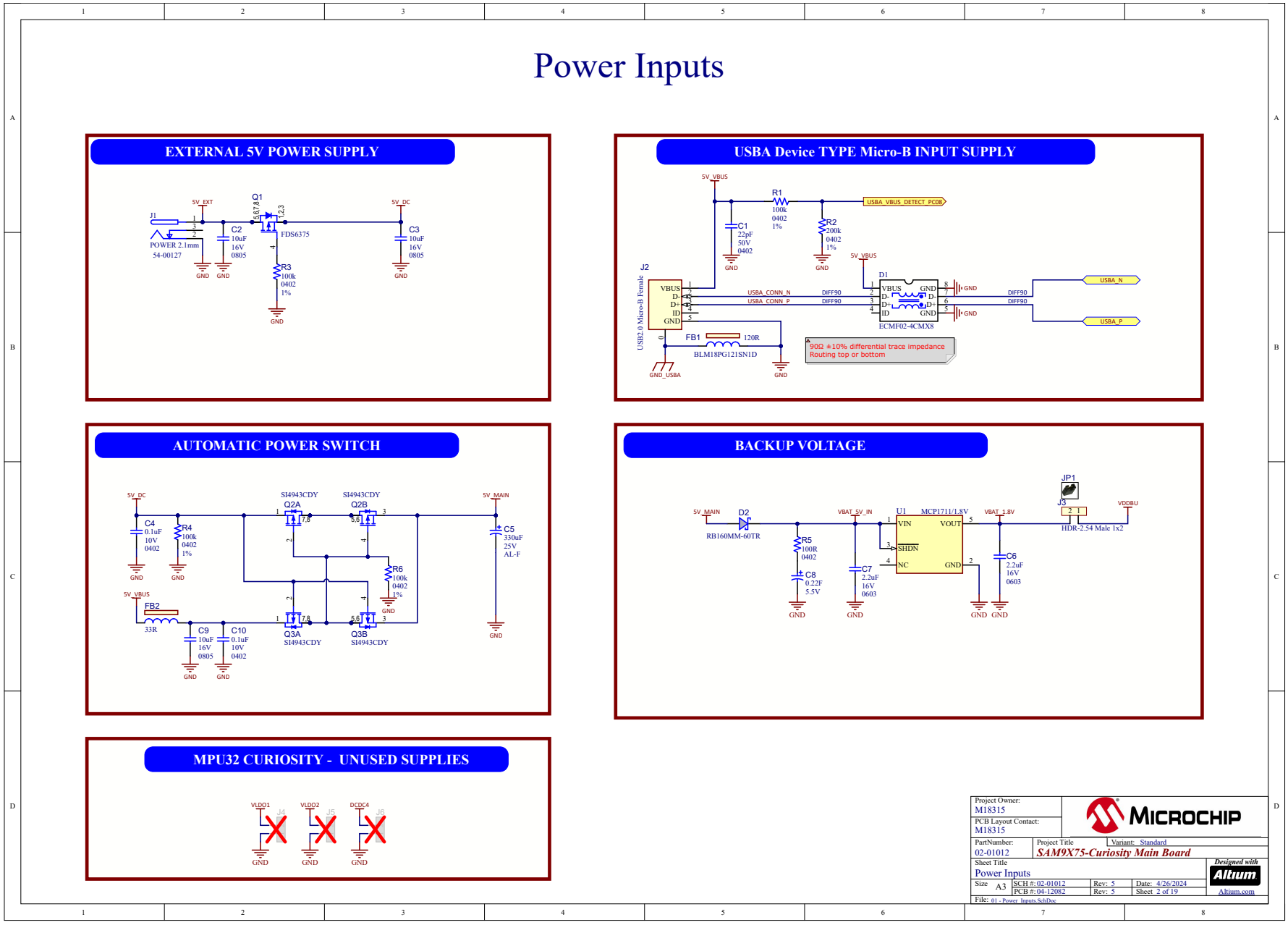


Figure 6-3. Power Supplies

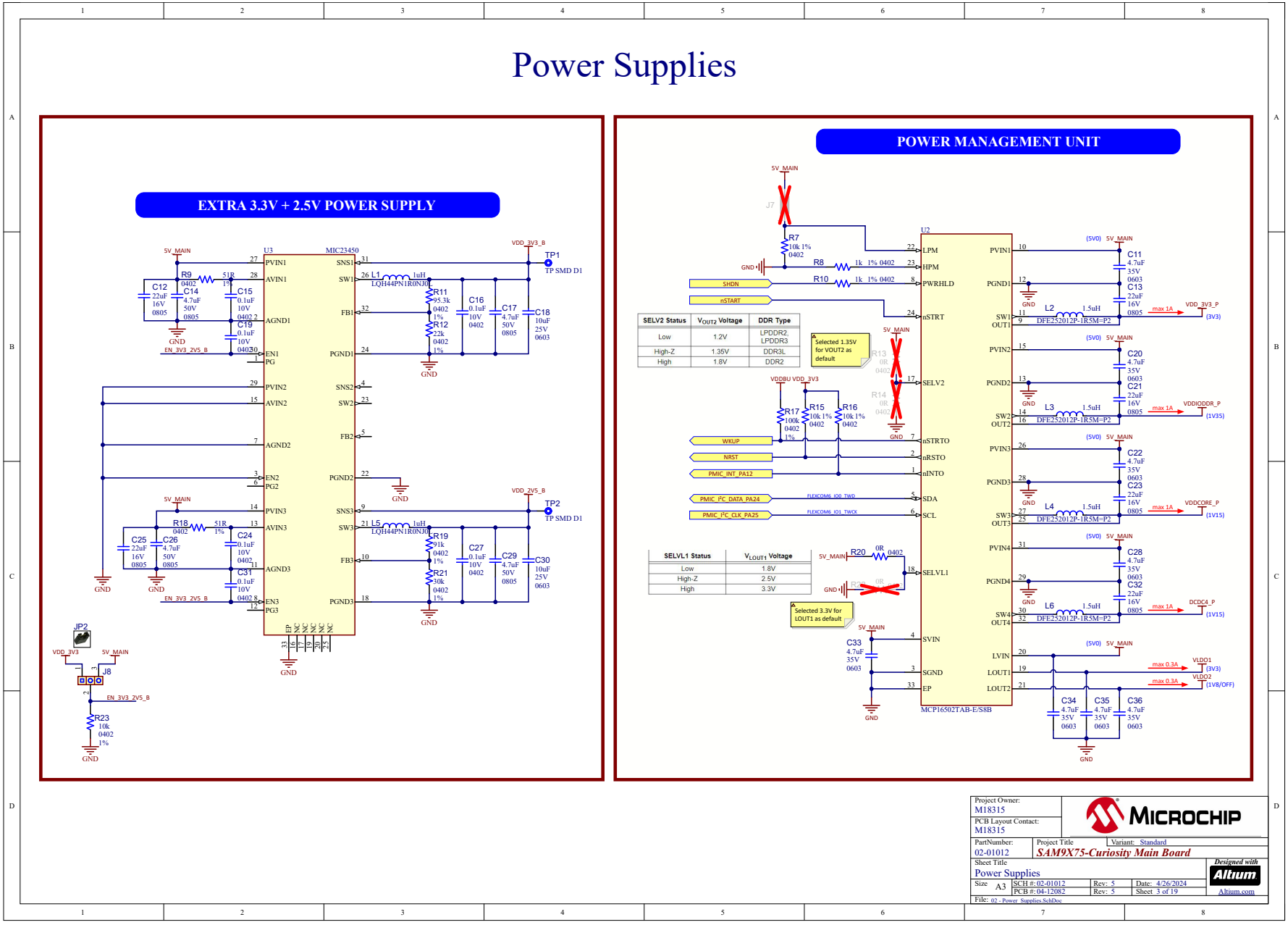


Figure 6-4. MPU System

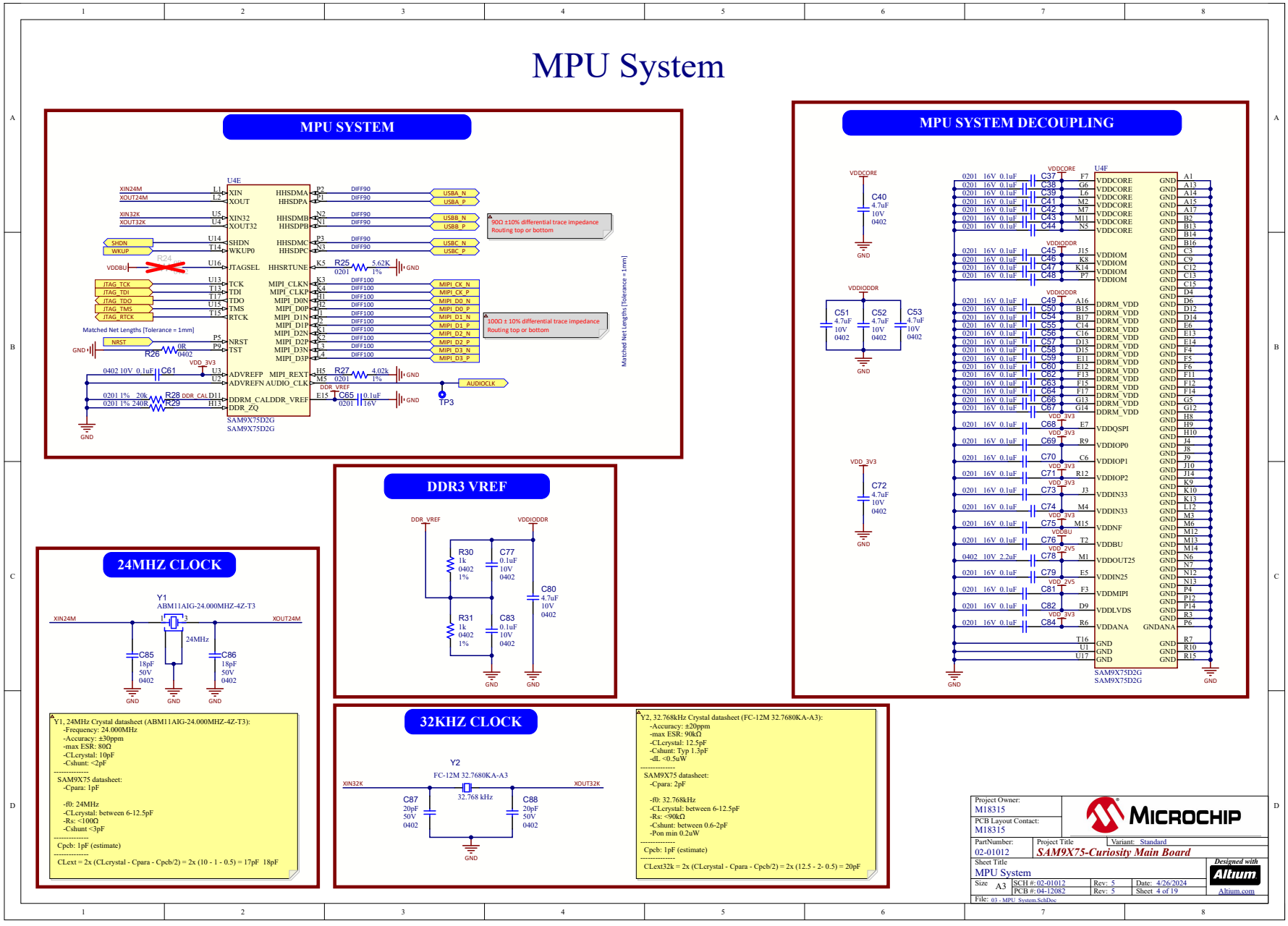


Figure 6-5. MPU Memories

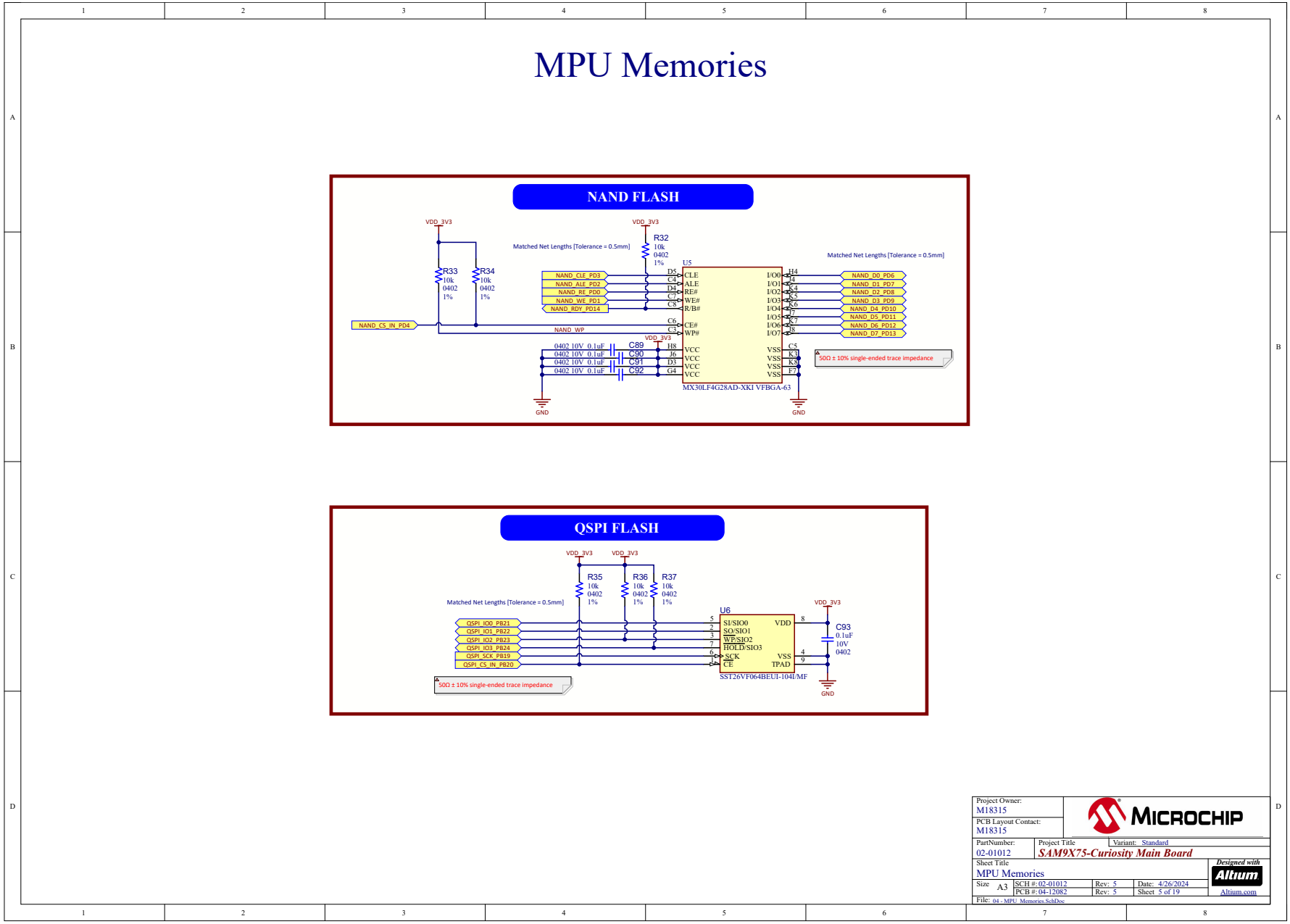


Figure 6-6. PIO Assignment

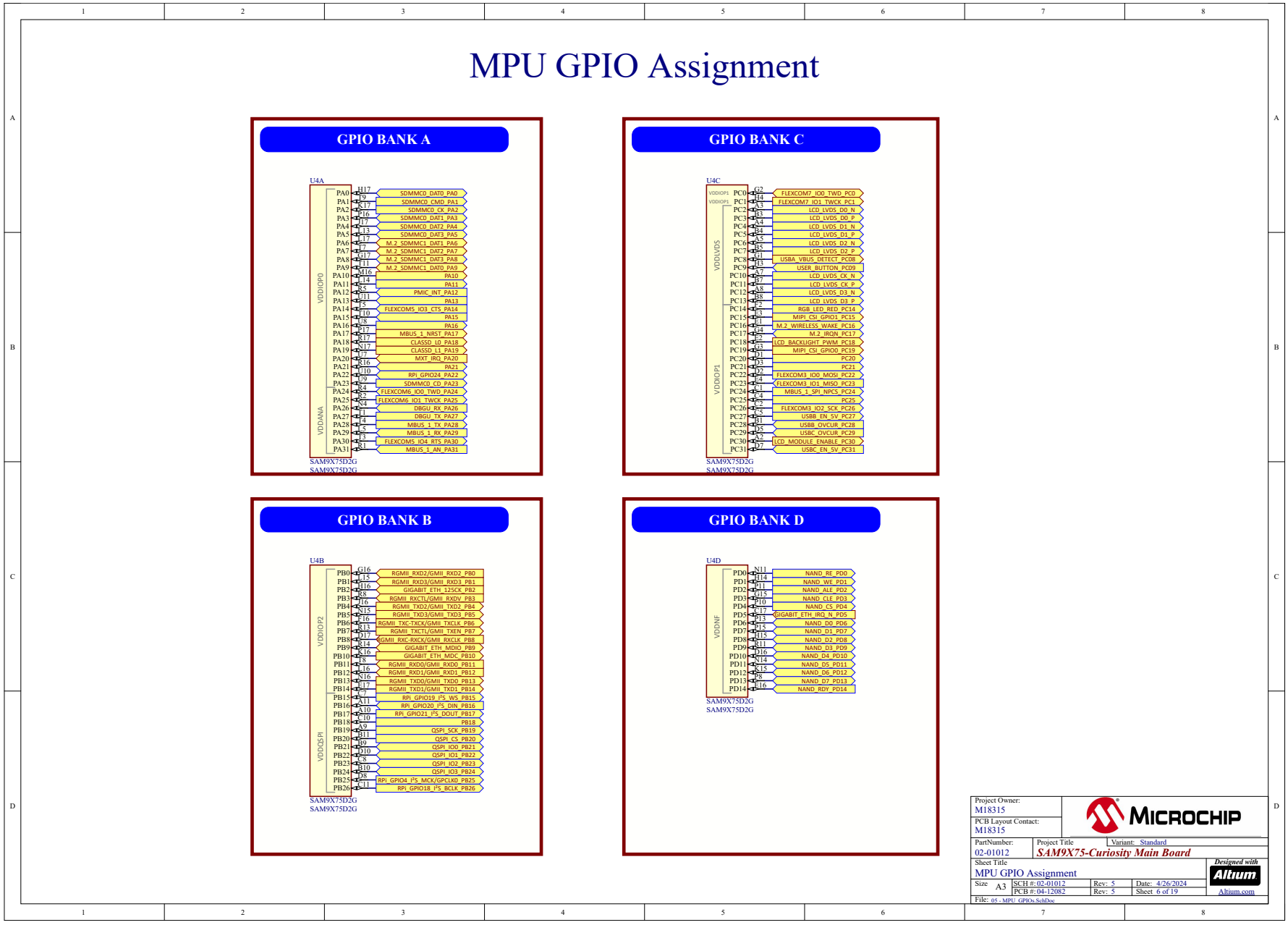


Figure 6-7. MPU Interfaces Distribution

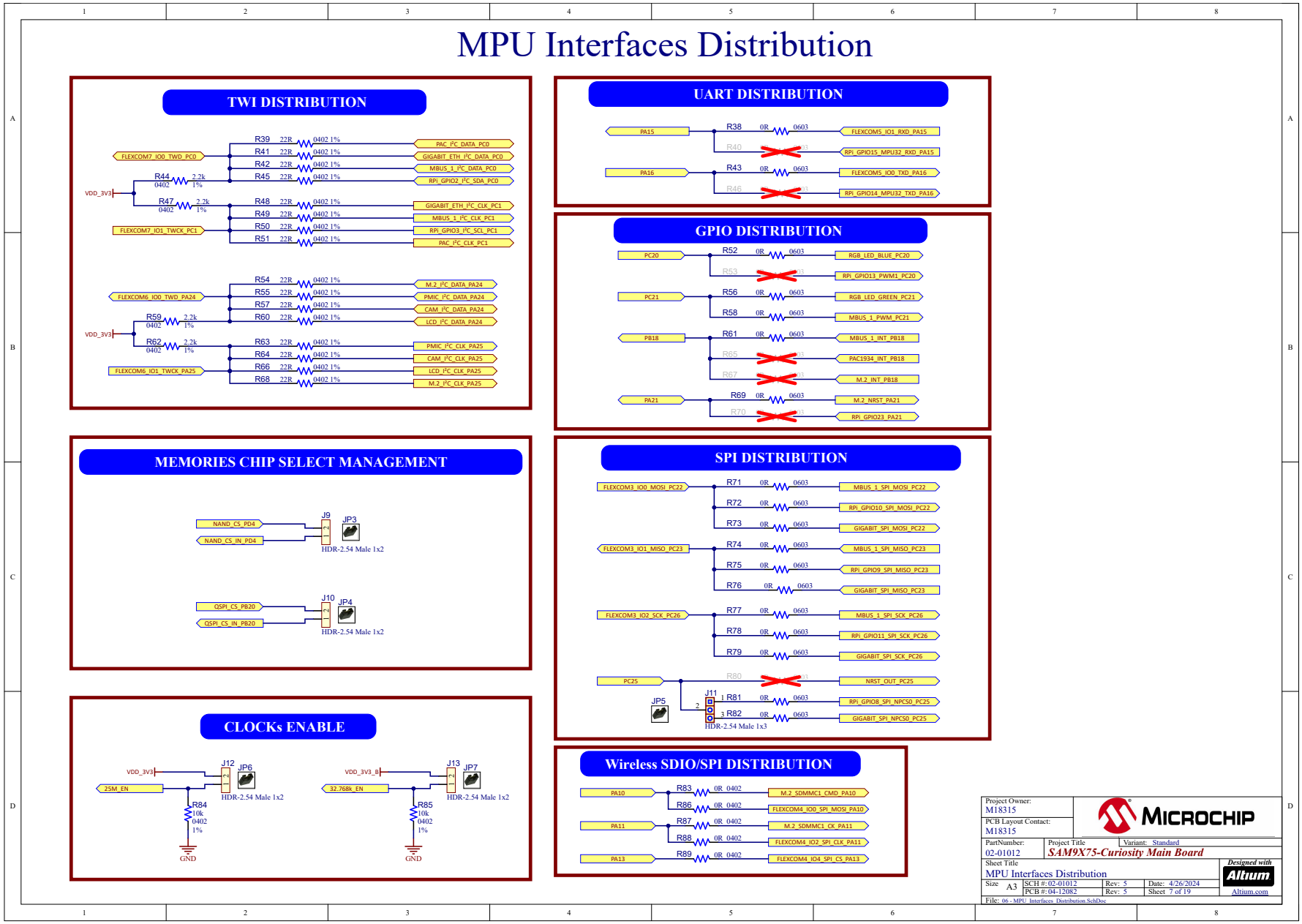


Figure 6-8. microSD Card Interface

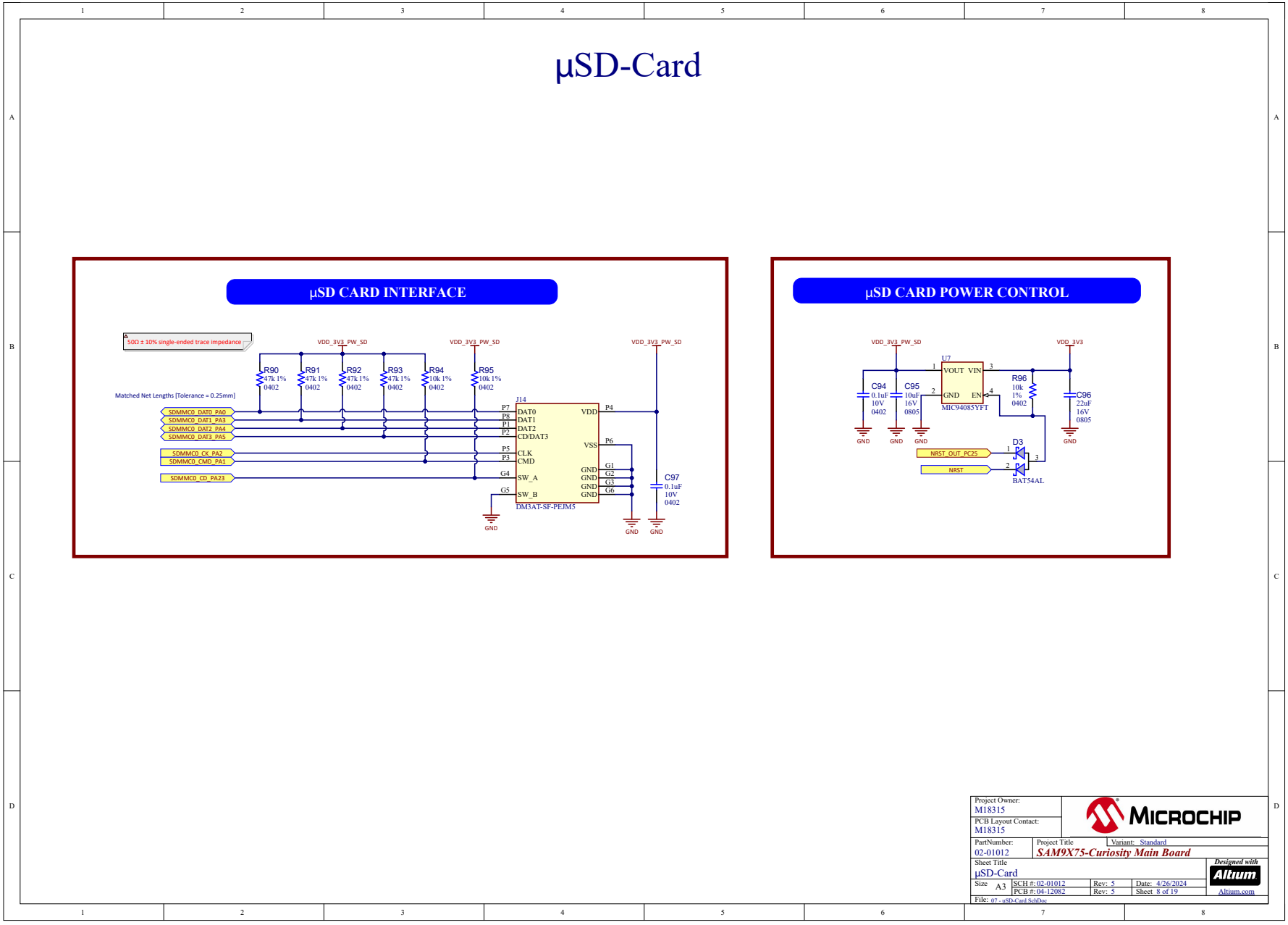


Figure 6-9. USB Interfaces

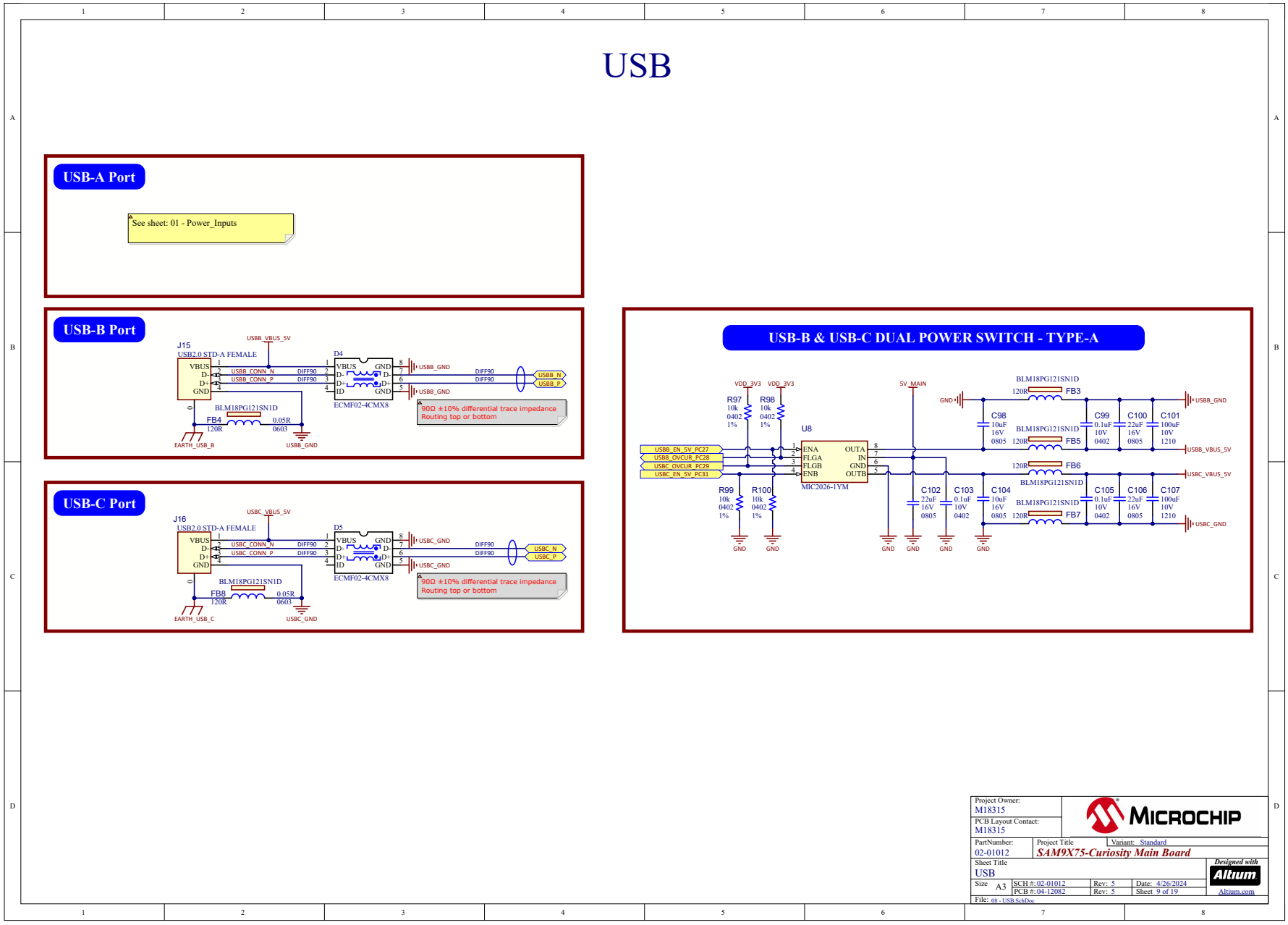


Figure 6-10. 10/100/1000 SODIMM Ethernet Interface

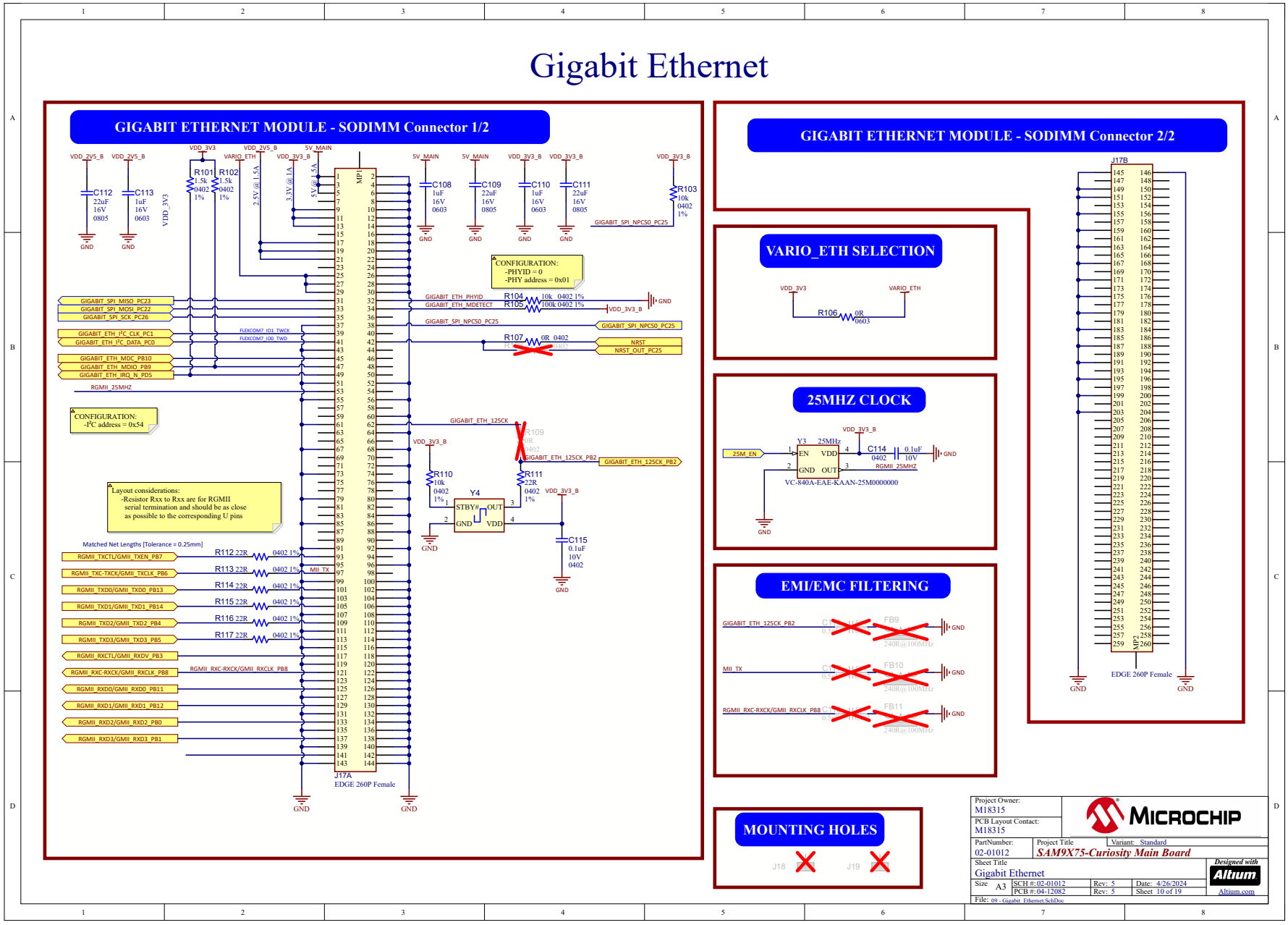


Figure 6-11. Wireless M.2 Interface

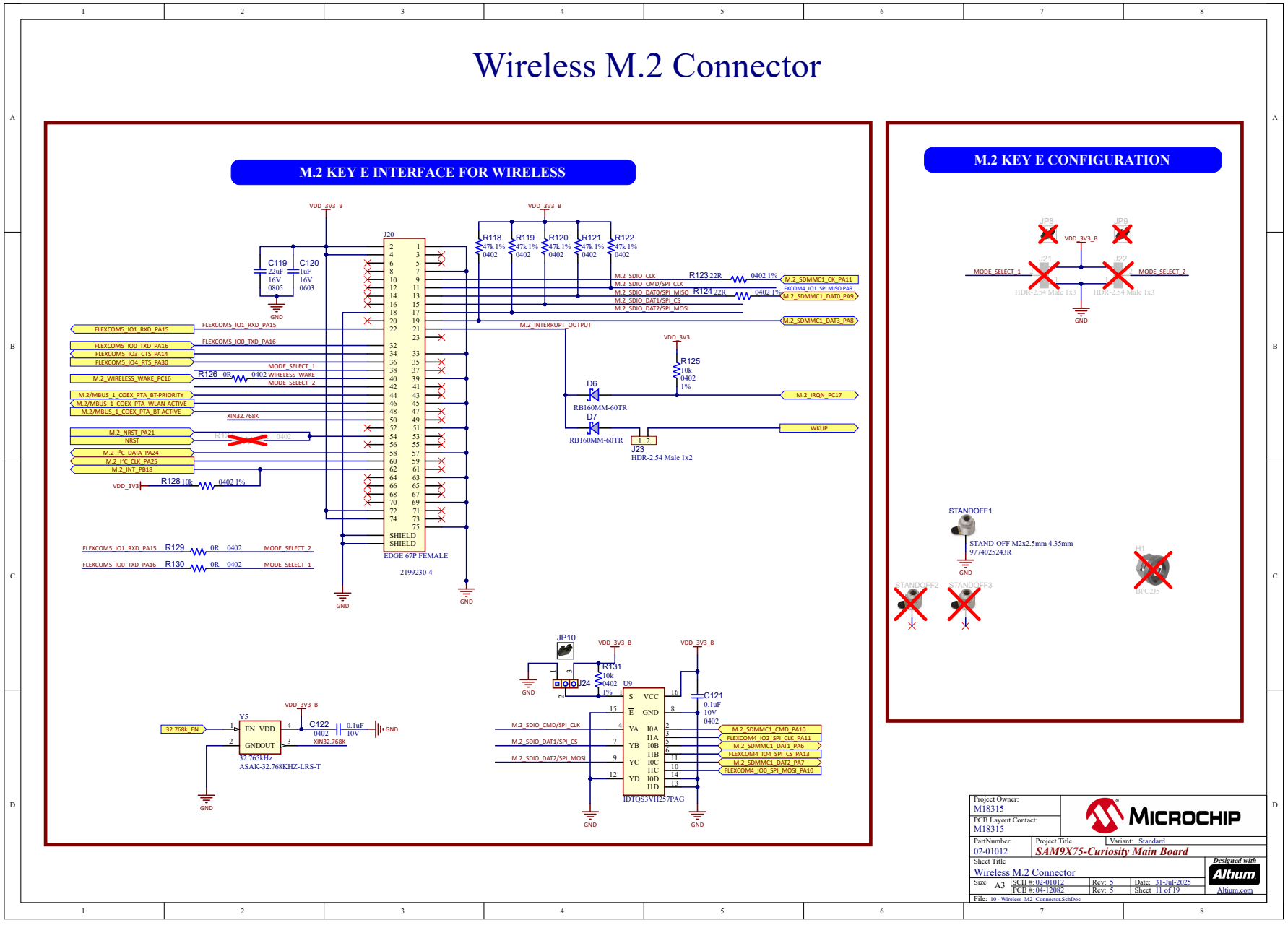


Figure 6-12. mikroBUS Interface

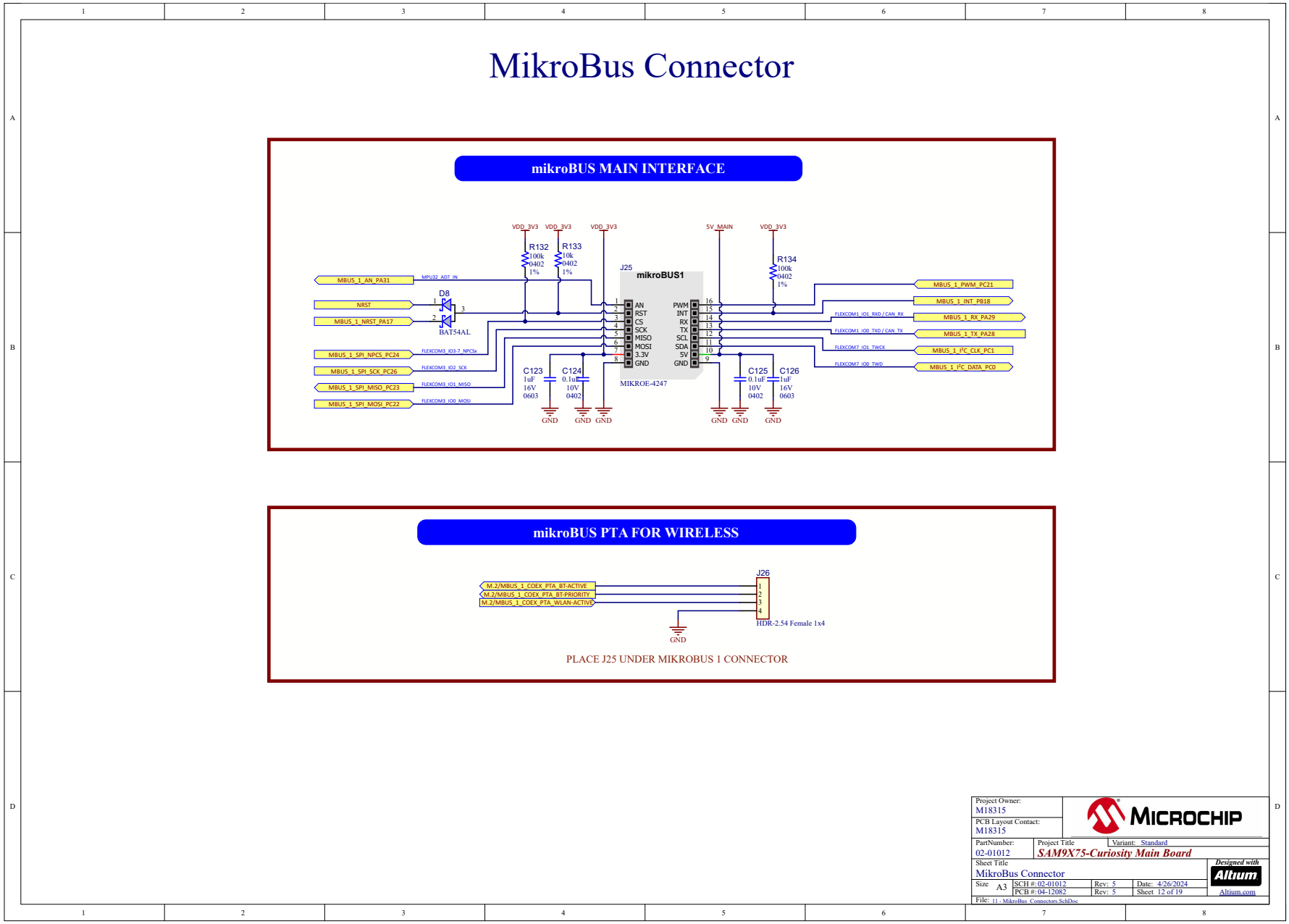


Figure 6-13. RPi 40-Pin Interface

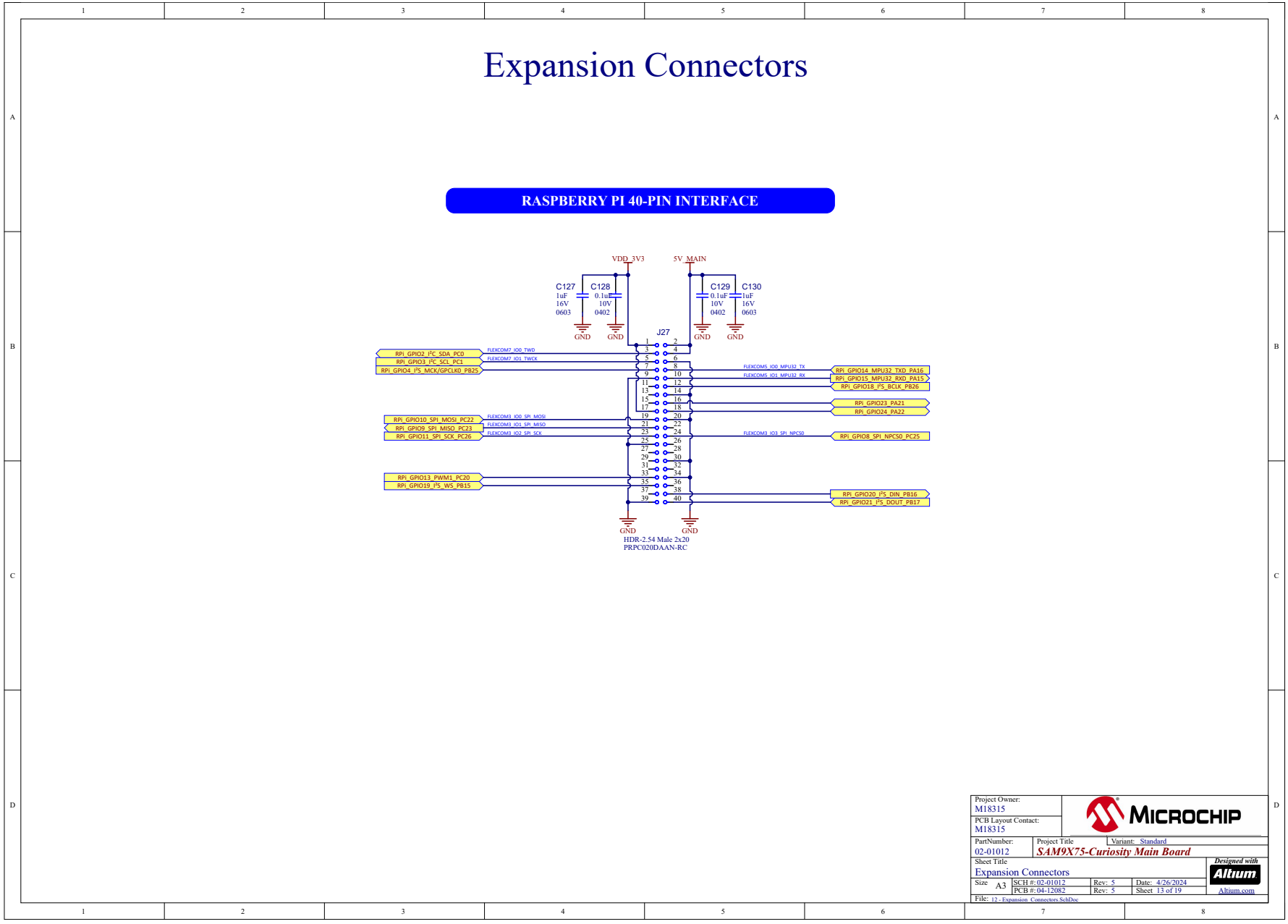


Figure 6-14. Video Interfaces

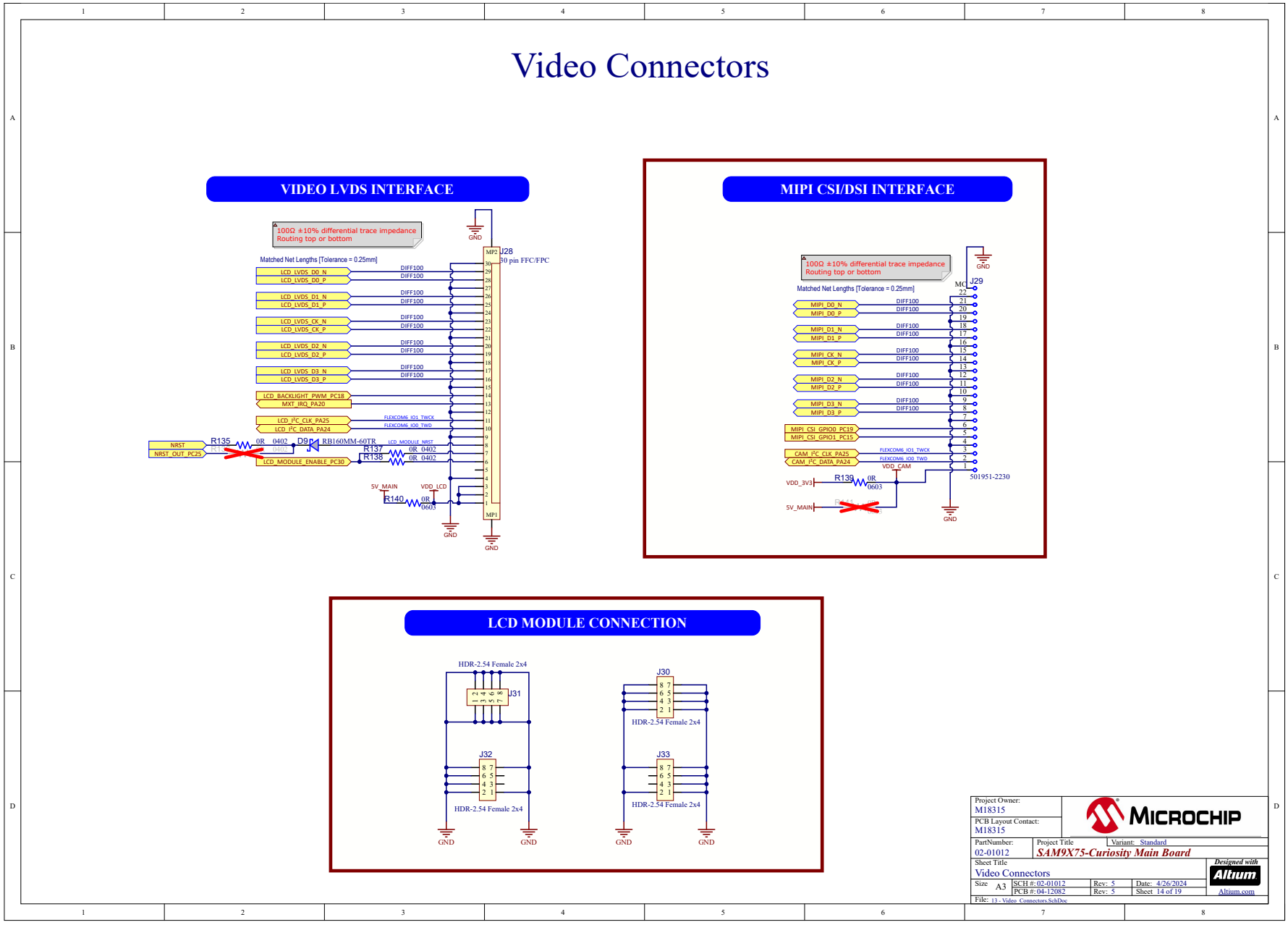


Figure 6-15. User Interface

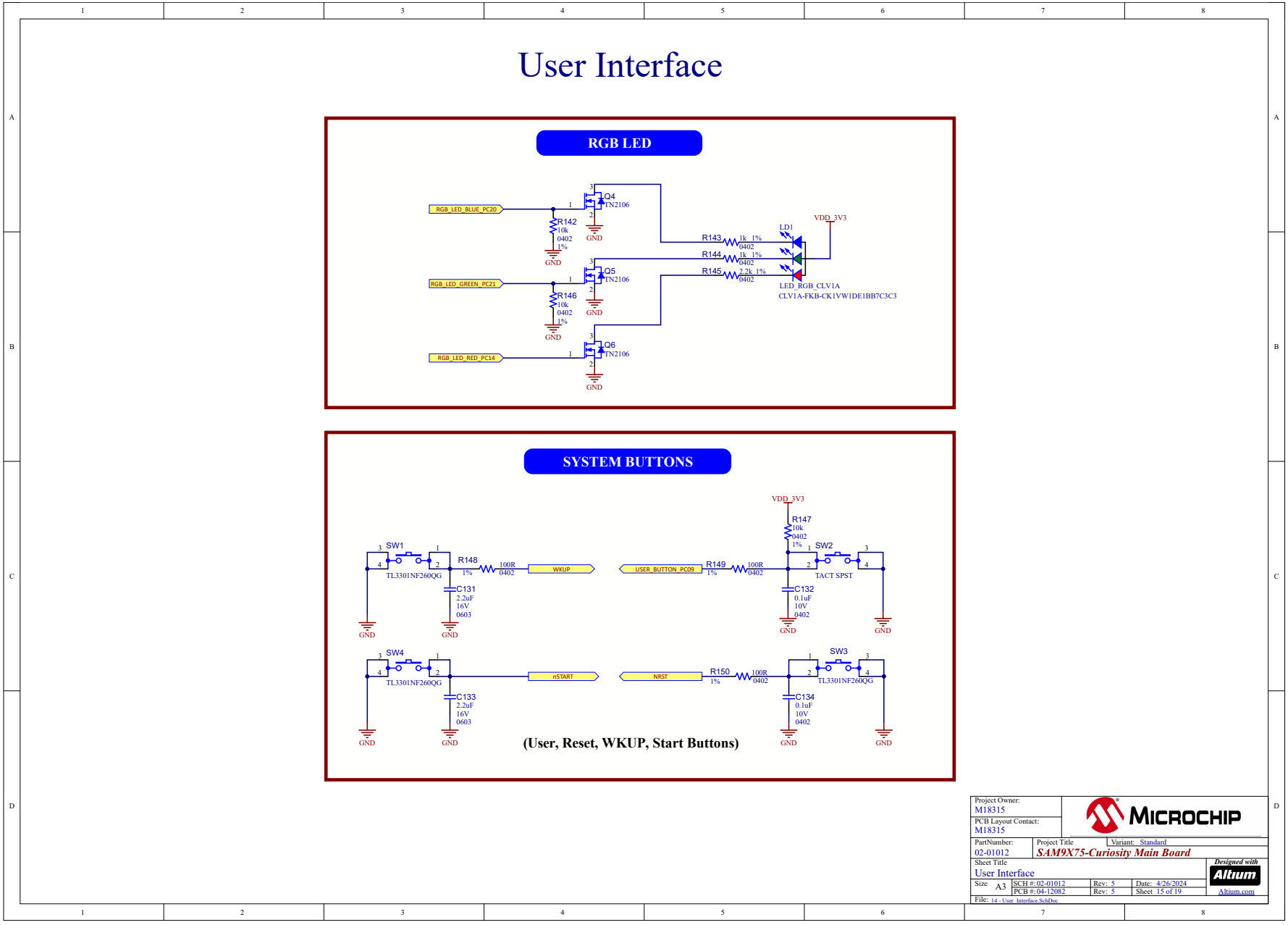


Figure 6-16. Debug Interface

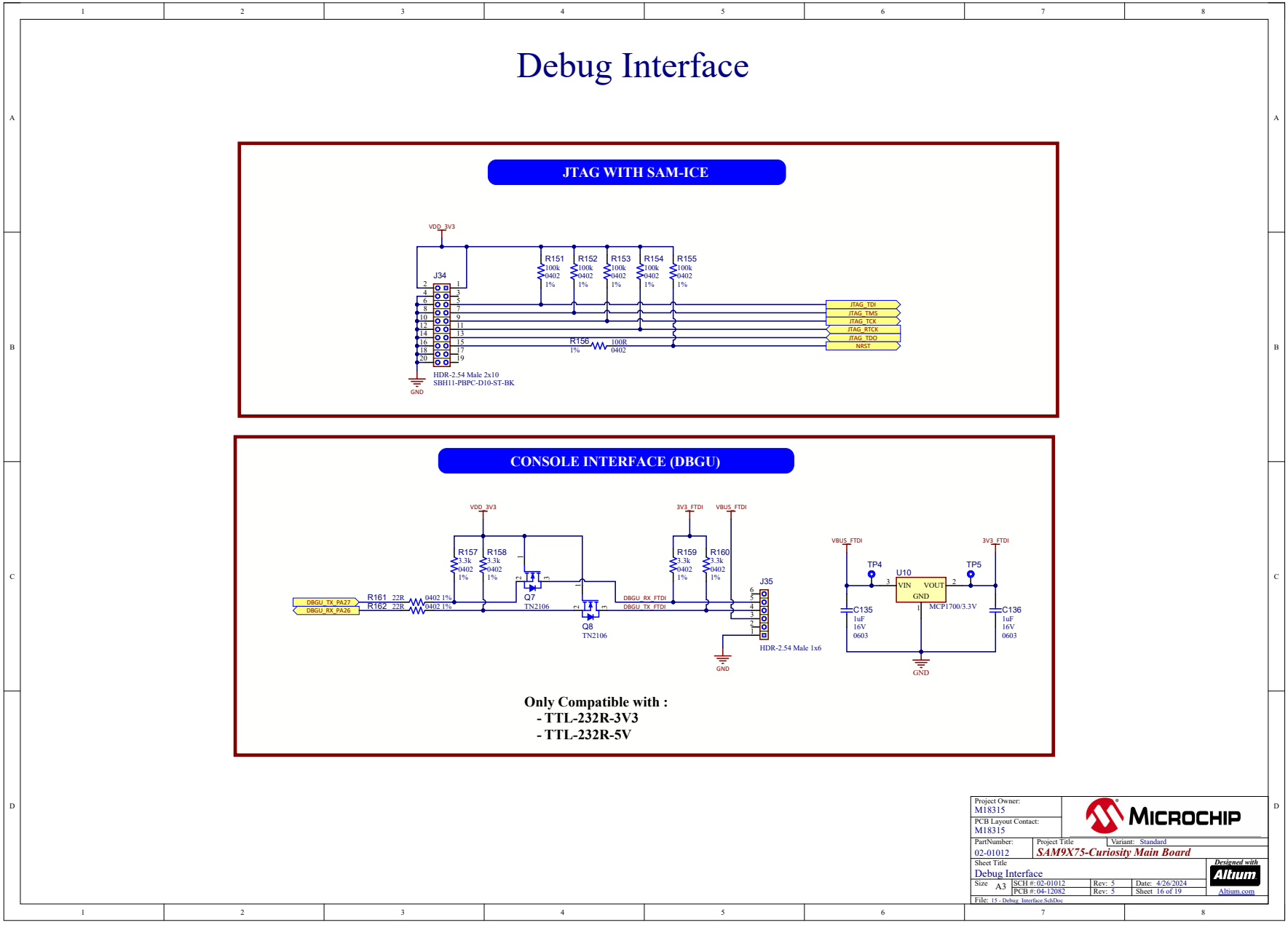


Figure 6-17. Audio Class D

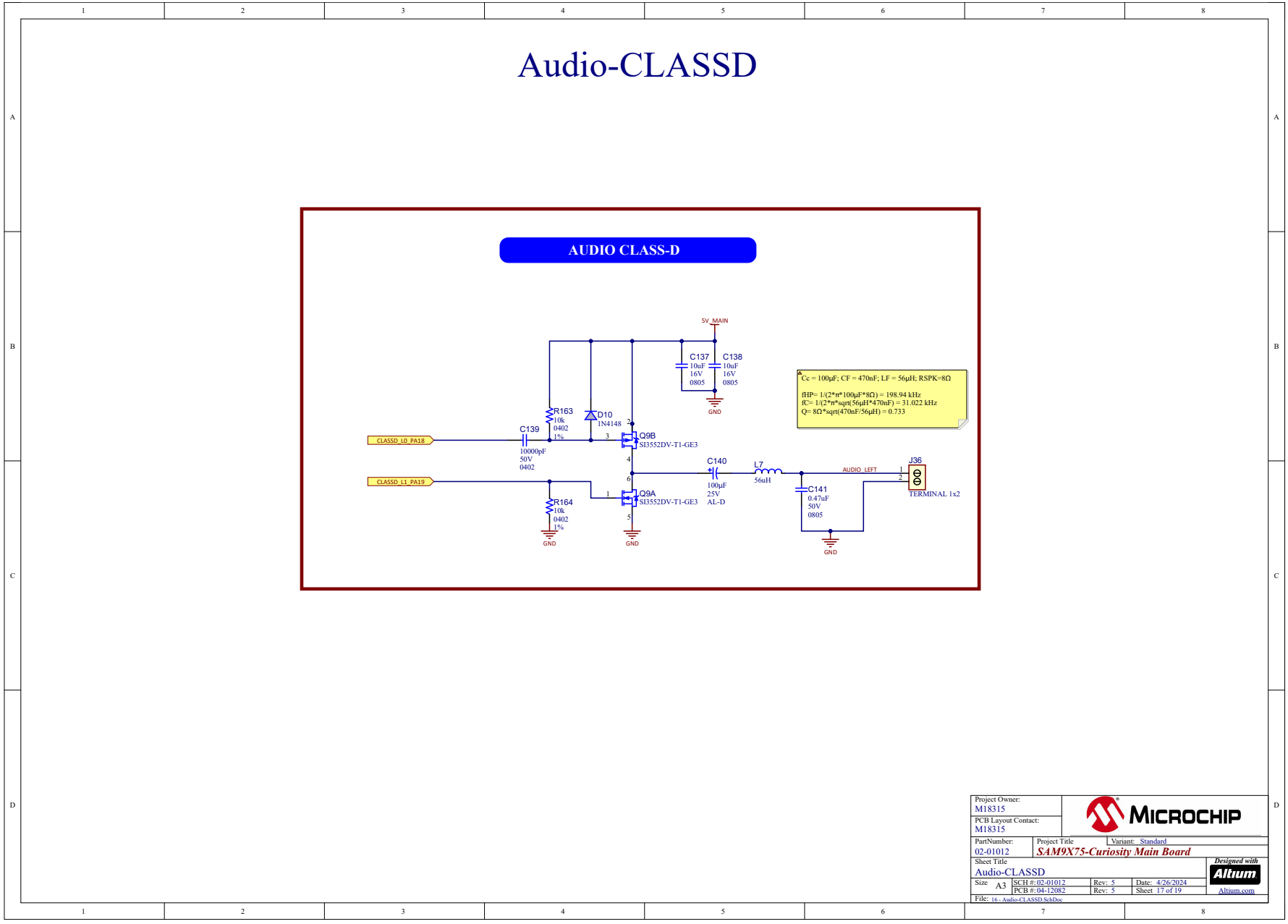


Figure 6-18. Power Measurement

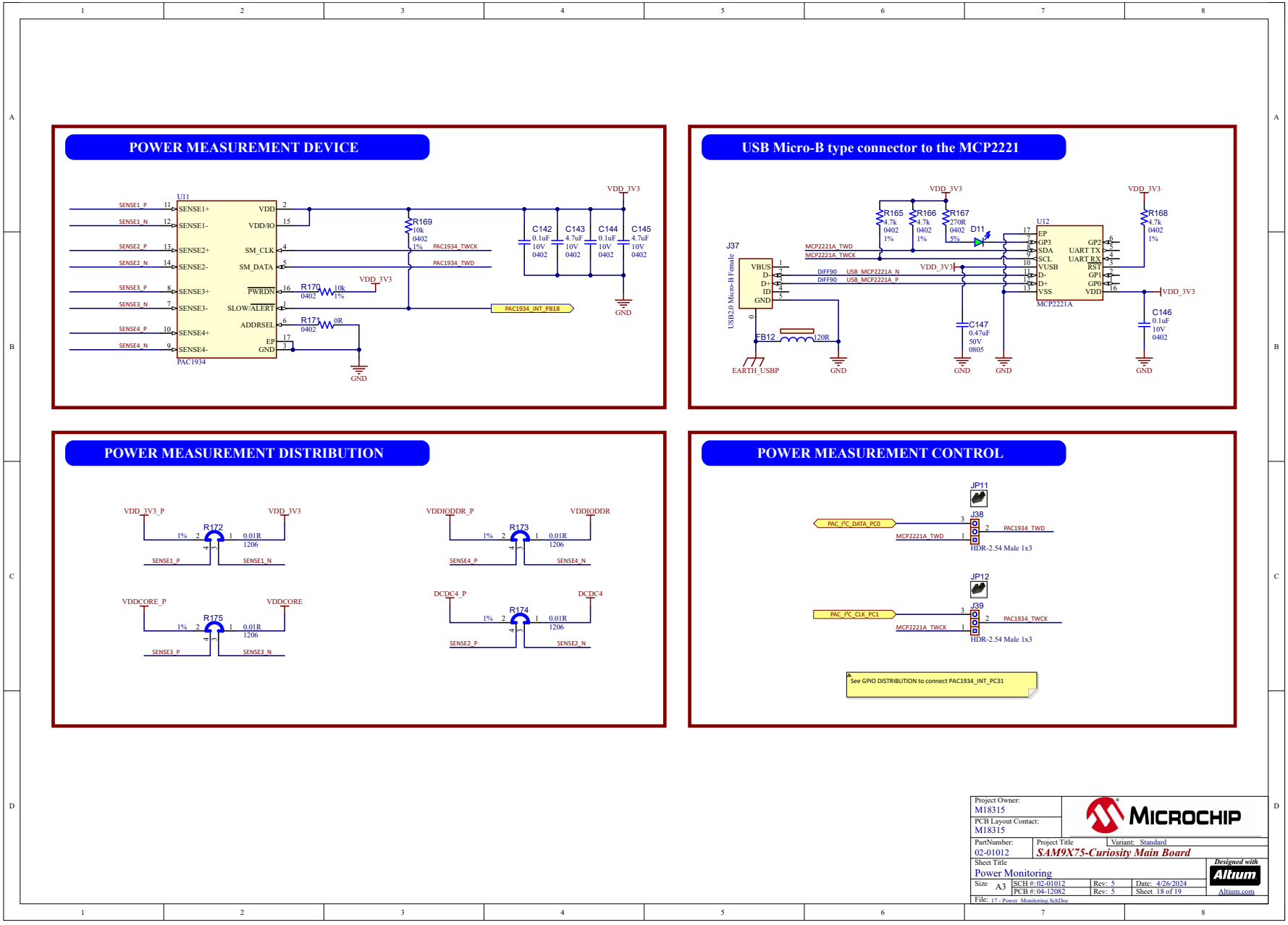
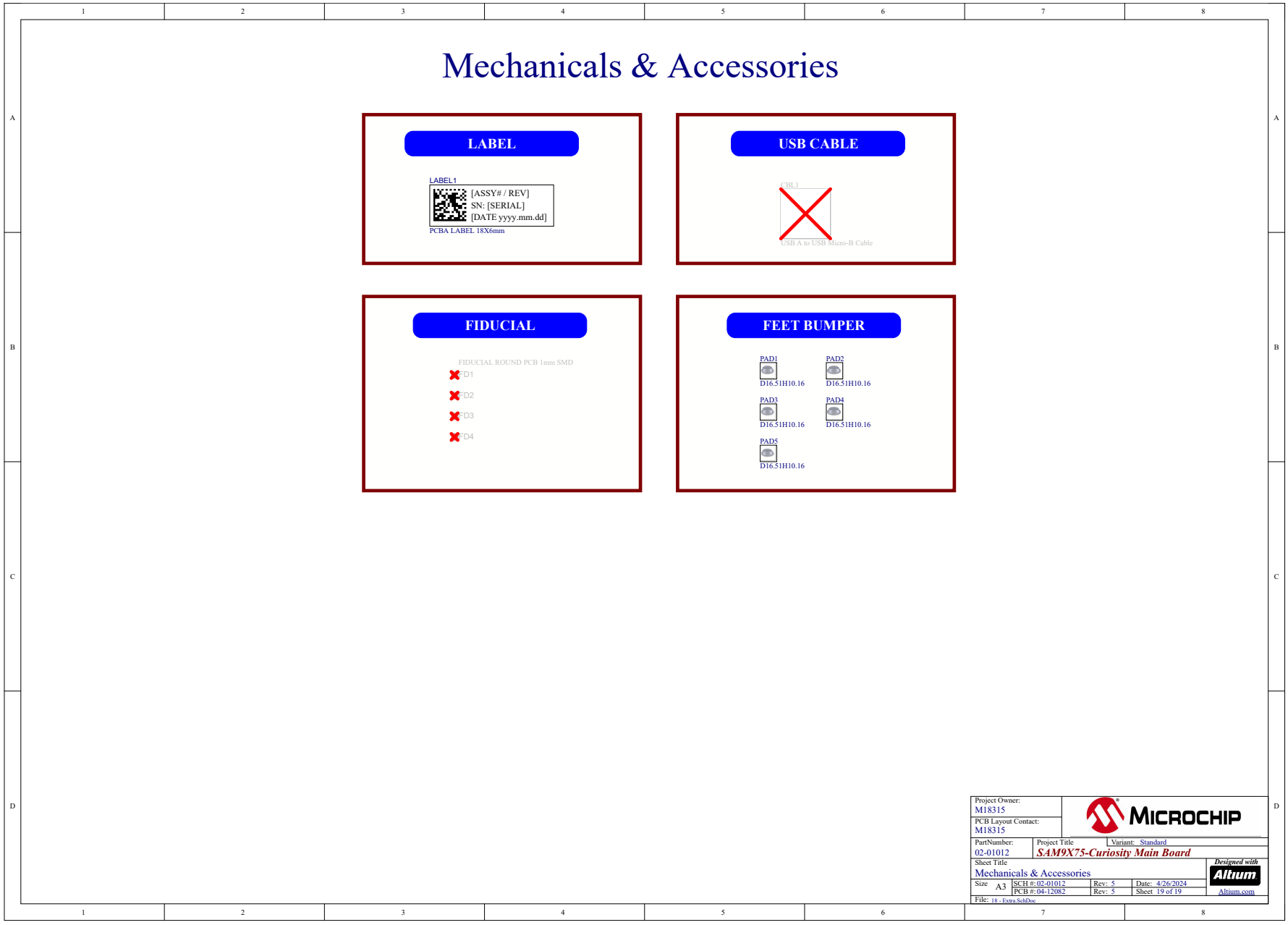


Figure 6-19. Mechanicals and Accessories



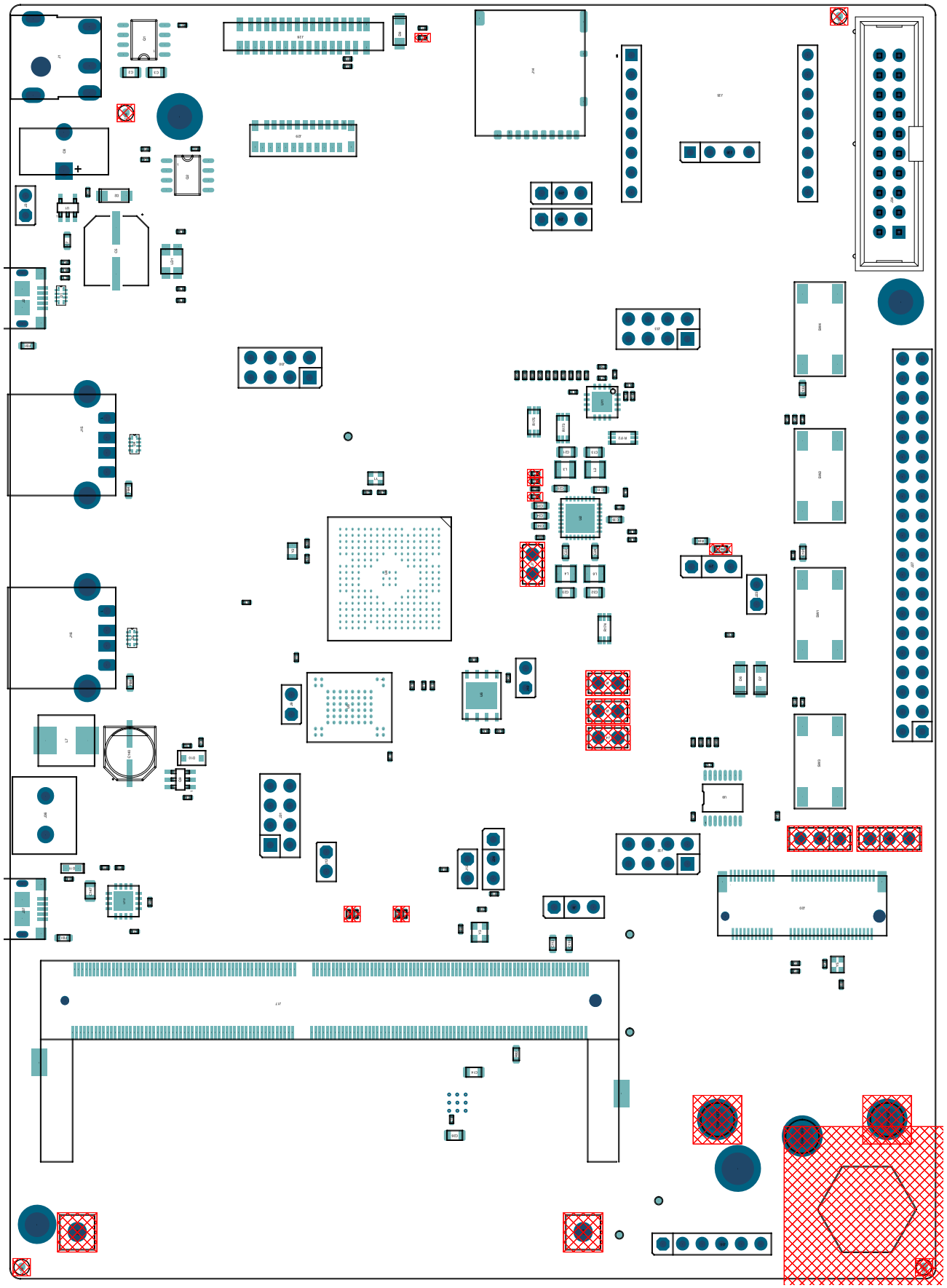
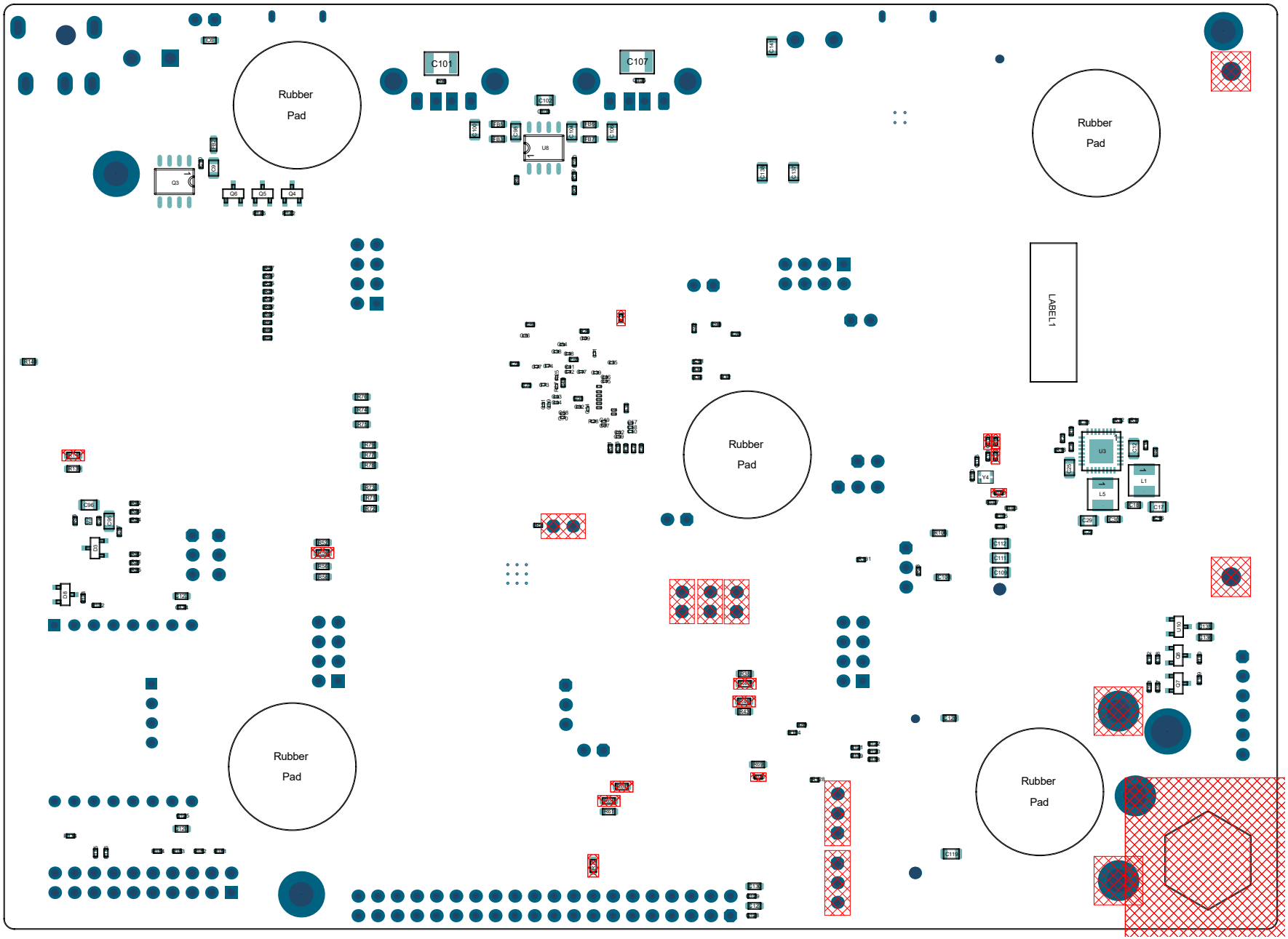


Figure 6-20. Top Assembly

Figure 6-21. Bottom Assembly



7. Revision History

7.1. DS60001859B - 09/2025

Audio Class D: added Warning Updated Figure 6-11

7.2. DS60001859A - 07/2024

First issue.

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