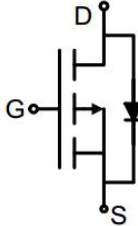
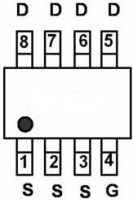



P-Channel Enhancement Mode Power MOSFET

<p>Description</p> <p>The G090P02S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.</p> <p>General Features</p> <ul style="list-style-type: none"> ● V_{DS} -20V ● I_D (at $V_{GS} = -10V$) -11A ● $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 9mΩ ● $R_{DS(ON)}$ (at $V_{GS} = -2.5V$) < 12.5mΩ ● 100% Avalanche Tested ● RoHS Compliant <p>Application</p> <ul style="list-style-type: none"> ● Power switch ● DC/DC converters 	 <p>Schematic diagram</p>  <p>pin assignment</p>  <p>SOP-8</p>
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Ordering Information

Device	Package	Marking	Packaging
G090P02S	SOP-8	G090P02	4000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-20	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	-11
		$T_C = 100^\circ\text{C}$	-7
Pulsed Drain Current (note1)	I_{DM}	-44	A
Gate-Source Voltage	V_{GS}	± 12	V
Power Dissipation	P_D	3.3	W
Single pulse avalanche energy (note2)	E_{AS}	49	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ\text{C}$

Thermal Resistance

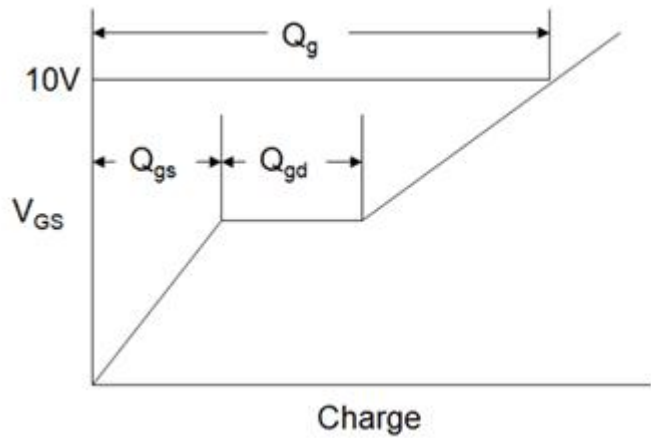
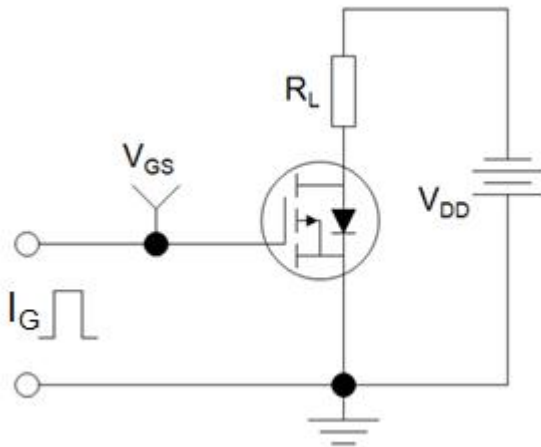
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient, $t \leq 10\text{s}$	R_{thJA}	38	$^\circ\text{C/W}$

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 12V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.4	-0.65	-1.1	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -5A$	--	7.5	9.0	m Ω
		$V_{GS} = -2.5V, I_D = -5A$	--	10	12.5	
Forward Transconductance	g_{FS}	$V_{DS} = -5V, I_b = -15A$	--	72	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = -10V,$ $f = 1.0MHz$	--	4800	--	pF
Output Capacitance	C_{oss}		--	650	--	
Reverse Transfer Capacitance	C_{rss}		--	590	--	
Total Gate Charge	Q_g	$V_{DD} = -10V,$ $I_D = -5A,$ $V_{GS} = -10V$	--	111	--	nC
Gate-Source Charge	Q_{gs}		--	7	--	
Gate-Drain Charge	Q_{gd}		--	15	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -10V,$ $I_D = -5A,$ $R_G = 3\Omega$	--	18	--	ns
Turn-on Rise Time	t_r		--	32	--	
Turn-off Delay Time	$t_{d(off)}$		--	136	--	
Turn-off Fall Time	t_f		--	59	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	-11	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = -5A, V_{GS} = 0V$	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = -5A, V_{GS} = 0V$ $di/dt = -500A/\mu s$	--	100	--	nC
Reverse Recovery Time	T_{rr}		--	33	--	ns

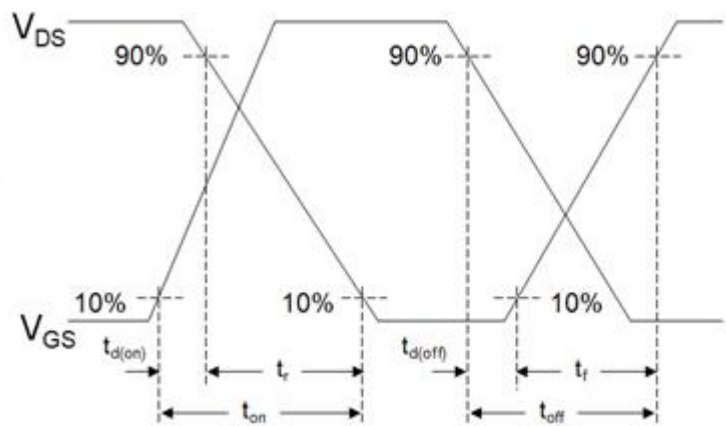
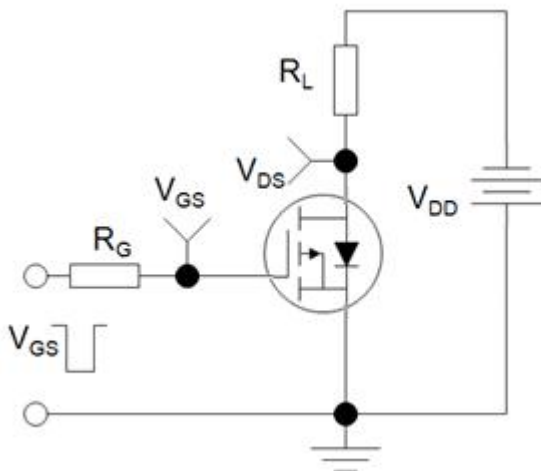
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : $T_J = 25^\circ\text{C}, V_{DD} = -20V, V_{GS} = -10V, L = 0.5mH, R_g = 25\Omega$
The table shows the minimum avalanche energy, which is 132mJ when the device is tested until failure
3. Identical low side and high side switch with identical R_G

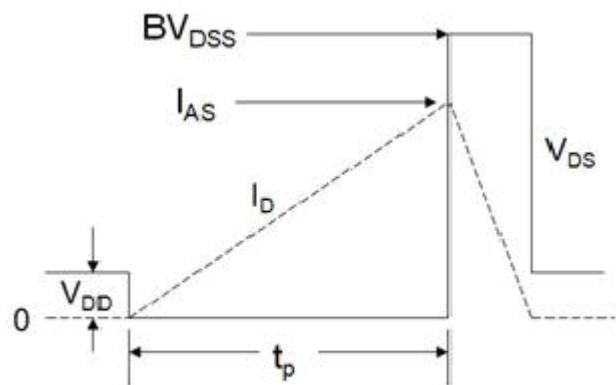
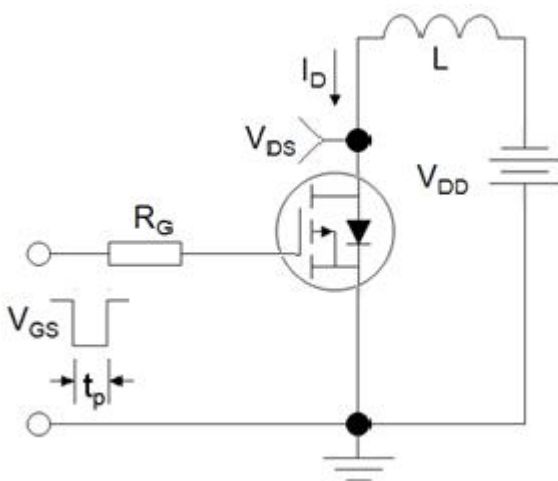
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

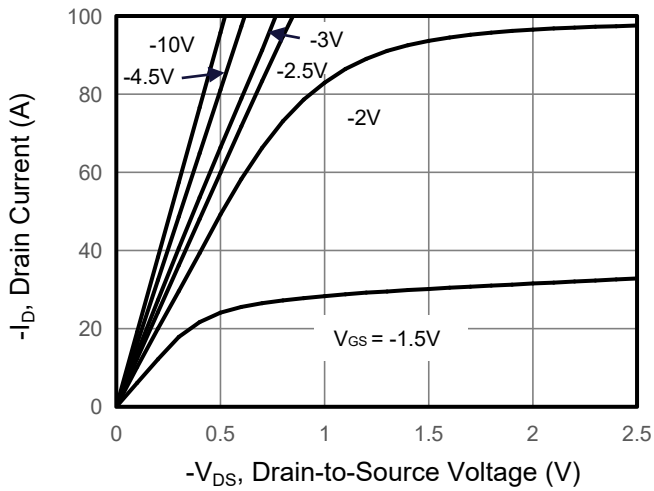


Figure 2. Transfer Characteristics

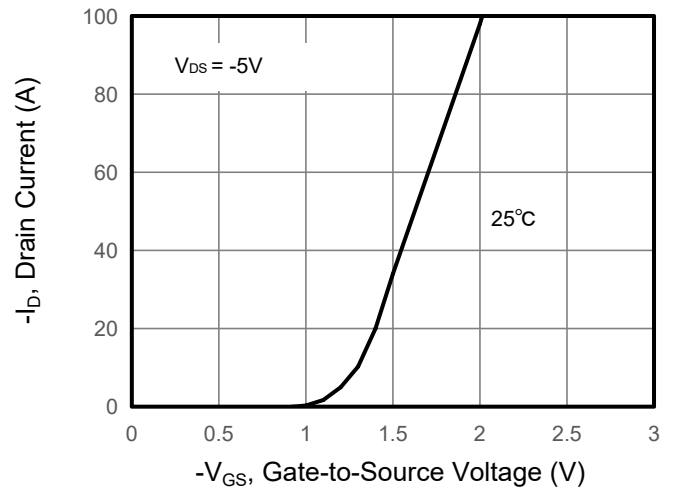


Figure 3. Drain Source On Resistance

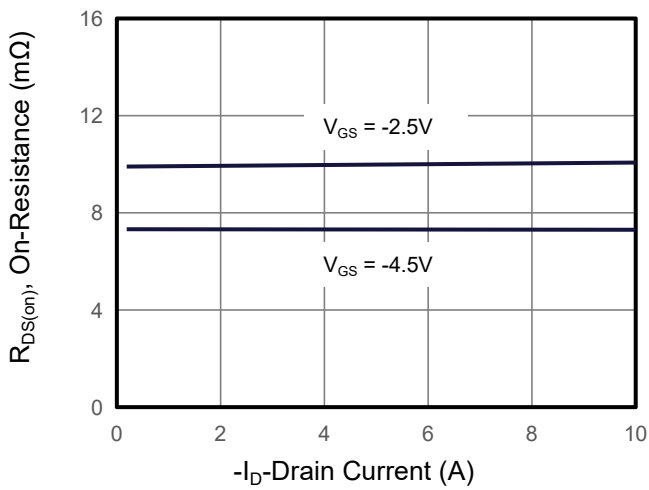


Figure 4. Gate Charge

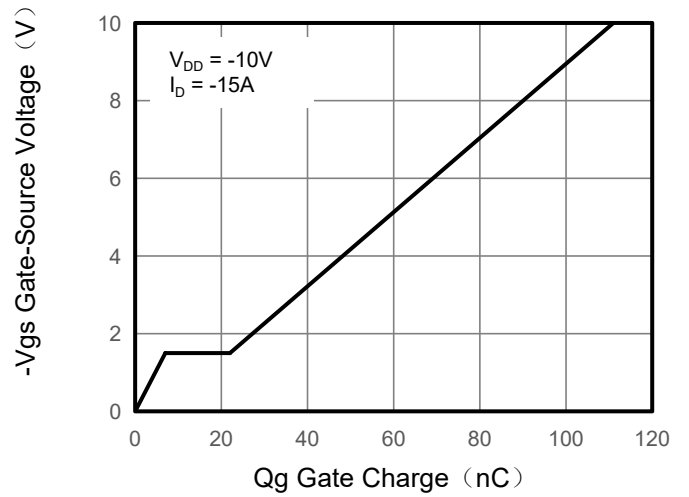


Figure 5. Capacitance

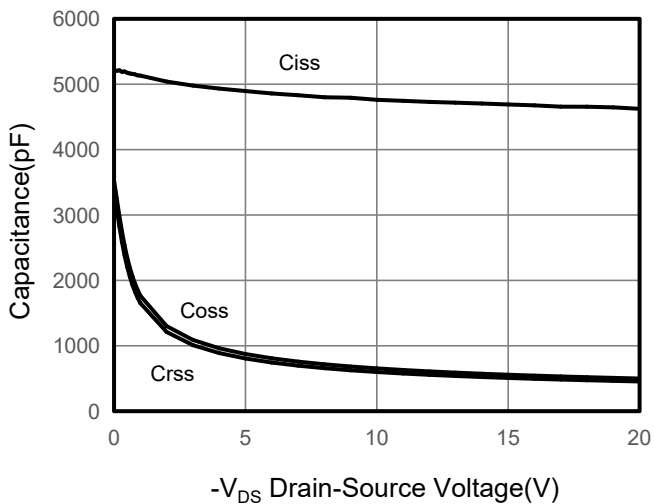
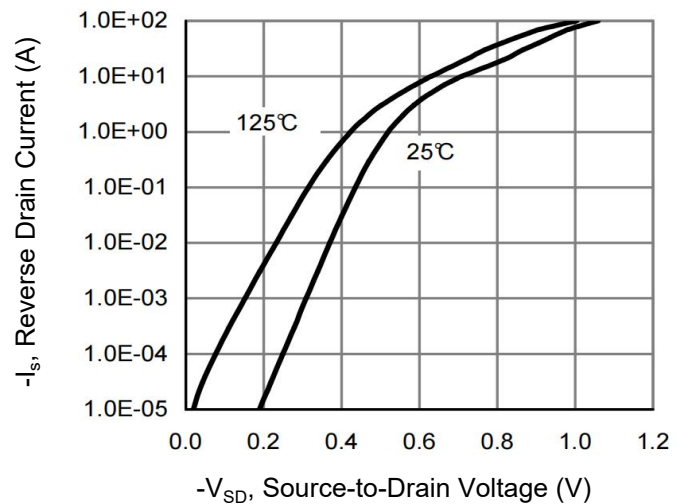


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

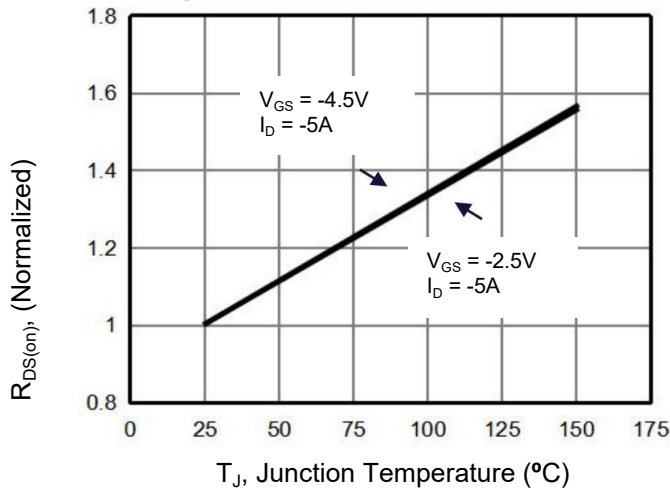


Figure 8. Safe Operation Area

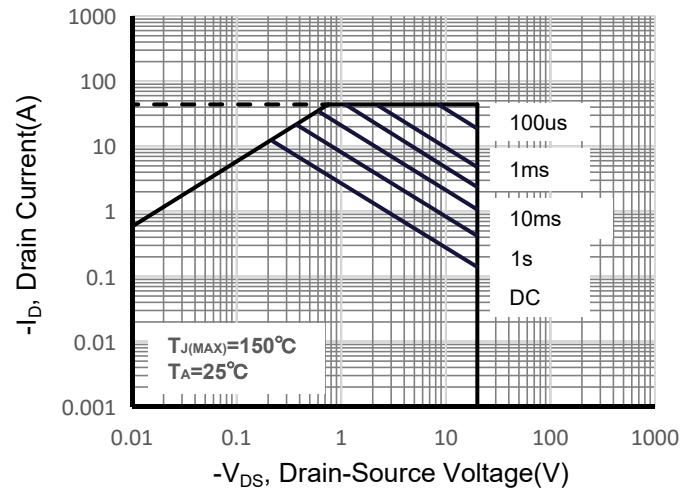


Figure 9. Maximum Continuous Drain Current vs Case Temperature

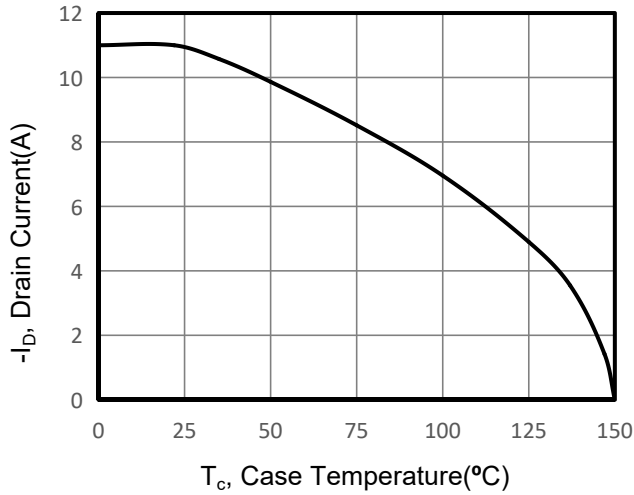
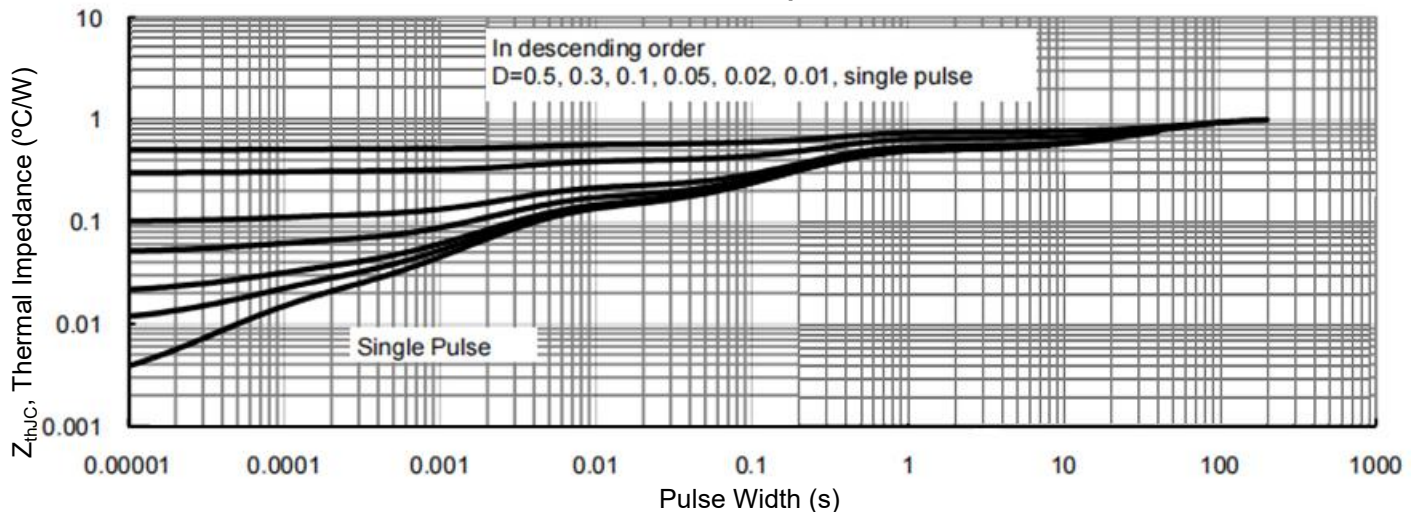


Figure 10. Normalized Maximum Transient Thermal Impedance



SOP-8 Package Information

