Application Note AN-44
LinkSwitch®-II Family

Design Guide

Introduction

LinkSwitch-II is a highly integrated monolithic switching IC family designed for off-line power supplies with outputs up to 6.1 W. Ideally suited for chargers, adapters, auxillary supplies and LED drivers, LinkSwitch-II provides constant voltage and constant current (CV/CC) output regulation without using an optocoupler or secondary feedback circuitry. The integrated output cable voltage drop compensation (LNK61x only), transformer inductance compensation, and external component temperature variation compensation allow high accuracy even at the end of the output cable. ON/OFF control optimizes efficiency across load and line, enabling designs to easily meet no-load and power supply efficiency requirements.

Each member of this family has a high-voltage power MOSFET and its controller integrated onto the same die. The internal start-up bias current is drawn from a high-voltage current source connected to the DRAIN pin, eliminating the need for external start-up components. The internal oscillator is frequency-modulated (jitter) to reduce EMI when operating in full frequency mode. In addition, the ICs have integrated functions that provide system-level protection. The auto-restart function limits dissipation in the MOSFET, the transformer, and the output diode during overload, output short-circuit, and open-loop conditions. The auto-recovering hysteretic thermal shutdown function disables MOSFET switching during a thermal fault. Power Integrations' EcoSmart® technology enables supplies designed around the LinkSwitch-II family members to consume <200 mW of no-load power at 230 VAC without an external bias circuit, and to consume below 30 mW with a low-cost bias circuit. This simplifies meeting harmonized energy efficiency standards such as the California Energy Commission (CEC), European Code of Conduct, and ENERGY STAR.

Basic Circuit Configuration

The circuit in Figure 1 shows the basic configuration of a flyback power supply designed using LinkSwitch-II. Because of the high-level integration of LinkSwitch-II, far fewer design issues are left to be addressed externally, resulting in one common circuit configuration for all applications. For example, different output power levels may require different values for some circuit components, but the circuit configuration stays unchanged.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply using the LinkSwitch-II family of devices. It provides guidelines to enable an engineer to quickly select key components and to complete a suitable transformer design. To simplify the task this application note refers directly to the PIXIs design spreadsheet, part of the PI Expert™ design software suite.

In addition to this application note you may also find the LinkSwitch-II Reference Design Kit (RDK), containing engineering prototype boards, reports, and device samples, useful as the

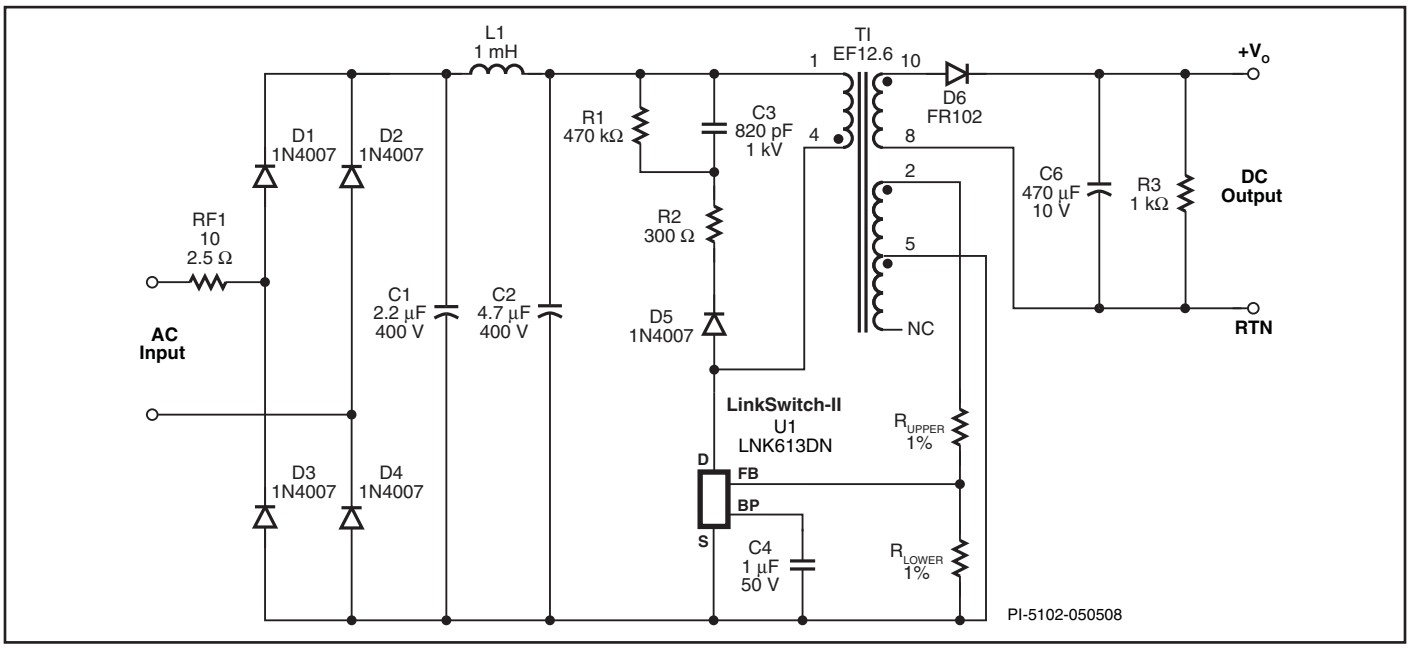

Figure 1. Typical LinkSwitch II Flyback Power Supply With Primary Sensed Feedback.

starting point for a new design. Further details on downloading PI Expert, obtaining a RDK, and updates to this document can be found at www.powerint.com.

Quick Start

To start immediately, use the following information to quickly design the transformer and select the components for a first prototype. Only the information described below needs to be entered into the PIXls spreadsheet; other parameters will be automatically selected based on a typical design. References to spreadsheet cell locations are provided in square brackets [cell reference].

- Enter AC input voltage range VAC_{MIN}, VAC_{MAX}, and minimum line frequency f_L [B3, B4, B5].
- Enter nominal output voltage (at end of cable if applicable) V_O [B6].
- Enter the nominal output current value [B7].
- Enter efficiency estimate [B9].
  - 0.7 for universal input voltage (85-265 VAC) or single 100/115 VAC (85-132 VAC), 0.75 for a single 230 VAC (185-265 VAC) design. (Adjust the number as needed after measuring the efficiency of the first prototype-board at maximum load and VAC_{MIN}.)
- Enter loss allocation factor Z [B10].
  - 0.5 for typical application (adjust the number accordingly after first proto-board evaluation)
- Select if external bias is desired. Enter YES or NO [B12].
  - Select YES for improved efficiency and minimized no-load input power.
- Enter C_{IN} input capacitance [B13].
  - ≥2 µF/W for universal (85-265 VAC) or single (100/115 VAC) line voltage.
  - 1 µF/W for single 230 VAC or single (195-265 VAC) line voltage.
  - Note: After selecting the LinkSwitch-II device, if the computed duty cycle [D59] is greater than 55%, increase the input capacitance.
- Select the LinkSwitch-II device from the drop-down list or enter directly [B16].
  - Select the device in Table 1 according to output power.

Output Power Table

Product	85 – 265 VAC	
	Adapter	Open Frame
LNK6X3PG/DG	2.5 W	3.1 W
LNK6X4PG/DG	3.5 W	4.1 W
LNK6X5PG/DG	4.5 W	5.1 W
LNK6X6PG/DG	5.5 W	6.1 W

Table 1. Output Power Table.

Note: LNK60x devices do not have output cable drop compensation. LNK61x devices have selectable output cable drop compensation.

- Enter device package PG for 7-pin dip, DG 7-pin SO8 surface mount (not LNK6x6), or GG 7-pin dip surface mount (LNK6x6 only) [B17].
- Enter the maximum operating frequency F_S [B21]. (F_S is the maximum operating frequency with nominal component values.)
  - Note: Recommended frequency is between 60 kHz and 90 kHz.
- Enter V_{DS} [B23], the on-state drain-source voltage drop. Use 10 V if no better data is available.
- Enter the output rectifier's forward voltage drop V_D [B24]. Use 0.5 for Schottky and 0.7 for standard PN-junction diodes.
- Verify that K_P [D25] is greater than 1.3 to ensure discontinuous operation. For best regulation performance, select a value for K_P greater than 1.5.
- If an external bias is selected in [B12], Enter the desired bias voltage [B33]. 10 V is recommended to minimize no-load input power.
- Enter 4.5 µs for D_{CON} [B37], the output rectifier's conduction time
- Enter the core type from the drop down menu [B44]. If the desired core is not listed, then you may enter a core's characteristics A_E, L_E and A_L ([B46] [B47] [B48]).
- Enter the bobbin width BW [B49].
- Enter the margin tape width in [B50], if margin tape is desired. Note: This reduces the winding width by twice the entered value.
- Enter the number of primary layers L [B51]. Use a maximum of 3 layers to limit the primary leakage inductance value.
- Enter the primary inductance tolerance $L_{P(TOLERANCE)}$ [B68].
- Enter in the transformer's core maximum flux density $B_{M(TARGET)}$ [B71]. Note: Use no more than the max flux density, 2500 Gauss, to keep the transformer's audible noise to acceptable levels. Follow the guidance in column F to address any warnings.
- Verify that the core's gap L_G [D76], the wire gauge AWG [D81], and the primary's winding current density CMA [D83] are within acceptable limits.
- Verify that the LinkSwitch-II drain voltage [D94] is less than 680 V.
- Use resistor values R_{UPPER} [D39] and R_{LOWER} [D40] for feedback resistors (Figure 1).
- Using PIV_S [D95] and I_{SRMS} [D88] determine the proper output rectifier.
- Select the input capacitor voltage rating to be above V_{MAX} [D56], and select the ripple current rating to be above I_{RIPPLE} [D62].
- Using V_O [B6], I_{SP} [D87], and I_{RIPPLE} [D89], determine the proper output filter capacitor.
- Using I_{AVG} [D60] and an estimated peak reverse voltage of 600 V to 1000 V, determine the input rectifier diodes (typically 1N4006 or 1N4007 types).
- Using I_{AVG} [D60] determine the proper input filter inductor current rating. Usually an inductor value of 1 mH to 2 mH is adequate to meet conducted EMI requirements.
- After building the prototype power supply, measure the output voltage and current at the peak power point. Enter the values used for R_{UPPER} and R_{LOWER} in cells [B98] and [B99], respectively.
- Enter the measured voltage in cell [B100]. Enter the measured current at the transition from CV to CC operation in cell [B101]. PIXls calculates the fine-tuned feedback resistors' values for the power supply. Install the closest 1% value resistors for R_{UPPER} [D102] and R_{LOWER} [D103].

Step-by-Step Design Procedure

Step 1. Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, I_O, η, Z, V_B, t_C, Bias Support, C_{IN}

ENTER APPLICATION VARIABLES					
VACMIN	85			V	Minimum AC Input Voltage
VACMAX	265			V	Maximum AC Input Voltage
fL	50			Hz	AC Mains Frequency
VO	5			V	Output Voltage (at continuous power)
IO	0.6			A	Power Supply Output Current (corresponding to peak power)
Power			3.00	W	Continuous Output Power
n			0.70		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
Add Bias Winding	YES		YES		Choose Yes to add a Bias winding to power the LinkSwitch-II.
CIN	9.4			uF	Input Capacitance

Figure 2. Application Variables Section of the Design Spreadsheet.

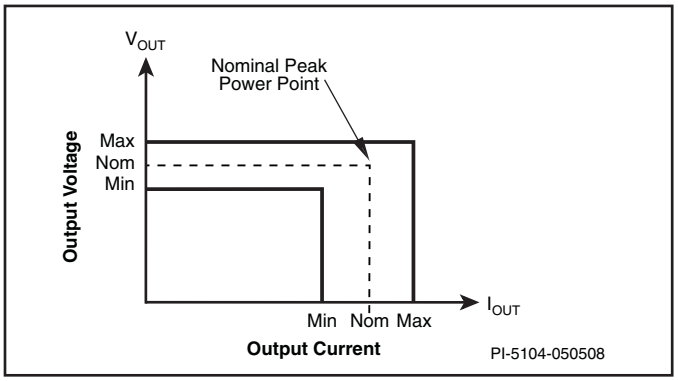

Figure 3. Output Characteristic Envelope Definitions.

Determine the input voltage range from Table 2.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100/115	85	132
230	195	265
Universal	85	265

Table 2. Standard Worldwide Input Line Voltage Ranges.

Note: For designs that have a DC rather than an AC input, enter the values for minimum and maximum DC input voltages, V_{MIN} and V_{MAX}, directly into the grey override cell on the design spreadsheet (see Figure 4).

Line Frequency, F_L

Typical line frequencies are 50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC, and 50 Hz for single 230 VAC inputs. These values represent typical, rather than minimum, frequencies. For most applications this gives adequate overall design margin. To design for the absolute worst case, or based on the product specifications, reduce these numbers by 6% (to 47 Hz or 56 Hz). For half-wave rectification use $F_L/2$. For DC input enter the voltage directly into Cells [B55] and [B56].

Nominal Output Voltage, V_O (V)

For both CV/CC and CV-only designs V_O is the nominal output voltage measured at the end of an attached cable carrying nominal output current. The tolerance for the output voltage is ±5% (including initial tolerance and over the datasheet-specified junction temperature range).

Nominal Output Current, I_O (A)

For CV/CC designs I_O is the nominal output current at nominal output voltage. For CV-only designs enter the specified output current plus 10%. The 10% factor ensures that while delivering the required output current the supply remains in CV mode, even with the effect of tolerances and temperature.

The nominal output voltage and current may not be the same as the name-plate specification in the case of an external adapter. Typically the nameplate specification represents the minimum output voltage and current of the adapter, ensuring that when measured, the adapter delivers at least $V_{O(MIN)}$ and $I_{O(MIN)}$, to satisfy energy-efficiency measurement-test methods. Refer to Figure 3 for definitions of output voltage and current.

Power Supply Efficiency, η

Enter the estimated efficiency of the complete power supply: measure voltage and current at the end of the output cable (if applicable) under full load conditions and worst-case line (generally lowest input voltage). (Start with 0.7 for universal input (85-265 VAC) or single 100/115 VAC (85-132 VAC) input voltage and 0.75 for a single 230 VAC (185-265 VAC) input voltage design.) Adjust the number accordingly after measuring the efficiency of the first prototype-board at the peak output power point, and at both VAC_{MIN} and VAC_{MAX}.

Power Supply Loss Allocation Factor, Z

This factor represents the ratio of power loss from the seondary relative to the total power loss from both the primary and secondary in the power supply. Z is used with the calculated efficiency to determine the actual power the power stage must deliver. For example, losses in the input stage (EMI filter, rectification, etc.) are not processed by the power stage

DC INPUT VOLTAGE PARAMETERS					
VMIN			89.82	V	Minimum DC bus voltage
VMAX			374.77	V	Maximum DC bus voltage

Figure 4. DC Input Voltage Parameters Section of the Design Spreadsheet.

(transferred through the transformer). Therefore, although they reduce efficiency, the transformer design is not impacted.

$$Z = \frac{\text{Secondary Side Losses}}{\text{Total Losses}}$$

Use a value of 0.5 if no other data is available.

Bridge Diode Conduction Time, t_C (ms)
This is the duration of the incoming AC sine wave during which the input diodes conduct, charging the input capacitance. This value is used in the calculation of the minimum voltage across the input capacitance at $V_{AC(MIN)}$. The actual value for t_C can be found by measuring the input current waveform on a prototype. Use a value of 3 ms if no other data is available.

Add Bias Winding, YES/NO
Enter YES if an external bias supply for LinkSwitch-II is required and a bias winding should be added to the transformer. External bias support increases efficiency, especially at light load, and lowers no-load input power consumption by disabling the internal high-voltage supply for the IC. If an external bias is not required, enter NO.

The efficiency gained (especially with light loads) when an external bias supply is used may raise the average efficiency enough to allow use of lower-cost options. In such cases, a low-cost PN- junction output diode may replace a higher-cost Schottky barrier-type diode, or the cable may be replaced by one constructed using a smaller diameter wire (higher impedance).

Total Input Capacitance, C_{IN} (µF)
Enter total input capacitance using Table 3 for guidance. The capacitance is used to calculate the minimum voltage, V_{MIN}, across the bulk capacitor. Select a value for C_{IN} that keeps V_{MIN} >70 V.

Total Input Capacitance per Watt Output Power (µF/W)	
AC Input Voltage (VAC)	**Full Wave Rectification**
100/115	3
230	1
85-265	3

Table 3. Suggested Total Input Capacitance for Different Input Voltage Ranges.

Step 2 – Enter LinkSwitch-II Variables: LinkSwitch-II Device and Package, V_{DS} and V_D.

Select the correct LinkSwitch-II device.

Refer to the LinkSwitch-II power table (Table 4) and select a device for the desired output power and operating conditions (sealed adapter or open frame).

Select the Package Type
In cell [B17], type PG for the 7-pin DIP, DG for the 7-pin surface mount SO8 or GG for 7-pin DIP surface-mount package (LNK6x6 only). (See Figure 5 for this and the next four steps).

LinkSwitch-II Output Power Table T_J ≤100 °C		
Product	85 – 265 VAC	
	Adapter	**Open Frame**
LNK6X3P/D	2.5 W	3.1 W
LNK6X4P/D	3.5 W	4.1 W
LNK6X5P/D	4.5 W	5.1 W
LNK6X6P/G	5.5 W	6.1 W

Table 4. Output Power Table.

Note: LNK60x devices do not have output cable drop compensation. LNK61x has selectable output cable drop compensation.

Select the Operating Frequency, F_S
Enter the nominal operating switching frequency F_S. F_S is the switching frequency when the power supply is operating at the nominal peak output power point. Select a frequency range between 60 kHz and 90 kHz. The minimum and maximum frequency in operation varies depending on the tolerance of L_P and the internal current limit. A warning will be displayed should the calculated minimum or maximum frequency be outside the range of 45 kHz to 100 kHz.

LinkSwitch-II ON State Drain-to-Source Voltage, V_{DS} (V)
This parameter is the average ON-state voltage developed across the LinkSwitch-II DRAIN and SOURCE pins. If no value is entered, the PIXIs uses a default value of 10 V.

Output Diode Forward-voltage Drop, V_D (V)
Enter the average forward-voltage drop of the output diode. Use 0.5 V for a Schottky diode or 0.7 V for a PN-junction diode (if specific diode data is not available). V_D has a default value of 0.5 V.

Ratio of MOSFET Off Time to Secondary Diode Conduction Time, K_P
For proper regulation, LinkSwitch-II requires the power supply to operate in discontinuous conduction mode. Verify that K_P is greater than 1.3 to ensure discontinuous operation. A value of 1.5 or greater is recommended. K_P should always be greater than 1, indicating discontinuous conduction mode, and is the ratio of primary MOSFET off time to the secondary diode conduction time.

$$K_P \equiv K_{DP} = \frac{(1-D) \times T}{t} = \frac{V_{OR} \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

Feedback Winding Parameter
The Feedback Winding Parameters are calculated by the PIXIs spreadsheet. N_{FB} is the number of feedback winding turns in the transformer. V_{FLY} and V_{FOR} represent the voltage across the feedback winding while the MOSFET is on (V_{FOR}) or off (V_{FLY}).

Bias Winding Parameters
If a bias winding is chosen (YES in cell [B12]), enter the bias voltage for V_B (Figure 7). Use 10 V to minimize no-load input power.

N_B is the number of additional turns stacked on top of the feedback turns (AC stacked).

ENTER LinkSwitch-II VARIABLES					
Chosen Device	LNK604		LNK604		Chosen LinkSwitch-II device
Package	PG		PG		Select package (PG, GG or DG)
ILIMITMIN			0.24	A	Minimum Current Limit
ILIMITTYP			0.25	A	Typical Current Limit
ILIMITMAX			0.28	A	Maximum Current Limit
FS			66.00	kHz	Typical Device Switching Frequency at maximum power
VOR			85.25	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10.00	V	LinkSwitch-II on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
KP			2.47		Ensure KDP > 1.3 for discontinuous mode operation

Figure 5. Enter LinkSwitch-II Variables Section of the Design Spreadsheet.

FEEDBACK WINDING PARAMETERS					
NFB			5.00		Feedback winding turns
VFLY			4.58	V	Flyback Voltage
VFOR			4.83	V	Forward voltage

Figure 6. Feedback Winding Parameters Section of the Design Spreadsheet.

BIAS WINDING PARAMETERS					
VB			10.00	V	Bias Winding Voltage. Ensure that VB > VFLY. Bias winding is assumed to be AC-STACKED on top of Feedback winding
NB			7.00		Bias Winding number of turns

Figure 7. Bias Winding Parameters Section of the Design Spreadsheet.

Step 3 – Select Output Diode Conduction Time, D_{CON} (µs)

D_{CON} is the output diode conduction time at the peak output power point. Changing the value for D_{CON} can be used to adjust the number of secondary and feedback winding turns for better bobbin winding window coverage. Increasing D_{CON} increases the number of turns.

The minimum value for D_{CON} is limited to 4.5 µs to ensure that under light loads when the feedback winding is sampled, 2.5 µs after the internal MOSFET is turned off, the output diode is still conducting. The maximum value of D_{CON} is normally limited by the value of K_P. As D_{CON} increases, K_P decreases until it reaches its minimum value of 1.3.

Resistors R_{UPPER} and R_{LOWER} are the calculated initial values for the feedback winding resistors (Figure 1).

Step 4 – Choose Core and Bobbin Based on Output Power and Enter A_E, L_E, A_L, B_W, L

These symbols represent core effective cross-sectional area A_E (cm^2), core effective path length L_E (cm), core ungapped effective inductance A_L ($nH/Turn^2$), bobbin width B_W (mm) and number of primary layers L.

By default, if the Core cell is left empty, the spreadsheet selects the smallest core size that meets the peak flux density limit. The user can change this selection and choose an alternate core from a list of commonly available cores (shown in Table 6). Table 5 provides guidance on the power capability of specific core sizes.

Core Size	Output Power Capability
EF12.6	3.3 W
EE13	3.3 W
EE16	6.1 W

Table 5. Output Power Capability of Commonly Used Sizes in LinkSwitch-II Designs.

DESIGN PARAMETERS					
DCON			4.50	us	Output diode conduction time
TON			4.20	us	LinkSwitch-II On-time (calculated at minimum inductance)
RUPPER			11.80	k-ohm	Upper resistor in Feedback resistor divider
RLOWER			7.91	k-ohm	Lower resistor in resistor divider

Figure 8. Design Parameters Section of the Design Spreadsheet.

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type					
Core	EE16		EE16		Enter Transformer Core. Based on the output power the recommended core sizes are EE13 or EE16
Bobbin			EE16_BOBBIN		Generic EE16_BOBBIN
AE			19.20	mm^2	Core Effective Cross Sectional Area
LE			35.00	mm^2	Core Effective Path Length
AL			1140.00	nH/turn^2	Ungapped Core Effective Inductance
BW			8.60	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			3.00		Number of Primary Layers
NS			6.00		Number of Secondary Turns. To adjust Secondary number of turns change DCON

Figure 9. Enter Transformer Core/Construction Variables Section of the Design Spreadsheet.

Transformer Core Size	
EE10	EF16
EF12.6	EF20
EE13	EF25
EE16	EFD15
EE19	EFD20
EE22	EFD25
EEL16	EFD30
EE16W	EI16
EEL19	EI19
EEL22	EI22
EE25	EI25
EEL25	

Table 6. List of Cores Provided in LinkSwitch-II PIXIs Spreadsheet.

The gray override cells [B44 through B51] can be used to enter the core and bobbin parameters directly. This is useful for either selecting a core that is not on the list, or if the specific core or bobbin information differs from that recalled by the spreadsheet.

For designs that require safety isolation between primary and secondary but are not using triple insulated wire, enter the width of the safety margin to be used on each side of the bobbin as parameter M. Universal input designs typically require a total margin of 6.2 mm, and a value of 3.1 mm entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical. However, for a total required margin of 6.2 mm (for example), enter 3.1 mm even if the physical margin is only on one side of the bobbin.

For designs using triple-insulated wire it may still be necessary to enter a small margin to meet required safety creepage distances. Typically many bobbins exist for each core size, each with different mechanical spacing. Refer to the bobbin data sheet or seek guidance from your safety expert or transformer vendor, to determine the requirement for your design. The margin reduces the available area for windings, so margin construction may not be suitable for transformers with smaller cores. If, after entering the margin, more than three primary layers (L) are required, either select a larger core or switch to a zero-margin design using triple-insulated wire.

Enter the number of primary layers (L). The maximum number of recommended primary layers is three. A larger number of layers increases leakage inductance, which increases losses.

N_S is the number of secondary turns. To increase the number of turns, increase the value of D_{CON} [B37].

Step 5 – Iterate Transformer Design and Generate Key Transformer Design Parameters

Iterate the design, making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column. Messages marked "!!! Info" provide guidance for acceptable parameters that can be further optimized. Once all

DC INPUT VOLTAGE PARAMETERS					
VMIN			89.82	V	Minimum DC bus voltage
VMAX			374.77	V	Maximum DC bus voltage

Figure 10. DC Input Voltage Parameters Section of the Design Spreadsheet.

CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.28		Maximum duty cycle measured at VMIN
IAVG			0.05	A	Input Average current
IP			0.24	A	Peak primary current
IR			0.24	A	Primary ripple current
IRMS			0.08	A	Primary RMS current

Figure 11. Current Waveform Shape Parameters Section of the Design Spreadsheet.

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			1589.61	uH	Minimum Primary Inductance
LPTYP			1766.23	uH	Typical Primary inductance
LP_TOLERANCE			10.00		Tolerance in primary inductance
NP			93.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG			183.79	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET			2500.00	Gauss	Target Flux Density
BM			2472.89	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 2500 is recommended
BP			2992.19	Gauss	Peak Operating Flux Density (calculated at maximum inducatnce and max current limit), BP < 3000 is recommended
BAC			1236.44	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			165.37		Relative Permeability of Ungapped Core
LG			0.11	mm	Gap Length (LG > 0.1 mm)
BWE			25.80	mm	Effective Bobbin Width
OD			0.28	mm	Maximum Primary Wire Diameter including insulation
INS			0.05		Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.23	mm	Bare conductor diameter
AWG			32.00		Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			64.00		Bare conductor effective area in circular mils
CMA		Info	765.31		!!! Info. CMA is on the higher side of recommenation but design will work. Consider reducing primary layers if possible

Figure 12. Transformer Primary Design Parameters Section of the Design Spreadsheet.

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TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			3.68	A	Peak Secondary Current
ISRMS			1.33	A	Secondary RMS Current
IRIPPLE			1.19	A	Output Capacitor RMS Ripple Current
CMS			266.09		Secondary Bare Conductor minimum circular mils
AWGS			25.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)

Figure 13. Transformer Secondary Design Parameters Section of the Design Spreadsheet.

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VOLTAGE STRESS PARAMETERS					
VDRAIN			573.79	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)
PIVS			29.18	V	Output Rectifier Maximum Peak Inverse Voltage

Figure 14. Voltage Stress Parameters Section of the Design Spreadsheet.

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FINE TUNING					
RUPPER_ACTUAL			11.80	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL			7.91	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measued) Output Voltage (VDC)			5.00	V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)			0.60	Amps	Measured Output current from first prototype
RUPPER_FINE			11.80	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 11.8 k-ohms
RLOWER_FINE			7.91	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 7.87 k-ohms

Figure 15. Fine Tuning Section of the Design Spreadsheet.

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warnings have been cleared, use the transformer design parameters to either wind a prototype transformer, or to send to a vendor for obtaining samples.

Primary Inductance, $L_{P(TYP)}$, $L_{P(MIN)}$ (µH), $L_{P(TOLERANCE)}$, (%)
The key transformer electrical parameters are $L_{P(TYP)}$, $L_{P(MIN)}$ (µH), $L_{P(TOLERANCE)}$ and represents the minimum primary inductance needed to deliver the nominal peak output power ($V_O \times I_O$).

As it is more common to specify the primary inductance to a vendor as a nominal value with tolerance, the value for $L_{P(TYP)}$ is calculated via the expression

$$L_{P(TYP)} = L_{P(MIN)} \times \left(1 + \frac{L_{P(TOLERANCE)}}{100}\right)$$

where $L_{P(TOLERANCE)}$ is the entered percentage tolerance. If no value is entered, PIXIs uses 10 by default, signifying $L_{P(TOLERANCE)}$ of ±10%.

The expression used to calculate $L_{P(MIN)}$ includes the output cable voltage drop via the entered value for efficiency and Z factor.

Primary Winding Number of Turns, N_P
This is the total number of primary winding turns.

Gapped Core Effective Inductance, A_{LG} (nH/T²)
This is the target core effective inductance at $L_{P(MIN)}$ for the typical A_{LG} value multiplied by 1+($L_{P(TOLERANCE)/100}$). This value is typically used by transformer vendors to purchase the cores with the correct gap size.

Target Flux Density, B_{M_TARGET} (Gauss)
B_{M_TARGET} is the operating core flux density and the AC flux swing. Use a maximum value of 2500 (0.25 T) to minimize audible noise generation.

Core Gap Length, L_G (mm)
L_G is the estimated core gap length. Values below 0.1 mm are generally not recommended for center-leg gapped cores due to the resultant increase in primary inductance tolerance. If you require such a low value, consult with your transformer vendor for guidance.

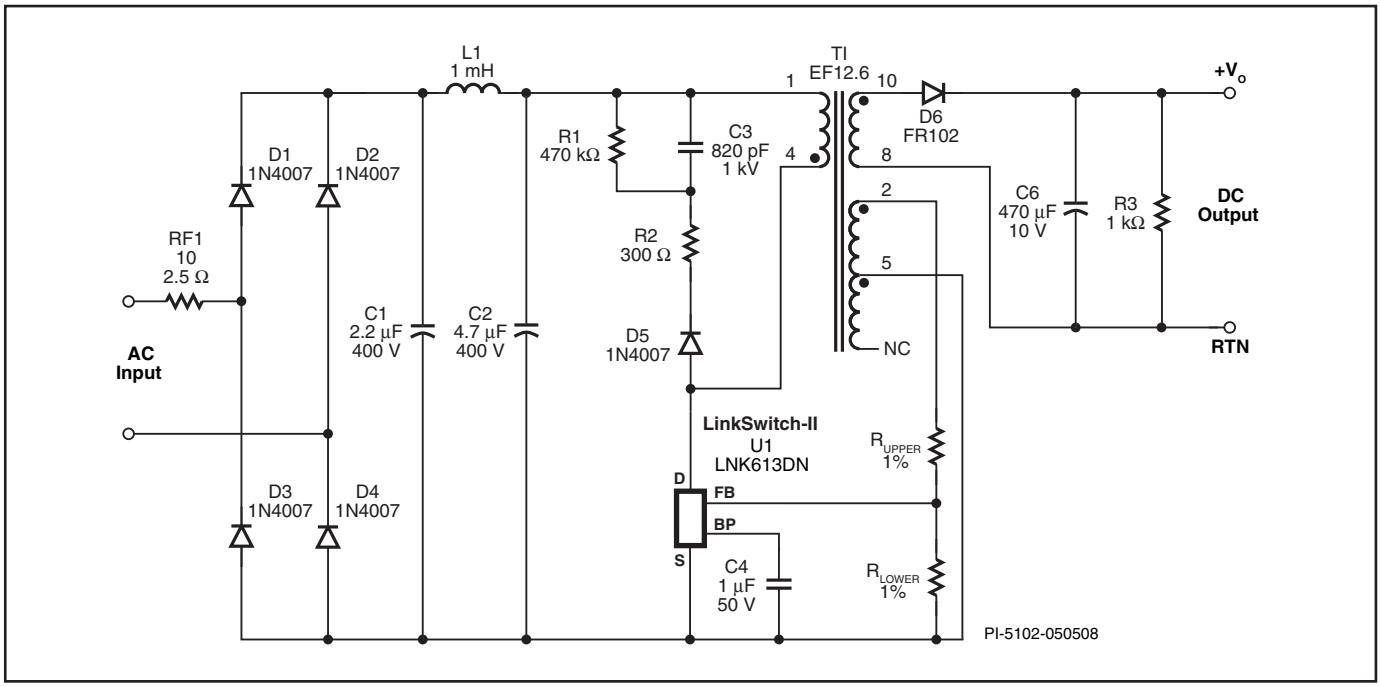


Figure 16. Typical LinkSwitch-II Flyback Power Supply.

Maximum Primary Winding Wire Outside Diameter, OD (mm)
This is the calculated maximum outside wire diameter to allow the primary winding to fit into the number of specified layers. When selecting the wire type use double-coated magnetic wire (rather than single-coated types) for improved reliability and reduced primary capacitance (lower no-load input power).

Primary Winding Wire Bare Conductor Diameter, DIA (mm)

Primary Winding Wire Gauge, AWG
This is the calculated conductor diameter rounded to the next smallest standard American Wire Gauge size.

Primary Winding Bare Conductor Effective Area, CM(C_{MILS})
CM is the effective conductor area in circular mils.

Primary Winding Wire Current Capacity, CMA (C_{MILS}/A)
CMA is the primary conductor area in circular mils (where 1 mil = 1/1000th of inch) per Amp. Values below the recommended minimum of 200 maybe acceptable if worst case winding temperature is verified.

Step 6 – Selection of Input Stage
The recommended input stage is shown in Table 7. It consists of a fusible element, input rectification, and line filter network.

The fusible element can be either a fusible resistor or a fuse. If a fusible resistor is selected, use a flameproof type. Depending on the differential line input surge requirements, a wire-wound type may be required. Avoid using metal or carbon film types as these can fail due to the inrush current when VAC_{MAX} is applied repeatedly to the supply.

In designs using a Y capacitor, place the EMI filter inductor on the opposite side of the input to the Y capacitor connection. For example, place the input inductor (L_{IN1}) between the negative terminals of the input capacitors (C_{IN1} and C_{IN2}) where the Y capacitor returns to the DC rail (see Figure 26).

For designs with outputs ≤1 W, it is generally lower cost to use half-wave rectification; and >1 W, full-wave rectification. The EMI immunity of half-wave rectified designs is improved by adding a second diode in the lower return rail. This provides EMI gating (EMI currents only flow when the diode is conducting) and doubles the differential surge immunity since the surge voltage is shared across two diodes.

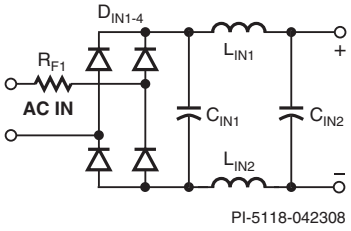
Half-wave rectification may be unsuitable if the supply specification requires output electrostatic discharge (ESD) testing. During such testing up to ±15 kV discharges of fixed energy are applied to the secondary of the supply (with respect to the primary). With half-wave rectification this voltage also appears across the input diodes, and may cause failure. With full-wave rectification the diode stress is clamped to the voltage across the input capacitance, preventing diode failure.

Conducted EMI filtering is provided by L_{IN1} and L_{IN2}, which together with C_{IN1} and C_{IN2}, form a pi (π) filter. A single inductor is suitable for designs below 3 W or where EMI is measured with the output of the supply floating (i.e. not connected to safety earth ground). Although two inductors are generally required above 3 W, a ferrite bead may be sufficient, especially where the output of the supply is floating.

Normally the total input capacitance is divided equally between the two input capacitors (C_{IN1} and C_{IN2}). However, for lower cost, two different capacitance values may be used. In this case select C_{IN1} as ≥1 µF (or as needed) to prevent overvoltage of the capacitor during differential mode surge. Select the second capacitor C_{IN2} to meet both an overall capacitance (C_{IN1} + C_{IN2}) of ≥2 µF/W of output power, and 3 µF/W of output power for highest low-line efficiency.

Differential-mode EMI generation is a strong function of the equivalent series resistance (ESR) of C_{IN2}, as this capacitor supplies the primary switching current. Selecting a lower ESR capacitor series for C_{IN2} than C_{IN1} can help reduce differential mode (low frequency) conducted EMI while optimizing the overall cost of the two capacitors.

Table 7 shows the input filter schematic, gives a formula for selecting C_{IN1} + C_{IN2}, and tells how to adjust the input capacitance for other input voltage ranges.



R_{F1}: 8.2 Ω, 1 W, Fusible, flameproof
L_{IN1}: 470 µH – 2.2 mH, 0.05 A – 0.3 A
L_{IN2}: Ferrite bead or 470 µH – 2.2 mH, 0.05 A – 0.3 A
C_{IN1} + C_{IN2}: ≥ 2 µF/W_{OUT}, 400 V, 85 VAC - 265 VAC
: ≥ 2 µF/W_{OUT}, 200 V, 100 VAC - 115 VAC
: ≥ 1 µF/W_{OUT}, 400 V, 185 VAC - 265 VAC
D_{INX}: 1N4007, 1 A, 1000 V

Table 7. Input Stage Recommendation.

Step 7 – Selection of BYPASS Pin Capacitor, Bias Winding and Feedback Components

BYPASS Pin Capacitor

For LinkSwitch-II LNK60x Devices (without output cable drop compensation)

Use a 1 µF BYPASS pin capacitor (C4 in Figure 16) with a voltage rating greater than 7 V. The capacitor's dielectric material is not critical. However, the absolute minimum value (including tolerance and temperature) must be ≥0.5 µF. The capacitor must be physically located close to the LinkSwitch-II BYPASS pin.

For LinkSwitch-II LNK61x Family of Devices (with output cable drop compensation)

Select the amount of output cable compensation via the value of the BYPASS pin capacitor (C4 in Figure 16). A value of 1 µF selects standard cable compensation. A 10 µF capacitor selects enhanced cable compensation. Table 8 shows the amount of compensation as a percentage of the output voltage from zero to full load for each LinkSwitch-II device and capacitor value.

Select the cable compensation to most closely match the percentage output voltage drop in the output cable. For example, a 5 V, 700 mA LNK615 design with a cable impedance of 300 mΩ has a cable voltage drop of -0.21 V. With a desired nominal output voltage of 5 V (at the end of the cable) this represents a voltage drop of -4.2%. In this case select the +5% (vs +7%) compensation, to give the smallest error, and to choose the BP pin capacitor value of 1 µF.

LinkSwitch-II Output Cable Compensation

Device	Bypass Pin Capacitor Value	Output Voltage Change Factor (%)
LNK613	1 µF	3.5
	10 µF	5.5
LNK614	1 µF	4.5
	10 µF	6.5
LNK615	1 µF	5
	10 µF	7
LNK616	1 µF	6
	10 µF	9

Table 8. Output Cable Voltage Drop Compensation vs Device and BP Pin Capacitor Value.

Bias Winding Components

The addition of a bias circuit decreases the no-load input power from ~200 mW down to less than 30 mW. This increases efficiencies at lighter loads enough to allow using cost-reducing options while still meeting average efficiency requirements. A PN-junction diode may replace a higher-cost Schottky-barrier diode, or the output cable may be replaced by one constructed of smaller diameter wire (higher impedance).

The power supply schematic shown in Figure 19 uses the bias circuit. Diode D6, capacitor C5, and resistor R4 form the bias circuit. If the output voltage is less than 8 V, then an additional transformer winding is needed, AC-stacked on top of the feedback winding. This provides a high enough voltage to supply the BYPASS pin even during low switching frequency operation at no-load.

In Figure 19 the additional bias winding (from pin 2 to pin 1) is stacked on top of the feedback winding (pin 4 to pin 2). Diode D6 rectifies the output and C5 is the filter capacitor. A 10 µF capacitor is recommended to hold up the bias voltage during the low frequency operation at no-load. The capacitor type is not critical but its voltage rating should be above the maximum value of V_{BIAS}. The recommended current into the BP pin is equal to the IC supply current (~0.5 mA). The value of R4 is calculated according to

$$(V_{BIAS} - V_{BP})/I_{S2}$$

where V_{BIAS} (10 V typical) is the voltage across C5, I_{S2} (0.5 mA typical) is the IC supply current, and V_{BP} (6.2 V typical) is the BP pin voltage. The parameters I_{S2} and V_{BP} are provided in the parameter table of the LinkSwitch-II data sheet. Diode D6 can be any low-cost diode such as FR102, 1N4148, or BAV19/20/21. The diode voltage stress is given in the Bias Winding Parameter section of the design spreadsheet.

If the feedback winding voltage (V_{FLY} in the design spreadsheet) is >7 V an additional winding is not required. In this case, connect D6 directly to the feedback winding at pin 2 of the transformer and eliminate the bias winding between pins 1 and 2.

Feedback Pin Resistor Values
Initial Values
Resistors R_{UPPER} and R_{LOWER} form a resistor divider network that sets the voltage on the FEEDBACK (FB) pin during both the on-time and off-time of the internal MOSFET.

During CV operation the controller regulates the FB pin voltage to remain at V_{FBth} using an ON/OFF state-machine. The feedback pin voltage is sampled 2.5 µs after the turn-off of the internal MOSFET. At light loads the current limit reduces to decrease the transformer flux density.

During CC operation the switching frequency is adjusted as the feedback pin voltage changes, to provide constant output-current regulation.

During the MOSFET on time the FB pin voltage is used to monitor the DC input voltage and thereby minimize CC variation across the input line range.

The initial values of R_{UPPER} and R_{LOWER} are provided in cells [D39] and [D40], for use in the initial prototype build. Once a prototype has been built and tested follow the Fine-tuning procedure described below to determine the final resistor values. Use the closest 1% values for best results. Place R_{UPPER} and R_{LOWER} as close to the Feedback pin as possible.

Fine-tuning
Enter the fine-tuning values into the Fine Tuning section of the design spreadsheet (Figure 15) after building a prototype power supply. Enter the actual values used for feedback resistors R_{UPPER} and R_{LOWER} in cells [D98] and [D99], and the measured power supply output voltage and current at the peak output power point in cells [D100] and [D101]. The PIXls spreadsheet will calculate the refined feedback resistor values for $R_{UPPER(FINE)}$ and $R_{LOWER(FINE)}$ to center both the output voltage and current.

Step 8 – Selection of Output Diode and Pre-load

The output rectifier diode should be either a fast or an ultrafast recovery PN junction or Schottky-barrier type.

Select a diode with sufficient margin to the specified voltage rating (V_R). Typically $V_R \geq 1.2 \times PIVs$, where PIVs is taken from the Voltage Stress Parameters section of the spreadsheet. Once a prototype is completed use an oscilloscope to measure the actual diode stress at VAC_{MAX}.

Select the diode with the closest rating to $I_D \geq 2 \times I_O$, where I_D is the diode's rated current and I_O is the output current. Take the diode's self-heating into consideration and use a larger diode, if needed, to meet thermal or efficiency requirements.

Table 9 lists some of the suitable Schottky and ultra-fast diodes that may be used with LinkSwitch-II circuits.

As the output voltage is sampled at the switching frequency, a minimum switching frequency is maintained at no-load to give acceptable transient load performance. Therefore, if the supply can operate unloaded, use a pre-load resistor to prevent the output voltage from rising under very light (<~25 mW) or no-load conditions (see resistor R3 in Figure 16).

For designs where output voltage regulation must be maintained at zero load, start with a resistor value that represents a load of approximately 25 mW at the nomimal output voltage. For example, for a 5 V output use a pre-load resistor value of 1 kΩ.

Series Number	Type	VR Range	I_F	Package	Manufacturer
		V	A		
1N5817 to 1N5819	Schottky	20-40	1	Leaded	Vishay
SB120 to SB1100	Schottky	20-100	1	Leaded	Vishay
11DQ50 to 11DQ60	Schottky	50-60	1	Leaded	Vishay
1N5820 to 1N5822	Schottky	20-40	3	Leaded	Vishay
MBR320 to MBR360	Schottky	20-60	3	Leaded	Vishay
SS12 to SS16	Schottky	20-60	1	SMD	Vishay
SS32 to SS36	Schottky	20-60	3	SMD	Vishay
UF4002 to UF4006	Ultrafast	100-600	1	Leaded	Vishay
UF5401 to UF5408	Ultrafast	100-800	3	Leaded	Vishay
ES1A to ES1D	Ultrafast	50-200	1	SMD	Vishay
ES2A to ES2D	Ultrafast	50-200	2	SMD	Vishay
SL12 to SL23	Schottky (low V_F)	20-30	1	SMD	Vishay
SL22 to SL23	Schottky (low V_F)	20-30	2	SMD	Vishay
SL42 to SL44	Schottky (low V_F)	20-30	4	SMD	Vishay

Table 9. List of Recommended Diodes That May be Used With LinkSwitch-II Designs.

For designs where the output voltage can rise under no-load conditions, select the pre-load resistor value such that the output voltage is within the maximum output voltage specification. Limit the maximum voltage rise at no-load to <50% of the normal output voltage to minimize increases in input power due to increases in the primary clamp and bias winding dissipation.

Since a pre-load resistor also increases the no-load losses, where the specification allows, adjust the no-load voltage to trade-off lower no-load input power with high no-load output voltage as needed.

Step 9 – Select Output Capacitor and Optional Post Filter

Select the capacitor voltage to be ≥1.2 × $V_{O(MAX)}$.

Select the initial capacitor choice using the maximum allowable equivalent series resistance (ESR) expression below:

$$ESR_{MAX} = \frac{V_{RIPPLE(MAX)}}{I_{SP}}$$

Where $V_{RIPPLE(MAX)}$ is the maximum specified output ripple and noise and I_{SP} is the secondary peak current from the Transformer Secondary Parameters section of the design spreadsheet.

The absolute minimum capacitance (excluding the effect of ESR) is given by:

$$C_{OUT(MIN)} = \frac{I_{O(MAX)}\left(\frac{1}{F_S} - D_{CON}\right)}{V_{RIPPLE(MAX)}}$$

Where $I_{O(MAX)}$ is the maximum output current, F_S is switching frequency, D_{CON} is the output diode conduction time and $V_{RIPPLE(MAX)}$ is the maximum allowable output ripple voltage. Verify that the ripple current rating of the capacitor is ≥ the I_{RIPPLE} value (from the Transformer Secondary Parameters section of the design spreadsheet). If not, select the smallest capacitance value that meets this requirement. Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from the data sheet maximum. This should be considered to ensure that the capacitor is not oversized for cost reasons.

To reduce the physical size of the output capacitor an output LC post filter can be used to reduce the ESR related switching noise. In this case select either a 1 µH to 3.3 µH inductor with a current rating ≥I_O or a ferrite bead for designs with I_O<~500 mA. The second capacitor is typically 100 µF or 220 µF with a low ESR for good transient response. As the secondary ripple current does not pass through this capacitor there are no specific ESR or ripple current requirements.

The output capacitor may also be split into two physical capacitors. Here the overall ripple current rating is equal to the sum of the ratings of each individual capacitor.

Step 10 – Selection of Primary Clamp Components

Three common clamp arrangements, shown in Table 10, are suitable for LinkSwitch-II designs.

For RCD and RCDZ type circuits, minimize the value of C_{C1} and maximize R_{C2} while maintaining the peak drain voltage to <680 V. Larger values of C_{C1} may cause higher output ripple voltages due to the longer settling time of the clamp voltage impacting the sampled voltage on the feedback winding.

Common Primary Clamp Configurations

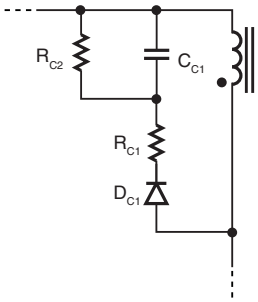
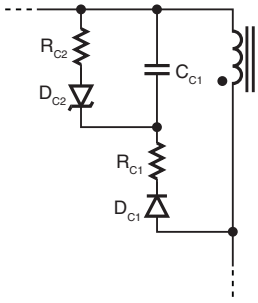
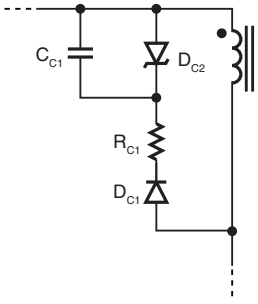
RCD	RCDZ (Zener Bleed)	RDZ (Zener)
 PI-5107-110308	 PI-5108-110308	 PI-5109-041308
D_{C1}: 1N4007, 1 A, 1000 V R_{C1}: 100 Ω - 300 Ω, 1/4 W C_{C1}: 470 pF - 1000 pF R_{C2}: 330 kΩ - 680 kΩ, 1/2 W	D_{C1}: 1N4007, 1 A, 1000 V D_{C2}: BZY97Cxxx (xxx = 90 V to 120 V) R_{C1}: 100 Ω - 300 Ω, 1/4 W R_{C2}: 47 kΩ - 150 kΩ, 1/2 W C_{C1}: 470 pF - 1000 pF	D_{C1}: 1N4007, 1 A, 1000 V R_{C1}: 100 Ω - 300 Ω, 1/4 W C_{C1}: 470 pF - 1000 pF (optional) D_{C2}: BZY97Cxxx(xxx = 150 V to 200 V)

Table 10. Primary Clamp Configurations Suitable for LinkSwitch-II Designs.

For RDZ configuratjions, C_{C1} is optional and helps recover some of the leakage inductance energy. Resistor R_{C1} dampens ringing and should be tuned to minimize undershoot (see Tips For Design Section) and reduce conducted EMI. The RCD configuration provides lowest cost. The RCDZ circuit maintains the low EMI generation of the RCD configuration but lowers no-load input power consumption. The RDZ configuration provides lowest no-load consumption, but at the cost of higher EMI.

Example Transformer Winding Arrangement Including E-Shields™

Once the PIXls spreadsheet design is complete all the necessary information is available to create a transformer design. In this section some practical tips are presented on winding order and the inclusion of Power Integrations proprietary E-Shield techniques. Shield windings improve conducted EMI performance and simplify the input filter stage by eliminating the need for a common mode choke and reducing the value of or eliminating the Y-class capacitor connected between the primary and secondary. Refer to Figures 17 and 18 to reference winding numbers (WDx).

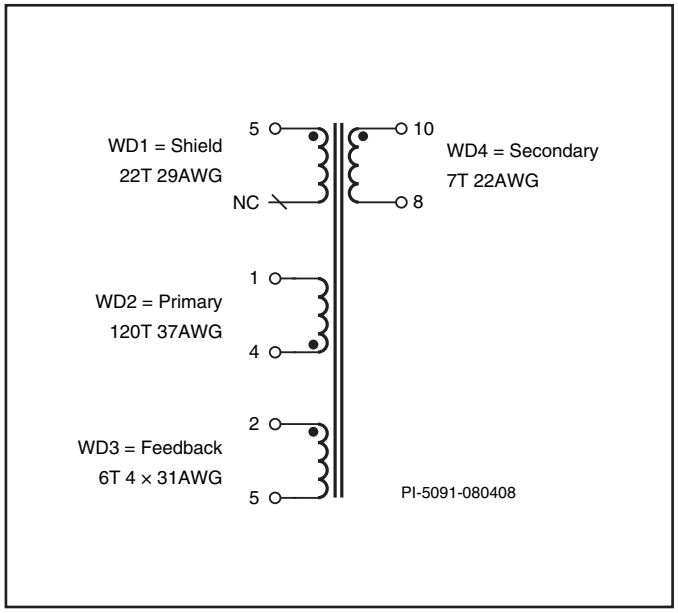


Figure 17. Typical Transformer Schematic.

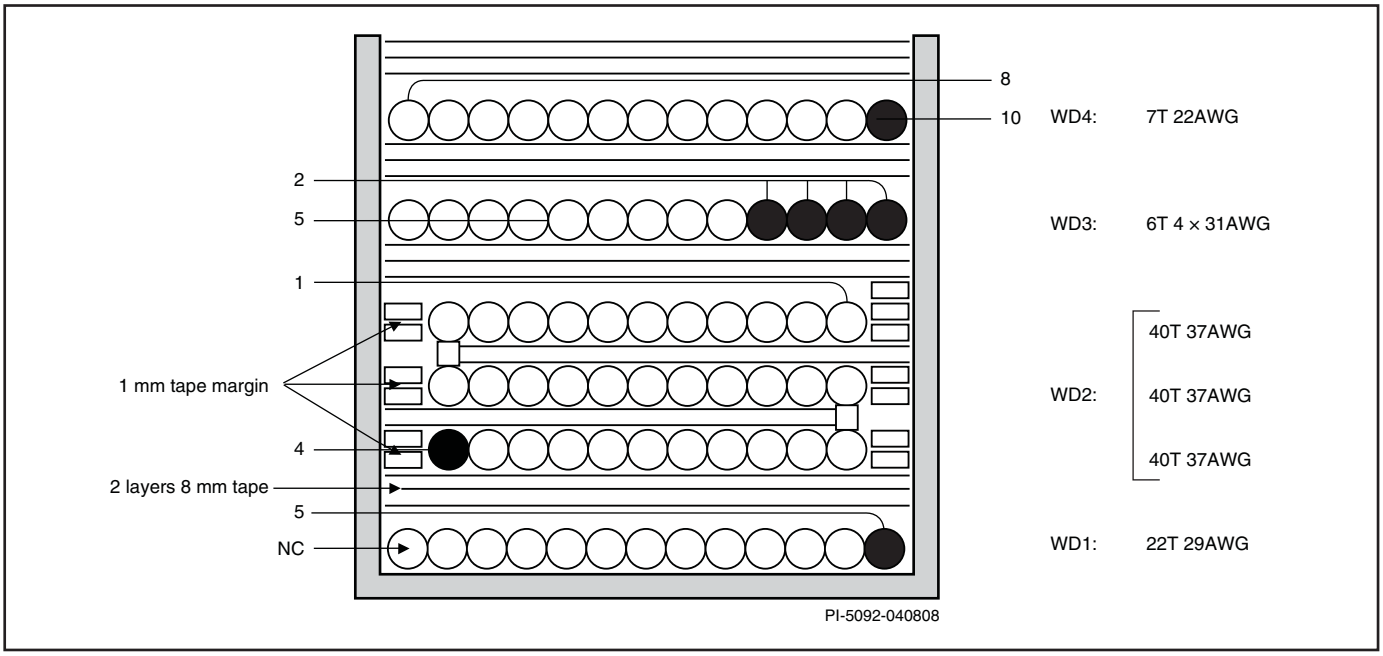


Figure 18. Typical Mechanical Construction of LinkSwitch-II Transformer.

Shield Winding

The first layer of the transformer is a shield (WD1). Calculate the number of turns by taking the number of primary turns N_P [D69] from PIXls and dividing it by the number of layers L [D51]. Divide the result by 2 ($N_{SHEILD} = 0.5 \times (N_P/L)$). This gives a starting value which may need to be adjusted to minimize conducted EMI emissions. Note that the start (black dot) of the shield winding is on the opposite side of the bobbin from the start of the primary winding. The finish end of the shield winding is floating. Select a wire gauge that completely fills the bobbin width.

Primary Winding

The second winding (WD2) is the primary. From PIXls find the number of turns N_P [D69], number of layers L [D51] and the wire gauge AWG [D81]. As shown in Figure 18, the start of the primary is on the opposite side of the bobbin from the Shield's start. An optional 1 mm tape can be used to improve EMI repeatability by making the transformer design less sensitive to production variation. To include the tape margin, enter a margin value of 1 mm into cell [B50] of the PIXls spreadsheet.

Feedback Winding

The feedback winding is the third winding (WD3) on the bobbin. From PIXls find the number of turns N_{FB} [D28]. To reduce conducted EMI emissions, this winding must cover the complete bobbin width. A multi-filar winding is used to achieve this and some experimentation may be needed to find the optimum wire gauge and number of filar (parallel winding wires). Generally more than 4 filar is not recommended due to manufacturability considerations when multi-filar windings are terminated onto a single bobbin pin.

Secondary Winding

The final winding is the Secondary Winding (WD4). From PIXls find the number of secondary turns N_S [D52]. Start the secondary winding on the same side of the bobbin as the start of the feedback winding. Select a gauge wire to completely fill the bobbin winding window width. Triple-insulated wire is recommended for the secondary winding to avoid the need to use wide tape margins to meet safety spacing requirements (6 mm to 6.2 mm typical) and minimize the transformer core size required.

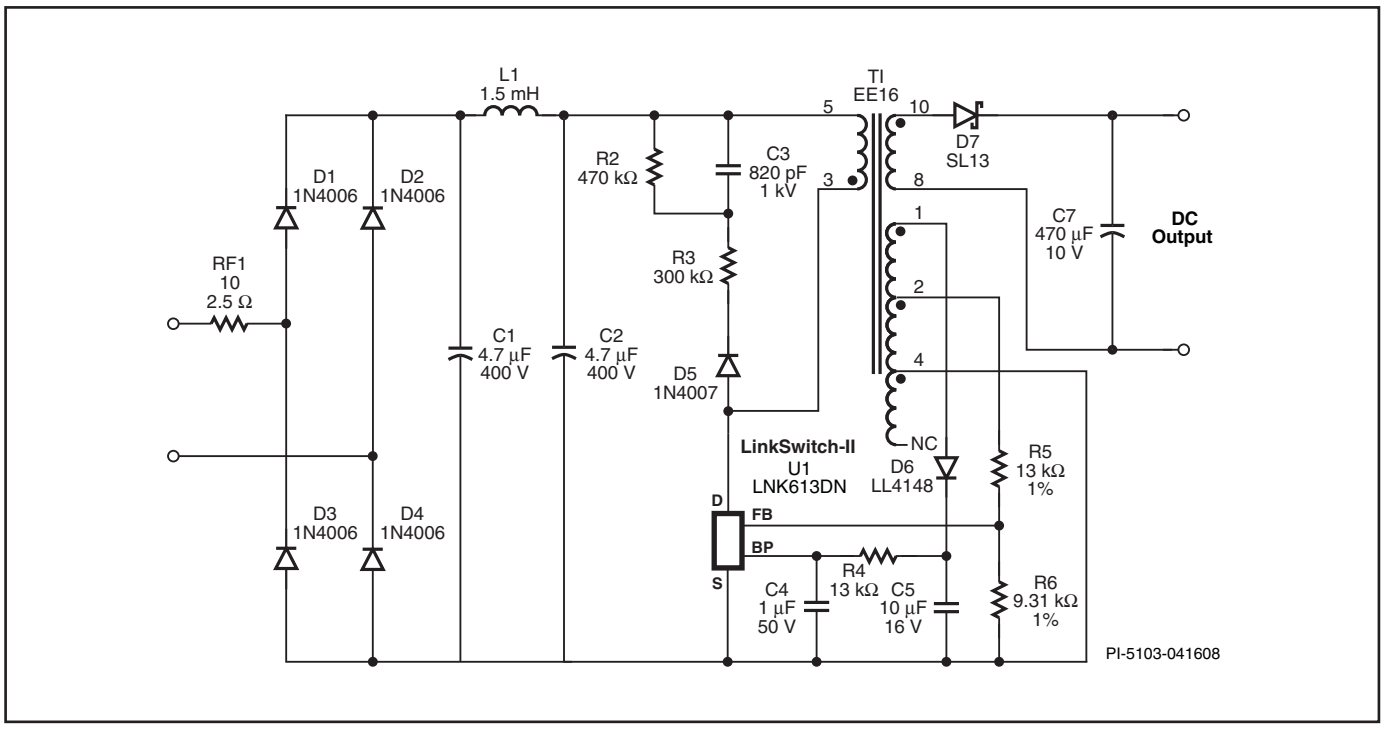


Figure 19. LinkSwitch-II Flyback Power Supply with Bias Circuit for Reduced No-load Input Power and Higher Light Load Efficiency.

Example of a Transformer With the Additional Bias Winding
Figures 20 and 21 show the schematic and build diagram, respectively, for a transformer that requires a bias winding.

The construction technique for this transformer is the same as that for a transformer without a bias winding, except the bias winding is inserted between the primary and the feedback winding layers. The number of additional turns added to the feedback winding is (N_B) shown in cell [D34] of PIXls.

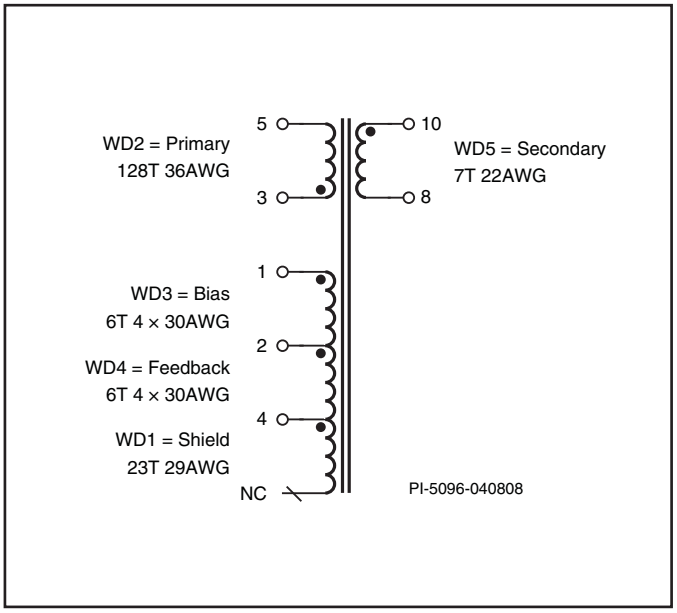


Figure 20. Transformer Schematic with Bias Winding.

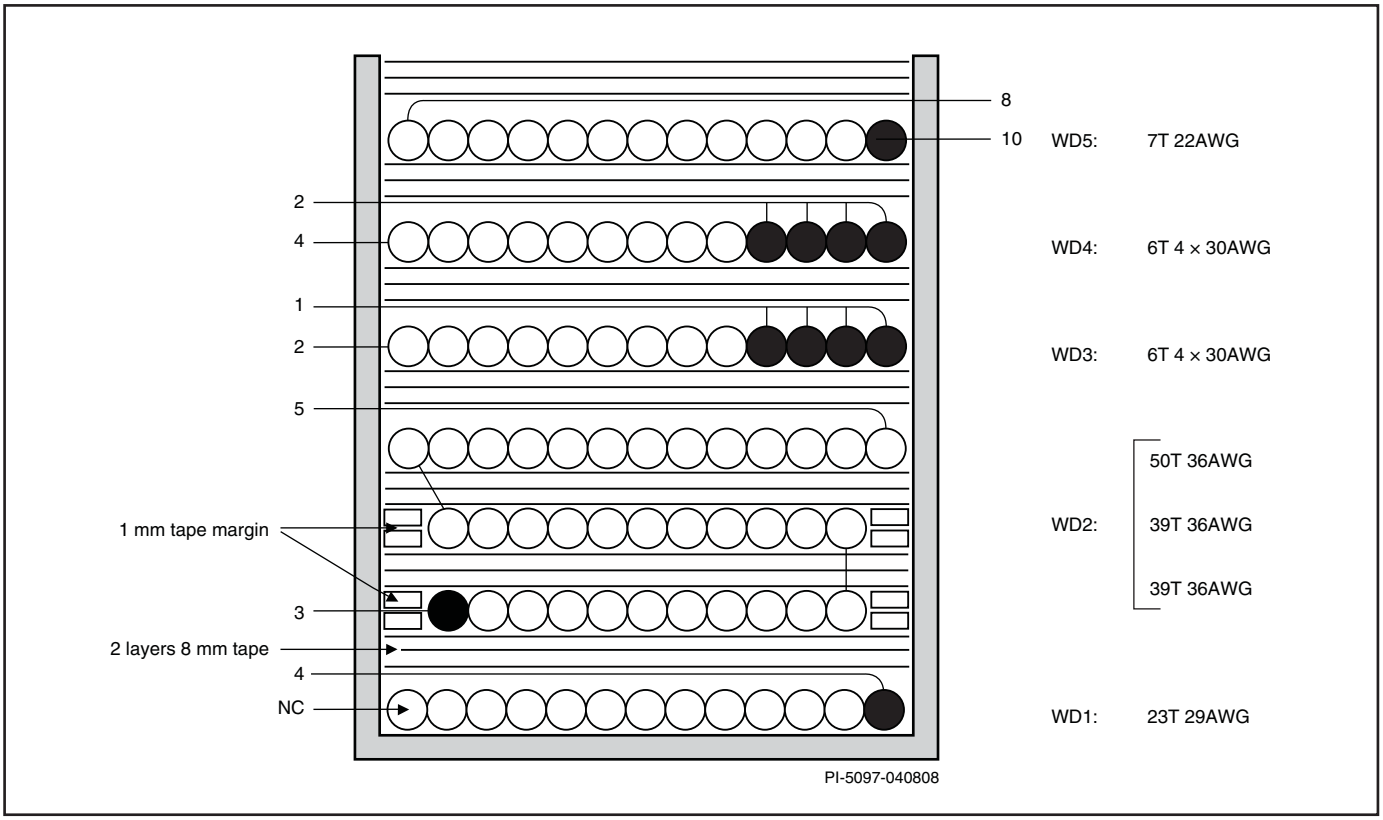


Figure 21. Transformer with Additional Bias Winding Build Diagram.

Tips For Designs

Reflected Output Voltage (V_{OR}) Adjustment

Users of design spreadsheets for other Power Integrations device families may notice that some parameters (V_{OR}, N_S and N_P) cannot be changed directly in the LinkSwitch-II spreadsheet. To change these parameters, use the relationships shown below:

V_{OR}: Increasing D_{CON} or F_S will decrease the value of V_{OR}
N_S: Increasing D_{CON} decreases N_S
N_P: Determined by $B_{M(TARGET)}$

Output Tolerance

Each LinkSwitch-II device is factory-trimmed to ensure a very tight initial CC tolerance of ±2.5% using a representative power-supply test module (shown in Figure 21 of the LinkSwitch-II data sheet). This is represented in the data sheet by the parameter I_O, Normalized Output Current.

The tight tolerances of the Feedback Pin Voltage (V_{FBth}) and small temperature coefficient (TC_{VFB}) provide tight regulation of the output voltage during CV operation

In the P/G package, LinkSwitch-II provides an overall output tolerance (including line, component variation, and temperature) of ±5% for the output voltage in CV operation and ±10% for the output current during CC operation, over a junction temperature range of 0 °C to 100 °C.

For the D package (SO8) additional CC variance may occur due to stress caused by the manufacturing flow (i.e. solder-wave immersion or IR reflow). A sample power supply build is therefore recommended to verify production tolerances for each design.

Design Recommendations

Circuit Board Layout

LinkSwitch-II is a highly integrated power supply solution that integrates on a single die both the controller and the high voltage MOSFET. The presence of high switching currents and voltages together with analog signals makes it especially important to follow good PCB design practices to ensure stable and trouble-free power supply operation. See Figures 22 and 23 for recommended circuit board layouts for the LinkSwitch-II.

When designing a printed circuit board for the LinkSwitch-II based power supply, it is important to follow the guidelines below:

Single-point Grounding

Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the LinkSwitch-II SOURCE pin and bias-winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor.

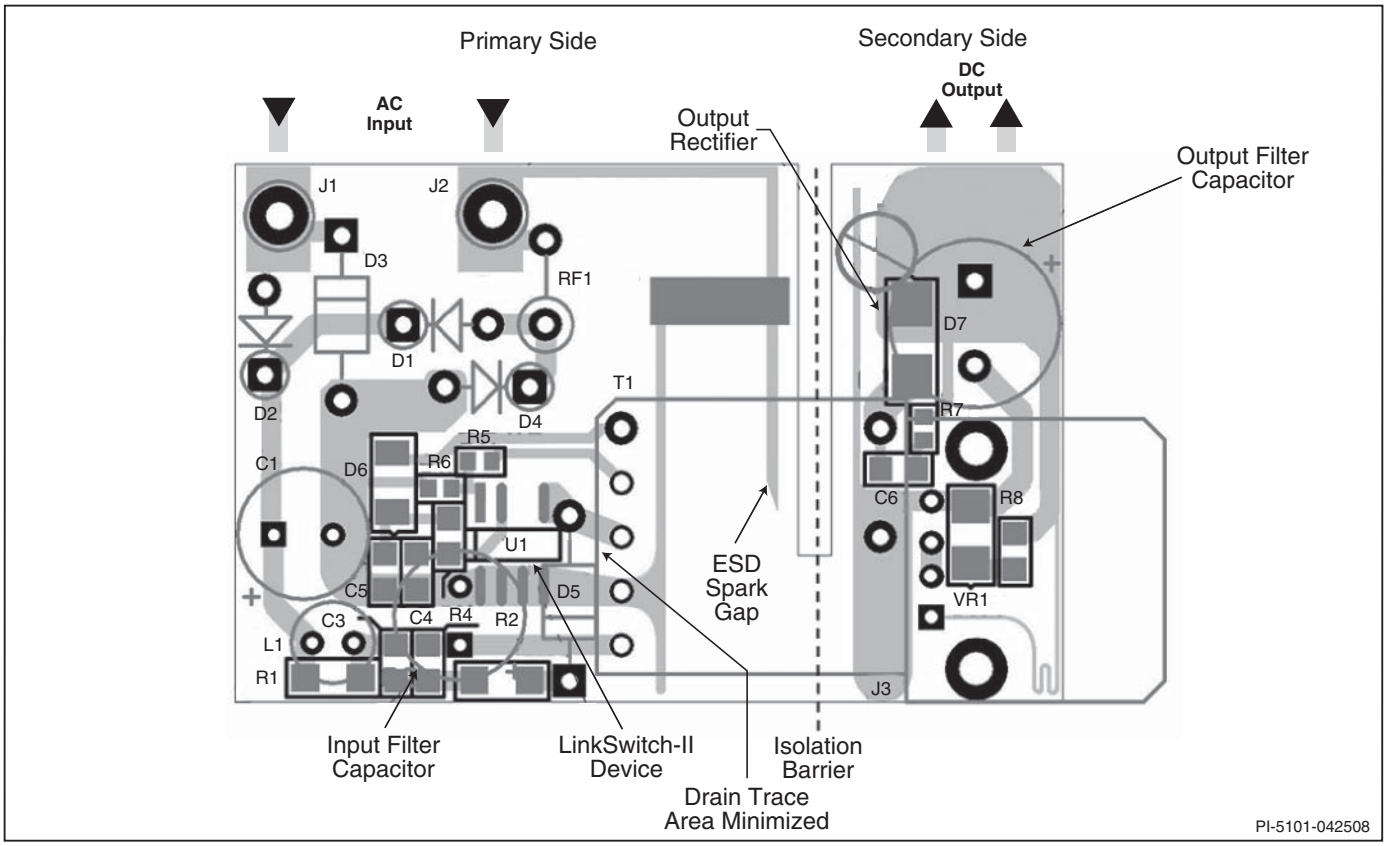


Figure 22. PCB Layout Example Using SO8 Package for 2.5 W Output Power.

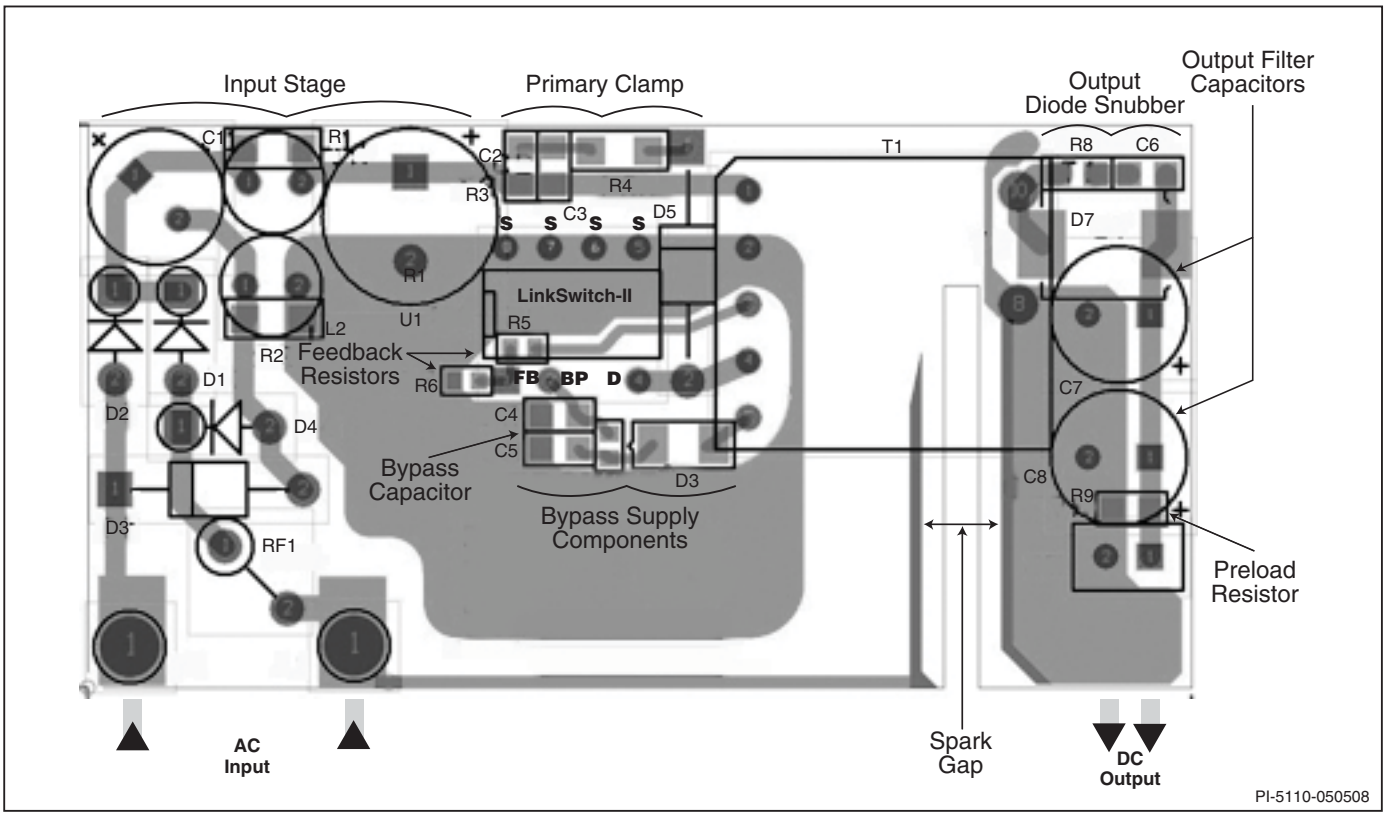


Figure 23. PCB Layout Example Using P Package for 5.1 W Output Power.

Bypass Capacitor
The BYPASS pin capacitor should be located as close as possible to the SOURCE and BYPASS pins.

Feedback Resistors
Place the feedback resistors directly at the FEEDBACK pin of the LinkSwitch-II device. This minimizes noise coupling.

Thermal Considerations
The copper area connected to the source pins provides the LinkSwitch-II heat sink. A good estimate is that the LinkSwitch-II will dissipate 10% of the output power. Provide enough copper area to keep the source pin temperature below 90 °C. Higher temperatures are allowable only if an output current (CC) tolerance above ±10% is acceptable in your design. In this case, a maximum source pin temperature below 110 °C is recommended to provide margin for part-to-part $R_{DS(ON)}$ variation.

Secondary Loop Area
To minimize reflected trace inductance and EMI minimize the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor. In addition, provide sufficient copper area at the anode and cathode terminal of the diode for heatsinking. Provide a larger area at the quiet cathode terminal. A large anode area can increase high-frequency radiated EMI.

Electrostatic Discharge Spark Gap
A trace is placed along the isolation barrier to form one electrode of a spark gap. The other electrode on the secondary is formed by the output return node. The spark gap directs ESD energy from the secondary back to the AC input. The trace from the AC input to the spark gap electrode should be spaced away from other traces to prevent unwanted arcing to other nodes, and possible circuit damage.

Drain Clamp Optimization
LinkSwitch-II senses the feedback winding on the primary side to regulate the output. The voltage that appears on the feedback winding is a reflection of the secondary winding voltage while the internal MOSFET is off. Therefore, any leakage-inductance induced ringing can affect output regulation. Optimizing the drain clamp to minimize the high frequency ringing gives the best regulation. Figure 24 shows the desired drain voltage waveform. Compare this to Figure 25 with a large undershoot, caused by ringing due to leakage inductance. This ringing, and its effects, degrades the output voltage regulation performance. To reduce this ringing (and the undershoot it may cause) adjust the value of the resistor in series with the clamp diode.

Quick Design Checklist

As with any power supply design, verify your LinkSwitch-II design on the bench to make sure that component specifications are not exceeded under worst-case conditions.

The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that peak V_{DS} does not exceed 680 V at highest input voltage and maximum output power.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage, and maximum output load, observe drain current waveforms at start-up for any signs of transformer saturation and excessive leading-edge current spikes. LinkSwitch-II has a leading edge blanking time of 170 ns to prevent premature termination of the ON-cycle.
3. Thermal check – At maximum output power, both minimum and maximum input voltage, and maximum ambient temperature, verify that temperature specifications are not exceeded for LinkSwitch-II, transformer, output diodes, and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch-II, as specified in the data sheet. To assure 10% CC tolerance a maximum source-pin temperature of 90 °C is recommended.

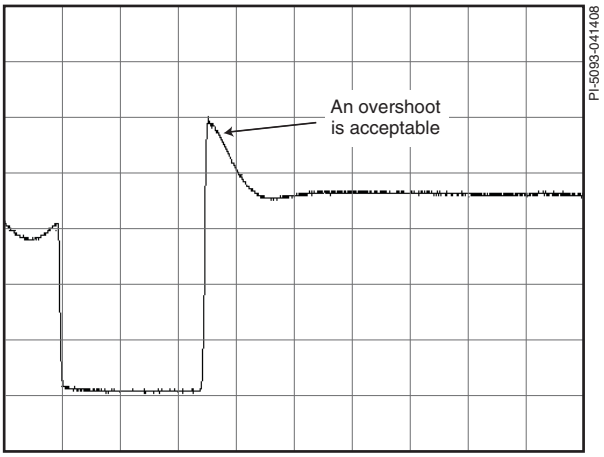


Figure 24. Desired Drain Waveform.

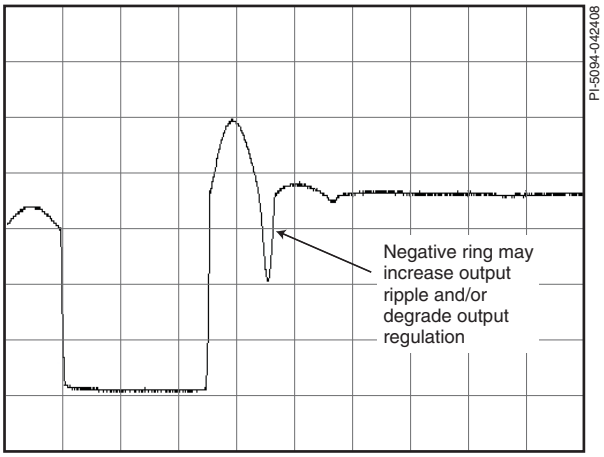


Figure 25. Undesirable Drain Waveform.

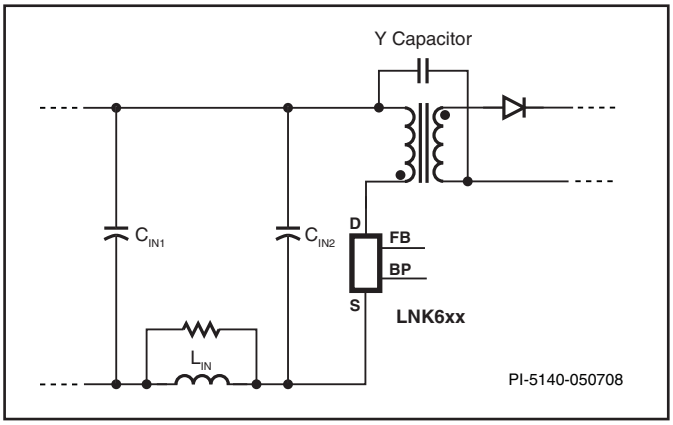


Figure 26. Correct Location of Input Inductor When Using a Y Capacitor.

Notes

Notes

Revision	Notes	Date
A	Initial Release	05/08
B	Minor changes to pages 4, 7, 12	07/08
C	Updated Figure 17 and Table 10 schematics	01/09

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