

Technical Document

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Features

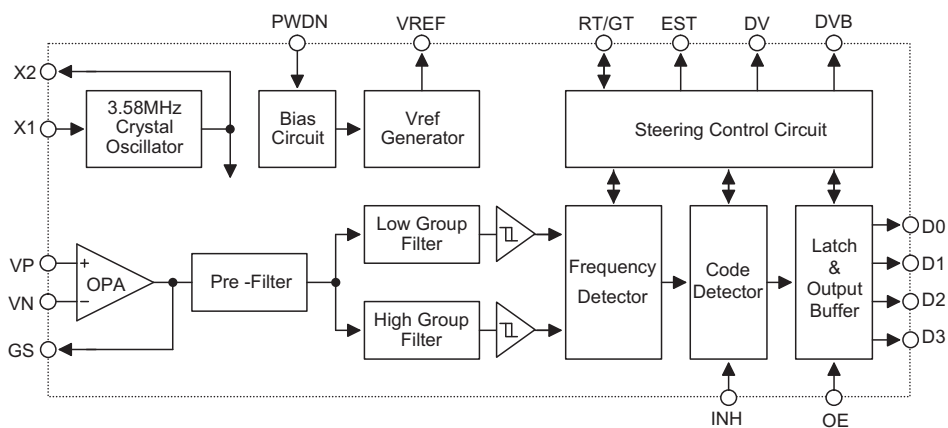
- Operating voltage: 2.5V~5.5V
- Minimal external component requirements
- No external filter required
- Low standby current in power down mode)
- Excellent performance
- Tristate data output for MCU interface
- 3.58MHz crystal or ceramic resonator oscillator
- 1633Hz can be inhibited by the INH pin
- 18-pin DIP/SOP packaging

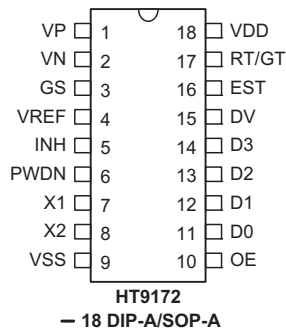
General Description

The HT9172 is a Dual Tone Multi Frequency (DTMF) receiver device which includes an integrated digital decoder and band split filter functions as well as power-down and inhibit mode operations. The device uses digital counting techniques to detect and decode the full range of 16 DTMF tone pairs into a 4-bit code

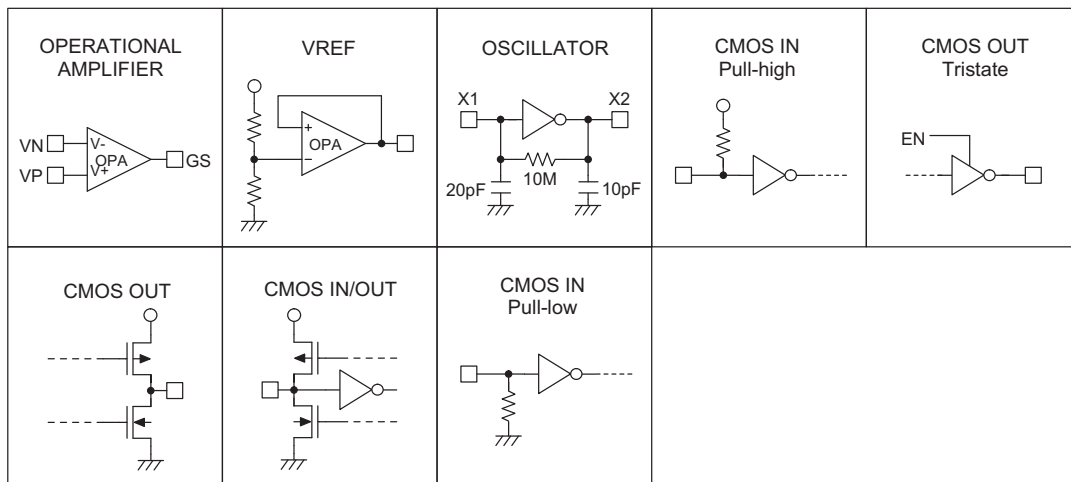
output. Highly accurate switched capacitor filters are utilised to divide the DTMF dual tone frequencies into low and high group signals. An integrated dial tone rejection circuit is provided to eliminate the need for pre-filtering.

Block Diagram



Pin Assignment

Pin Description

| Pin Name | I/O | Internal Connection | Description |
|----------|-----|-----------------------|---|
| VP | I | Operational Amplifier | Operational amplifier non-inverting input |
| VN | I | Operational Amplifier | Operational amplifier inverting input |
| GS | O | | Operational amplifier output terminal |
| VREF | O | VREF | Reference voltage output, normally $V_{DD}/2$ |
| X1 | I | oscillator | The system oscillator consists of an inverter, a bias resistor and the required on-chip load capacitor. A standard 3.579545MHz crystal connected to the X1 and X2 terminals implements the oscillator function. |
| X2 | O | | |
| PWDN | I | CMOS IN Pull-low | Active high. This enables the device to go into its power down mode and inhibits the oscillator. This pin input is pulled low internally. |
| INH | I | CMOS IN Pull-low | Active high. This inhibits the detection of tones representing characters A, B, C and D. This pin input is pulled low internally. |
| VSS | — | — | Negative power supply, ground |
| OE | I | CMOS IN Pull-high | D0~D3 output enable, active high |
| D0~D3 | O | CMOS OUT Tristate | Received data output terminals OE="H": Output enable OE="L": High impedance |
| DV | O | CMOS OUT | Data valid output. When the device has received a valid DTMF tone, this line will go high; otherwise it remains low. |
| EST | O | CMOS OUT | Early steering output - see Functional Description |
| RT/GT | I/O | CMOS IN/OUT | Tone acquisition time and release time can be set through connection with external resistor and capacitor. |
| VDD | — | — | Positive power supply, 2.5V~5.5V for normal operation |

Approximate Internal Connection Circuits

Absolute Maximum Ratings

| | | | |
|----------------------|--------------------------------|-----------------------------|----------------------------------|
| Supply Voltage | $V_{SS}-0.3V$ to $V_{SS}+6V$ | Storage Temperature | $-50^{\circ}C$ to $125^{\circ}C$ |
| Input Voltage | $V_{SS}-0.3V$ to $V_{DD}+0.3V$ | Operating Temperature | $-40^{\circ}C$ to $85^{\circ}C$ |

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|------------------|---------------------------------|-----------------|---|--------|--------|--------|------|
| | | V _{DD} | Conditions | | | | |
| V _{DD} | Operating Voltage | — | — | 2.5 | 5 | 5.5 | V |
| I _{DD} | Operating Current | 5V | — | — | 3 | 7 | mA |
| I _{STB} | Standby Current | 5V | V _{PWDN} =V _{DD} , (Not include PWDN pull-low current) | — | 1 | 5 | μA |
| V _{IL} | Input Low Voltage | 5V | — | — | — | 1.0 | V |
| V _{IH} | Input High Voltage | 5V | — | 4.0 | — | — | V |
| I _{IL} | Input Low Current | 5V | V _{VP} =V _{VN} =0V | — | — | 0.1 | μA |
| I _{IH} | Input High Current | 5V | V _{VP} =V _{VN} =5V | — | — | 0.1 | μA |
| R _{OE} | Pull-high Resistance (OE) | 5V | V _{OE} =0V | 70 | 110 | 160 | kΩ |
| R _{PL} | Pull-low Resistance (INH, PWDN) | 5V | V _{INH} =5.0V, V _{PWDN} =5.0V | 150 | 250 | 375 | kΩ |
| R _{IN} | Input Impedance (VN, VP) | 5V | — | — | 10 | — | MΩ |
| I _{OH} | Source Current (D0~D3, EST, DV) | 5V | V _{OUT} =4.5V | -0.4 | -0.8 | — | mA |
| I _{OL} | Sink Current (D0~D3, EST, DV) | 5V | V _{OUT} =0.5V | 1.0 | 2.5 | — | mA |
| f _{OSC} | System Frequency | 5V | Crystal=3.5795MHz | 3.5759 | 3.5795 | 3.5831 | MHz |

A.C. Characteristics
 $f_{osc}=3.5795\text{MHz}$, $T_a=25^\circ\text{C}$

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|-------------------------------|---------------------------------|-----------------|-----------------------------------|------|------|------|-----------------|
| | | V _{DD} | Conditions | | | | |
| DTMF Signal | | | | | | | |
| | Input Signal Level | 3V | | -36 | — | -6 | dBm |
| | | 5V | | -29 | — | 1 | |
| | Twist Accept Limit (Positive) | 5V | | — | 10 | — | dB |
| | Twist Accept Limit (Negative) | 5V | | — | 10 | — | dB |
| | Dial Tone Tolerance | 5V | | — | 18 | — | dB |
| | Noise Tolerance | 5V | | — | -12 | — | dB |
| | Third Tone Tolerance | 5V | | — | -16 | — | dB |
| | Frequency Deviation Acceptance | 5V | | — | — | ±1.5 | % |
| | Frequency Deviation Rejection | 5V | | ±3.5 | — | — | % |
| t _{PU} | Power Up Time (See Figure 4.) | 5V | | — | 30 | — | ms |
| Gain Setting Amplifier | | | | | | | |
| R _{IN} | Input Resistance | 5V | — | — | 10 | — | MΩ |
| I _{IN} | Input Leakage Current | 5V | $V_{SS}<(V_{VP},V_{VN})<V_{DD}$ | — | 0.1 | — | μA |
| V _{OS} | Offset Voltage | 5V | — | — | ±25 | — | mV |
| P _{SRR} | Power Supply Rejection | 5V | 100 Hz -3V<V _{IN} <3V | — | 60 | — | dB |
| C _{MRR} | Common Mode Rejection | 5V | | — | 60 | — | dB |
| A _{VO} | Open Loop Gain | 5V | | — | 65 | — | dB |
| f _T | Gain Band Width | 5V | — | — | 1.5 | — | MHz |
| V _{OUT} | Output Voltage Swing | 5V | R _L >100kΩ | — | 4.5 | — | V _{PP} |
| R _L | Load Resistance (GS) | 5V | — | — | 50 | — | kΩ |
| C _L | Load Capacitance (GS) | 5V | — | — | 100 | — | pF |
| V _{CM} | Common Mode Range | 5V | No load | — | 3.0 | — | V _{PP} |
| Steering Control | | | | | | | |
| t _{DP} | Tone Present Detection Time | 5V | | 5 | 11 | 14 | ms |
| t _{DA} | Tone Absent Detection Time | 5V | | — | 4 | 8.5 | ms |
| t _{ACC} | Acceptable Tone Duration | 5V | | — | — | 42 | ms |
| t _{REJ} | Rejected Tone Duration | 5V | | 20 | — | — | ms |
| t _{IA} | Acceptable Inter-digit Pause | 5V | | — | — | 42 | ms |
| t _{IR} | Rejected Inter-digit Pause | 5V | | 20 | — | — | ms |
| t _{PDO} | Propagation Delay (RT/GT to DO) | 5V | | — | 8 | 11 | μs |
| t _{PDV} | Propagation Delay (RT/GT to DV) | 5V | | — | 12 | — | μs |
| t _{DOV} | Output Data Set Up (DO to DV) | 5V | | — | 4.5 | — | μs |
| t _{DDO} | Disable Delay (OE to DO) | 5V | | — | 300 | — | ns |
| t _{EDO} | Enable Delay (OE to DO) | 5V | | — | 50 | 60 | ns |

Note: DO=D0-D3

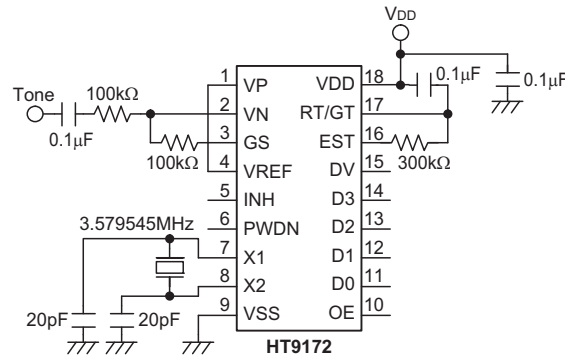


Figure 1. Test Circuit

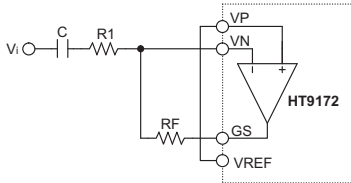
Functional Description

Overview

The HT9172 tone decoder consists of three band pass filters and two digital decode circuits to convert a DTMF tone into a digital code output.

The device contains an operational amplifier to adjust the input signal level as shown in Figure 2.

(a) Standard Input Circuit



(b) Differential Input Circuit

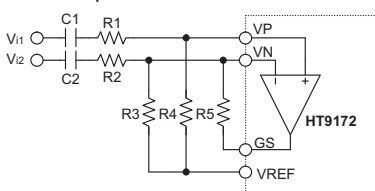


Figure 2. Amplifier Input Application Circuits

The pre-filter is a band rejection filter which will reject frequencies between 350Hz to 400Hz.

The low group filter, filters the low group frequency signal output whereas the high group filter, filters the high group frequency signal output.

Each filter output is followed by a zero-crossing detector with incorporates hysteresis. When the signal amplitude at the output exceeds a specified level, it is transferred to a full swing logic signal.

When the input signal is recognized as an effective DTMF tone, the DV line will go high, and the corresponding DTMF tone code will be generated.

Steering Control Circuit

The steering control circuit is used to measure the effective signal duration and for protecting against valid signal drop out. This is achieved using an analog delay which is implemented using an external RC time-constant, controlled by the output line EST.

The timing diagram is shown in Figure 3. The EST pin is normally low and will pull the RT/GT pin low via the external RC network. When a valid tone input is detected, the EST pin will go high, which will in turn pull the RT/GT pin high through the RC network.

When the voltage on RT/GT rises from 0 to V_{TRT} , which is 2.35V for a 5V power supply, the input signal is effective, and the corresponding code will be generated by the code detector. After D0~D3 have been latched, DV will go high. When the voltage on RT/GT falls from VDD to V_{TRT} , i.e. when there is no input tone, the DV output will go low, and D0~D3 will maintain their present data until a next valid tone input is produced.

By selecting suitable external RC values, the minimum acceptable input tone duration, t_{ACC} , and the minimum acceptable inter-tone rejection, t_{IR} , can be set. The values of the external RC components, can be chosen using the following formula. Also refer to Figure 5 for details.

$$t_{ACC} = t_{DP} + t_{GTP};$$

$$t_{IR} = t_{DA} + t_{GTA};$$

where t_{ACC} : Tone duration acceptable time
 t_{DP} : EST output delay time ("L" → "H")
 t_{GTP} : Tone present time
 t_{IR} : Inter-digit pause rejection time

Timing Diagrams

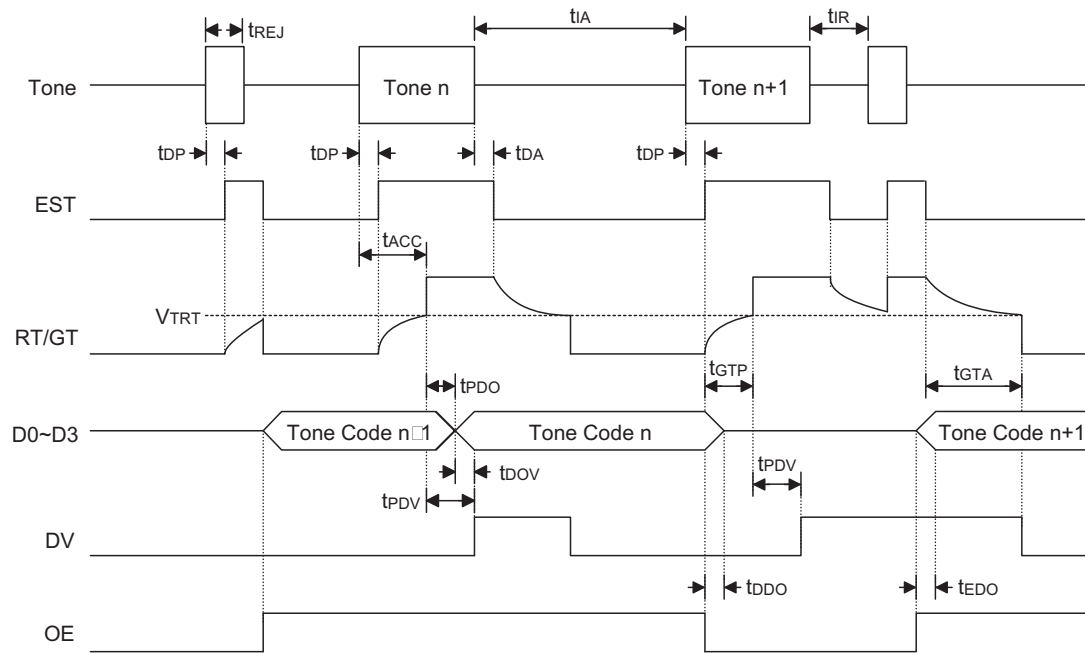


Figure 3. Steering Timing

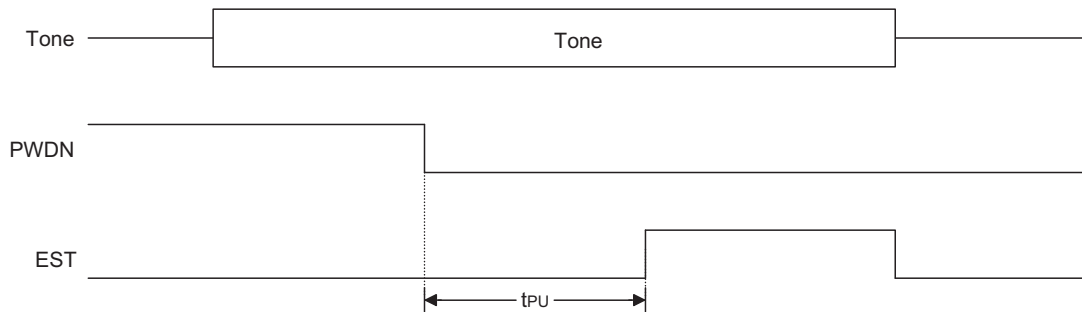
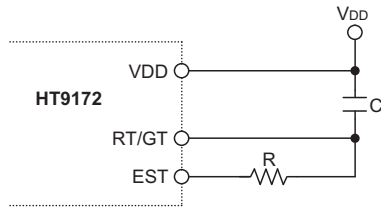


Figure 4. Power-up Timing

(a) Fundamental circuit:

$$t_{GTP} = R \times C \times \ln(V_{DD} / (V_{DD} - V_{TRT}))$$

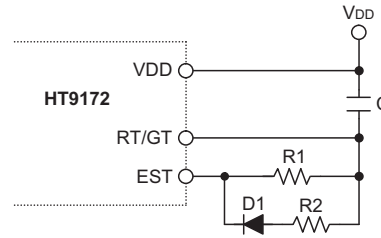
$$t_{GTA} = R \times C \times \ln(V_{DD} / V_{TRT})$$



(c) $t_{GTP} > t_{GTA}$:

$$t_{GTP} = R1 \times C \times \ln(V_{DD} / (V_{DD} - V_{TRT}))$$

$$t_{GTA} = (R1 // R2) \times C \times \ln(V_{DD} / V_{TRT})$$



(b) $t_{GTP} < t_{GTA}$:

$$t_{GTP} = (R1 // R2) \times C \times \ln(V_{DD} - V_{TRT})$$

$$t_{GTA} = R1 \times C \times \ln(V_{DD} / V_{TRT})$$

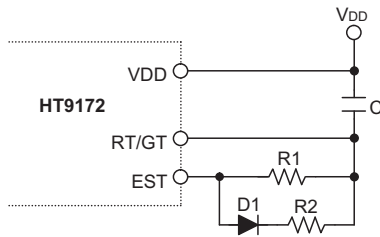


Figure 5. Steering Time Adjustment Circuits

DTMF Dialing Matrix

| | COL1 | COL2 | COL3 | COL4 |
|------|------|------|------|------|
| ROW1 | 1 | 2 | 3 | A |
| ROW2 | 4 | 5 | 6 | B |
| ROW3 | 7 | 8 | 9 | C |
| ROW4 | * | 0 | # | D |

DTMF Data Output Table

| Low Group (Hz) | High Group (Hz) | Digit | OE | D3 | D2 | D1 | D0 |
|----------------|-----------------|-------|----|----|----|----|----|
| 697 | 1209 | 1 | H | L | L | L | H |
| 697 | 1336 | 2 | H | L | L | H | L |
| 697 | 1477 | 3 | H | L | L | H | H |
| 770 | 1209 | 4 | H | L | H | L | L |
| 770 | 1336 | 5 | H | L | H | L | H |
| 770 | 1477 | 6 | H | L | H | H | L |
| 852 | 1209 | 7 | H | L | H | H | H |
| 852 | 1336 | 8 | H | H | L | L | L |
| 852 | 1477 | 9 | H | H | L | L | H |
| 941 | 1336 | 0 | H | H | L | H | L |
| 941 | 1209 | * | H | H | L | H | H |
| 941 | 1477 | # | H | H | H | L | L |
| 697 | 1633 | A | H | H | H | L | H |
| 770 | 1633 | B | H | H | H | H | L |
| 852 | 1633 | C | H | H | H | H | H |
| 941 | 1633 | D | H | L | L | L | L |
| — | — | ANY | L | Z | Z | Z | Z |

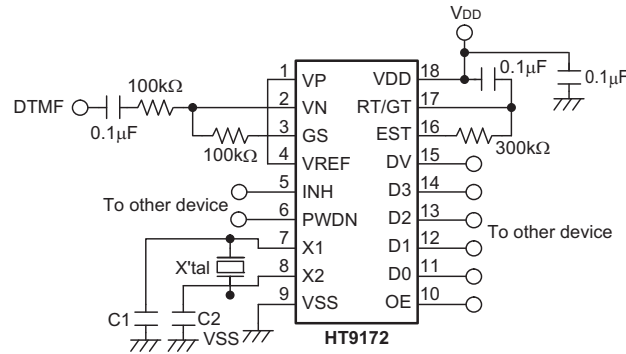
Note: "Z" High impedance; "ANY" Any digit

Data Output

The data outputs, D0~D3, are tristate outputs. When the OE input is low, the D0~D3 data outputs, will be in a high impedance condition.

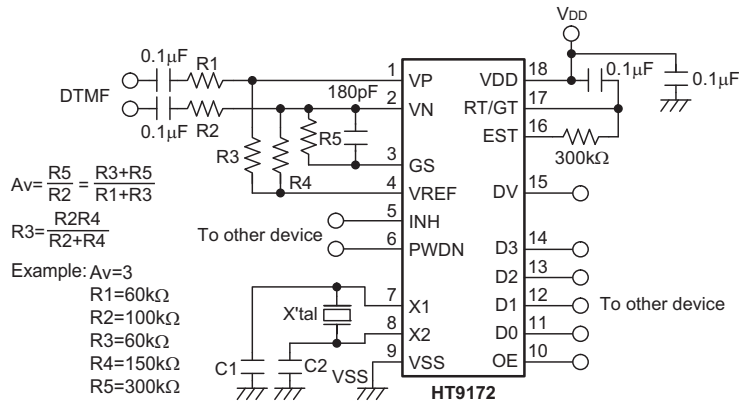
Application Circuits

Application Circuit 1



Note: X'tal = 3.579545MHz crystal
 C1 = C2 ≅ 20pF
 X'tal = 3.58MHz ceramic resonator
 C1 = C2 ≅ 39pF

Application Circuit 2



Note: X'tal = 3.579545MHz crystal
 C1 = C2 ≅ 20pF
 X'tal = 3.58MHz ceramic resonator
 C1 = C2 ≅ 39pF

Package Information

18-pin DIP (300mil) Outline Dimensions

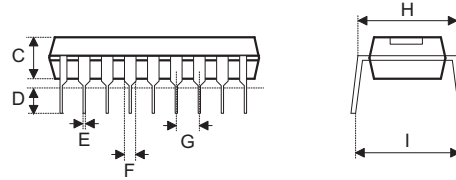
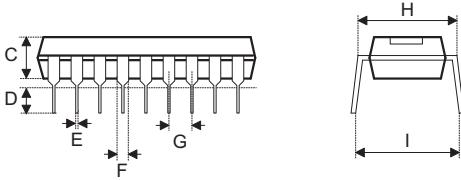
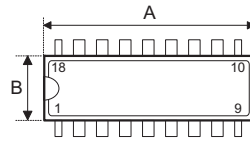
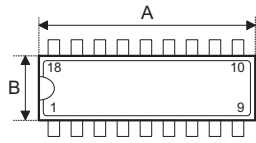


Fig1. Full Lead Packages

Fig2. 1/2 Lead Packages

- MS-001d (see fig1)

| Symbol | Dimensions in mil | | |
|--------|-------------------|------|------|
| | Min. | Nom. | Max. |
| A | 880 | — | 920 |
| B | 240 | — | 280 |
| C | 115 | — | 195 |
| D | 115 | — | 150 |
| E | 14 | — | 22 |
| F | 45 | — | 70 |
| G | — | 100 | — |
| H | 300 | — | 325 |
| I | — | — | 430 |

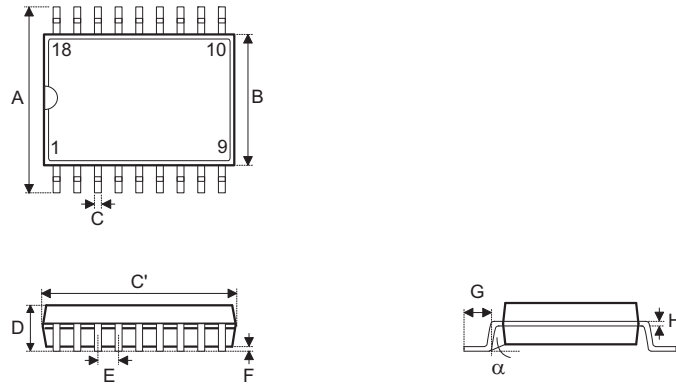
- MS-001d (see fig2)

| Symbol | Dimensions in mil | | |
|--------|-------------------|------|------|
| | Min. | Nom. | Max. |
| A | 845 | — | 880 |
| B | 240 | — | 280 |
| C | 115 | — | 195 |
| D | 115 | — | 150 |
| E | 14 | — | 22 |
| F | 45 | — | 70 |
| G | — | 100 | — |
| H | 300 | — | 325 |
| I | — | — | 430 |

- MO-095a (see fig2)

| Symbol | Dimensions in mil | | |
|--------|-------------------|------|------|
| | Min. | Nom. | Max. |
| A | 845 | — | 885 |
| B | 275 | — | 295 |
| C | 120 | — | 150 |
| D | 110 | — | 150 |
| E | 14 | — | 22 |
| F | 45 | — | 60 |
| G | — | 100 | — |
| H | 300 | — | 325 |
| I | — | — | 430 |

18-pin SOP (300mil) Outline Dimensions

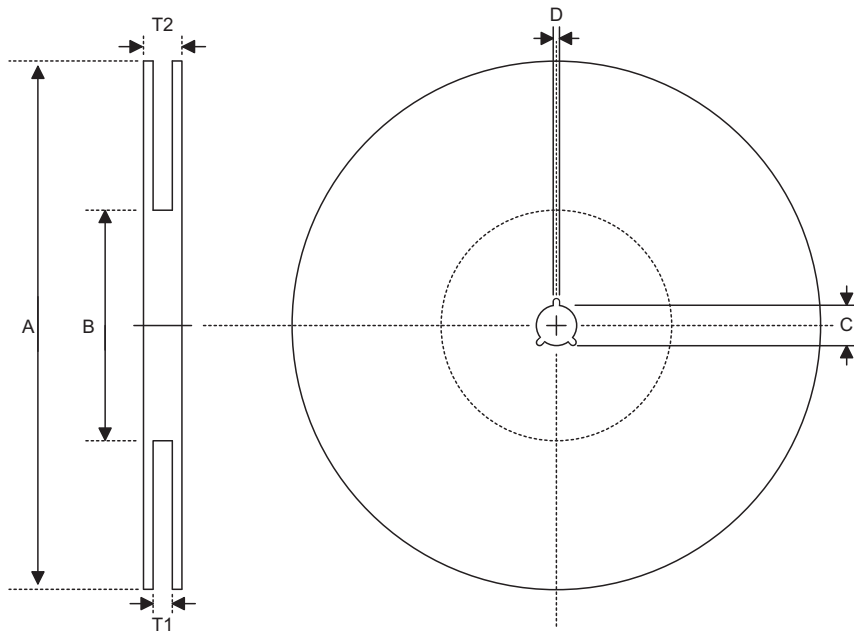


• MS-013

| Symbol | Dimensions in mil | | |
|----------|-------------------|------|------|
| | Min. | Nom. | Max. |
| A | 393 | — | 419 |
| B | 256 | — | 300 |
| C | 12 | — | 20 |
| C' | 447 | — | 463 |
| D | — | — | 104 |
| E | — | 50 | — |
| F | 4 | — | 12 |
| G | 16 | — | 50 |
| H | 8 | — | 13 |
| α | 0° | — | 8° |

Product Tape and Reel Specifications

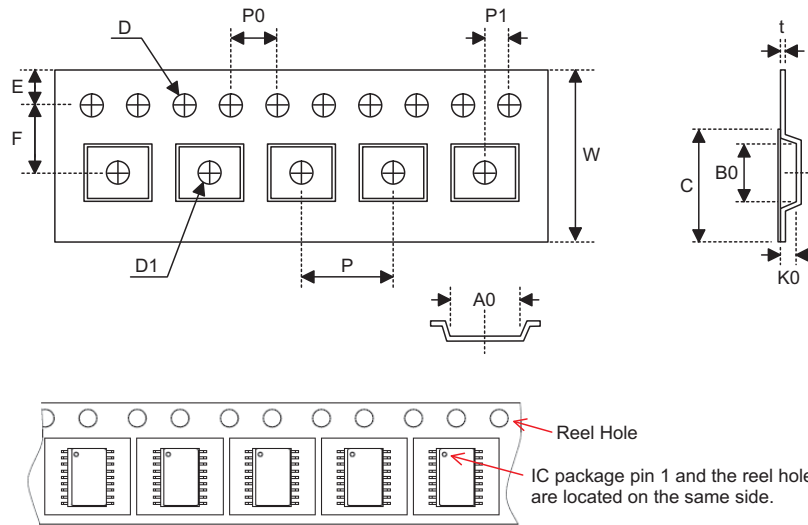
Reel Dimensions



SOP 18W

| Symbol | Description | Dimensions in mm |
|--------|-----------------------|---------------------------|
| A | Reel Outer Diameter | 330.0±1.0 |
| B | Reel Inner Diameter | 100.0±1.5 |
| C | Spindle Hole Diameter | 13.0 ^{+0.5/-0.2} |
| D | Key Slit Width | 2.0±0.5 |
| T1 | Space Between Flange | 24.8 ^{+0.3/-0.2} |
| T2 | Reel Thickness | 30.2±0.2 |

Carrier Tape Dimensions



SOP 18W

| Symbol | Description | Dimensions in mm |
|--------|--|-----------------------------|
| W | Carrier Tape Width | 24.0 ^{+0.3/-0.1} |
| P | Cavity Pitch | 16.0±0.1 |
| E | Perforation Position | 1.75±0.1 |
| F | Cavity to Perforation (Width Direction) | 11.5±0.1 |
| D | Perforation Diameter | 1.5±0.1 |
| D1 | Cavity Hole Diameter | 1.50 ^{+0.25/-0.00} |
| P0 | Perforation Pitch | 4.0±0.1 |
| P1 | Cavity to Perforation (Length Direction) | 2.0±0.1 |
| A0 | Cavity Length | 10.9±0.1 |
| B0 | Cavity Width | 12.0±0.1 |
| K0 | Cavity Depth | 2.8±0.1 |
| t | Carrier Tape Thickness | 0.30±0.05 |
| C | Cover Tape Width | 21.3±0.1 |

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