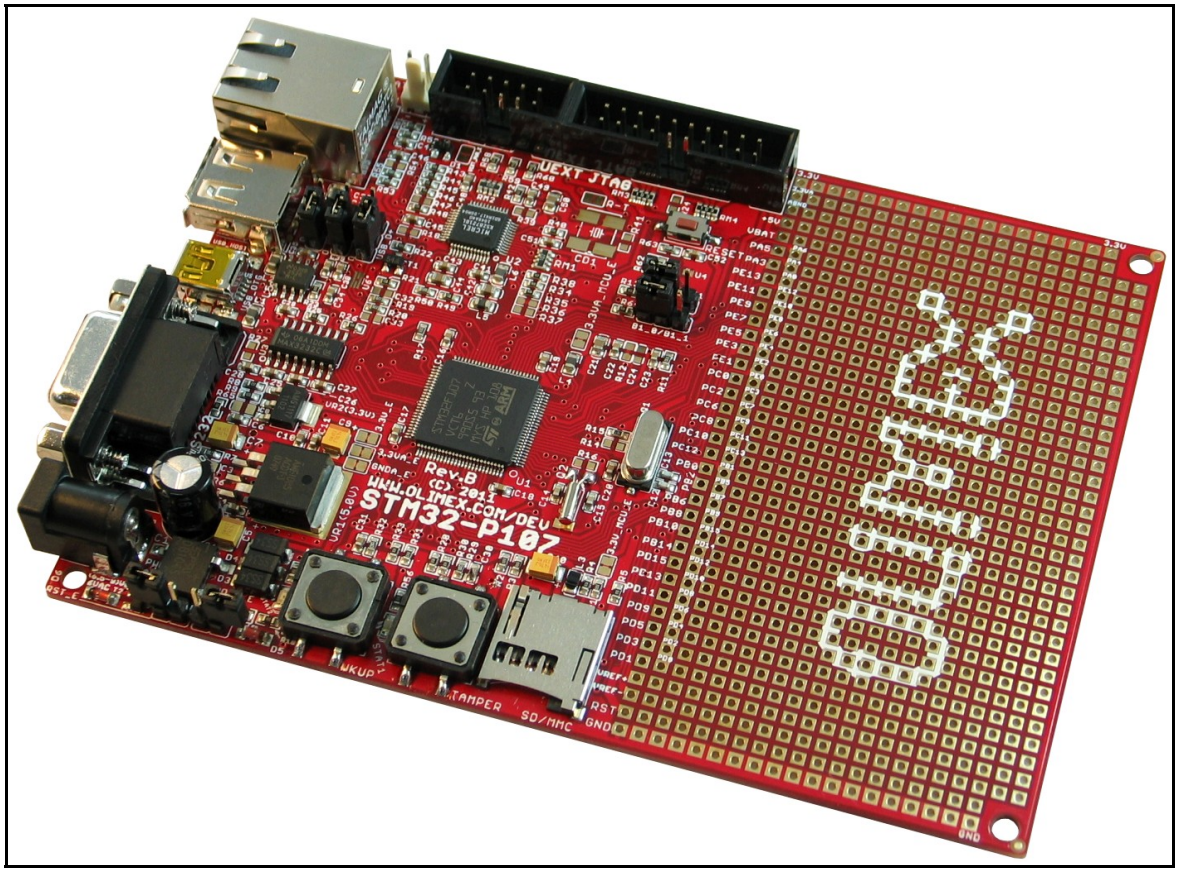


STM32-P107 development board

User's Manual

Pb-free, Green

All boards produced by Olimex are ROHS compliant

Rev. F, August 2012

INTRODUCTION

STM32-P107 prototype board provides easy way for developing and prototyping with the new STM32F107VCT6 connectivity line microcontroller, produced by STMicroelectronics. STM32-P107 has JTAG port for programming and debugging, USB_OTG, user button, two status leds, and most of the GPIOs are on extension headers where you can connect your additional circuits.

BOARD FEATURES

- CPU: STM32F107VCT6 32 bit ARM-based microcontroller with 256 KB Flash, 64 KB RAM, USB OTG, Ethernet, 10 timers, 2 CANs, 2 ADCs, 14 communication interfaces
- JTAG connector with ARM 2x10 pin layout for programming/debugging
- USB_OTG
- USB_HOST
- 100Mbit Ethernet
- RS232
- Mini SD/MMC card connector
- UEXT connector
- Power Jack
- Two user buttons
- RESET button and circuit
- Two status leds
- Power-on led
- 3V battery connector
- Extension port connectors for many of microcontrollers pins
- PCB: FR-4, 1.5 mm (0,062"), soldermask, silkscreen component print
- Dimensions: 132.08x96.52mm (5.2x3.8")

ELECTROSTATIC WARNING

The STM32-P107 board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

BOARD USE REQUIREMENTS

Cables: The cable you will need depends on the programmer/debugger you use. If you use ARM-JTAG, you will need LPT cable, if you use ARM-JTAG-EW, ARM-USB-OCD, ARM-USB-OCD-H, ARM-USB-TINY, or ARM-USB-TINY-H you will need 1.8 meter USB A-B cable, for ARM-USB-OCD and ARM-USB-OCD-H you will need RS232 cable, too.

Hardware: Programmer/Debugger – one of the Olimex ARM Programmers: ARM-JTAG, ARM-JTAG-EW, ARM-USB-OCD, ARM-USB-OCD-H, ARM-USB-OCD-TINY, ARM-USB-OCD-H.

Software: ARM C compiler

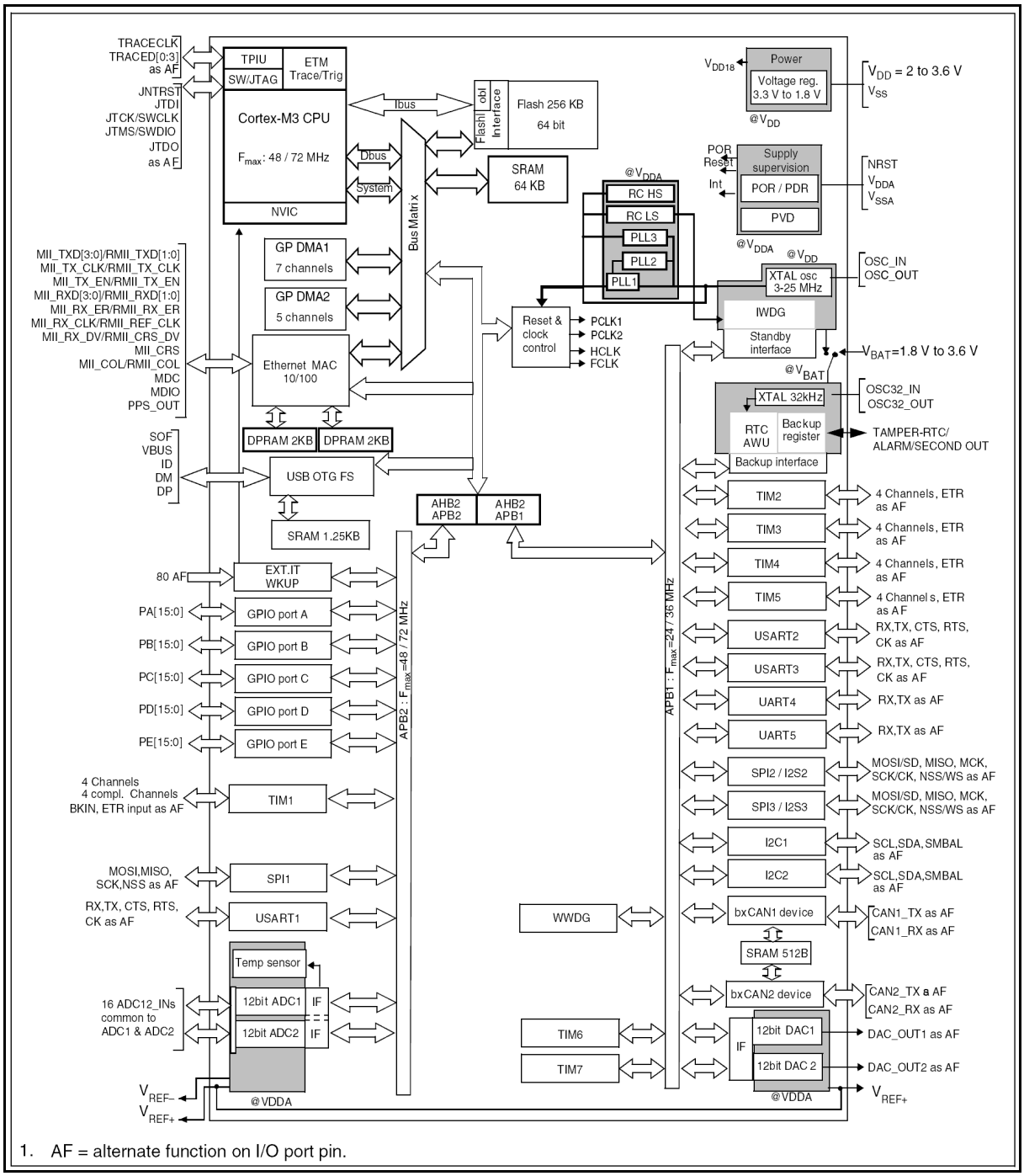
PROCESSOR FEATURES

STM32-P107 board use ARM-based 32-bit microcontroller **STM32F107VCT6** with these features:

- Core: ARM 32-bit Cortex™-M3 CPU
  - 72 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 256 Kbytes of Flash memory
  - 64 Kbytes of SRAM
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 25 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC with calibration
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - VBAT supply for RTC and backup registers
- 2 × 12-bit, 1 µs A/D converters (16 channels)
  - Conversion range: 0 to 3.6 V
  - Sample and hold capability
  - Temperature sensor
  - up to 2 MSps in interleaved mode
- 2 × 12-bit D/A converters
- DMA: 12-channel DMA controller

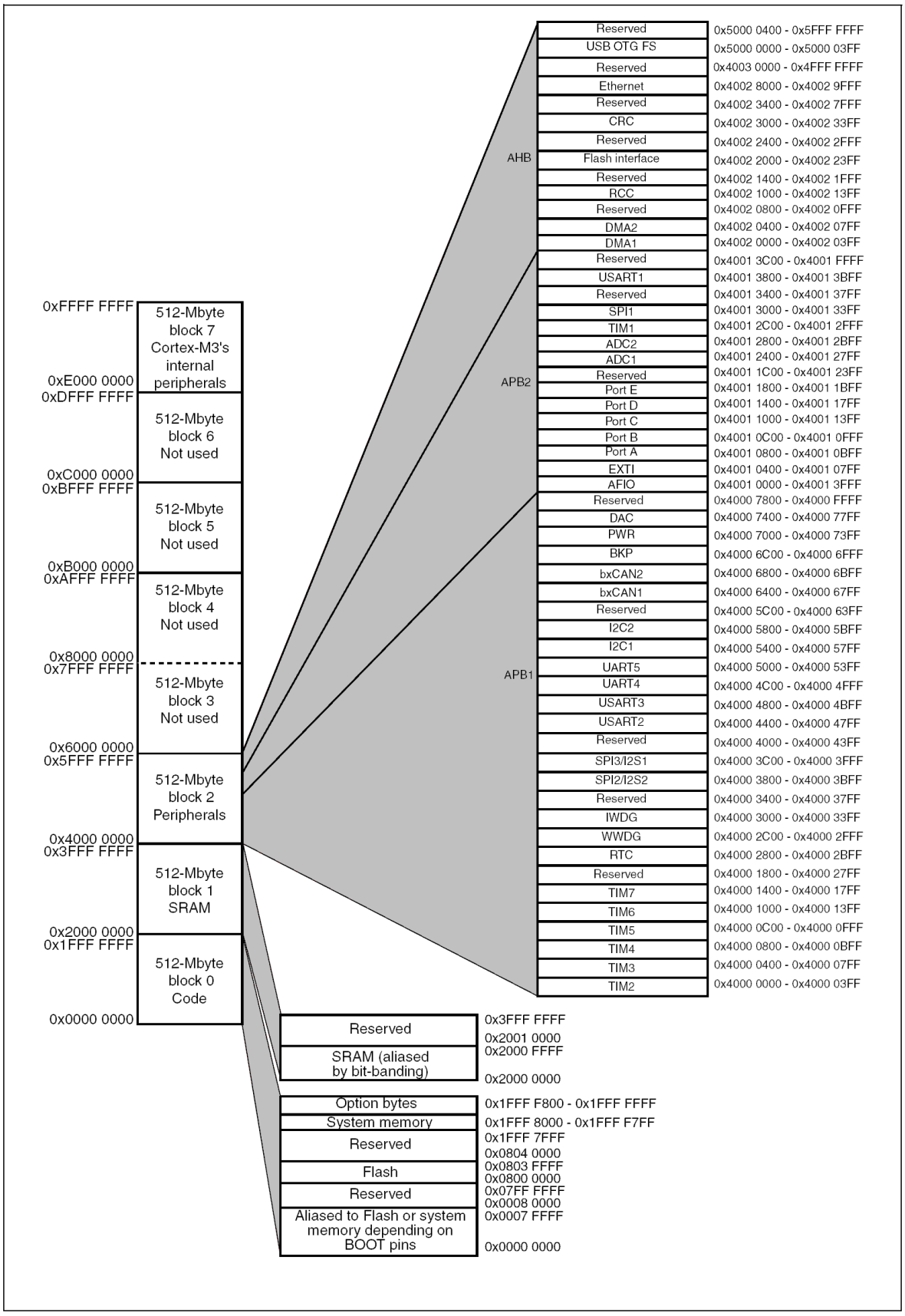
    - Supported peripherals: timers, ADCs, DAC, I^2Ss, SPIs, I^2Cs and USARTs
- Debug mode
    - Serial wire debug (SWD) & JTAG interfaces
    - Cortex-M3 Embedded Trace Macrocell™
- 80 fast I/O ports
    - 80 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant
- 10 timers
    - four 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
    - 1 × 16-bit motor control PWM timer with dead-time generation and emergency stop
    - 2 × watchdog timers (Independent and Window)
    - SysTick timer: a 24-bit downcounter
    - 2 × 16-bit basic timers to drive the DAC
- 14 communication interfaces
    - 2 × I^2C interfaces (SMBus/PMBus)
    - 5 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
    - 3 SPIs (18 Mbit/s), 2 with a multiplexed I^2S interface that offers audio class accuracy via advanced PLL schemes
    - 2 × CAN interfaces (2.0B Active) with 512 bytes of dedicated SRAM
    - USB 2.0 full-speed device/host/OTG controller with on-chip PHY that supports HNP/SRP/ID with 1.25 Kbytes of dedicated SRAM
    - 10/100 Ethernet MAC with dedicated DMA and SRAM (4 Kbytes): IEEE1588 hardware support, MII/RMII available on all packages
- CRC calculation unit, 96-bit unique ID

BLOCK DIAGRAM

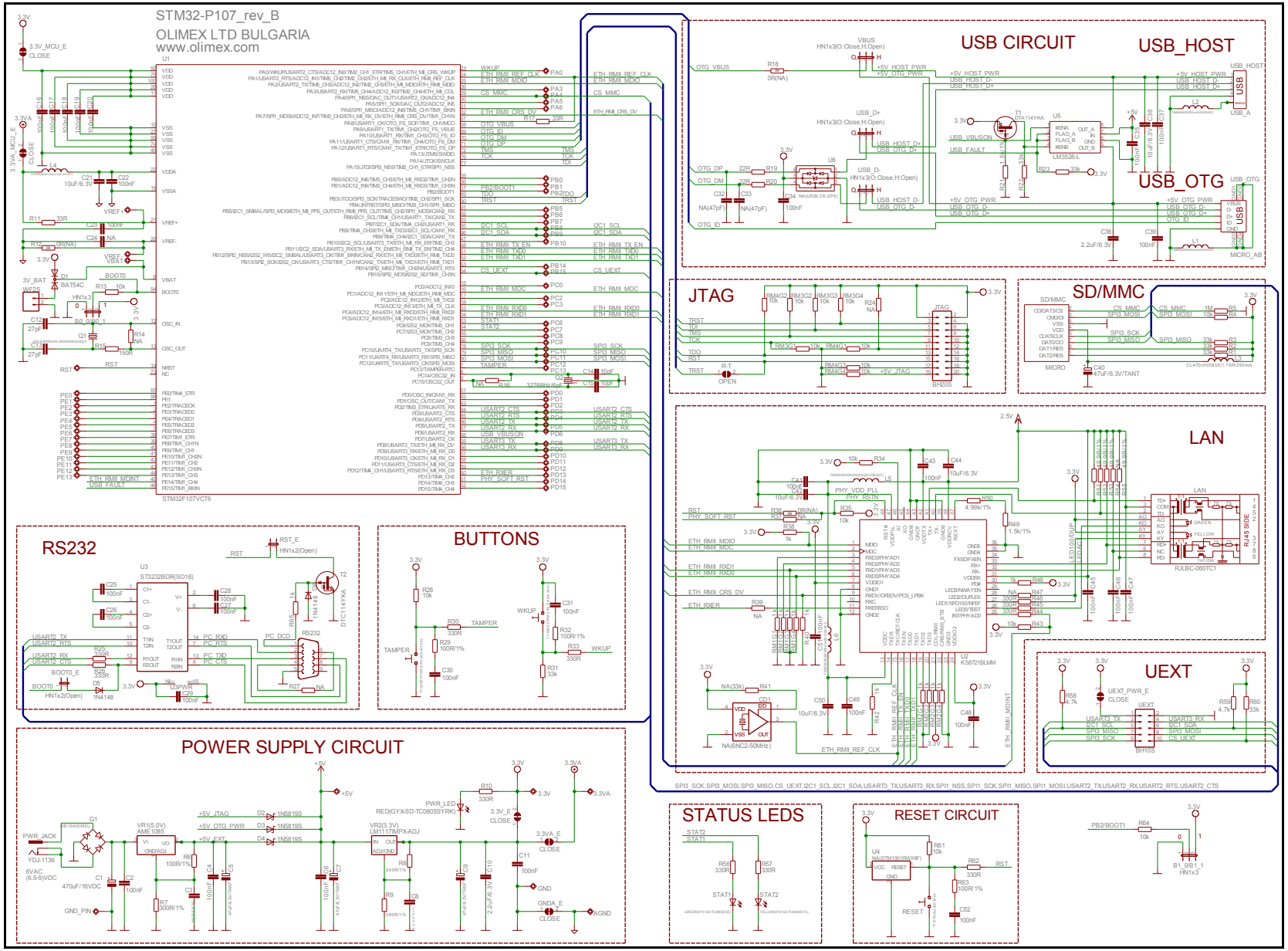


1. AF = alternate function on I/O port pin.

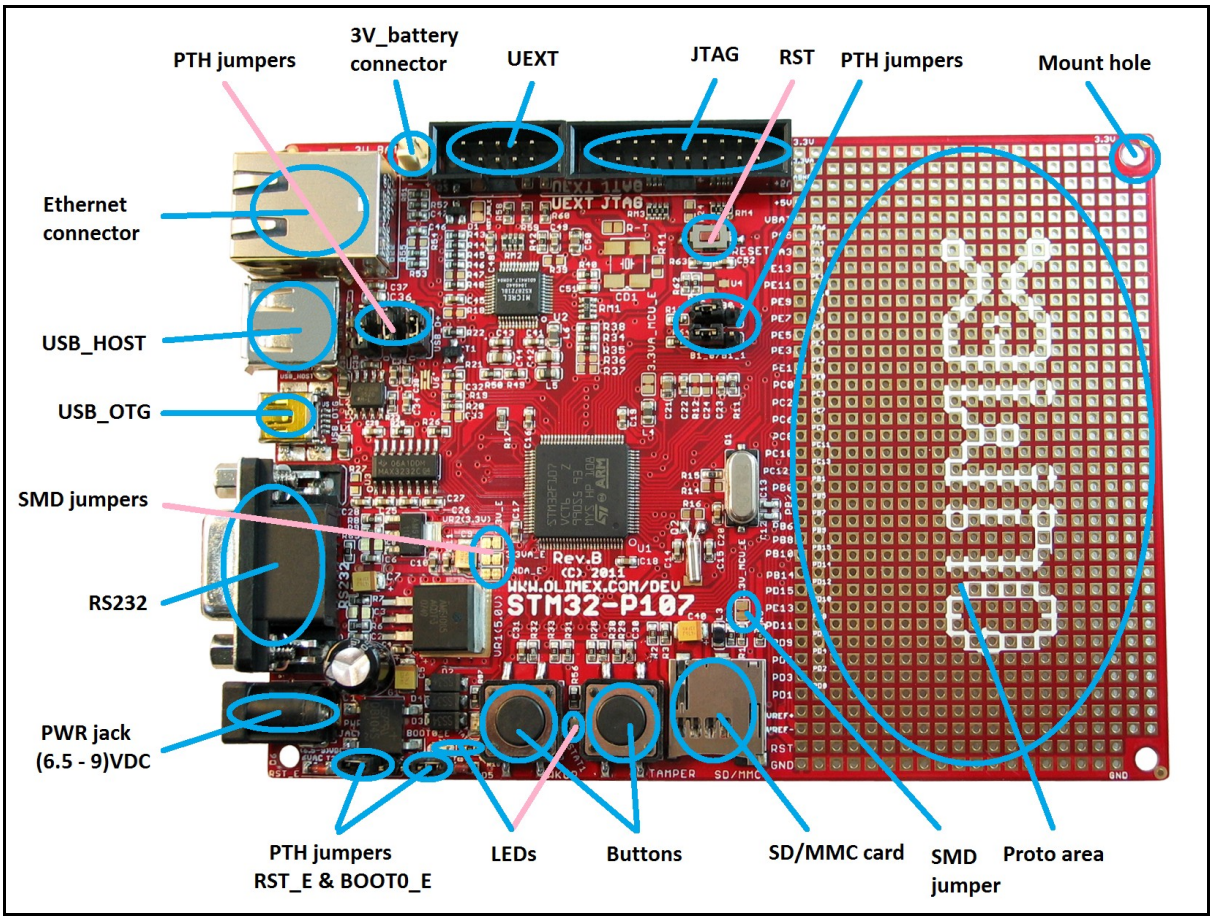
MEMORY MAP


0xFFFF FFFF
512-Mbyte block 7 Cortex-M3's internal peripherals
0xE000 0000
0xDFFF FFFF
512-Mbyte block 6 Not used
0xC000 0000
0xBFFF FFFF
512-Mbyte block 5 Not used
0xB000 0000
0xAFFF FFFF
512-Mbyte block 4 Not used
0x8000 0000
0x7FFF FFFF
512-Mbyte block 3 Not used
0x6000 0000
0x5FFF FFFF
512-Mbyte block 2 Peripherals
0x4000 0000
0x3FFF FFFF
512-Mbyte block 1 SRAM
0x2000 0000
0x1FFF FFFF
512-Mbyte block 0 Code
0x0000 0000
AHB
APB2
APB1
Reserved 0x5000 0400 - 0x5FFF FFFF
USB OTG FS 0x5000 0000 - 0x5000 03FF
Reserved 0x4003 0000 - 0x4FFF FFFF
Ethernet 0x4002 8000 - 0x4002 9FFF
Reserved 0x4002 3400 - 0x4002 7FFF
CRC 0x4002 3000 - 0x4002 33FF
Reserved 0x4002 2400 - 0x4002 2FFF
Flash interface 0x4002 2000 - 0x4002 23FF
Reserved 0x4002 1400 - 0x4002 1FFF
RCC 0x4002 1000 - 0x4002 13FF
Reserved 0x4002 0800 - 0x4002 0FFF
DMA2 0x4002 0400 - 0x4002 07FF
DMA1 0x4002 0000 - 0x4002 03FF
Reserved 0x4001 3C00 - 0x4001 FFFF
USART1 0x4001 3800 - 0x4001 3BFF
Reserved 0x4001 3400 - 0x4001 37FF
SPI1 0x4001 3000 - 0x4001 33FF
TIM1 0x4001 2C00 - 0x4001 2FFF
ADC2 0x4001 2800 - 0x4001 2BFF
ADC1 0x4001 2400 - 0x4001 27FF
Reserved 0x4001 1C00 - 0x4001 23FF
Port E 0x4001 1800 - 0x4001 1BFF
Port D 0x4001 1400 - 0x4001 17FF
Port C 0x4001 1000 - 0x4001 13FF
Port B 0x4001 0C00 - 0x4001 0FFF
Port A 0x4001 0800 - 0x4001 0BFF
EXTI 0x4001 0400 - 0x4001 07FF
AFIO 0x4001 0000 - 0x4001 3FFF
Reserved 0x4000 7800 - 0x4000 FFFF
DAC 0x4000 7400 - 0x4000 77FF
PWR 0x4000 7000 - 0x4000 73FF
BKP 0x4000 6C00 - 0x4000 6FFF
bxCAN2 0x4000 6800 - 0x4000 6BFF
bxCAN1 0x4000 6400 - 0x4000 67FF
Reserved 0x4000 5C00 - 0x4000 63FF
I2C2 0x4000 5800 - 0x4000 5BFF
I2C1 0x4000 5400 - 0x4000 57FF
UART5 0x4000 5000 - 0x4000 53FF
UART4 0x4000 4C00 - 0x4000 4FFF
USART3 0x4000 4800 - 0x4000 4BFF
USART2 0x4000 4400 - 0x4000 47FF
Reserved 0x4000 4000 - 0x4000 43FF
SPI3/I2S1 0x4000 3C00 - 0x4000 3FFF
SPI2/I2S2 0x4000 3800 - 0x4000 3BFF
Reserved 0x4000 3400 - 0x4000 37FF
IWDG 0x4000 3000 - 0x4000 33FF
WWDG 0x4000 2C00 - 0x4000 2FFF
RTC 0x4000 2800 - 0x4000 2BFF
Reserved 0x4000 1800 - 0x4000 27FF
TIM7 0x4000 1400 - 0x4000 17FF
TIM6 0x4000 1000 - 0x4000 13FF
TIM5 0x4000 0C00 - 0x4000 0FFF
TIM4 0x4000 0800 - 0x4000 0BFF
TIM3 0x4000 0400 - 0x4000 07FF
TIM2 0x4000 0000 - 0x4000 03FF
Reserved
0x3FFF FFFF
0x2001 0000
SRAM (aliased by bit-banding)
0x2000 FFFF
0x2000 0000
Option bytes 0x1FFF F800 - 0x1FFF FFFF
System memory 0x1FFF 8000 - 0x1FFF F7FF
Reserved
0x1FFF 7FFF
0x0804 0000
Flash
0x0803 FFFF
0x0800 0000
Reserved
0x07FF FFFF
0x0008 0000
Aliased to Flash or system memory depending on BOOT pins
0x0007 FFFF
0x0000 0000

SCHEMATIC


STM32-P107_rev_B
OLIMEX LTD BULGARIA
www.olimex.com
USB CIRCUIT
USB_HOST
USB_OTG
JTAG
SD/MMC
LAN
RS232
BUTTONS
UEXT
POWER SUPPLY CIRCUIT
STATUS LEDS
RESET CIRCUIT

BOARD LAYOUT



POWER SUPPLY CIRCUIT

STM32-P107 can take power from three sources:

- PWR connector where (6.5-9)V DC or 6V AC is applied by external power source.
- +5V_ OTG-PWR from USB OTG
- +5V_JTAG from JTAG

The programmed board power consumption is about 70 mA.

RESET CIRCUIT

STM32-P107 reset circuit includes JTAG connector pin 15, U2 (STE101P) pin 28 (RESET), R73(10k), R74(330Ohm), R75(100Ohm/1%), C55(100nF), STM32F107 pin 14 (NRST) and RESET button.

CLOCK CIRCUIT

Quartz crystal 25 MHz is connected to **STM32F107** pin 12 (OSC_IN) and pin 13 (OSC_OUT).

Quartz crystal 32.768kHz is connected to **STM32F107** pin 8 (PC14/OSC32_IN) and pin 9 (PC15/OSC32_OUT).

JUMPER DESCRIPTION

PWR_SEL

When position 1-2 is shorted – the board is power supplied from JTAG.

When position 3-4 is shorted – the board is power supplied from USB_OTG.

When position 5-6 is shorted – the board is power supplied from External power source.

Default state is – position 5-6 – shorted.

B0_0/B0_1

When this jumper is in position B0_1 – BOOT0 is connected to 3.3V, and when the jumper is in position B0_0 – BOOT0 is connected to GND.

Default state is B0_0.

B1_0/B1_1

When this jumper is in position B1_1 – BOOT1 is connected to 3.3V, and when the jumper is in position B1_0 – BOOT1 is connected to GND.

Default state is B1_0.

VBUS

When is in position "H" - connects +5V_HOST_PWR to OTG_VBUS.

When is in position "O" - connects +5V_OTG_PWR to OTG_VBUS.

Default state is "O".

USB_D+

When is in position "H" - connects USB_HOST_D+ to OTG_DP.

When is in position "O" - connects USB_OTG_D+ to OTG_DP.

Default state is "O".

USB_D-

When is in position "H" - connects USD_HOST_D- to OTG_DM.

When is in position "O" - connects USB_OTG_D- to OTG_DM.

Default state is "O".

PWDW_D

When is closed – disables Ethernet transceiver (STE101P) Power Down Mode. STE101P is active.
Default state is closed.

3.3V_MCU_E

Enable microcontroller 3.3V power supply

Default state is closed.

3.3V_E

Enable regulator VR2 (3.3V) - LM1117

Default state is closed.

3.3VA_E

Enables board 3.3V analog power supply.

Default state is closed.

3.3VA_MCU_E

Enables microcontroller 3.3V analog power supply.

Default state is closed.

GNDA_E

Enables board analog GND.

Default state is closed.

R-T

Connects RST to TRST

Default state is open.

RST_E, BOOT_E jumpers

Note that it is recommended to move those jumpers together – either both should be open or both should be closed.

When both are closed RS232 boot is enabled.

Default states are RST_E – open; BOOT_E – open.

INPUT/OUTPUT

Status LED1 (green) with name **STAT1** connected to STM32F107 pin 63 (PC6/I2S2_MCK/TIM3_CH1).

Status LED2 (yellow) with name **STAT2** connected to STM32F107 pin 64 (PC7/I2S3_MCK/TIM3_CH2).

Power-on LED (red) with name **PWR** – this led shows that +3.3V is applied to the board.

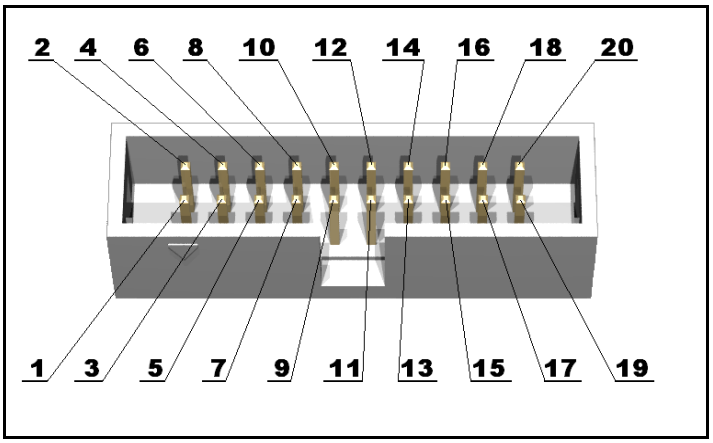
User button with name **WKUP** connected to STM32F107 pin 23 (PA0/WKUP).

User button with name **TAMPER** connected to STM32F107 pin 7 (PC13/TAMPER-RTC).

Reset button with name **RESET** connected to STM32F107 pin 14 (NRST).

CONNECTOR DESCRIPTIONS

JTAG

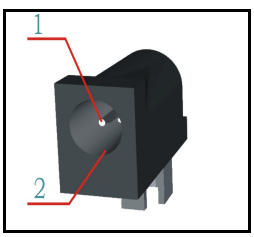


The JTAG connector allows the software debugger to talk via a JTAG (Joint Test Action Group) port directly to the core. Instructions may be inserted and executed by the core thus allowing STM32F107 memory to be programmed with code and executed step by step by the host software.
For more details refer to IEEE Standard 1149.1 - 1990 Standard Test Access Port and Boundary Scan Architecture and STM32F107 datasheets and users manual.

Pin #	Signal Name	Pin #	Signal Name
1	3.3V	2	3.3V
3	TRST	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	PULL-DOWN	12	GND
13	TDO	14	GND
15	RST	16	GND
17	PULL-DOWN	18	GND
19	+5V_JTAG	20	GND

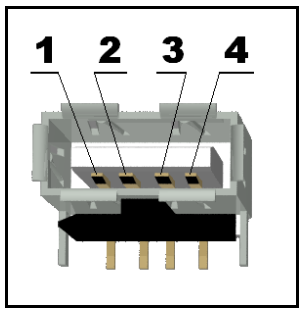
PWR_JACK

Pin #	Signal Name
1	Power Input
2	GND



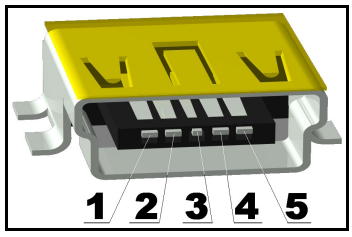
USB_HOST

Pin #	Signal Name
1	+5V_HOST_PWR
2	USB_HOST_D-
3	USB_HOST_D+
4	GND



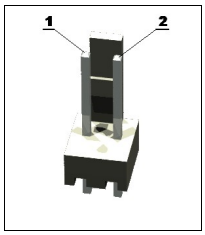
USB_OTG

Pin #	Signal Name
1	+5V_OTG_PWR
2	USB_OTG_D-
3	USB_OTG_D+
4	OTG_ID
5	GND



3V_BAT

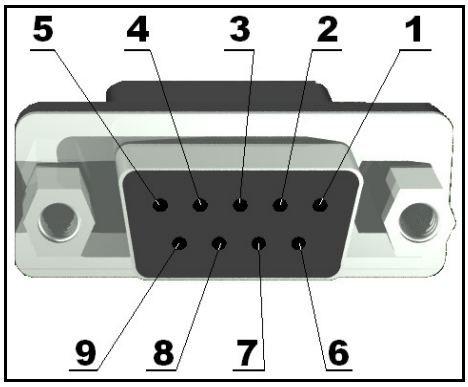
Pin #	Signal Name
1	VBAT
2	GND



RS232

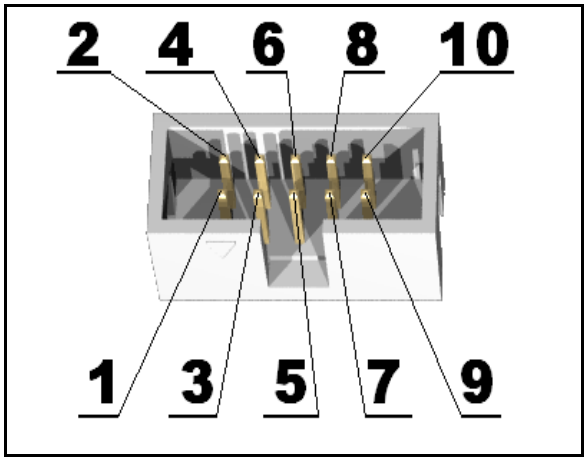
The RS232 port can be used for communication when in bootloader mode. To enter bootloader mode you need to close RST_E and BOOT0_E jumpers. Note that the default position of those jumpers is closed, e.g. bootloader mode disabled.

Pin #	Signal Name
1	NC
2	T1OUT
3	R1IN
4	NC
5	GND
6	NC
7	CTS
8	RTS
9	NC

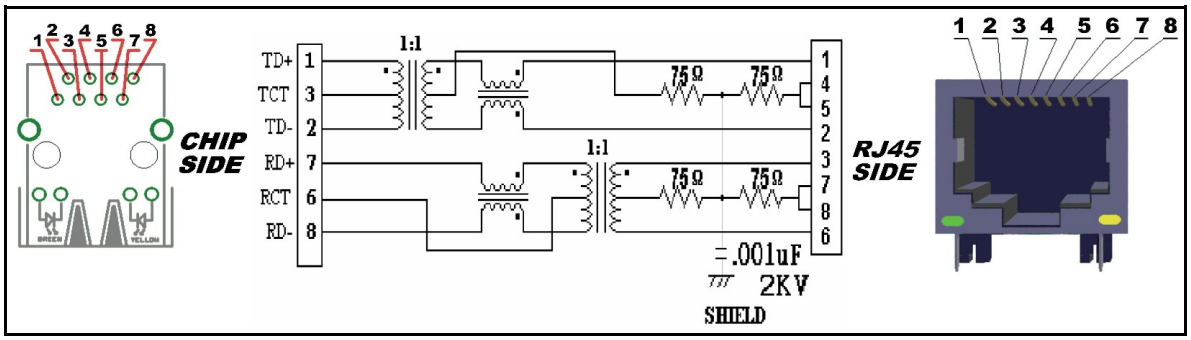


UEXT

Pin #	Signal Name
1	3.3V
2	GND
3	USART2_TX
4	USART2_RX
5	I2C1_SCL
6	I2C1_SDA
7	SPI3_MISO
8	SPI3_MOSI
9	SPI3_SCK
10	CS_UEXT



LAN

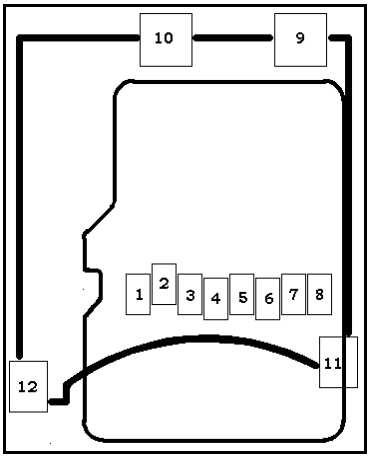


Pin #	Signal Name Chip Side	Pin #	Signal Name Chip Side
1	TX+	5	Not Connected (NC)
2	TX-	6	VDD
3	VDD	7	RX+
4	Not Connected (NC)	8	RX-

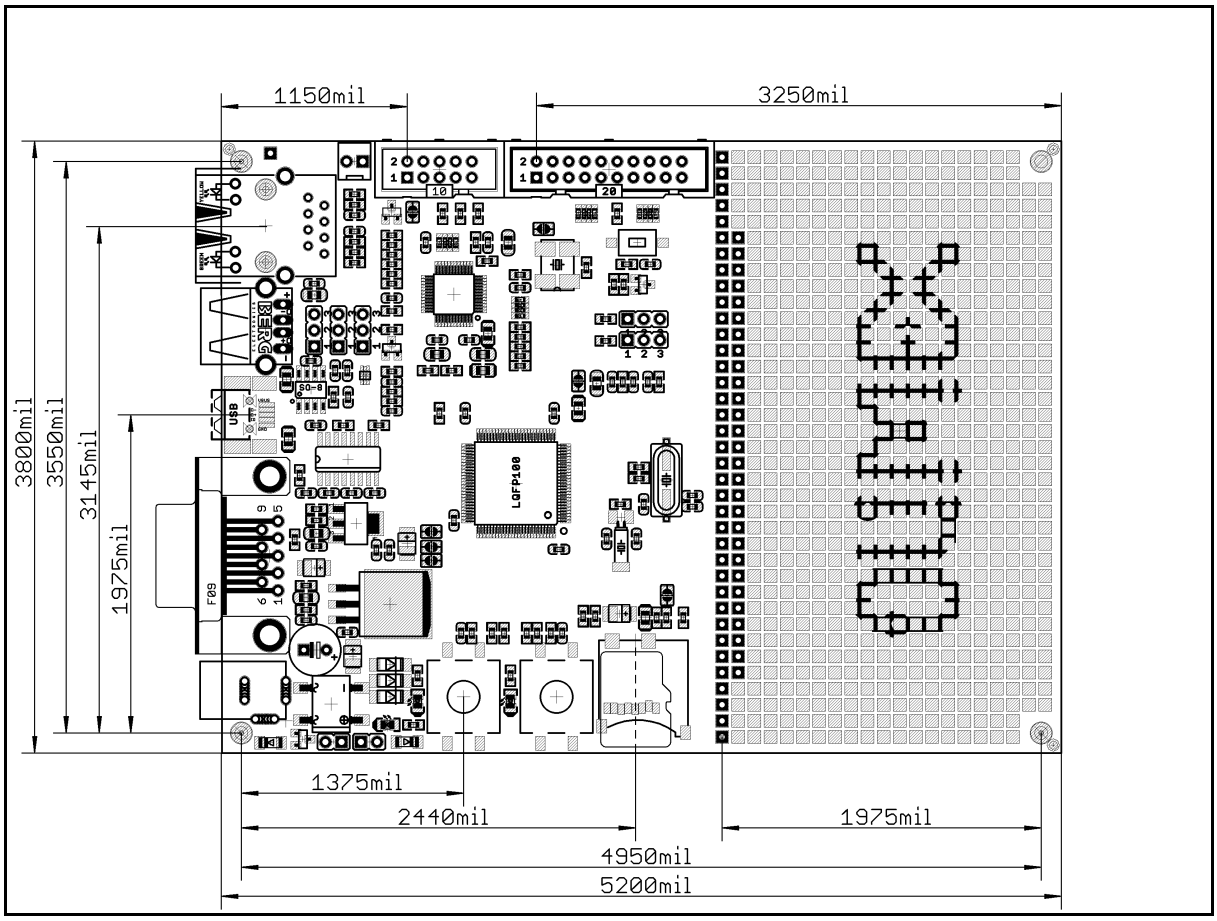
LED	Color	Usage
Right	Green	Link status
Left	Yellow	Activity status

SD/MMC

Pin #	Signal Name
1	MCIDAT2
2	CS_MMC
3	SPI3_MOSI
4	3.3V
5	SPI3_SCK
6	GND
7	SPI3_MISO
8	MCIDAT1
9	Not connected
10	Not connected
11	Not connected
12	Not connected



MECHANICAL DIMENSIONS



All measures are in mils.

AVAILABLE DEMO SOFTWARE

- NEW STM32-P107 demo package with Micrel PHY
- Blinking LED Demo software for EW-ARM 5.50
- Ethernet Demo software for EW-ARM 5.50
- USB Demo software for EW-ARM 5.50
- SD card Demo software for EW-ARM 5.50

ORDER CODE

STM32-P107 – assembled and tested

How to order?
You can order to us directly or by any of our distributors.
Check our web www.olimex.com/dev for more info.

Manual revision history:

REV. Initial	- created December 2009
REV. A	- edited by TU December 2010
REV. B	- demo software added and mechanical dimensions detailed
REV. C	- Rev. A schematic and added more programmers in BOARD USE REQUIREMENTS.
REV. D	- edited June 2011 – changed schematic
REV. E	- changed schematics to rev. B, added board revision history
REV.F	- added BOOT0_E, RST_E description, changed dimensions, updated revision B pictures, updated disclaimer

Board revision history:

rev.A

========

1. ST2052BD is exchanged with LM3526-L.

2. SD/MMC signals are changed as follows:

SPI1_MOSI	->	SPI3_MOSI
SPI1_SCK	->	SPI3_SCK
SPI1_MISO	->	SPI3_MISO

and SPI1_NSS renamed to CS_MMC

3. Changed the polarity to + of C36

In Rev.B

========

1. All libraries are updated

2. Ethernet PHY is changed from STE101P to MICREL's one - KS8721BLMM

3. All 10uF/6.3V/TANT are changed to 0805 and a lot of element names are changed.

4. PWR_SEL jumpers are replaced by diodes.

5. USART3 is connected to UEXT while USART2 is connected to RS232 and bootloader functionality is enabled! Two additional jumpers are added!!!

6. Added UEXT_PWR_E jumper!

7. A lot jumpers are added into jumpers description table

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The software is released under GPL.

It is possible that the pictures in this manual differ from the latest revision of the board.

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