To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

RENESAS

R1LV1616H-I Series

Wide Temperature Range Version
16 M SRAM (1-Mword × 16-bit / 2-Mword × 8-bit)

REJ03C0195-0101
Rev.1.01
Nov.18.2004

Description

The R1LV1616H-I Series is 16-Mbit static RAM organized 1-Mword × 16-bit / 2-Mword × 8-bit. R1LV1616H-I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in 48-pin plastic TSOPI for high density surface mounting.

Features

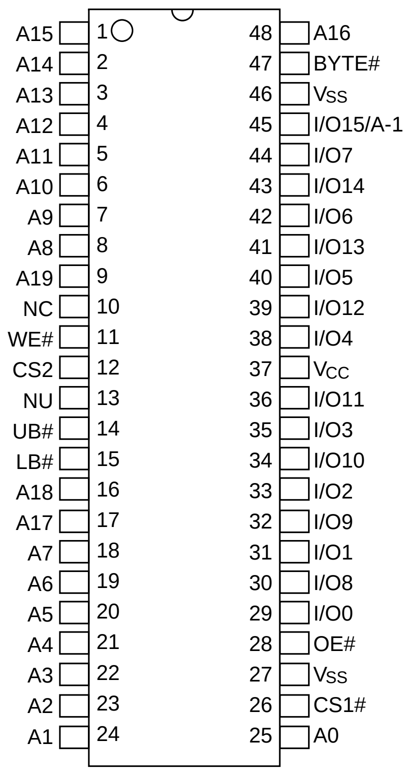
- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 45/55 ns (max)
- Power dissipation:
  - Active: 9 mW/MHz (typ)
  - Standby: 1.5 µW (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range: −40 to +85°C
- Byte function (×8 mode) available by BYTE# & A-1.

Ordering Information

Type No.	Access time	Package
R1LV1616HSA-4LI	45 ns	48-pin plastic TSOPI (48P3R-B)
R1LV1616HSA-4SI	45 ns	
R1LV1616HSA-5SI	55 ns	

Pin Arrangement

48-pin TSOP



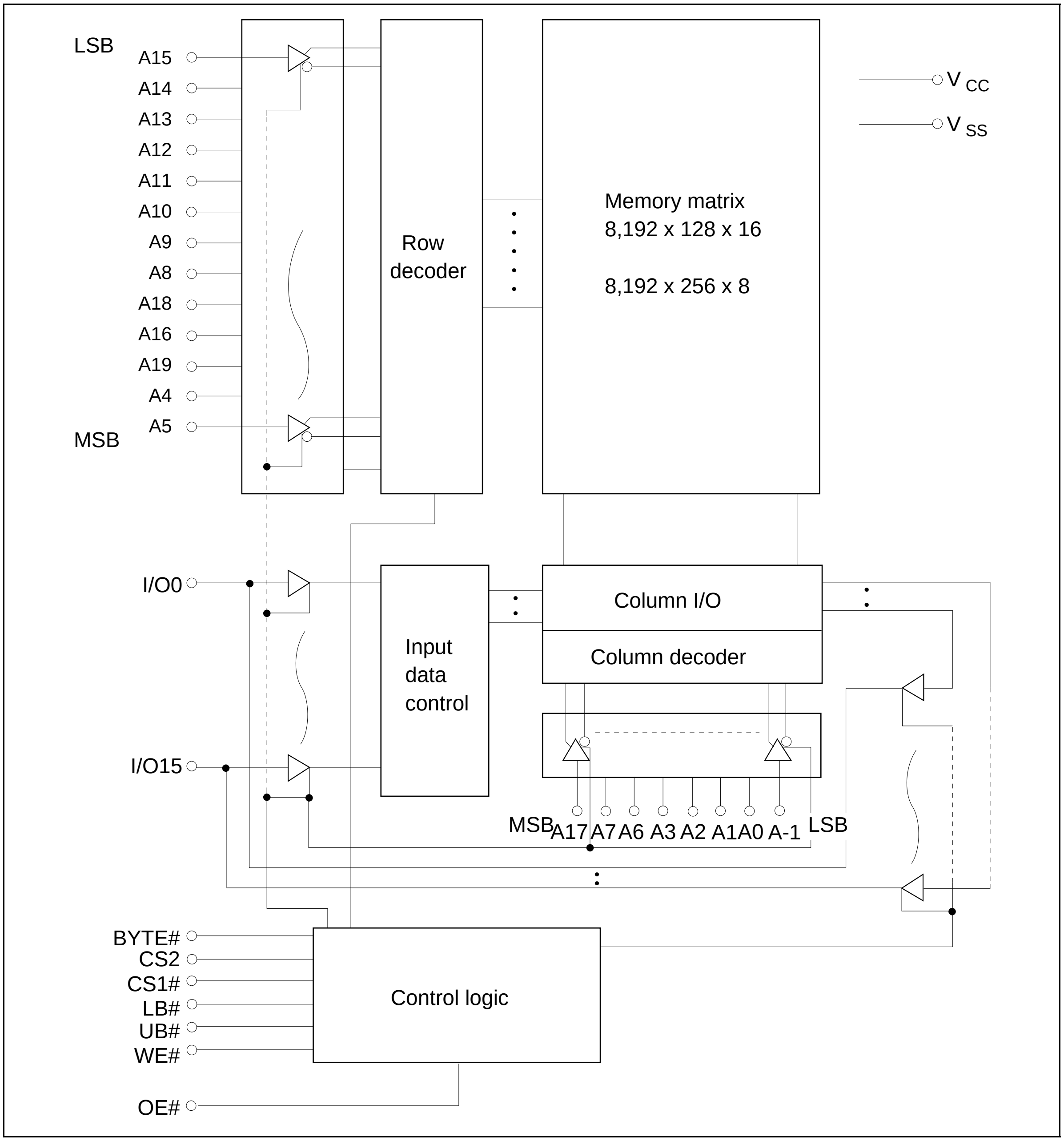
(Top view)

Pin Description (TSOP)

Pin name	Function
A0 to A19	Address input (word mode)
A-1 to A19	Address input (byte mode)
I/O0 to I/O15	Data input/output
CS1# ($\overline{CS1}$)	Chip select 1
CS2	Chip select 2
WE# ($\overline{WE}$)	Write enable
OE# ($\overline{OE}$)	Output enable
LB# ($\overline{LB}$)	Lower byte select
UB# ($\overline{UB}$)	Upper byte select
BYTE# ($\overline{BYTE}$)	Byte enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection
NU*[1]	Not used (test mode pin)

Note: 1. This pin should be connected to a ground (V_{SS}), or not be connected (open).

Block Diagram (TSOP)



Operation Table (TSOP)

Byte mode

CS1#	CS2	WE#	OE#	UB#	LB#	BYTE#	I/O0 to I/O7	I/O8 to I/O14	I/O15	Operation
H	×	×	×	×	×	L	High-Z	High-Z	High-Z	Standby
×	L	×	×	×	×	L	High-Z	High-Z	High-Z	Standby
L	H	H	L	×	×	L	Dout	High-Z	A-1	Read
L	H	L	×	×	×	L	Din	High-Z	A-1	Write
L	H	H	H	×	×	L	High-Z	High-Z	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Word mode

CS1#	CS2	WE#	OE#	UB#	LB#	BYTE#	I/O0 to I/O7	I/O8 to I/O14	I/O15	Operation
H	×	×	×	×	×	H	High-Z	High-Z	High-Z	Standby
×	L	×	×	×	×	H	High-Z	High-Z	High-Z	Standby
×	×	×	×	H	H	H	High-Z	High-Z	High-Z	Standby
L	H	H	L	L	L	H	Dout	Dout	Dout	Read
L	H	H	L	H	L	H	Dout	High-Z	High-Z	Lower byte read
L	H	H	L	L	H	H	High-Z	Dout	Dout	Upper byte read
L	H	L	×	L	L	H	Din	Din	Din	Write
L	H	L	×	H	L	H	Din	High-Z	High-Z	Lower byte write
L	H	L	×	L	H	H	High-Z	Din	Din	Upper byte write
L	H	H	H	×	×	H	High-Z	High-Z	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.3*[2]	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–40 to +85	°C

Notes: 1. V_T min: –2.0 V for pulse half-width ≤ 10 ns.
2. Maximum voltage is +4.6 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	–0.3	—	0.6	V	1
Ambient temperature range	Ta	–40	—	+85	°C	

Note: 1. V_{IL} min: –2.0 V for pulse half-width ≤ 10 ns.

DC Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions*[2]
Input leakage current		$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	1	µA	CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating current		I_{CC}	—	—	20	mA	CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/ V_{IL}, $I_{I/O}$ = 0 mA
Average operating current		I_{CC1} (READ)	—	22*[1]	35	mA	Min. cycle, duty = 100%, $I_{I/O}$ = 0 mA, CS1# = V_{IL}, CS2 = V_{IH}, WE# = V_{IH}, Others = V_{IH}/V_{IL}
		I_{CC1}	—	30*[1]	50	mA	Min. cycle, duty = 100%, $I_{I/O}$ = 0 mA, CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
		I_{CC2}*[3] (READ)	—	3*[1]	8	mA	Cycle time = 70 ns, duty = 100%, $I_{I/O}$ = 0 mA, CS1# = V_{IL}, CS2 = V_{IH}, WE# = V_{IH}, Others = V_{IH}/V_{IL} Address increment scan or decrement scan
		I_{CC2}*[3]	—	20*[1]	30	mA	Cycle time = 70 ns, duty = 100%, $I_{I/O}$ = 0 mA, CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL} Address increment scan or decrement scan
		I_{CC3}	—	3*[1]	8	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, CS1# ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby current		I_{SB}	—	0.1*[1]	0.5	mA	CS2 = V_{IL}
Standby current	-4SI -5SI	I_{SB1}	—	0.5*[1]	8	µA	0 V ≤ Vin (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS1# ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V or (3) LB# = UB# ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V, CS1# ≤ 0.2 V Average value
	-4LI	I_{SB1}	—	0.5*[1]	25	µA	
Output high voltage		V_{OH}	2.4	—	—	V	I_{OH} = –1 mA
		V_{OH}	V_{CC} – 0.2	—	—	V	I_{OH} = –100 µA
Output low voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
		V_{OL}	—	—	0.2	V	I_{OL} = 100 µA

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
2. BYTE# ≥ V_{CC} – 0.2 V or BYTE# ≤ 0.2 V
3. I_{CC2} is the value measured while the valid address is increasing or decreasing by one bit.
Word mode: LSB (least significant bit) is A0.
Byte mode: LSB (least significant bit) is A-1.

Capacitance

(Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	8	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

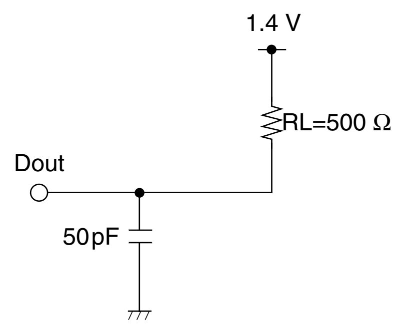
RENESAS

AC Characteristics

(Ta = –40 to +85°C, V_{CC} = 2.7 V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.4 V, V_{IH} = 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.4 V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	R1LV1616H-I -4SI, -4LI Min	R1LV1616H-I -4SI, -4LI Max	R1LV1616H-I -5SI Min	R1LV1616H-I -5SI Max	Unit	Notes
Read cycle time	t_{RC}	45	—	55	—	ns	
Address access time	t_{AA}	—	45	—	55	ns	
Chip select access time	t_{ACS1}	—	45	—	55	ns	
	t_{ACS2}	—	45	—	55	ns	
Output enable to output valid	t_{OE}	—	30	—	35	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
LB#, UB# access time	t_{BA}	—	45	—	55	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	10	—	ns	2, 3
	t_{CLZ2}	10	—	10	—	ns	2, 3
LB#, UB# enable to low-Z	t_{BLZ}	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	0	20	ns	1, 2, 3
	t_{CHZ2}	0	20	0	20	ns	1, 2, 3
LB#, UB# disable to high-Z	t_{BHZ}	0	15	0	20	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	15	0	20	ns	1, 2, 3

Write Cycle

Parameter	Symbol	R1LV1616H-I -4SI, -4LI Min	R1LV1616H-I -4SI, -4LI Max	R1LV1616H-I -5SI Min	R1LV1616H-I -5SI Max	Unit	Notes
Write cycle time	t_{WC}	45	—	55	—	ns	
Address valid to end of write	t_{AW}	45	—	50	—	ns	
Chip selection to end of write	t_{CW}	45	—	50	—	ns	5
Write pulse width	t_{WP}	35	—	40	—	ns	4
LB#, UB# valid to end of write	t_{BW}	45	—	50	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	25	—	25	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	15	0	20	ns	1, 2
Write to output in high-Z	t_{WHZ}	0	15	0	20	ns	1, 2

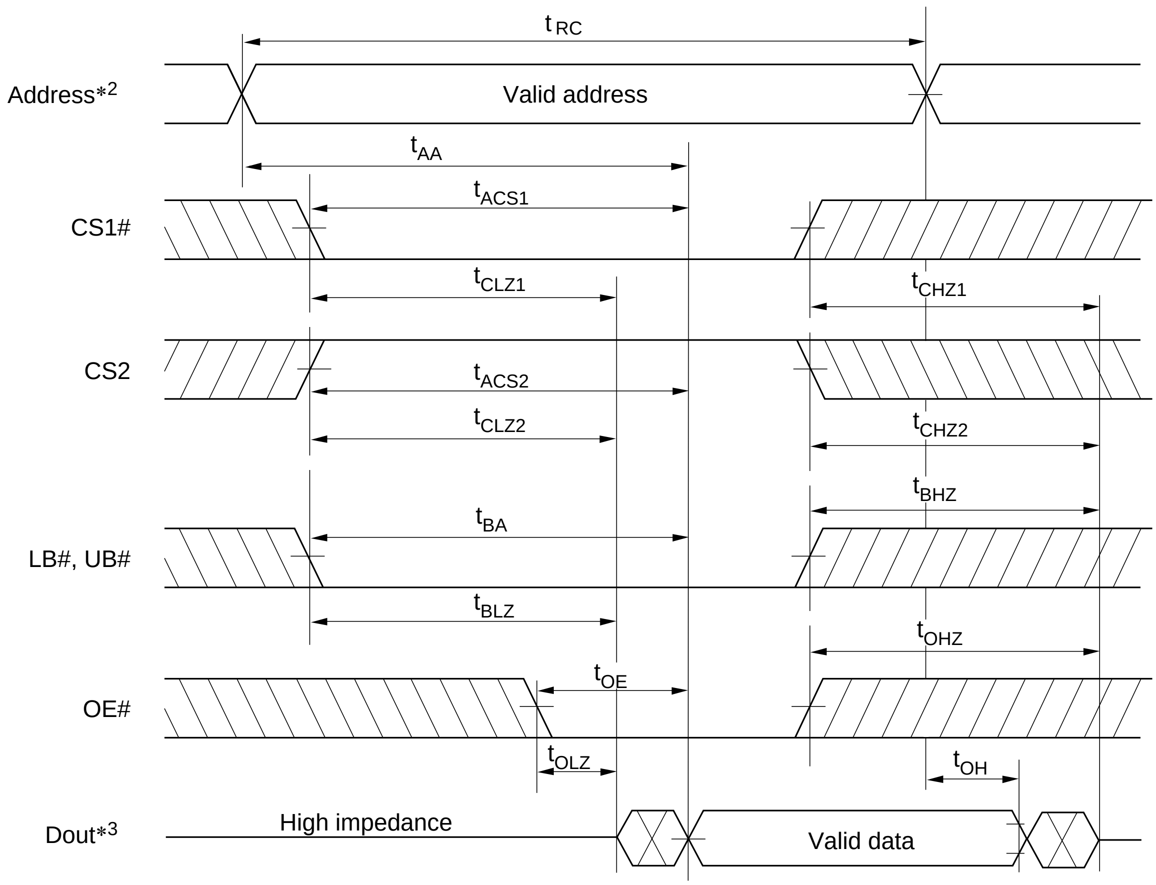
Byte Control

		R1LV1616H-I					
		-4SI, -4LI		-5SI			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
BYTE# setup time	t_{BS}	5	—	5	—	ms	
BYTE# recovery time	t_{BR}	5	—	5	—	ms	

Notes:
1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS1# going low or CS2 going high to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

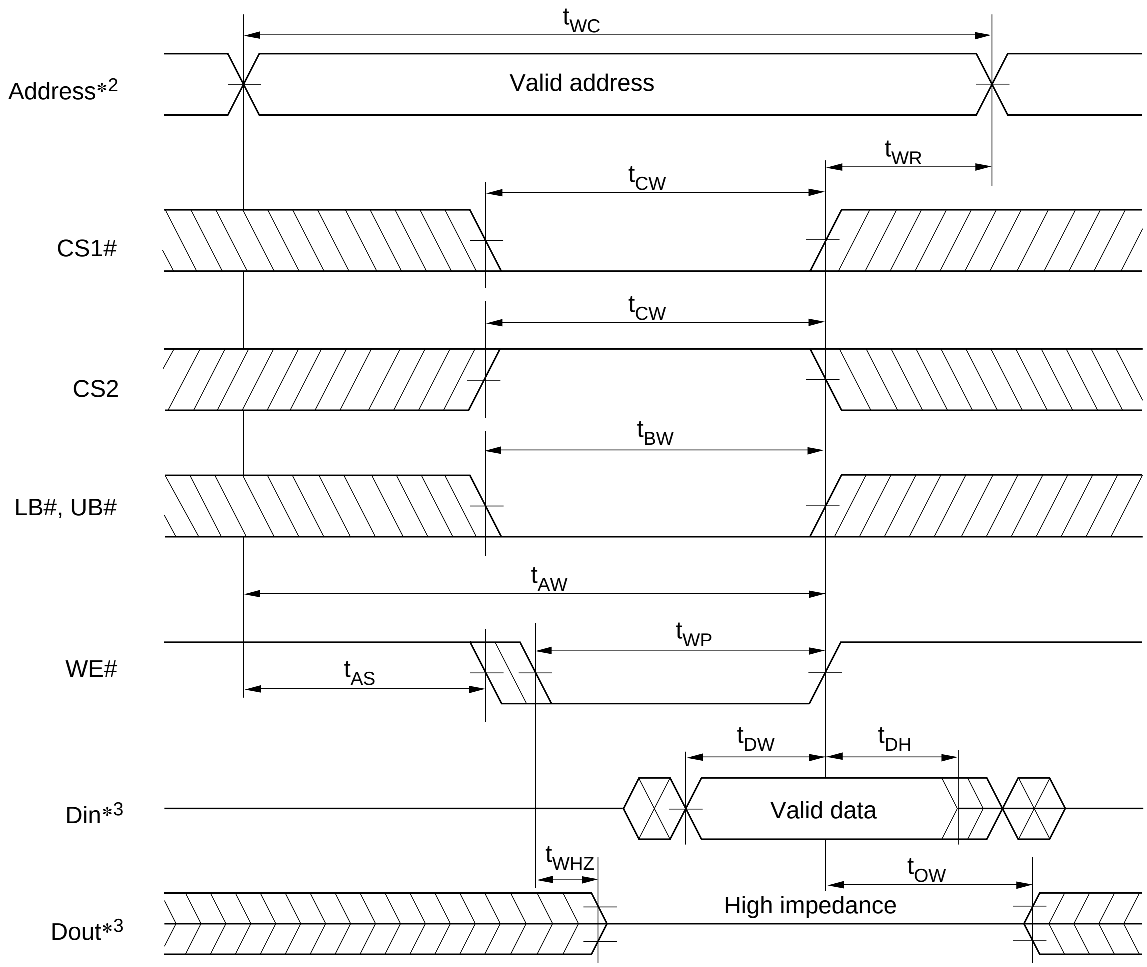
Timing Waveform

Read Cycle*[1]



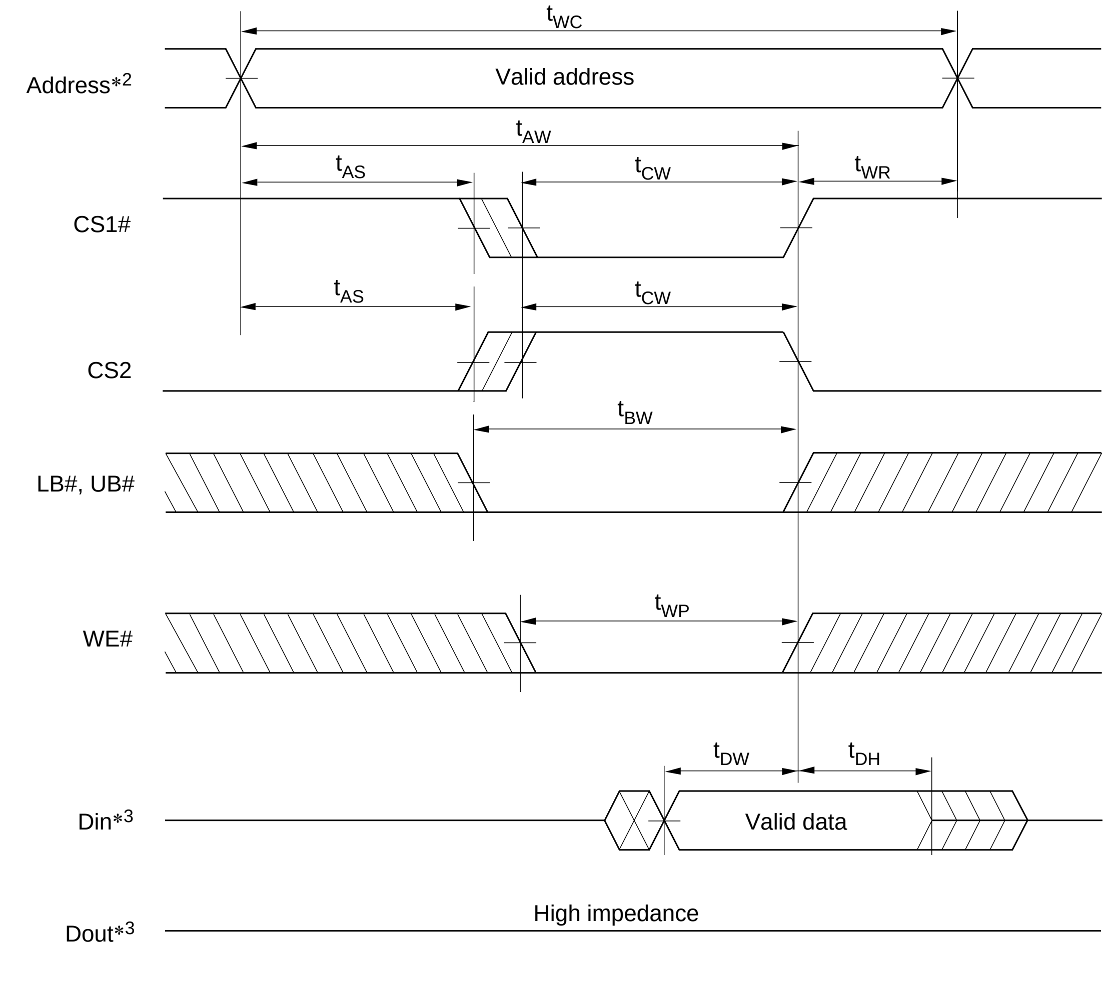
Notes: 1. BYTE# > V_{CC} – 0.2 V or
BYTE# < 0.2 V
2. Word mode: A0 to A19
Byte mode: A-1 to A19
3. Word mode: I/O0 to I/O15
Byte mode: I/O0 to I/O7

Write Cycle (1)*[1] (WE# Clock)



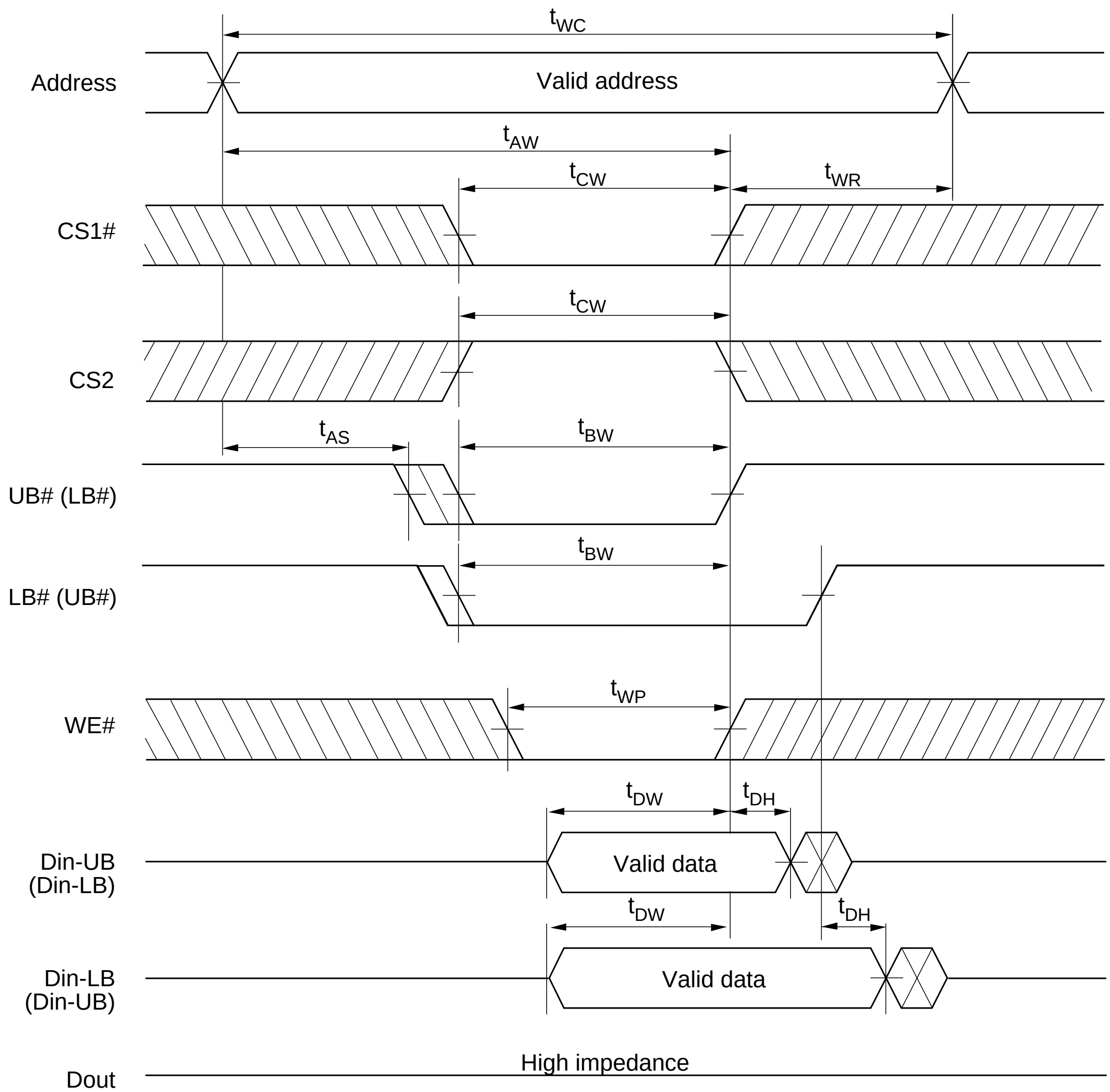
Notes: 1. BYTE# > V_{CC} – 0.2 V or
BYTE# < 0.2 V
2. Word mode: A0 to A19
Byte mode: A-1 to A19
3. Word mode: I/O0 to I/O15
Byte mode: I/O0 to I/O7

Write Cycle (2)*[1] (CS1#, CS2 Clock, OE# = V_{IH})



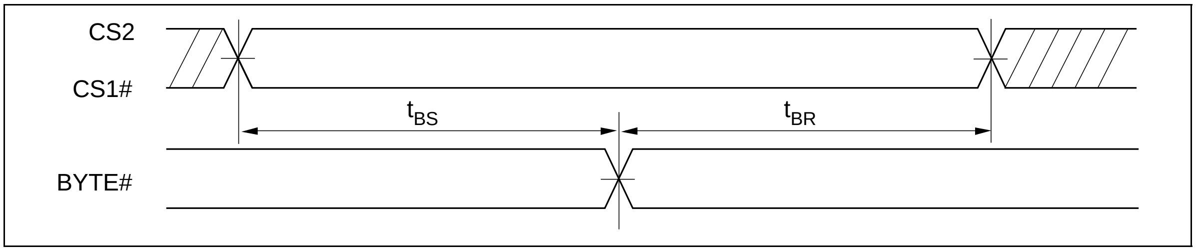
Notes: 1. BYTE# > V_{CC} – 0.2 V or BYTE# < 0.2 V
2. Word mode: A0 to A19
Byte mode: A-1 to A19
3. Word mode: I/O0 to I/O15
Byte mode: I/O0 to I/O7

Write Cycle (3)*[1] (LB#, UB# Clock, OE# = V_{IH})



Note: 1. BYTE# > V_{CC} – 0.2 V

Byte Control (TSOP)



Low V_{CC} Data Retention Characteristics

(Ta = –40 to +85°C)

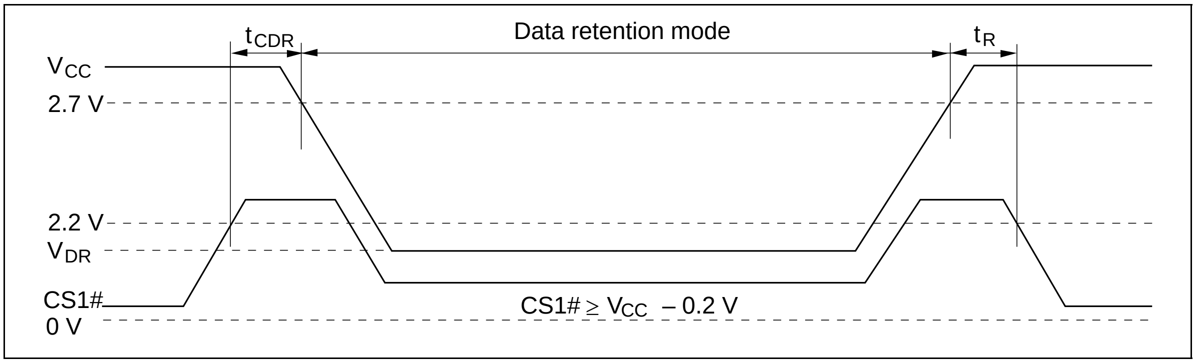
Parameter		Symbol	Min	Typ	Max	Unit	Test conditions*[2, 3]
V_{CC} for data retention		V_{DR}	1.5	—	3.6	V	Vin ≥ 0 V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V, CS1# ≥ V_{CC} – 0.2 V or (3) LB# = UB# ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V, CS1# ≤ 0.2 V
Data retention current	-4SI -5SI	I_{CCDR}	—	0.5*[1]	8	µA	V_{CC} = 3.0 V, Vin ≥ 0 V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V, CS1# ≥ V_{CC} – 0.2 V or (3) LB# = UB# ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V, CS1# ≤ 0.2 V Average value
	-4LI	I_{CCDR}	—	0.5*[1]	25	µA	
Chip deselect to data retention time		t_{CDR}	0	—	—	ns	See retention waveforms
Operation recovery time		t_R	5	—	—	ms	

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.

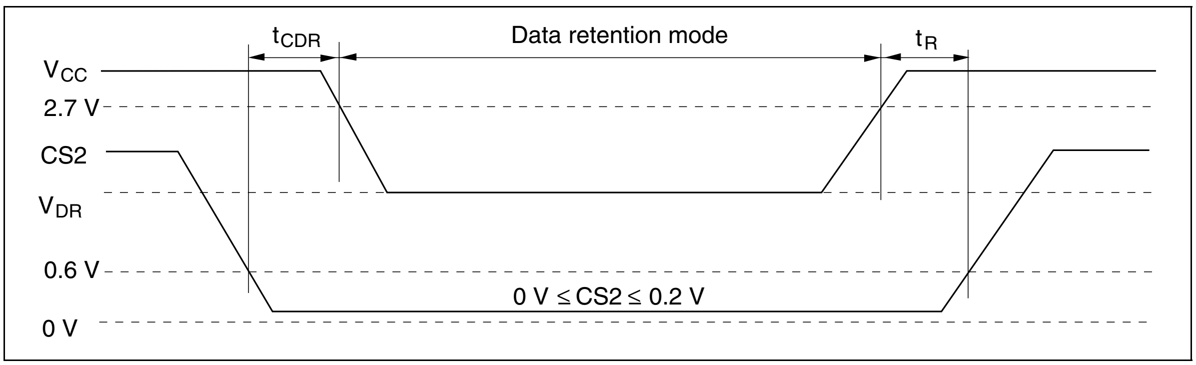
2. BYTE# ≥ V_{CC} – 0.2 V or BYTE# ≤ 0.2 V

3. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high impedance state.

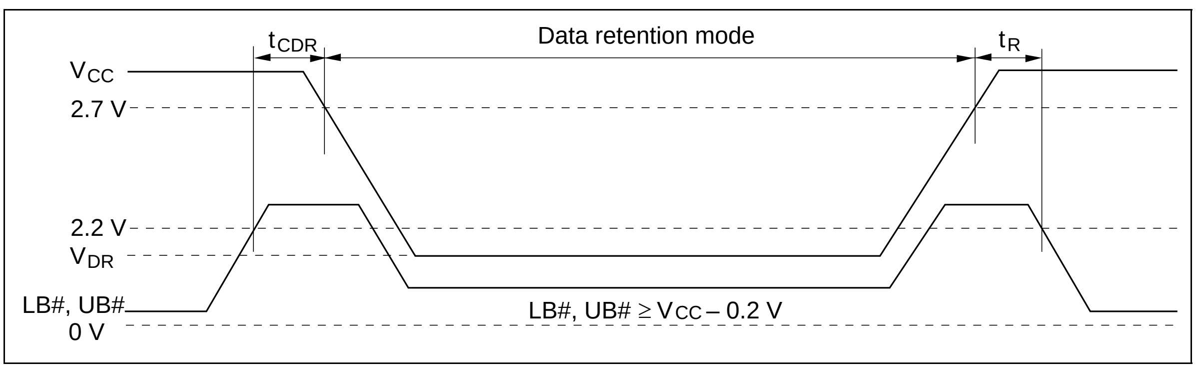
Low V_{CC} Data Retention Timing Waveform (1) (CS1# Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Low V_{CC} Data Retention Timing Waveform (3) (LB#, UB# Controlled)



Revision History R1LV1616H-I Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
1.00	Apr. 22, 2004	—	Initial issue
1.01	Nov. 18, 2004	—	Addition of 2-Mword × 8-bit function

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Colophon .2.0