FM25L16B

16Kb Serial 3V F-RAM Memory

Features

16K bit Ferroelectric Nonvolatile RAM

- Organized as 2,048 x 8 bits
- High Endurance 100 Trillion (10^{14}) Read/Writes
- 38 Year Data Retention (@ +75°C)
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Very Fast Serial Peripheral Interface - SPI

- Up to 20 MHz Frequency
- Direct Hardware Replacement for EEPROM
- SPI Mode 0 & 3 (CPOL, CPHA=0,0 & 1,1)

Sophisticated Write Protection Scheme

- Hardware Protection
- Software Protection

Low Power Consumption

- Low Voltage Operation 2.7-3.6V
- 200 µA Active Current (1 MHz)
- 3 µA (typ.) Standby Current

Industry Standard Configuration

- Industrial Temperature -40°C to +85°C
- 8-pin "Green"/RoHS SOIC and TDFN Packages

Description

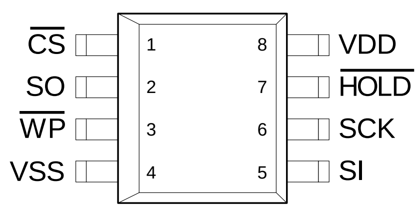
The FM25L16B is a 16-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes like a RAM. It provides reliable data retention for 38 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

The FM25L16B performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte has been transferred to the device. The next bus cycle may commence without the need for data polling. The FM25L16B is capable of supporting 10^{14} read/write cycles, or a million times more write cycles than EEPROM.

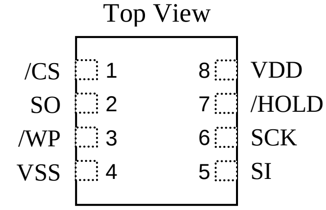
These capabilities make the FM25L16B ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss.

The FM25L16B provides substantial benefits to users of serial EEPROM as a hardware drop-in replacement. The FM25L16B uses the high-speed SPI bus, which enhances the high-speed write capability of F-RAM technology. Device specifications are guaranteed over an industrial temperature range of -40°C to +85°C.

Pin Configuration



Top View



Pin Name	Function
/CS	Chip Select
/WP	Write Protect
/HOLD	Hold
SCK	Serial Clock
SI	Serial Data Input
SO	Serial Data Output
VDD	Supply Voltage
VSS	Ground

Ordering Information	
FM25L16B-G	"Green"/RoHS 8-pin SOIC
FM25L16B-GTR	"Green"/RoHS 8-pin SOIC, Tape & Reel
FM25L16B-DG	"Green"/RoHS 8-pin TDFN
FM25L16B-DGTR	"Green"/RoHS 8-pin TDFN, Tape & Reel

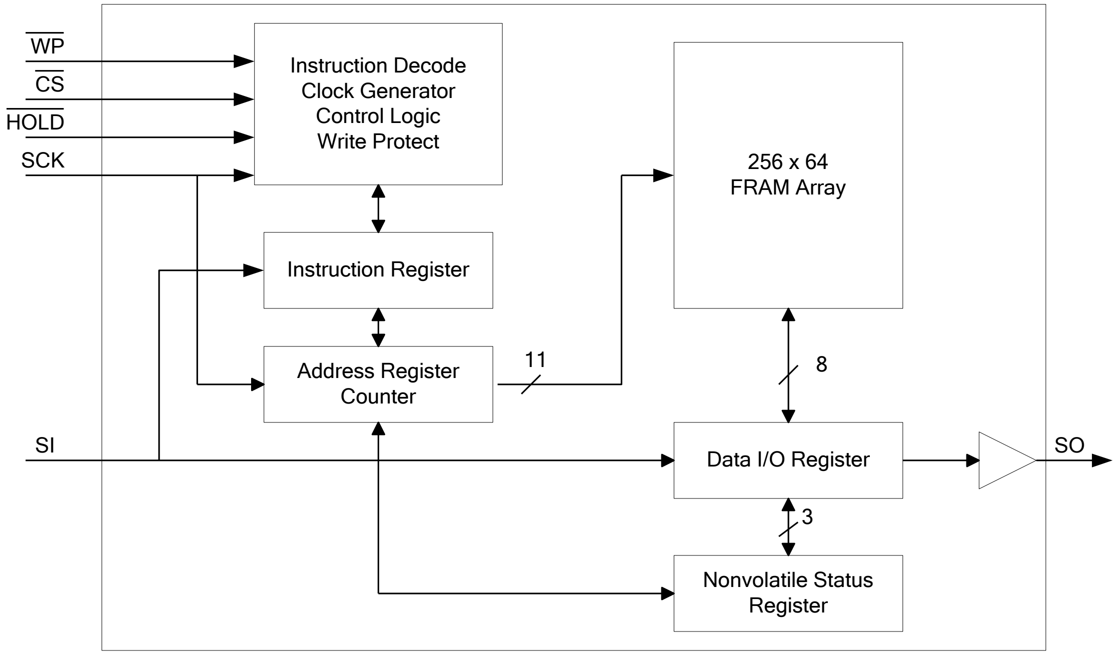


Figure 1. Block Diagram

Pin Descriptions

Pin Name	I/O	Description
/CS	Input	Chip Select: This active low input activates the device. When high, the device enters low-power standby mode, ignores other inputs, and all outputs are tri-stated. When low, the device internally activates the SCK signal. A falling edge on /CS must occur prior to every op-code.
SCK	Input	Serial Clock: All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Since the device is static, the clock frequency may be any value between 0 and 20 MHz and may be interrupted at any time.
/HOLD	Input	Hold: The /HOLD pin is used when the host CPU must interrupt a memory operation for another task. When /HOLD is low, the current operation is suspended. The device ignores any transition on SCK or /CS. All transitions on /HOLD must occur while SCK is low.
/WP	Input	Write Protect: This active low pin prevents write operations to the status register. This is critical since other write protection features are controlled through the status register. A complete explanation of write protection is provided on pages 6 and 7.
SI	Input	Serial Input: All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet I_{DD} specifications. * SI may be connected to SO for a single pin data interface.
SO	Output	Serial Output: This is the data output pin. It is driven during a read and remains tri-stated at all other times including when /HOLD is low. Data transitions are driven on the falling edge of the serial clock. * SO may be connected to SI for a single pin data interface.
VDD	Supply	Power Supply (2.7V to 3.6V)
VSS	Supply	Ground

Overview

The FM25L16B is a serial F-RAM memory. The memory array is logically organized as 2,048 x 8 and is accessed using an industry standard Serial Peripheral Interface or SPI bus. Functional operation of the F-RAM is similar to serial EEPROMs. The major difference between the FM25L16B and a serial EEPROM with the same pinout is the F-RAM's superior write performance.

Memory Architecture

When accessing the FM25L16B, the user addresses 2,048 locations of 8 data bits each. These data bits are shifted serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an op-code, and a two-byte address. The upper 5 bits of the address range are 'don't care' values. The complete address of 11-bits specifies each byte address uniquely.

Most functions of the FM25L16B either are controlled by the SPI interface or are handled automatically by on-board circuitry. The access time for memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. So, by the time a new bus transaction can be shifted into the device, a write operation will be complete. This is explained in more detail in the interface section.

Users expect several obvious system benefits from the FM25L16B due to its fast write cycle and high endurance as compared with EEPROM. In addition there are less obvious benefits as well. For example in a high noise environment, the fast-write operation is less susceptible to corruption than an EEPROM since it is completed quickly. By contrast, an EEPROM requiring milliseconds to write is vulnerable to noise during much of the cycle.

Note that the FM25L16B contains no power management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that V_{DD} is within datasheet tolerances to prevent incorrect operation. It is recommended that the part is not powered down with chip select active.

Serial Peripheral Interface – SPI Bus

The FM25L16B employs a Serial Peripheral Interface (SPI) bus. It is specified to operate at speeds up to 20 MHz. This high-speed serial bus provides high performance serial communication to a host microcontroller. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The FM25L16B operates in SPI Mode 0 and 3.

The SPI interface uses a total of four pins: clock, data-in, data-out, and chip select. A typical system configuration uses one or more FM25L16B devices with a microcontroller that has a dedicated SPI port, as Figure 2 illustrates. Note that the clock, data-in, and data-out pins are common among all devices. The Chip Select and Hold pins must be driven separately for each FM25L16B device.

For a microcontroller that has no dedicated SPI bus, a general purpose port may be used. To reduce hardware resources on the controller, it is possible to connect the two data pins (SI, SO) together and tie off (high) the Hold pin. Figure 3 shows a configuration that uses only three pins.

Protocol Overview

The SPI interface is a synchronous serial interface using clock and data pins. It is intended to support multiple devices on the bus. Each device is activated using a chip select. Once chip select is activated by the bus master, the FM25L16B will begin monitoring the clock and data lines. The relationship between the falling edge of /CS, the clock and data is dictated by the SPI mode. The device will make a determination of the SPI mode on the falling edge of each chip select. While there are four such modes, the FM25L16B supports Modes 0 and 3. Figure 4 shows the required signal relationships for Modes 0 and 3. For both modes, data is clocked into the FM25L16B on the rising edge of SCK and data is expected on the first rising edge after /CS goes active. If the clock begins from a high state, it will fall prior to beginning data transfer in order to create the first rising edge.

The SPI protocol is controlled by op-codes. These op-codes specify the commands to the device. After /CS is activated the first byte transferred from the bus master is the op-code. Following the op-code, any addresses and data are then transferred. Note that the WREN and WRDI op-codes are commands with no subsequent data transfer.

Important: The /CS must go inactive (high) after an operation is complete and before a new op-code can be issued. There is one valid op-code only per active chip select.

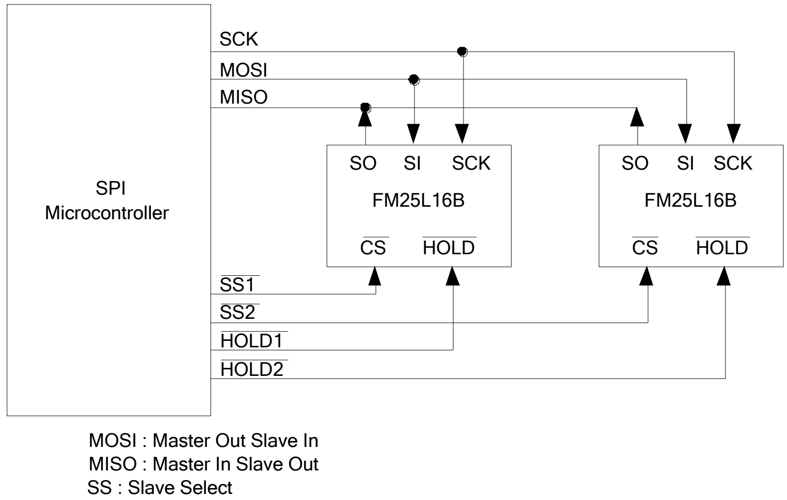


Figure 2. System Configuration with SPI port

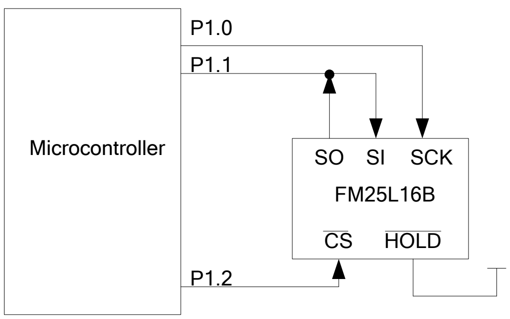


Figure 3. System Configuration without SPI port

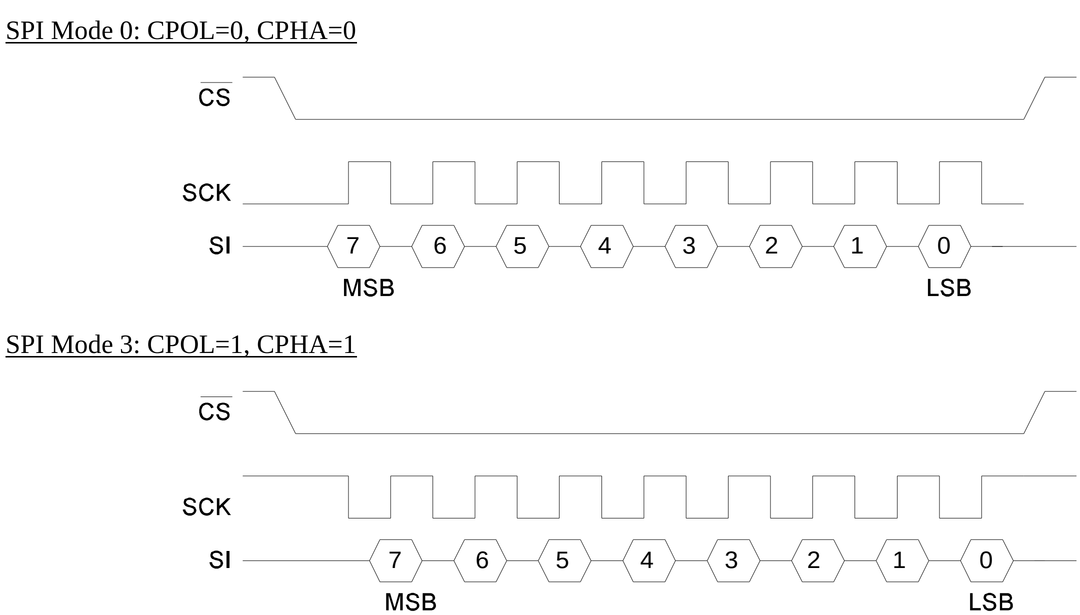


Figure 4. SPI Modes 0 & 3

Data Transfer

All data transfers to and from the FM25L16B occur in 8-bit groups. They are synchronized to the clock signal (SCK), and they transfer most significant bit (MSB) first. Serial inputs are registered on the rising edge of SCK. Outputs are driven from the falling edge of SCK.

Command Structure

There are six commands called op-codes that can be issued by the bus master to the FM25L16B. They are listed in the table below. These op-codes control the functions performed by the memory. They can be divided into three categories. First, there are commands that have no subsequent operations. They perform a single function such as to enable a write operation. Second are commands followed by one byte, either in or out. They operate on the status register. The third group includes commands for memory transactions followed by an address and one or more bytes of data.

Table 1. Op-code Commands

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110b
WRDI	Write Disable	0000 0100b
RDSR	Read Status Register	0000 0101b
WRSR	Write Status Register	0000 0001b
READ	Read Memory Data	0000 0011b
WRITE	Write Memory Data	0000 0010b

WREN - Set Write Enable Latch

The FM25L16B will power up with writes disabled. The WREN command must be issued prior to any write operation. Sending the WREN op-code will allow the user to issue subsequent op-codes for write operations. These include writing the status register and writing the memory.

Sending the WREN op-code causes the internal Write Enable Latch to be set. A flag bit in the status register, called WEL, indicates the state of the latch. WEL=1 indicates that writes are permitted. Attempting to write the WEL bit in the status register has no effect. Completing any write operation will automatically clear the write-enable latch and prevent further writes without another WREN command. Figure 5 below illustrates the WREN command bus configuration.

WRDI - Write Disable

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the status register and verifying that WEL=0. Figure 6 illustrates the WRDI command bus configuration.

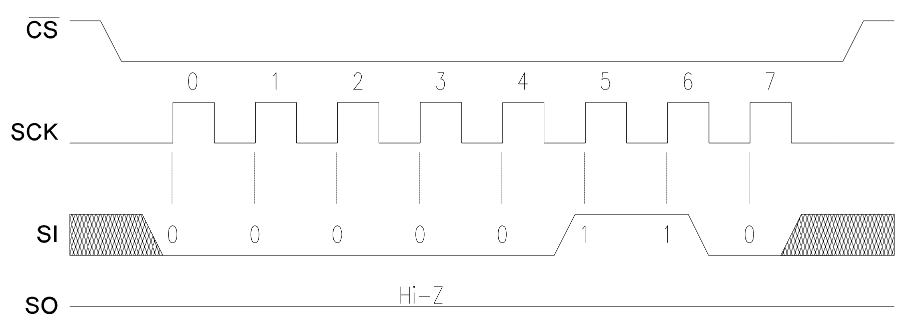


Figure 5. WREN Bus Configuration

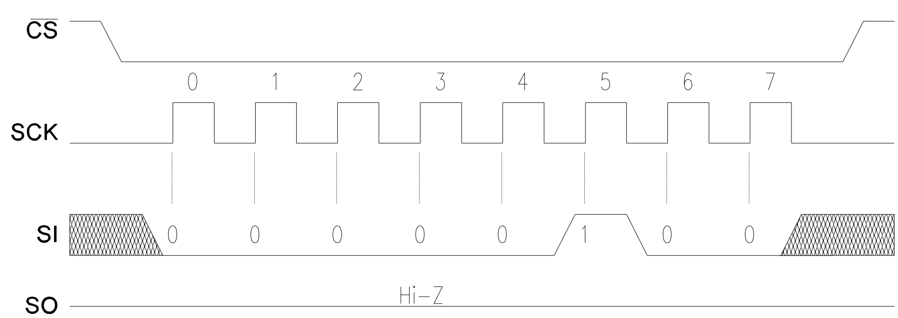


Figure 6. WRDI Bus Configuration

RDSR - Read Status Register

The RDSR command allows the bus master to verify the contents of the Status Register. Reading Status provides information about the current state of the write protection features. Following the RDSR op-code, the FM25L16B will return one byte with the contents of the Status Register. The Status Register is described in detail in a later section.

WRSR – Write Status Register

The WRSR command allows the user to select certain write protection features by writing a byte to the Status Register. Prior to issuing a WRSR command, the /WP pin must be high or inactive. Note that on the FM25L16B, /WP only prevents writing to the Status Register, not the memory array. Prior to sending the WRSR command, the user must send a WREN command to enable writes. Note that executing a WRSR command is a write operation and therefore clears the Write Enable Latch. The bus configuration of RDSR and WRSR are shown below.

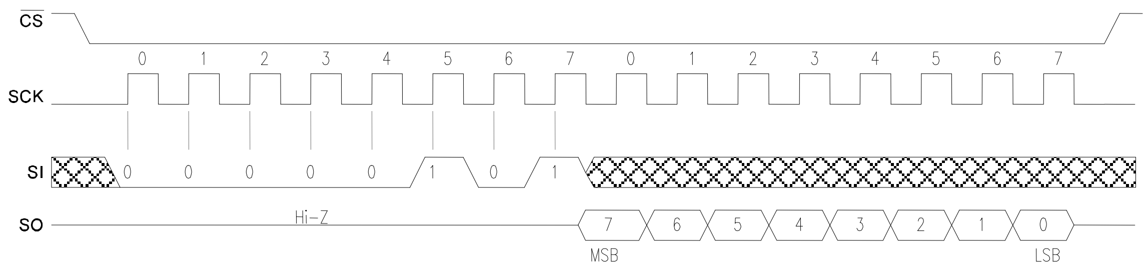


Figure 7. RDSR Bus Configuration

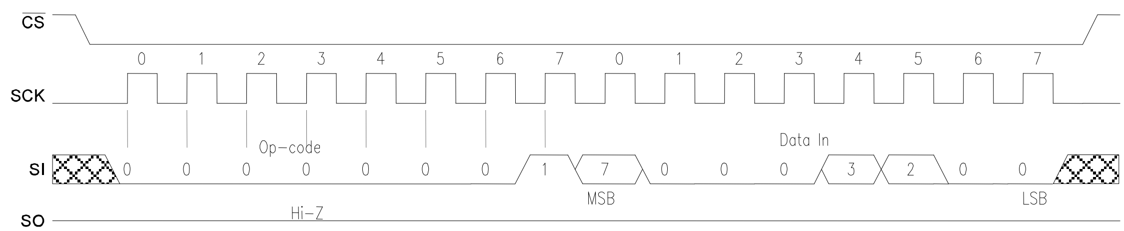


Figure 8. WRSR Bus Configuration (WREN not shown)

Status Register & Write Protection

The write protection features of the FM25L16B are multi-tiered. First, a WREN op-code must be issued prior to any write operation. Assuming that writes are enabled using WREN, writes to memory are controlled by the Status Register. As described above, writes to the status register are performed using the WRSR command and subject to the /WP pin. The Status Register is organized as follows.

Table 2. Status Register

Bit	7	6	5	4	3	2	1	0
Name	WPEN	0	0	0	BP1	BP0	WEL	0

Bits 0 and 4-6 are fixed at 0 and cannot be modified. Note that bit 0 (Ready in EEPROMs) is unnecessary as the F-RAM writes in real-time and is never busy. The WPEN, BP1 and BP0 control write protection features. They are nonvolatile (shaded yellow). The WEL flag indicates the state of the Write Enable Latch. Attempting to directly write the WEL bit in the status register has no effect on its state. This bit is internally set and cleared via the WREN and WRDI commands, respectively.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write protected as shown in the following table.

Table 3. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	600h to 7FFh (upper ¼)
1	0	400h to 7FFh (upper ½)
1	1	000h to 7FFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The WPEN bit controls the effect of the hardware /WP pin. When WPEN is low, the /WP pin is ignored. When WPEN is high, the /WP pin controls write access to the status register. Thus the Status Register is write protected if WPEN=1 and /WP=0.

This scheme provides a write protection mechanism, which can prevent software from writing the memory under any circumstances. This occurs if the BP1 and BP0 are set to 1, the WPEN bit is set to 1, and /WP is set to 0. This occurs because the block protect bits prevent writing memory and the /WP signal in hardware prevents altering the block protect bits (if WPEN is high). Therefore in this condition, hardware must be involved in allowing a write operation. The following table summarizes the write protection conditions.

Table 4. Write Protection

WEL	WPEN	/WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

Memory Operation

The SPI interface, which is capable of a relatively high clock frequency, highlights the fast write capability of the F-RAM technology. Unlike SPI-bus EEPROMs, the FM25L16B can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

Write Operation

All writes to the memory array begin with a WREN op-code. The next op-code is the WRITE instruction. This op-code is followed by a two-byte address value. The upper 5-bits of the address are ignored. In total, the 11-bits specify the address of the first data byte of the write operation. Subsequent bytes are data and they are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 7FFh is reached, the counter will roll over to 000h. Data is written MSB first. A write operation is shown in Figure 9.

Unlike EEPROMs, any number of bytes can be written sequentially and each byte is written to memory immediately after it is clocked in (after the 8^{th} clock). The rising edge of /CS terminates a WRITE op-code operation.

Read Operation

After the falling edge of /CS, the bus master can issue a READ op-code. Following this instruction is a two-byte address value. The upper 5-bits of the address are ignored. In total, the 11-bits specify the address of the first byte of the read operation. After the op-code and address are complete, the SI line is ignored. The bus master issues 8 clocks, with one bit read out for each. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 7FFh is reached, the counter will roll over to 000h. Data is read MSB first. The rising edge of /CS terminates a READ op-code operation. A read operation is shown in Figure 10.

Hold

The /HOLD pin can be used to interrupt a serial operation without aborting it. If the bus master pulls the /HOLD pin low while SCK is low, the current operation will pause. Taking the /HOLD pin high while SCK is low will resume an operation. The transitions of /HOLD must occur while SCK is low, but the SCK pin can toggle during a hold state.

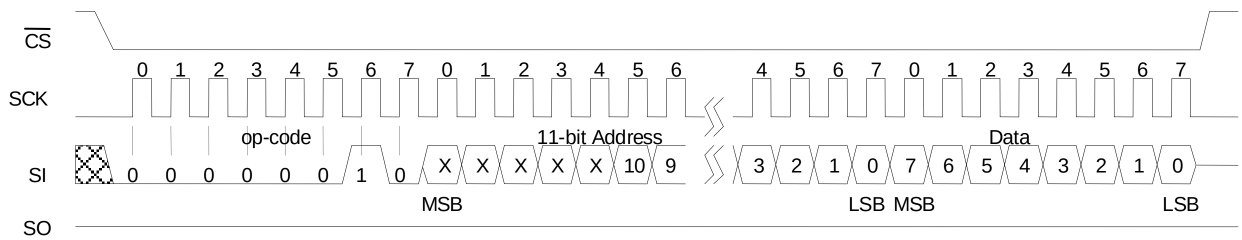


Figure 9. Memory Write (WREN not shown)

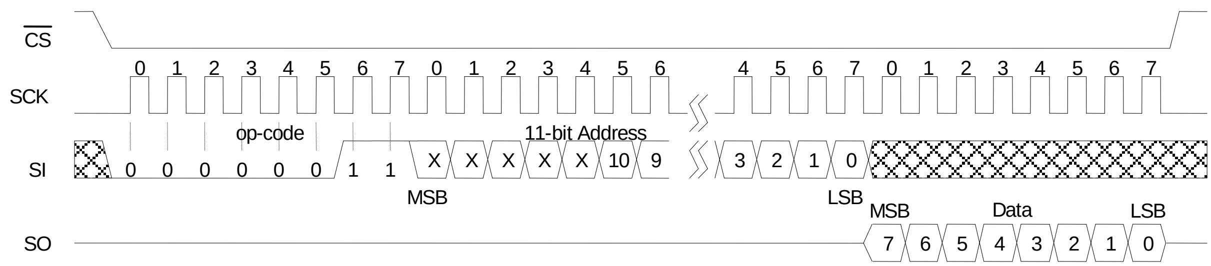


Figure 10. Memory Read

Endurance

The FM25L16B devices are capable of being accessed at least 10^{14} times, reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis for each access (read or write) to the memory array. The F-RAM architecture is based on an array of rows and columns. Rows are defined by A10-A3 and column addresses by A2-A0. See Block Diagram (pg 2) which shows the array as 256 rows of 64-bits each. The entire row is internally accessed once whether a single byte or all eight bytes are read or written. Each byte in the row is counted only once in an endurance calculation. The table below shows endurance calculations for 64-byte repeating loop, which includes an op-code, a starting address, and a sequential 64-byte data stream. This causes each byte to experience one endurance cycle through the loop. F-RAM read and write endurance is virtually unlimited even at 20MHz clock rate.

Table 5. Time to Reach Endurance Limit for Repeating 64-byte Loop

SCK Freq (MHz)	Endurance Cycles/sec.	Endurance Cycles/year	Years to Reach Limit
20	37,310	1.18×10^{12}	85.1
10	18,660	5.88×10^{11}	170.2
5	9,330	2.94×10^{11}	340.3

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +5.0V
V_{IN}	Voltage on any pin with respect to V_{SS}	-1.0V to +5.0V and $V_{IN} < V_{DD}$+1.0V
T_{STG}	Storage Temperature	-55°C to + 125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	260° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (AEC-Q100-002 Rev. E) - Charged Device Model (AEC-Q100-011 Rev. B) - Machine Model (AEC-Q100-003 Rev. E)	 4kV 1.25kV 300V
	Package Moisture Sensitivity Level	MSL-1

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply Voltage	2.7	3.3	3.6	V	
I_{DD}	VDD Supply Current @ SCK = 1.0 MHz @ SCK = 20.0 MHz			 0.2 3.0	 mA mA	1
I_{SB}	Standby Current	-	3	6	µA	2
I_{LI}	Input Leakage Current	-		±1	µA	3
I_{LO}	Output Leakage Current	-		±1	µA	3
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	-0.3		0.3 V_{DD}	V	
V_{OH}	Output High Voltage @ I_{OH} = -2 mA	V_{DD} – 0.8		-	V	
V_{OL}	Output Low Voltage @ I_{OL} = 2 mA	-		0.4	V	
V_{HYS}	Input Hysteresis	0.05 V_{DD}		-	V	4

Notes

1. SCK toggling between V_{DD}-0.3V and V_{SS}, other inputs V_{SS} or V_{DD}-0.3V.
2. SCK = SI = /CS=V_{DD}. All inputs V_{SS} or V_{DD}.
3. $V_{SS} \leq V_{IN} \leq V_{DD}$ and $V_{SS} \leq V_{OUT} \leq V_{DD}$.
4. Characterized but not 100% tested in production. Applies only to /CS and SCK pins.

AC Parameters (T_A = -40° C to + 85° C, C_L = 30pF, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
f_{CK}	SCK Clock Frequency	0	20	MHz	
t_{CH}	Clock High Time	22		ns	1
t_{CL}	Clock Low Time	22		ns	1
t_{CSU}	Chip Select Setup	10		ns	
t_{CSH}	Chip Select Hold	10		ns	
t_{OD}	Output Disable Time		20	ns	2
t_{ODV}	Output Data Valid Time		20	ns	
t_{OH}	Output Hold Time	0		ns	
t_D	Deselect Time	60		ns	
t_R	Data In Rise Time		50	ns	2,3
t_F	Data In Fall Time		50	ns	2,3
t_{SU}	Data Setup Time	5		ns	
t_H	Data Hold Time	5		ns	
t_{HS}	/HOLD Setup Time	10		ns	
t_{HH}	/HOLD Hold Time	10		ns	
t_{HZ}	/HOLD Low to Hi-Z		20	ns	2
t_{LZ}	/HOLD High to Data Active		20	ns	2

Notes

1. $t_{CH} + t_{CL} = 1/f_{CK}$.
2. Characterized but not 100% tested in production.
3. Rise and fall times measured between 10% and 90% of waveform.

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 3.3V)

Symbol	Parameter	Min	Max	Units	Notes
C_O	Output Capacitance (SO)	-	8	pF	1
C_I	Input Capacitance	-	6	pF	1

Notes

1. This parameter is periodically sampled and not 100% tested.
2. Slope measured at any point on V_{DD} waveform.

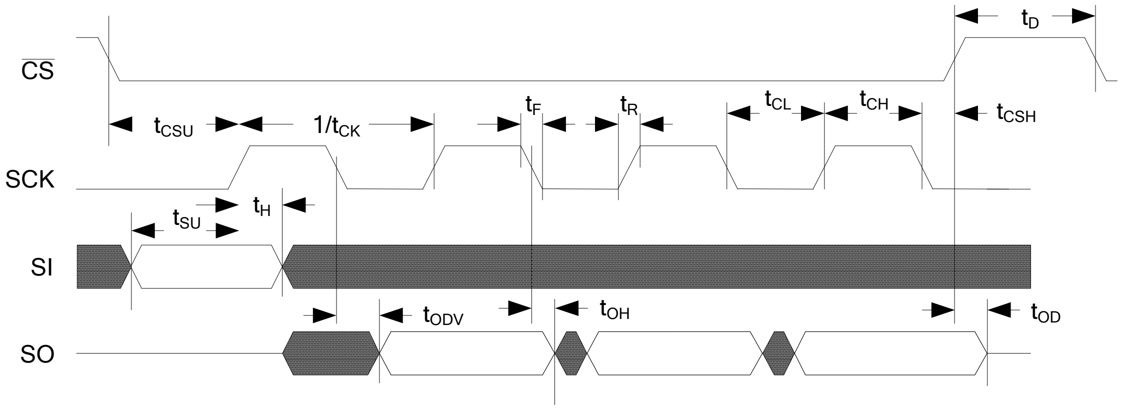
AC Test Conditions

Input Pulse Levels	10% and 90% of V_{DD}
Input rise and fall times	5 ns
Input and output timing levels	0.5 V_{DD}
Output Load Capacitance	30 pF

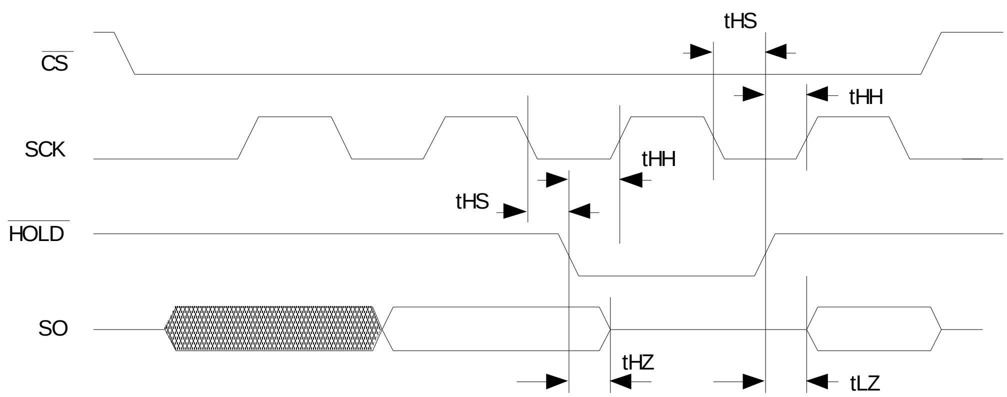
Data Retention

Symbol	Parameter	Min	Max	Units	Notes
T_{DR}	@ +85ºC	10	-	Years	
	@ +80ºC	19	-	Years	
	@ +75ºC	38	-	Years	

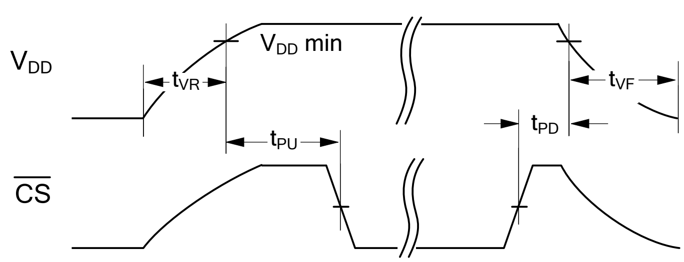
Serial Data Bus Timing



/Hold Timing



Power Cycle Timing



Power Cycle Timing (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

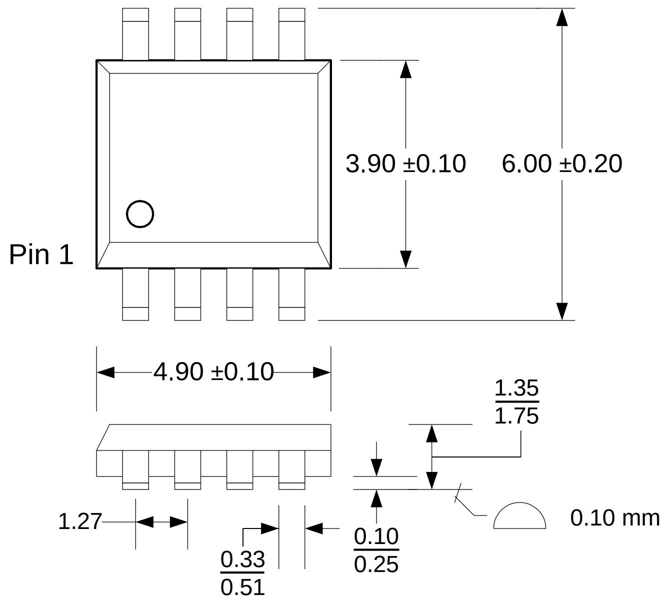
Symbol	Parameter	Min	Max	Units	Notes
t_{PU}	V_{DD}(min) to First Access Start	1	-	ms	
t_{PD}	Last Access Complete to V_{DD}(min)	0	-	µs	
t_{VR}	V_{DD} Rise Time	30	-	µs/V	1
t_{VF}	V_{DD} Fall Time	30	-	µs/V	1

Notes

1. Slope measured at any point on V_{DD} waveform.

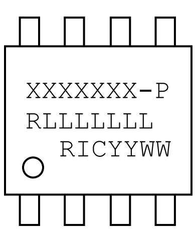
Mechanical Drawing

8-pin SOIC (JEDEC Standard MS-012, variation AA)



Refer to JEDEC MS-012 for complete dimensions and notes.
All dimensions in millimeters.

SOIC Package Marking Scheme

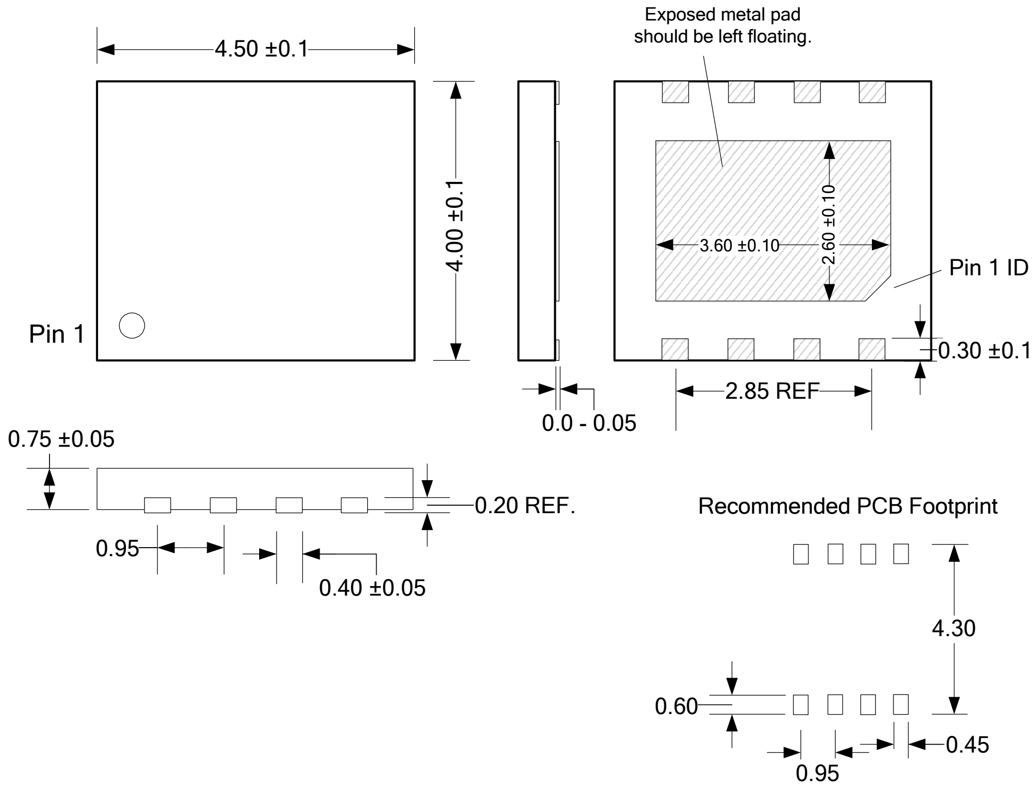


Legend:
XXXXXX= part number, P= package type (G=SOIC)
R=rev code, LLLLLLL= lot code
RIC=Ramtron Int'l Corp, YY=year, WW=work week

Example: FM25L16B, "Green" SOIC package, Year 2010, Work Week 47

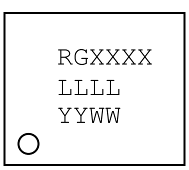
FM25L16B-G
A00002G1
RIC1047

8-pin TDFN (4.0mm x 4.5mm body, 0.95mm pitch)



Note: All dimensions in <u>millimeters</u>. **The exposed pad should be left floating.**

TDFN Package Marking Scheme for Body Size 4.0mm x 4.5mm



Legend:
R=Ramtron, G="green" TDFN package, XXXX=base part number
LLLL= lot code
YY=year, WW=work week

Example: "Green"/RoHS TDFN package, FM25L16B, Lot 0003,
Year 2011, Work Week 07

```
R5L16B
0003
1107
```

Revision History

Revision	Date	Summary
1.0	11/10/2010	Initial Release
1.1	12/15/2010	Added 4x4.5mm DFN package. Fixed endurance section on pg 8.
1.2	2/15/2011	Updated DFN package marking. Changed t_{PU} and t_{VF} spec limits.
1.3	3/22/2011	Added ESD ratings.
3.0	1/6/2012	Changed to Production status. Changed t_{VF} spec.

Errata

All errata for this product are fixed effective date code 1148 (YY=11, WW=48). For more information refer to datasheet 001-84485 Rev. *B or contact Cypress Technical Support at http://www.cypress.com/support.

Document History

Document Title: FM25L16B 16Kb Serial 3V F-RAM Memory
Document Number: 001-84485

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3902952	GVCH	02/25/2013	New Spec
*A	3924523	GVCH	03/07/2013	Changed t_{PU} spec value from 10ms to 1ms
*B	3994285	GVCH	05/14/2013	Added Appendix A - Errata for FM25L16B
*C	4045438	GVCH	06/30/2013	All errata items are fixed and the errata is removed.

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