dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Family Silicon Errata and Data Sheet Clarification

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family devices that you have received conform functionally to the current Device Data Sheet (DS70657**H**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The current silicon revision levels are:

PIC24EP32/dsPIC33EP32: **A3**
PIC24EP64/dsPIC33EP64: **A3**
PIC24EP128/dsPIC33EP128: **A3**
PIC24EP256/dsPIC33EP256: **A3**
PIC24EP512/dsPIC33EP512: **A7**

"N/A" indicates that the device family is not released, or that the particular silicon issue does not apply to this family.

Data Sheet clarifications and corrections start on Page 21, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID[1]	Silicon Revision/Device ID[2]	
PIC24EP32GP202	0x1C19	—	A3 0x4003
PIC24EP32GP203	0x1C1A		
PIC24EP32GP204	0x1C18		
dsPIC33EP32GP502	0x1C0D		
dsPIC33EP32GP503	0x1C0E		
dsPIC33EP32GP504	0x1C0C		
PIC24EP32MC202	0x1C11		
PIC24EP32MC203	0x1C12		
PIC24EP32MC204	0x1C10		
dsPIC33EP32MC202	0x1C01		
dsPIC33EP32MC203	0x1C02		
dsPIC33EP32MC204	0x1C00		
dsPIC33EP32MC502	0x1C05		
dsPIC33EP32MC503	0x1C06		
dsPIC33EP32MC504	0x1C04		
dsPIC33EP32MC506	0x1D27		
PIC24EP64GP202	0x1D39	A2 0x4002	A3 0x4003
PIC24EP64GP203	0x1D3A		
PIC24EP64GP204	0x1D38		
PIC24EP64GP206	0x1D3B		
dsPIC33EP64GP502	0x1D2D		
dsPIC33EP64GP503	0x1D2E		
dsPIC33EP64GP504	0x1D2C		
dsPIC33EP64GP506	0x1D2F		
PIC24EP64MC202	0x1D31		
PIC24EP64MC203	0x1D32		
PIC24EP64MC204	0x1D30		
PIC24EP64MC206	0x1D33		
dsPIC33EP64MC202	0x1D21		
dsPIC33EP64MC203	0x1D22		
dsPIC33EP64MC204	0x1D20		
dsPIC33EP64MC206	0x1D23		
dsPIC33EP64MC502	0x1D25		
dsPIC33EP64MC503	0x1D26		
dsPIC33EP64MC504	0x1D24		
dsPIC33EP64MC506	0x1D27		

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70663) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID[1]	Silicon Revision/Device ID[2]	
PIC24EP128GP202	0x1E59	—	A3 0x4003
PIC24EP128GP204	0x1E58		
PIC24EP128GP206	0x1E5B		
dsPIC33EP128GP502	0x1E4D		
dsPIC33EP128GP504	0x1E4C		
dsPIC33EP128GP506	0x1E4F		
PIC24EP128MC202	0x1E51		
PIC24EP128MC204	0x1E50		
PIC24EP128MC206	0x1E53		
dsPIC33EP128MC202	0x1E41		
dsPIC33EP128MC204	0x1E40		
dsPIC33EP128MC206	0x1E43		
dsPIC33EP128MC502	0x1E45		
dsPIC33EP128MC504	0x1E44		
dsPIC33EP128MC506	0x1E47		
PIC24EP256GP202	0x1F79	—	A3 0x4003
PIC24EP256GP204	0x1F78		
PIC24EP256GP206	0x1F7B		
dsPIC33EP256GP502	0x1F6D		
dsPIC33EP256GP504	0x1F6C		
dsPIC33EP256GP506	0x1F6F		
PIC24EP256MC202	0x1F71		
PIC24EP256MC204	0x1F70		
PIC24EP256MC206	0x1F73		
dsPIC33EP256MC202	0x1F61		
dsPIC33EP256MC204	0x1F60		
dsPIC33EP256MC206	0x1F63		
dsPIC33EP256MC502	0x1F65		
dsPIC33EP256MC504	0x1F64		
dsPIC33EP256MC506	0x1F67		

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70663) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Silicon Revision/Device ID(2)	
PIC24EP512GP202	0x1799	—	A7 0x4007
PIC24EP512GP204	0x1798		
PIC24EP512GP206	0x179B		
dsPIC33EP512GP502	0x178D		
dsPIC33EP512GP504	0x178C		
dsPIC33EP512GP506	0x178F		
PIC24EP512MC202	0x1791		
PIC24EP512MC204	0x1790		
PIC24EP512MC206	0x1793		
dsPIC33EP512MC202	0x1781		
dsPIC33EP512MC204	0x1780		
dsPIC33EP512MC206	0x1783		
dsPIC33EP512MC502	0x1785		
dsPIC33EP512MC504	0x1784		
dsPIC33EP512MC506	0x1787		

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70663) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary
CPU	div.sd	1.	When using the div.sd instruction, the overflow bit is not getting set when an overflow occurs.
CPU	DO Loop	2.	PSV access, including Table Reads or Writes in the last instruction of a DO loop, is not allowed.
SPI	Frame Sync Pulse	3.	Frame Sync pulse is not generated in Master mode when FRMPOL = 0.
SPI	Frame Sync Pulse	4.	When in SPI Slave mode, with the Frame Sync pulse set as an input, FRMDLY must be set to '0'.
UART	TX Interrupt	5.	A Transmit (TX) interrupt may occur before the data transmission is complete.
Power System	Flash Regulator	6.	The VREGSF (RCON<11>) bit always reads back as '0'.
ADC	DONE bit	7.	The ADC Conversion Status bit (DONE) does not work when an external interrupt is selected as the ADC trigger source.
PTG	Strobe Output	8.	Strobe output pulse width is incorrectly dependent on the PTGPWD<3:0> (PTGCON<7:4>) bit settings.
Op Amp	Enabling Op Amp mode	9.	When using any of these Op Amp modules or Analog Channels AN0, AN3 or AN6, to sample external signals, bit 11 of the CMxCON register must be set to '1'.
Op Amp	AC/DC Electrical Characteristics	10.	The AC/DC electrical characteristics for the op amp module (and the related ADC specifications) are not within the specifications published in the current data sheet.
PWM	Dead-Time Compensation	11.	Dead-Time Compensation is not enabled for Center-Aligned PWM mode.
Flash	Flash Programming	12.	The stall mechanism may not function properly when erasing or programming Flash memory.
QEI	Index Counter	13.	The QEI Index Counter does not count correctly in Quadrature Detector mode.
QEI	Modulo Mode	14.	Modulo mode functionality is incorrect when the count polarity bit is set.
PWM	Master Time Base Mode	15.	In Master Time Base mode, writing to the Period register, and any other timing parameter of the PWMx module, will cause the update of the other timing parameter to take effect one PWM cycle after the period update is effective.
ADC	1.1 Msps Sampling	16.	Selecting the same ANx input (AN0 or AN3) for CH0 and CH1 to achieve a 1.1 Msps sampling rate results in erroneous readings for CH1.
ADC	Channel Scan	17.	Channel scanning is limited to AN0 through AN15.
Output Compare	Interrupt	18.	Under certain circumstances, an output compare match may cause the Output Compare Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin.
ECAN™	DMA	19.	Write collisions on a DMA-enabled ECAN™ module do not generate DMAC error traps.
PWM	Immediate Update	20.	Dead time is not asserted when PDCx is updated to cause an immediate transition on the PWMxH and PWMxL outputs.
PWM	Center-Aligned Mode	21.	PWMxH is asserted for 100% of the PWM period in Complementary mode under certain circumstances.
PWM	Complementary Mode	22.	With dead time greater than zero, 0% and 100% duty cycle cannot be obtained on PWMxL and PWMxH outputs.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary
CPU	Program Memory	23.	Address error trap may occur while accessing certain program memory locations.
PWM	Center-Aligned Mode	24.	Updates to active MDC/PDCx/ALTDTRx/PHASEx registers occur only once every two PWM periods.
PWM	Independent Time Base Mode	25.	Under certain circumstances, updates to the OVRENH and OVRENL bits may be ignored by the PWMx module.
PWM	Center-Aligned Mode	26.	PHASEx register updates are delayed.
CTMU	A/D Operation	27.	CTMU does not work with the A/D Converter in 12-bit mode.
Input Capture	External Synchronization	28.	Input Capture and Output Compare modules cannot be synchronized.
JTAG	I/O	29.	$\overline{\text{MCLR}}$ pin operation may be disabled.
I/O	Pin Functions that are Not 5V Tolerant	30.	Select pins are not 5V tolerant.
JTAG	I/O	31.	Active-high logic pulse on the I/O pin with TMS function at POR.
QEI	Velocity Counter	32.	Under certain circumstances, the Velocity Counter Register 1 (VEL1CNT) misses count pulses.
QEI	Position Capture	33.	Under certain conditions, the captured position may be off by ±1 count.
QEI	Position Capture	34.	Position count captured at the rising edge of the HOME signal and not the INDEX signal.
PWM	Center-Aligned Mode	35.	Under certain conditions, PWMxH and PWMxL are deasserted.
PWM	Current Reset Mode	36.	When the PWMx generator is configured to operate in Current Reset mode, the PWM Reset will only happen in every alternate PWM cycle.
Op Amp/Comparator	External Reference	37.	Op Amp/Comparator voltage reference fails when the voltage on V_{REF+} is less than 1.33V.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

1. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

2. Module: CPU

Table Write (`TBLWTL`, `TBLWTH`) instructions cannot be the first or last instruction of a `DO` loop.

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

3. Module: SPI

When using the Frame Sync pulse output feature (FRMEN bit (SPIxCON2<15>) = 1), in Master mode (SPIFSD bit (SPIxCON2<14>) = 0), the Frame Sync pulse is not being generated with an active-low pulse (FRMPOL bit (SPIxCON2<13>) = 0).

Work around

The $\overline{SSx}$ pin is used as the Frame Sync pulse when the Frame Sync pulse output feature is used. Mapping the $\overline{SSx}$ input function and output function to the same pad, by using the Peripheral Pin Select (PPS) feature, resolves this issue.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

4. Module: SPI

When in SPI Slave mode (MSTEN bit (SPIxCON1<5>) = 0) and using the Frame Sync pulse output feature (FRMEN bit (SPIxCON2<15>) = 1) in Slave mode (SPIFSD bit (SPIxCON2<14>) = 1), the Frame Sync Pulse Edge Select bit must be set to '0' (FRMDLY bit (SPIxCON2<1>) = 0).

Work around

There is no work around. The Frame Sync Pulse Edge Select bit, FRMDLY, cannot be set to produce a Frame Sync pulse that coincides with the first bit clock.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

5. Module: UART

When using the UTXISEL<1:0> bits = 01 (interrupt when last character is shifted out of the Transmit Shift Register) and the final character is being shifted out through the Transmit Shift Register (TSR), the Transmit (TX) interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occurs only when all transmit operations are complete, hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

6. Module: Power System

The VREGSF bit functions as documented, but will always read back as '0'. Because of the Read-Modify-Write process, any BSET or BCLR instruction of the RCON register will also write a '0' to the VREGSF bit.

Work around

If the VREGSF bit is intended to be set to '1', the user software must also write a '1' to the VREGSF bit when setting or clearing any other bit in the RCON register.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

7. Module: ADC

The ADC Conversion Status (DONE) bit (AD1CON1<0>) does not indicate completion of the conversion when an external interrupt is selected as the ADC trigger source (SSRC<2:0> bits (AD1CON1<7:5>) = 0x1).

Work around

Use an ADC interrupt or poll the ADxIF bit in the IFSx registers to determine the completion of conversion.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

8. Module: PTG

When using the strobe output step commands (PTGCTRL 0b1110, PTGCTRL 0b1100 and PTGCTRL 0b1101) to write to the AD1CHS0 register, the PTGPWD<3:0> bits (PTGCON<7:4>) determine the number of times the PTG module will write to the AD1CHS0 register.

Work around

Set the PTGPWD<3:0> bits to '0000' so that the PTG module does not write to the AD1CHS0 register multiple times.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

9. Module: Op Amp

When using any of these Op Amp modules, or Analog Channels AN0, AN3 or AN6 to sample external signals, bit 11 of the CMxCON register must be set to '1'.

If Using This Feature:	These conditions must be met:	
	OPMODE (CMxCON<10>)	CMxCON<11>
AN0	CM2CON.OPMODE = 0	CM2CON<11> = 1
AN3	CM1CON.OPMODE = 0	CM1CON<11> = 1
AN6	CM3CON.OPMODE = 0	CM3CON<11> = 1
Op Amp 1	CM1CON.OPMODE = 1	CM1CON<11> = 1
Op Amp 2	CM2CON.OPMODE = 1	CM2CON<11> = 1
Op Amp 3	CM3CON.OPMODE = 1	CM3CON<11> = 1

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	—
PIC24EP64/dsPIC33EP64 devices	**A2**
PIC24EP128/dsPIC33EP128 devices	—
PIC24EP256/dsPIC33EP256 devices	—
PIC24EP512/dsPIC33EP512 devices	—

10. Module: Op Amp

The AC/DC electrical characteristics for the Op Amp module (and the related ADC module specifications) differ from the specifications in the published data sheet. Refer to Table 3 and Table 4 (below) for the A2 revision silicon specifications.

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	—
PIC24EP64/dsPIC33EP64 devices	**A2**
PIC24EP128/dsPIC33EP128 devices	—
PIC24EP256/dsPIC33EP256 devices	—
PIC24EP512/dsPIC33EP512 devices	—

TABLE 3: AC/DC CHARACTERISTICS: OP AMP

Param. No.	Symbol	Minimum	Typical	Maximum	Units	Conditions
CM21a	PM	—	40	—	Degree	
CM21b	PM	—	30	—	Degree	
CM23a	GBW	—	7	—	MHz	
CM23b	GBW	—	2	—	MHz	
CM49a	VOADC	AVSS + 0.350 AVSS + 0.500	— —	AVDD – 0.350 AVDD – 0.500	V V	IOUT = 390 µA, Op Amp 1 and 2 IOUT = 390 µA, Op Amp 3
CM49b	VOUT	AVSS + 0.375 AVSS + 0.525	— —	AVDD – 0.375 AVDD – 0.525	V V	IOUT = 390 µA, Op Amp 1 and 2 IOUT = 390 µA, Op Amp 3
CM51a	RINT1	351	468	613	Ω	

TABLE 4: AC/DC CHARACTERISTICS: ADC

Parameter No.	Symbol	Minimum	Typical	Maximum	Units	Conditions
AD57b	TSAMP	5 TAD	—	—	—	Op Amp 1 and 2, 12-bit mode, Configuration B
		5 TAD	—	—	—	Op Amp 3, 10-bit mode, Configuration B
		7 TAD	—	—	—	Op Amp 3, 12-bit mode, Configuration B

11. Module: PWM

When dead-time compensation is enabled (DTC<1:0> (PWMCONx<7:6>) = 11) in Center-Aligned mode (CAM (PWMCONx<2>) = 1), the dead time, as specified in the ALTDTRx register, is not being applied to the PWMxH output. The leading and trailing edges of the PWMxL output are extended by one-half the value of the ALTDTRx register, but the PWMxH leading and trailing edges are unaffected.

Work around

Using the values from the *"dsPIC33E/PIC24E Family Reference Manual"*, **"High-Speed PWM"** (DS70645), adjust the PWMx parameters as follows:

- Subtract one-half of the ALTDTRx dead time from PDCx
- Use twice the value for ALTDTRx. For example:
  - Frequency of 60 kHz, duty cycle of 50%
  - Desired dead time of 833 ns and dead-time compensation of 833 ns

Using the specified values from **"High-Speed PWM"** (DS70645):

- PHASEx = 1000
- PDCx = 500
- ALTDTRx = 833 ns/8.33 ns = 100
- DTRx = (833 ns/8.33 ns)/2 = 50

Applying the work around:

- ALTDTRx = 2 * 100 = 200
- PDCx = PDCx – 25 = 475

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

12. Module: Flash

The stall mechanism may not function properly when erasing or programming Flash memory.

Work around

Disable interrupts until the erase or programming operation is complete. Test for completion by inserting a bit test operation of the Write Control (WR) bit.

Code is provided in Example 1 that can be used to disable interrupts during RTSP erase/program operations.

EXAMPLE 1: WORK AROUND CODE

```
; Load write latches if programming
    …
; Setup NVMCON register to erase or program
    as required
        …
; Disable interrupts
    PUSH    SR
    MOV     #0x00E0, W0
    IOR     SR
; Write the KEY sequence
    MOV     #0x55, W0
    MOV     W0, NVMKEY
    MOV     #0xAA, W0
    MOV     W0, NVMKEY
; Start the programming sequence
    BSET    NVMCON, #15
; Insert two NOPs after programming
    NOP
    NOP
; Wait for operation to complete
prog_wait:
    BTSC    NVMCON, #15
    BRA     prog_wait
; Re-enable interrupts,
    POP     SR
```

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

13. Module: QEI

In Quadrature Encoder mode (CCM<1:0> (QEI1CON<1:0>) = 00), the Index Counter registers (INDX1CNTH and INDX1CNTL) cannot be relied upon to increment when the last known direction was positive and an index pulse occurs. The Index Counter registers can decrement even if the last known direction was positive. This does not apply to External Clock or Internal Timer QEI modes.

Work around

The index event can be used to implement a software counter. The direction could be determined by comparing the current POS1CNT value to that of the previous index event.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

14. Module: QEI

When Modulo Count mode (Mode 6) is selected for the position counter (PIMOD<2:0> (QEI1CON<12:10>) = 110) and the counter direction is set to negative (CNTPOL (QEI1CON<3>) = 1), the functions of the QEI1LEC and QEI1GEC registers are reversed.

Work around

When using Modulo Count mode in conjunction with a negative count direction (polarity), use the QEI1LEC register as the upper count limit and the QEI1GEC as the lower count limit.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

15. Module: PWM

The PWMx module can operate with variable period, duty cycle, dead-time and phase values. The master period and other timing parameters can be updated in the same PWM cycle. With immediate updates disabled, the new values should take effect at the start of the next PWM cycle.

As a result of this issue, the updated master period takes effect on the next PWM cycle, while the update of the additional timing parameter is delayed by one PWM cycle. The parameters affected by this erratum are as follows:

PWMx Primary Master Time Base Period Registers – update is effective on the next PWM cycle (PTPER).

Additional PWM timing parameters: update is effective one PWM cycle after the master period update:

- Duty Cycle – PDCx and MDC registers
- Phase – PHASEx register
- Dead Time – DTRx and ALTDTRx registers and dead-time compensation signals
- Clearing of current-limit and Fault conditions, and application of External Period Reset signal

Work around

If the application requires the master period and other parameters to be updated at the same time, enable both immediate updates:

- EIPU (PTCON<10>) = 1 – to enable immediate period updates
- IUE (PWMCONx<0>) = 1 – to enable immediate updates of additional parameters listed above

Enabling immediate updates will allow updates to the master period and other parameters to take effect immediately after writing to the respective registers.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

16. Module: ADC

Selecting the same ANx input (AN0 or AN3) for CH0 and CH1 to achieve a 1.1 Msps sampling rate results in erroneous readings for CH1.

Work around

Bring the analog signal into the device using both AN0 and AN3, connect externally, and then assign one input to CH0 and the other to CH1.

If selecting AN0 on CH1 (CH123Sx = 0), select AN3 on CH0 (CH0Sx = 3). Conversely, if selecting AN3 on CH1 (CH123Sx = 1), select AN0 on CH0 (CH0Sx = 0).

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

17. Module: ADC

Selection of channels for channel scan operation is limited to those available in the AD1CSSL register (AN0 through AN15). Selections in the AD1CSSH register (OA1 through OA3, CTMU TEMP and CTMU Open) are not available.

Work around

There is no work around of the CTMU TEMP and CTMU Open selections. OA1 through OA3 can be scanned using AN3, AN0 and AN6 for Op Amp 1, Op Amp 2 and Op Amp 3, respectively.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

18. Module: Output Compare

An output compare match may cause the Output Compare Interrupt Flag (OCxIF) to become set prior to the Change-of-State (COS) of the OCx pin. This has been observed when all of the following are true:

- The module is in One-Shot mode (OCM<2:0> = 001, 010 or 100);
- One of the timer modules is being used as the time base; and
- A timer prescaler other than 1:1 is selected

If the module is re-initialized by clearing OCM<2:0> after the One-Shot compare, the OCx pin may not be driven as expected.

Work around

After OCxIF is set, allow an interval (in CPU cycles) of at least twice the prescaler factor to elapse before clearing OCM<2:0>. For example, for a prescaler value of 1:8, allow 16 CPU cycles to elapse after the interrupt.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

19. Module: ECAN™

When DMA is used with the ECAN module, and the CPU and DMA write to an ECAN Special Function Register (SFR) at the same time, the DMAC error trap is not occurring. In addition, neither the PWCOL<3:0> bits of the DMAPWC SFR or the DMACERR bit of the INTCON1 SFR are being set. Since the PWCOLx bits are not set, subsequent DMA requests to that channel are not ignored.

Work around

There is no work around; however, under normal circumstances, this situation should not arise. When DMA is used with the ECAN module, the application should not be writing to the ECAN SFRs.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

20. Module: PWM

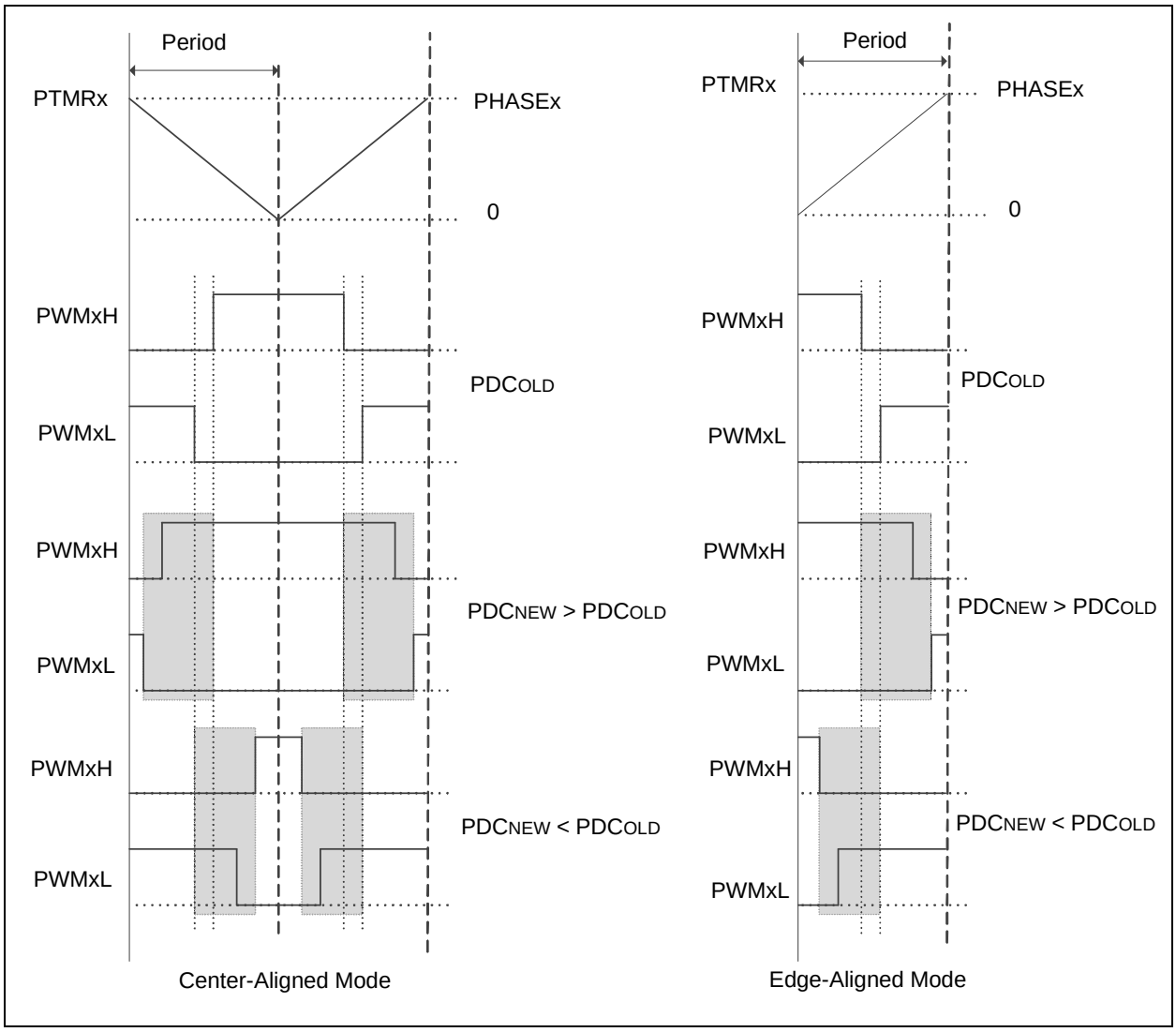
The PWMx generator may not assert dead time on the edges of transitions. This has been observed when all of the following conditions are present:

- The PWMx generator is configured to operate in Complementary mode with the independent time base or master time base;
- Immediate update is enabled; and
- The value in the PDCx register is updated in such a manner that the PWMxH and PWMxL outputs make an immediate transition.

The current duty cycle, PDCOLD, newly calculated duty cycle, PDCNEW and the point at which the write to the Duty Cycle register occurs within the PWMx time base, will determine if the PWMxH and PWMxL outputs make an immediate transition. PWMxH and PWMxL outputs make an immediate transition if the Duty Cycle register is written with a new value, PDCNEW, at a point of time when the PWMx time base is counting a value that is in between PDCNEW and PDCOLD. Additionally, writing to the Duty Cycle register close to the instant of time where dead time is being applied may result in reduced dead time, effective on the PWMxH and PWMxL transition edges.

In Figure 1-1, if the duty cycle write occurred in the shaded box, then PWMxH and PWMxL will make an immediate transition without dead time.

FIGURE 1-1: TIMING DIAGRAMS FOR CENTER-ALIGNED AND EDGE-ALIGNED MODES



Work around

None.

However, in most applications the duty cycle update timing can be controlled using the TRIGx trigger or special event trigger such that the above mentioned conditions are avoided altogether.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

21. Module: PWM

In Center-Aligned Complementary mode in Independent Time Base mode, the PWMx generator may assert the PWMxH output for 100% of the duty cycle. This has been observed when the value in its PDCx register is less than one-half the value in its ALTDTRx register.

Work around

Include a software routine to check that the duty cycle value written to the PDCx register is always at least one-half of the value in ALTDTRx. Example 1-1 shows one way of doing this, with `PDCtemp` representing the value to be written to the PDCx register.

EXAMPLE 1-1: WORK AROUND CODE

```
Altdtr_by2 = ALTDTRx / 2;
if (PDCtemp < Altdtr_by2)
{
    PDCx = Altdtr_by2;
}
else
{
    PDCx = PDCtemp;
}
```

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	—

22. Module: PWM

This issue is applicable when a PWMx generator is configured to operate in Independent Time Base mode with either Center-Aligned Complementary mode or Edge-Aligned Complementary mode. When dead time is non-zero, PWMxL is not asserted for 100% of the time when PDCx is zero. Similarly, when dead time is non-zero, PWMxH is not asserted for 100% of the time when PDCx is equal to PHASEx. This issue applies to Master Time Base mode as well.

Work around

In Center-Aligned mode:

- To obtain 0% duty cycle, first zero out the ALTDTRx register, then write zero to the PDCx register.
- To obtain 100% duty cycle, first zero out the ALTDTRx register, then write (PHASEx + 2) to the PDCx register.

In Edge-Aligned mode:

- To obtain 0% duty cycle, first zero out the registers, DTRx and ALTDTRx, then write zero to the PDCx register.
- To obtain 100% duty cycle, first zero out the registers, DTRx and ALTDTRx, then write (PHASEx + 1) to the PDCx register.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

23. Module: CPU

An unexpected address error trap may occur during accesses to program memory addresses, 0x001 through 0x200. This has been observed when one or more interrupt requests are asserted while reading or writing program memory addresses using TBLRDx, TBLWTx or PSV-based instructions.

Work around

Before executing instructions that read or write program memory addresses, 0x001 through 0x200, disable interrupts using the DISI instruction.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

24. Module: PWM

In Center-Aligned mode, updates to active MDC/PDCx/ALTDTRx/PHASEx registers occur only once every two PWM periods; that is, when the PWMx timer matches the PHASEx register. In other words, the double update feature is not available. Figure 1-2 illustrates this relationship.

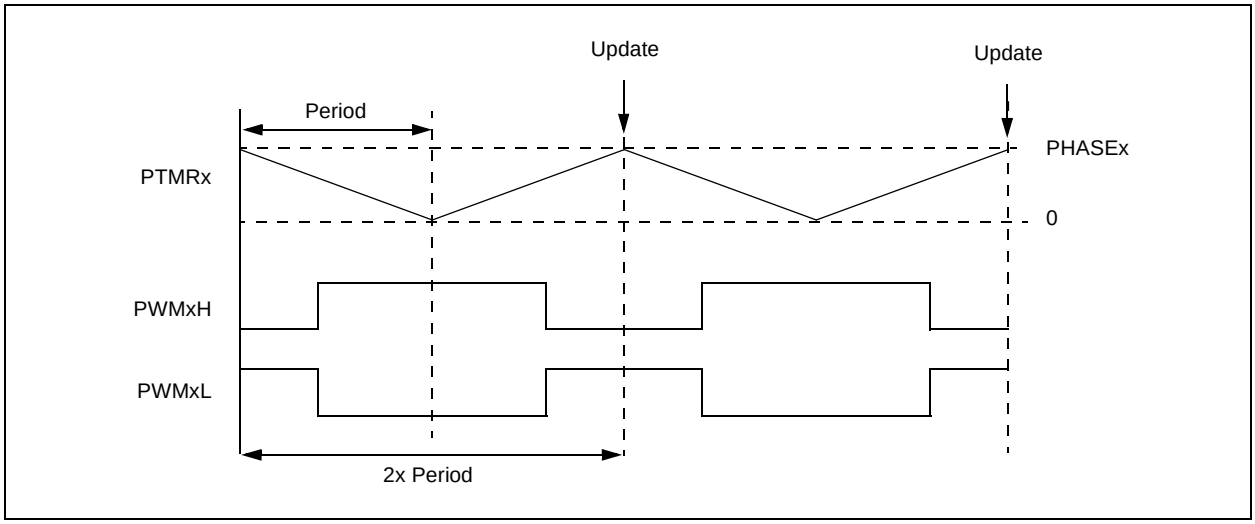
Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	—

FIGURE 1-2: TIMING DIAGRAM



25. Module: PWM

An update to the IOCONx register to turn off the override will be ignored by the PWMx module. The issue has been observed to occur when the IOCONx update to turn off the override occurs close to the time when dead time is being applied.

Work around

1. Turn off the PWMx dead time.
2. Alternatively, turn off the PWMx override with the following procedure:
   a) Disable the PWMx module (PTEN = 0)
   b) Clear the Override Enable bits (OVRENH = 0 and OVRENL = 0)
   c) Enable the PWMx module (PTEN = 1)

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

26. Module: PWM

In Center-Aligned Complimentary mode with Independent Time Base mode, updates to the PHASEx register take effect after a delay of two PWM periods.

This occurs only when the Immediate Update bit feature is disabled (IUE = 0). If the Immediate Update bit is enabled (IUE = 1), the PHASEx register updates will take effect immediately.

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

27. Module: CTMU

The CTMU cannot be used with the A/D Converter when the converter is operating in 12-bit mode.

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

28. Module: Input Capture

When an input capture module is selected as the Sync source for either an output compare module or another input capture module, synchronization may fail.

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

29. Module: JTAG

The $\overline{\text{MCLR}}$ pin (normally input only) may be set as an output pin through the JTAG interface. If it is set at an output high level, subsequent device Resets are prevented until the device is powered down.

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	—
PIC24EP64/dsPIC33EP64 devices	—
PIC24EP128/dsPIC33EP128 devices	—
PIC24EP256/dsPIC33EP256 devices	—
PIC24EP512/dsPIC33EP512 devices	—

30. Module: I/O

On all packages, pins with the following functions are not 5V tolerant:

- RC3
- RC4
- RC5
- RA9

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	—

31. Module: JTAG

At Power-on Reset (POR), when JTAG is disabled in the Configuration bits, the I/O pin with TMS function produces an active-high logic pulse with a pulse width in the order of milliseconds.

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	—

32. Module: QEI

The Velocity Counter (VEL1CNT) register is a 16-bit wide register that increments or decrements based on the signal from the quadrature decoder logic. Reading this register results in a Counter Reset. Typically, the user application should read the velocity counter at a rate of 1-4 kHz.

As a result of this issue, the velocity counter may miss a count if the user application reads the Velocity Counter register at the same time as a (+1 or -1) count increment occurs.

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

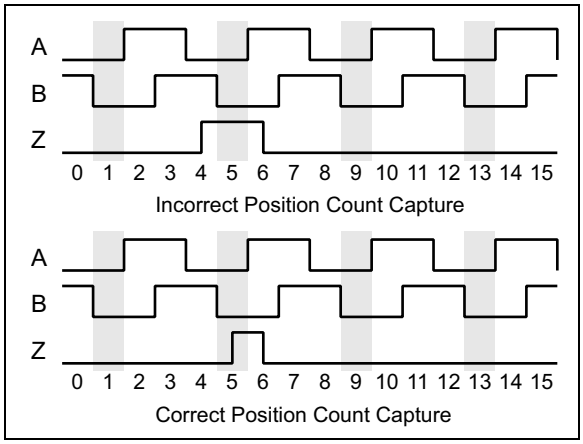
33. Module: QEI

When index count position capture is being used (QCAPEN (QEI1IOC<15> = 1), the position count may be one more or one less than the correct value, depending on the direction of the count.

This is only observed when the leading edge of the index pulse occurs prior to the leading edge of the index match state. When the index pulse starts after the leading edge of the index match state, the position count is captured correctly.

Figure 1-3 shows how this occurs. In these cases, Encoder Signals A, B and (index) Z are shown, with the module being configured for index match when A and B are '0'. The effects of a correct and incorrect capture are shown side by side (shaded area indicates the index match state); the position count is shown along the bottom.

FIGURE 1-3: CORRECT AND INCORRECT POSITION COUNT CAPTURES



Work around

There are two different work arounds depending on the encoder type.

For encoder signals with timing that ensures the index pulse always starts prior to the start of the index match state (i.e. encoders with a non-gated index pulse), measure the direction of the encoder motion. If the encoder is counting up, add one to the captured position count; if the encoder is counting down, subtract one from the captured position count.

For encoder signals where the index pulse leading edge approximately coincides with the start of the index match state (i.e. encoders with a gated index pulse), a small delay can be added to the index pulse, for instance, by using a simple R-C filter.

If the encoder does not meet either of these criteria, no work around is available.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	—
PIC24EP64/dsPIC33EP64 devices	—
PIC24EP128/dsPIC33EP128 devices	—
PIC24EP256/dsPIC33EP256 devices	—
PIC24EP512/dsPIC33EP512 devices	**A7**

34. Module: QEI

When QCAPEN (QEI1IOC<15>) is enabled, the position count is captured at the rising edge of the HOME signal, instead of the index match event, as indicated by the data sheet.

Work around

None.

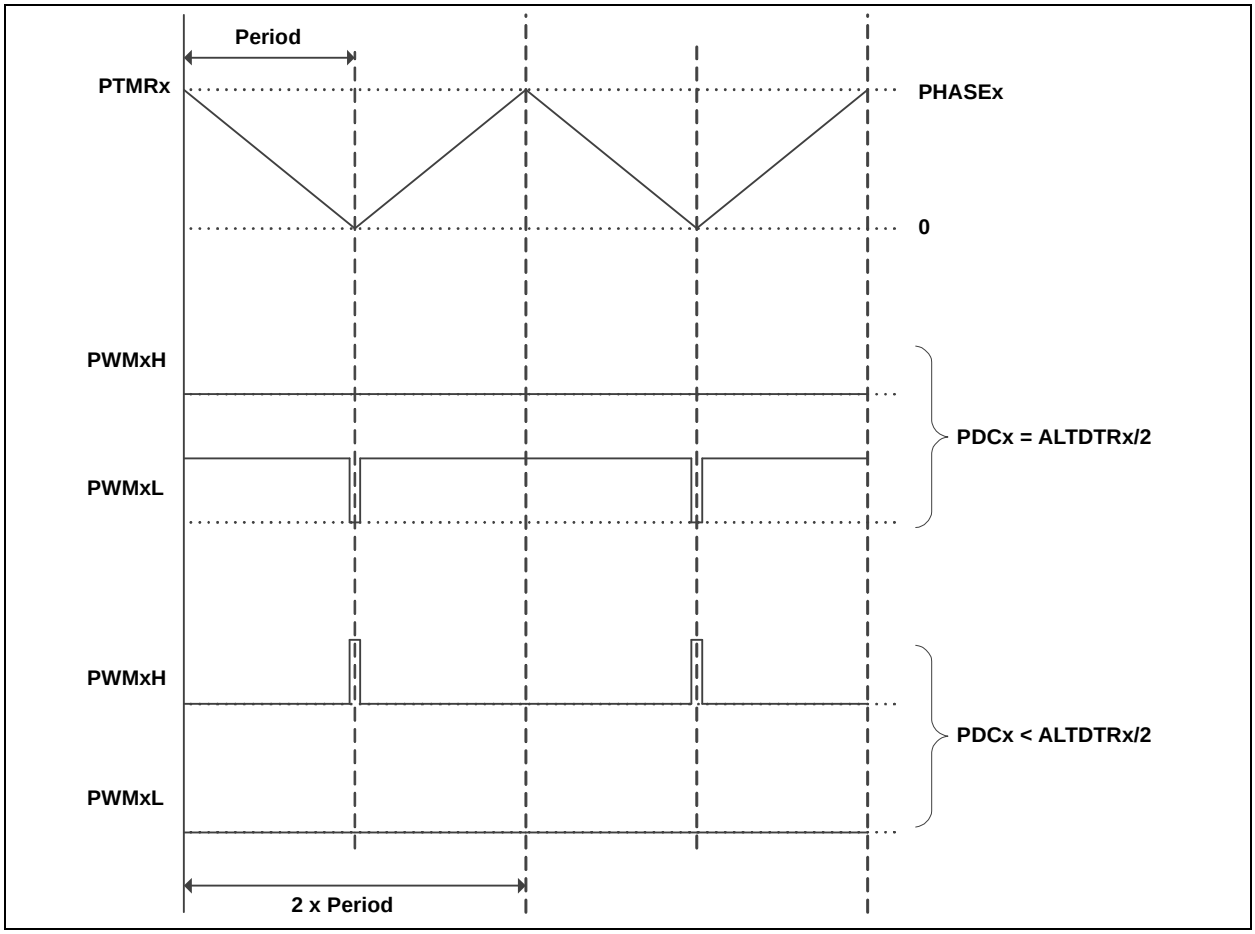
Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	—

35. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, if the value in the PDCx register is less than one-half the value in the ALTDTRx register, the PWMx generator will force the PWMxL to low and the PWMxH will generate pulses of width less than twice the dead time, as shown in Figure 1-4.

FIGURE 1-4: TIMING DIAGRAM



Work around

Include a software routine to ensure that the duty cycle value written to the PDCx register is always at least one-half of the value in ALTDTRx. Example 1-2 shows one method, with `PDCtemp` representing the variable which has the value to be written to the PDCx register. Alternatively, for duty cycle values less than half the desired dead time value, zero out the ALTDTRx register or dynamically reduce the value in the ALTDTRx register, such that ALTDTRx is always equal to 2 * PDCx, as shown in Example 1-3.

EXAMPLE 1-2: WORK AROUND CODE

```
Altdtr_by2 = ALTDTRx / 2;
if (PDCtemp < Altdtr_by2)
{
PDCx = Altdtr_by2;
}
else
{
PDCx = PDCtemp;
}
```

EXAMPLE 1-3: WORK AROUND CODE

```
#define DESIRED_DEADTIME 100
if (PDCtemp < (DESIRED_DEADTIME/2))
{
ALTDTRx = PDCtemp * 2;
PDCx = PDCtemp;
}
else
{
ALTDTRx = DESIRED_DEADTIME;
PDCx = PDCtemp;
}
```

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	—
PIC24EP64/dsPIC33EP64 devices	—
PIC24EP128/dsPIC33EP128 devices	—
PIC24EP256/dsPIC33EP256 devices	—
PIC24EP512/dsPIC33EP512 devices	**A7**

36. Module: PWM

When the PWMx generator is configured to operate in Current Reset mode (XPRES (PWMCONx<1>) = 1, Independent Time Base mode (ITB (PWMCONx<9>) = 1)), the PWMx Reset will happen only in every alternate PWM cycle.

Work around

1. Generate an interrupt when the comparator state changes. This interrupt should be high priority and could be either a comparator interrupt or PWMx Fault interrupt. The current-limit interrupt does not function in this mode. Inside the interrupt, update the PHASEx (period value) with a value less than the programmed duty cycle and then immediately update the PHASEx register with the value as required by the application (`PWM_period`), as shown in Example 1-4.

EXAMPLE 1-4: WORK AROUND CODE

```
PWMx ISR:
{
PHASEx = PDCx - 100;
PHASEx = PWM_period;
PWMxIF =0;
}
```

2. When the External Current Reset signal is applied to the PWMx generator (configured using the Current-Limit Control Signal Source Select bits (CLSRC<4:0>) in the PWMx Fault Current-Limit Control registers (FCLCONx<14:10>), depending on the PWM resolution selected (PCLKDIV<2:0> (PTCON2<2:0>)), the maximum pulse width of the External Current Reset signal is to be restricted to less than the values as shown in Table 1-1.

TABLE 1-1: MAXIMUM EXTERNAL CURRENT RESET SIGNAL WIDTH

PCLKDIV<2:0>	Max. External Current Reset Signal Width (in nS)
000	20
001	40
010	80
011	160
100	320
101	640
110	1280
111	2560

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

37. Module: Op Amp/Comparator

Op Amp/Comparator voltage reference can choose its source either from V_{REF+} or AV_{DD}, depending on the CVRSS bit (CVRCON<4>) setting.

If the CVRSS bit is set to '1', the comparator voltage reference source will be $CV_{RSRC} = (V_{REF+}) – (AV_{SS})$. Due to this issue, if CVRSS bit is set to '1' and the voltage on V_{REF+} is less than 1.33V, the op amp/comparator voltage reference will malfunction.

Work around

None.

Affected Families and Silicon Revisions

PIC24EP32/dsPIC33EP32 devices	**A3**
PIC24EP64/dsPIC33EP64 devices	**A2, A3**
PIC24EP128/dsPIC33EP128 devices	**A3**
PIC24EP256/dsPIC33EP256 devices	**A3**
PIC24EP512/dsPIC33EP512 devices	**A7**

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70657**H**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: REVISION HISTORY

Rev A Document (11/2011)

Initial release of this document; issued for revision A2 silicon.

Includes silicon issues 1 (CPU), 2, (CPU) 3 (SPI), 4 (SPI), 5 (UART), 6 (Power System), 7 (ADC), 8 (PTG), 9 (Op Amp), 10 (Op Amp), 11 (PWM), 12 (Flash), 13 (QEI), 14 (QEI) and 15 (PWM).

Rev B Document (4/2012)

Updated silicon issues 9 (Op Amp), 10 (Op Amp), and 12 (Flash).

Added silicon issues 16 (ADC), 17 (ADC), 18 (Output Compare), and 19 (ECAN™).

Rev C Document (6/2012)

Updated document to include all related device families (program memory sizes of 32, 128, 256 and 512 Kbytes) in this superfamily. In the process, revised the document format to accommodate the different silicon revision levels across the different families.

Added silicon issues 20, 21 and 22 (PWM), and 23 (CPU) to all device families.

Added data sheet clarification 1 (Packaging).

Rev D Document (8/2012)

Updated Table 1 to include both A2 and A3 silicon revision device IDs and removed PIC24EP512/dsPIC32EP512 (A4). Updated all Affected Families and Silicon Revisions tables.

Added silicon issues 24 (PWM) and 25 (PWM).

Added data sheet clarification 2 (High-Speed PWM Module).

Rev E Document (3/2013)

Adds silicon revision A2 for all 64 Kbyte devices to all existing silicon issues, except 9 and 10 (Op Amp).

Revises issue 24 (PWM) with a figure to illustrate the timing of the issue.

Revises issue 25 (PWM) to clarify conditions, and add work around options.

Added new silicon issues 26 (PWM), 27 (CTMU), 28 (Input Capture), 29 (JTAG), 30 (I/O), 31 (JTAG) and 32 (QEI) to silicon revision A3 for all device families, and revision A2 for 64 Kbyte device families only.

Updates data sheet revision level to “G”. Removes previous data sheet clarifications, which have been addressed in the new revision.

Rev F Document (7/2013)

Updated document to include 512 Kbytes memory. Adds silicon issues 33 (QEI), 34 (QEI), 35 (PWM), 36 (PWM) and 37 (Op Amp/Comparator). Revises silicon issue 15 (PWM) description. Revises silicon issue 20 (PWM) with new figure and text. Revises silicon issue 25 (PWM). Removes data sheet clarification 1 (Pin Diagrams) since this is now addressed in the current data sheet revision.

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Printed on recycled paper.

ISBN: 978-1-62077-326-0

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