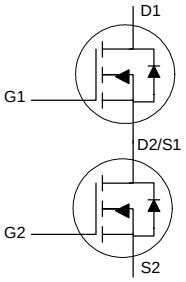
Asymmetric Dual N-channel Enhancement-mode Power MOSFETs

Simple Drive Requirement

Optimised Power Stage for Synchronous Buck Converter Applications

RoHS-compliant, halogen-free

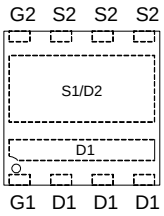


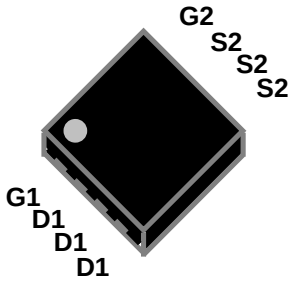
CH-1	BV_{DSS}	30V
	$R_{DS(ON)}$	18mΩ
	I_D	21A
CH-2	BV_{DSS}	30V
	$R_{DS(ON)}$	10.5mΩ
	I_D	39A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The AP6950GYT-HF-3 includes both hi-side ("control") FET and lo-side ("sync") FET for the power output stage of a synchronous buck converter. It is supplied in the PMPak®3x3 package, which offers a backside heat sink and a low package profile.





PMPAK®3 x 3

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	±20	±12	V
I_D at T_C=25°C	Continuous Drain Current (Chip Limited)	21	39	A
I_D at T_A=25°C	Continuous Drain Current[3]	8.3	11.8	A
I_D at T_A=70°C	Continuous Drain Current[3]	6.6	9.5	A
I_{DM}	Pulsed Drain Current[1]	40	40	A
P_D at T_A=25°C	Total Power Dissipation	1.9	2.2	W
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
Rthj-c	Maximum Thermal Resistance, Junction-case	10	5	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	65	55	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[4]	180	145	°C/W

Ordering Information

AP6950GYT-HF-3TR : in RoHS-compliant halogen-free PMPak®3x3, shipped on tape and reel (3000 pcs/reel)

CH-1 N-channel Electrical Specifications at T_j=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=8A	-	14	18	mΩ
		V_{GS}=4.5V, I_D=5A	-	23.2	30	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	1.4	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=8A	-	14	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=8A	-	4.2	6.7	nC
Q_{gs}	Gate-Source Charge	V_{DS}=15V	-	1.8	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	1.9	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V	-	6.5	-	ns
t_r	Rise Time	I_D=1A	-	6	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	15	-	ns
t_f	Fall Time	V_{GS}=10V	-	3	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	450	720	pF
C_{oss}	Output Capacitance	V_{DS}=15V	-	70	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	50	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.2	2.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=8A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=8A, V_{GS}=0V,	-	13	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	6	-	nC

Notes:

1.Pulse width limited by maximum junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec.

4.Surface mounted on 1 in^2 copper pad of FR4 board, on steady-state

CH-2 N-channel Electrical Specifications at T_j=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=11A	-	8	10.5	mΩ
		V_{GS}=4.5V, I_D=7A	-	13.3	16.5	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	1.4	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=11A	-	20	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=11A	-	7.5	12	nC
Q_{gs}	Gate-Source Charge	V_{DS}=15V	-	3	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	3	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V	-	9	-	ns
t_r	Rise Time	I_D=1A	-	5	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	20	-	ns
t_f	Fall Time	V_{GS}=10V	-	4	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	970	1550	pF
C_{oss}	Output Capacitance	V_{DS}=15V	-	120	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	80	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.2	2.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=11A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=11A, V_{GS}=0V,	-	16	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	10	-	nC

Notes:

1.Pulse width limited by maximum junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec.

4.Surface mounted on 1 in^2 copper pad of FR4 board, on steady-state

Typical CH-1 Electrical Characteristics

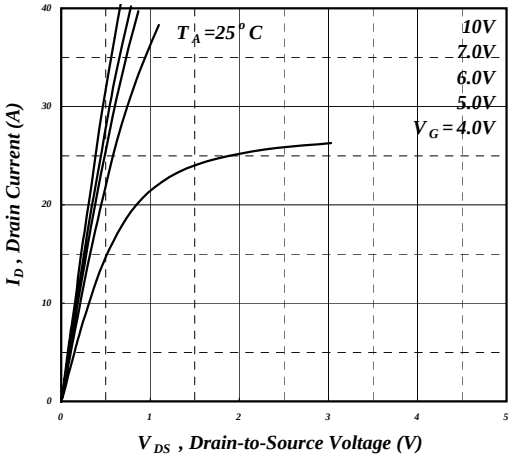


Fig 1. Typical Output Characteristics

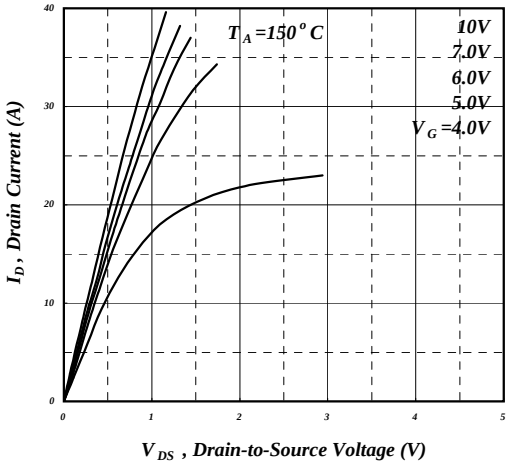


Fig 2. Typical Output Characteristics

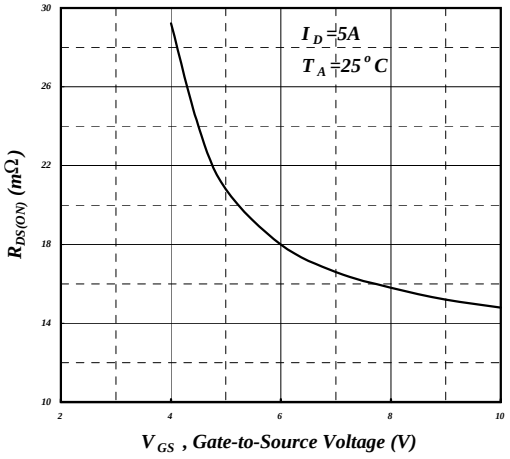


Fig 3. On-Resistance vs. Gate Voltage

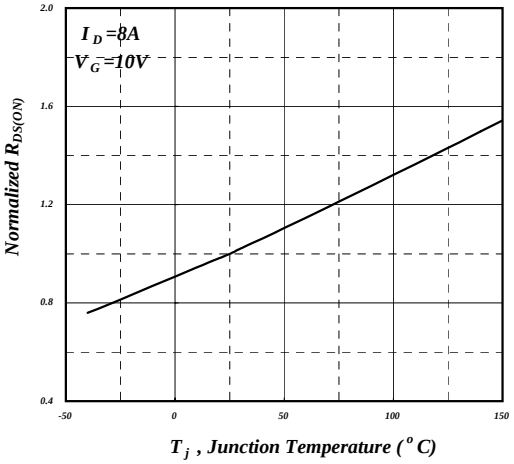


Fig 4. Normalized On-Resistance vs. Junction Temperature

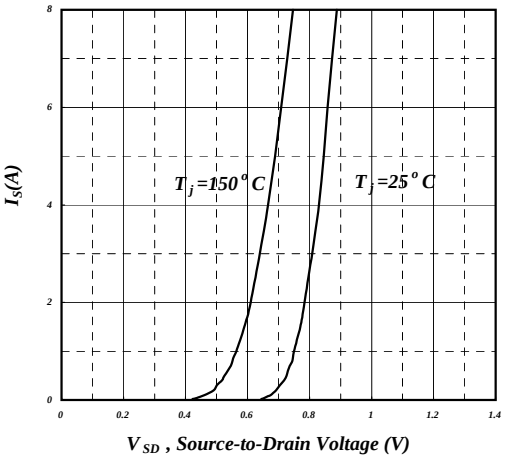


Fig 5. Forward Characteristic of Reverse Diode

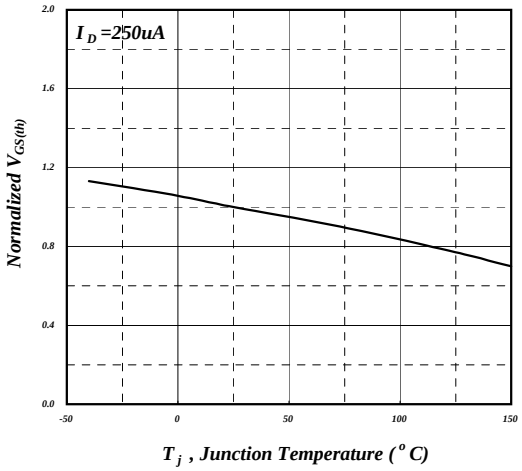


Fig 6. Gate Threshold Voltage vs. Junction Temperature

Typical CH-1 Electrical Characteristics (cont.)

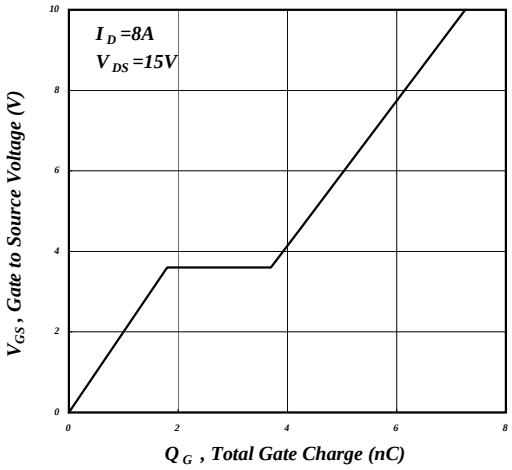


Fig 7. Gate Charge Characteristics

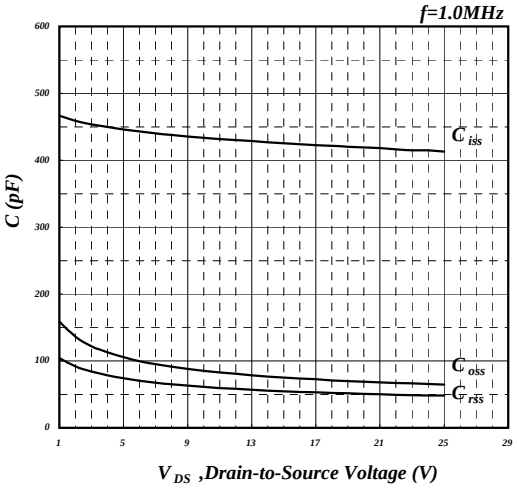


Fig 8. Typical Capacitance Characteristics

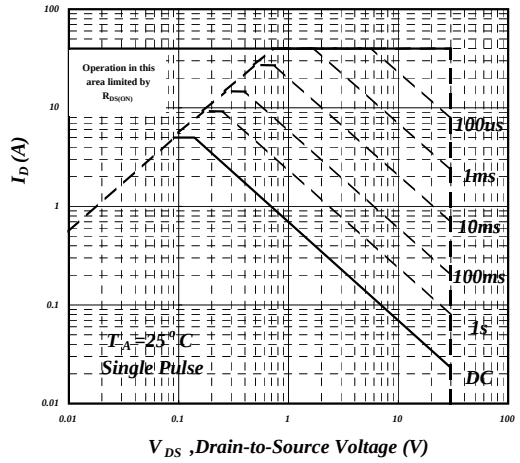


Fig 9. Maximum Safe Operating Area

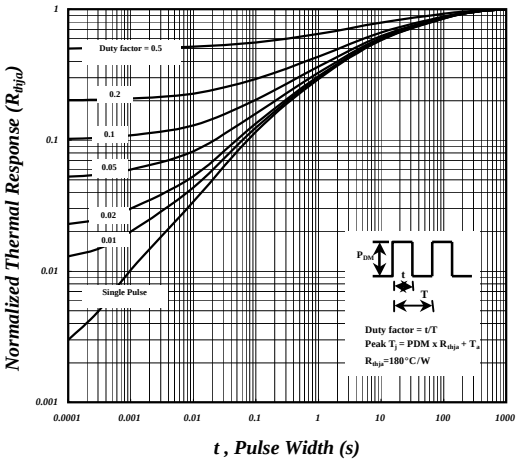


Fig 10. Effective Transient Thermal Impedance

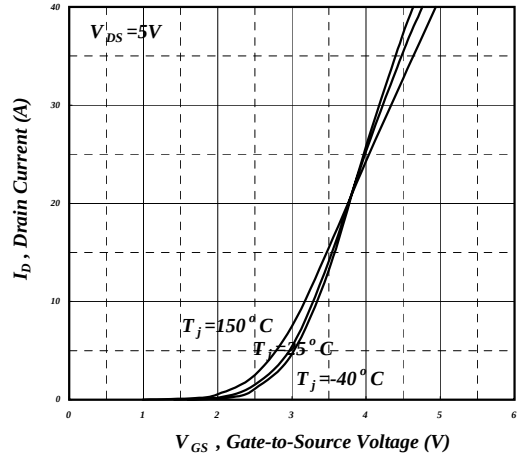


Fig 11. Transfer Characteristics

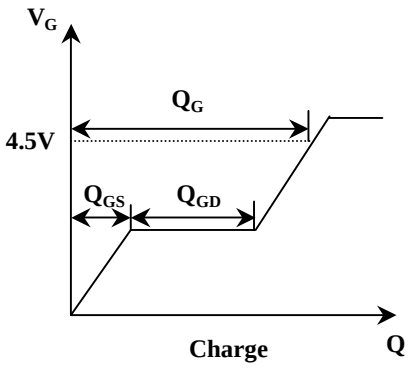


Fig 12. Gate Charge Waveform

Typical CH-2 Electrical Characteristics

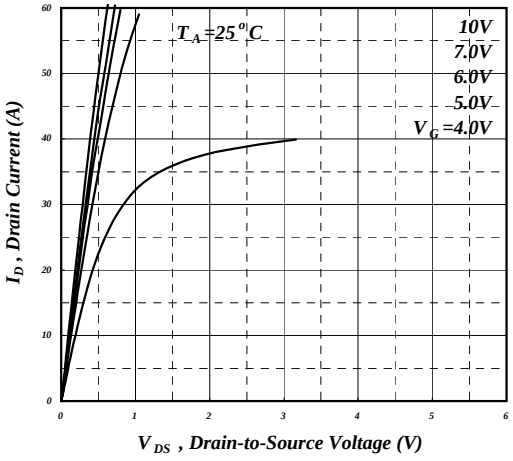


Fig 1. Typical Output Characteristics

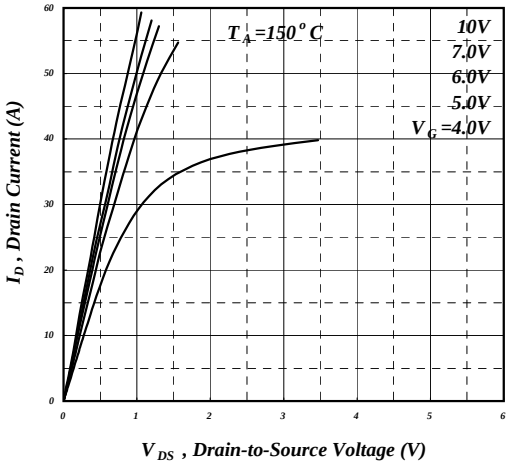


Fig 2. Typical Output Characteristics

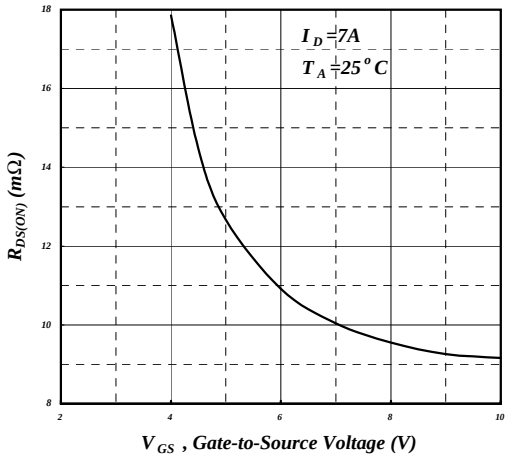


Fig 3. On-Resistance vs. Gate Voltage

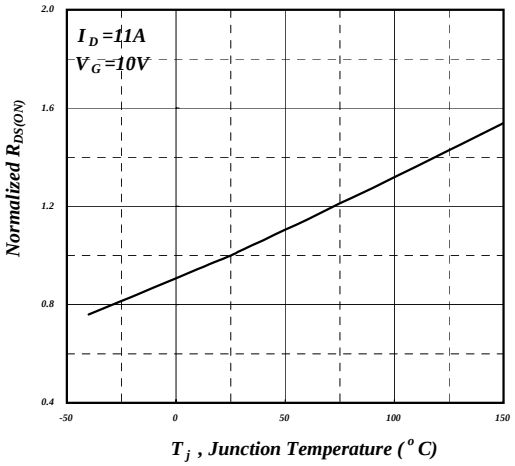


Fig 4. Normalized On-Resistance vs. Junction Temperature

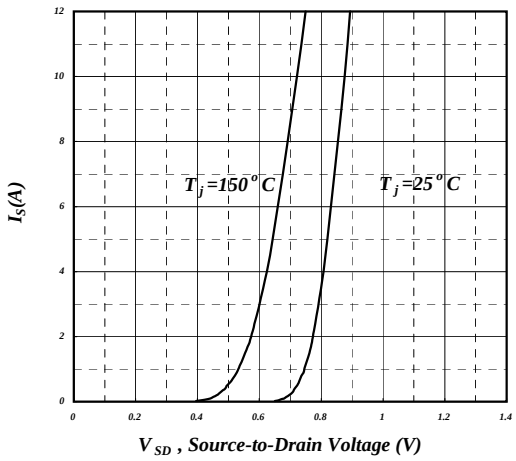


Fig 5. Forward Characteristic of Reverse Diode

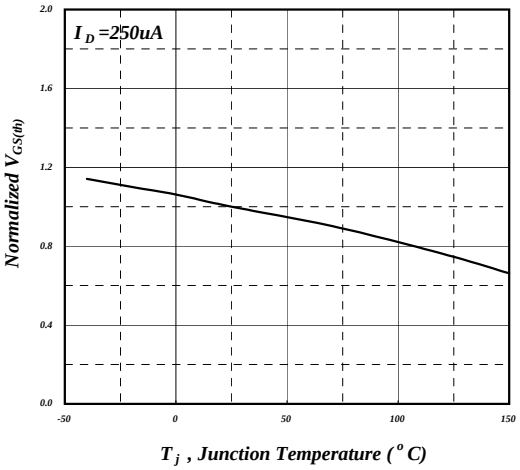


Fig 6. Gate Threshold Voltage vs. Junction Temperature

Typical CH-2 Electrical Characteristics (cont.)

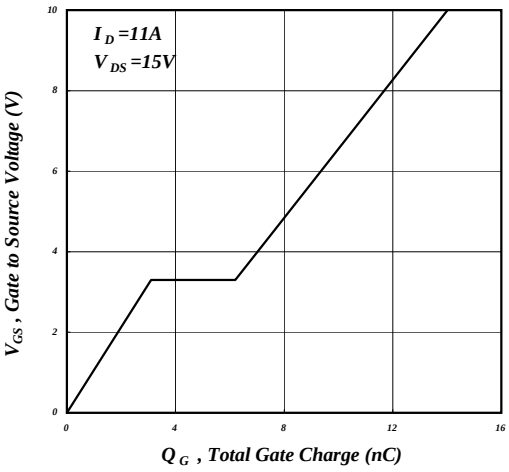
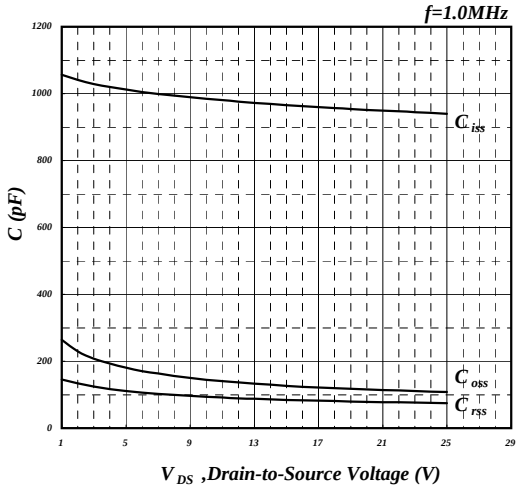


Fig 7. Gate Charge Characteristics



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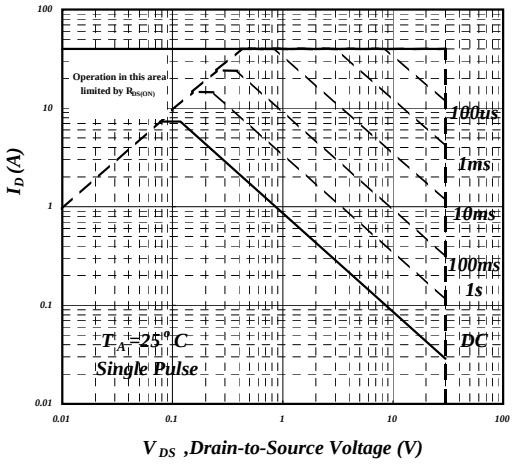


Fig 9. Maximum Safe Operating Area

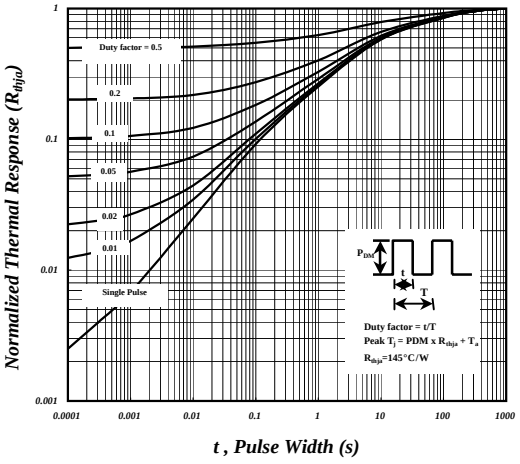


Fig 10. Effective Transient Thermal Impedance

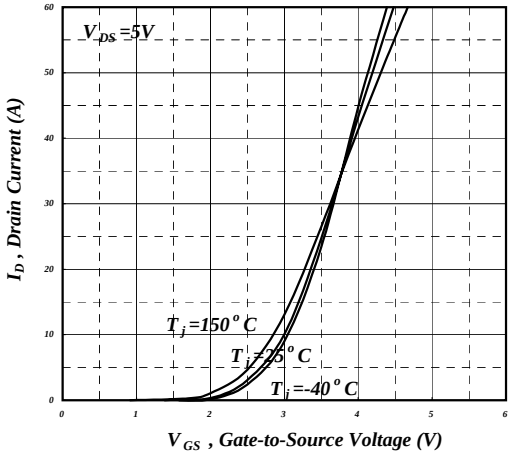


Fig 11. Transfer Characteristics

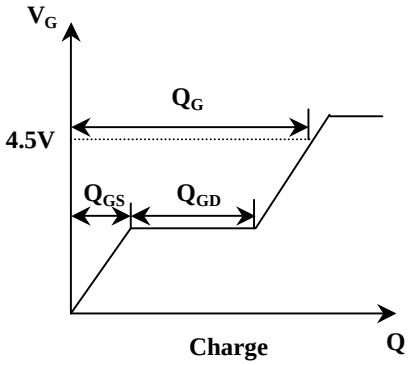
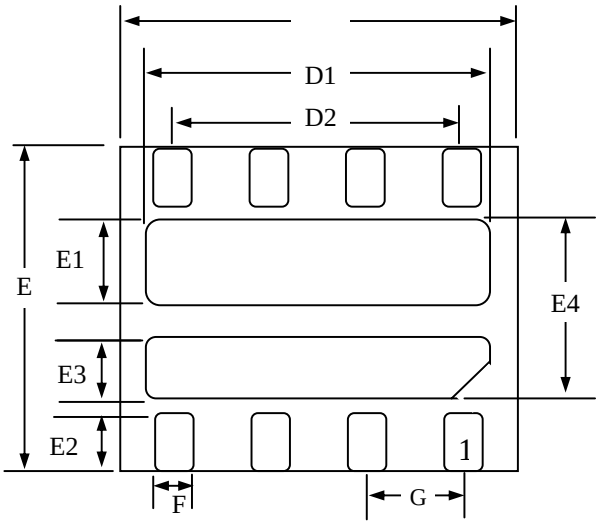
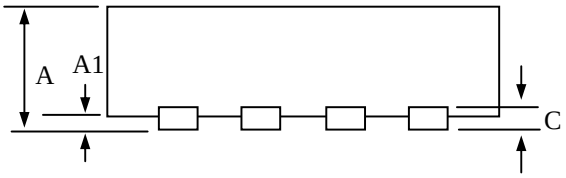


Fig 12. Gate Charge Waveform

Package Dimensions: PMPAK®3x3 (Dual Pad)



BOTTOM



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.800	0.850	0.900
A1	0.000	0.025	0.050
C	0.195	0.203	0.211
D	2.900	3.000	3.100
D1	2.350	2.400	2.450
D2	1.950 (ref)		
E	2.900	3.000	3.100
E1	0.940	0.990	1.040
E2	0.270	0.320	0.370
E3	0.470	0.520	0.570
F	0.350	0.400	0.450
G	0.650 (BSC)		
E4	1.860 (ref.)		

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information: