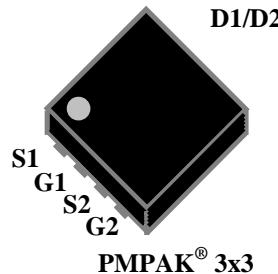




## Complementary N and P-channel Enhancement-mode Power MOSFETs

- Simple Drive Requirement
- Fast Switching Performance
- Good Thermal Performance
- RoHS-compliant, halogen-free

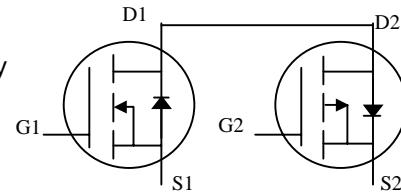
### Description



N-CH	$BV_{DSS}$	30V
	$R_{DS(ON)}$	30mΩ
	$I_D$	7.3A
P-CH	$BV_{DSS}$	-30V
	$R_{DS(ON)}$	60mΩ
	$I_D$	-5.3A

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, low on-resistance and cost-effectiveness.

The AP4537GYT-HF-3 is in the PMPAK®3x3 package, which is specially designed for applications requiring good thermal and electrical performance in a small footprint with a backside heat sink and a low package profile.



### Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
$V_{DS}$	Drain-Source Voltage	30	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$ at $T_A=25^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	7.3	-5.3	A
$I_D$ at $T_A=70^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	5.8	-4.2	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	28	-20	A
$P_D$ at $T_A=25^\circ\text{C}$	Total Power Dissipation	2.5		W
	Linear Derating Factor	0.02		W/ $^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

### Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-c}$	Thermal Resistance Junction-case	Max.	$^\circ\text{C}/\text{W}$
$R_{thj-a}$	Thermal Resistance Junction-ambient <sup>3</sup>	Max.	$^\circ\text{C}/\text{W}$

### Ordering Information

**AP4537GYT-HF-3TR** RoHS-compliant halogen-free PMPAK®3x3, shipped on tape and reel (3000 pcs/reel)

PMPAK® is a registered trademark of Advanced Power Electronics Corp.



**N-channel Electrical Specifications at  $T_j=25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30	-	-	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=4\text{A}$	-	-	30	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=3\text{A}$	-	-	48	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1	-	3	V
$g_{\text{fs}}$	Forward Transconductance	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=4\text{A}$	-	8.5	-	S
$I_{\text{DSS}}$	Drain-Source Leakage Current	$V_{\text{DS}}=24\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	$\text{uA}$
$I_{\text{GSS}}$	Gate-Source Leakage	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_{\text{D}}=4\text{A}$ $V_{\text{DS}}=15\text{V}$ $V_{\text{GS}}=4.5\text{V}$	-	4.5	7.2	nC
$Q_{\text{gs}}$	Gate-Source Charge		-	1	-	nC
$Q_{\text{gd}}$	Gate-Drain ("Miller") Charge		-	2.5	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time <sup>2</sup>	$V_{\text{DS}}=15\text{V}$ $I_{\text{D}}=1\text{A}$ $R_{\text{G}}=3.3\Omega$	-	8	-	ns
$t_r$	Rise Time		-	9	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time		-	16	-	ns
$t_f$	Fall Time	$V_{\text{GS}}=10\text{V}$ $V_{\text{GS}}=0\text{V}$ $V_{\text{DS}}=25\text{V}$	-	3	-	ns
$C_{\text{iss}}$	Input Capacitance		-	250	400	pF
$C_{\text{oss}}$	Output Capacitance		-	55	-	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance	f=1.0MHz	-	50	-	pF

### Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{\text{SD}}$	Forward On Voltage <sup>2</sup>	$I_{\text{S}}=1.2\text{A}, V_{\text{GS}}=0\text{V}$	-	-	1.2	V
$t_{\text{rr}}$	Reverse Recovery Time <sup>2</sup>	$I_{\text{S}}=4\text{A}, V_{\text{GS}}=0\text{V}$	-	15	-	ns
			-	7	-	nC

### Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse width  $\leq 300\text{us}$ , duty cycle  $\leq 2\%$ .
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board , t <10sec ; 90°C at steady state.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



**P-channel Electrical Specifications at  $T_j=25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-30	-	-	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{\text{GS}}=-10\text{V}, I_{\text{D}}=-4\text{A}$	-	-	60	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-3\text{A}$	-	-	80	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-1	-	-3	V
$g_{\text{fs}}$	Forward Transconductance	$V_{\text{DS}}=-10\text{V}, I_{\text{D}}=-4\text{A}$	-	9	-	S
$I_{\text{DSS}}$	Drain-Source Leakage Current	$V_{\text{DS}}=-24\text{V}, V_{\text{GS}}=0\text{V}$	-	-	-1	$\text{uA}$
$I_{\text{GSS}}$	Gate-Source Leakage	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_{\text{D}}=-4\text{A}$	-	7	11.2	nC
$Q_{\text{gs}}$	Gate-Source Charge	$V_{\text{DS}}=-15\text{V}$	-	1.5	-	nC
$Q_{\text{gd}}$	Gate-Drain ("Miller") Charge		-	3.5	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time <sup>2</sup>	$V_{\text{DS}}=-15\text{V}$	-	10	-	ns
$t_r$	Rise Time		-	11	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	22	-	ns
$t_f$	Fall Time		-	9	-	ns
$C_{\text{iss}}$	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	570	910	pF
$C_{\text{oss}}$	Output Capacitance		-	80	-	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		-	75	-	pF

### Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{SD}}$	Forward On Voltage <sup>2</sup>	$I_{\text{S}}=-1.2\text{A}, V_{\text{GS}}=0\text{V}$	-	-	-1.2	V
$t_{\text{rr}}$	Reverse Recovery Time <sup>2</sup>	$I_{\text{S}}=-4\text{A}, V_{\text{GS}}=0\text{V}$	-	19	-	ns
			-	13	-	nC

### Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse width  $\leq 300\text{us}$ , duty cycle  $\leq 2\%$ .
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board , t  $< 10\text{sec}$  ;  $90^\circ\text{C}$  at steady state.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

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## Typical N-channel Electrical Characteristics

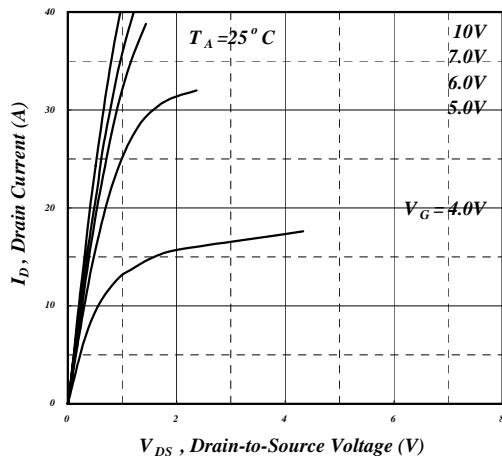


Fig 1. Typical Output Characteristics

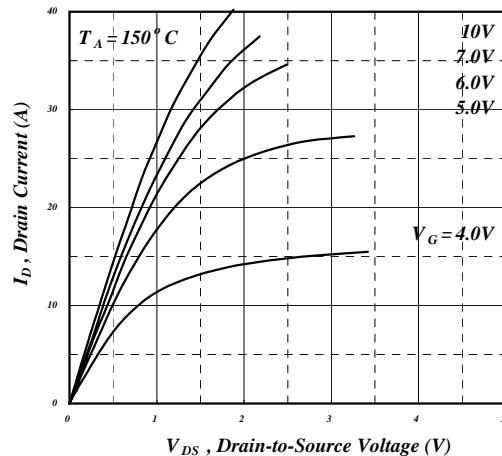


Fig 2. Typical Output Characteristics

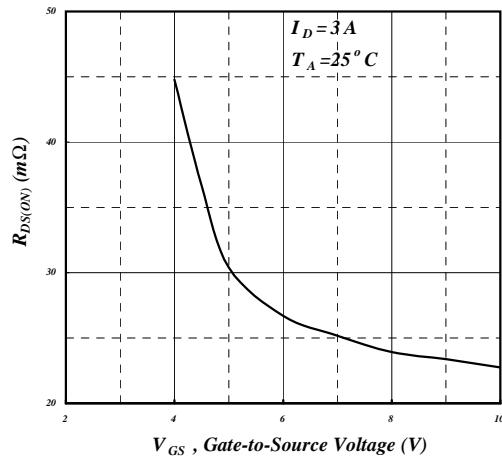


Fig 3. On-Resistance vs. Gate Voltage

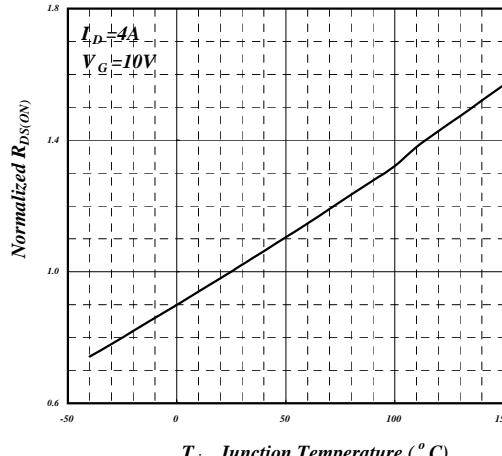


Fig 4. Normalized On-Resistance vs. Junction Temperature

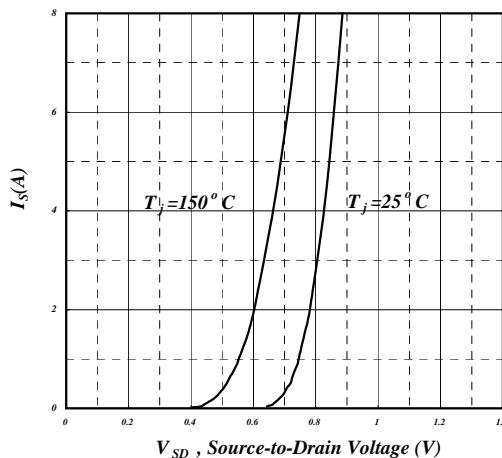


Fig 5. Forward Characteristic of Reverse Diode

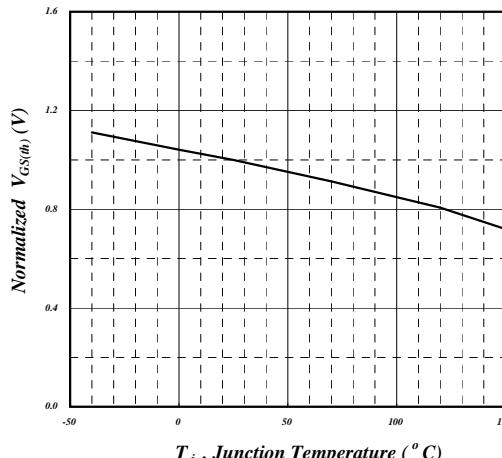


Fig 6. Gate Threshold Voltage vs. Junction Temperature



## Typical N-channel Electrical Characteristics (cont.)

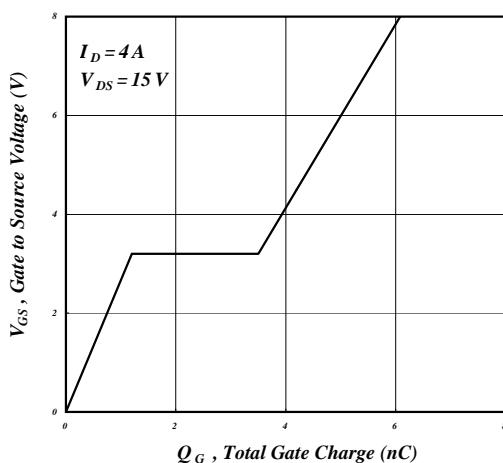


Fig 7. Gate Charge Characteristics

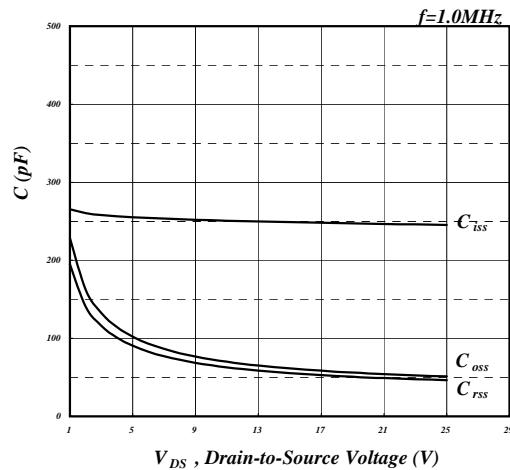


Fig 8. Typical Capacitance Characteristics

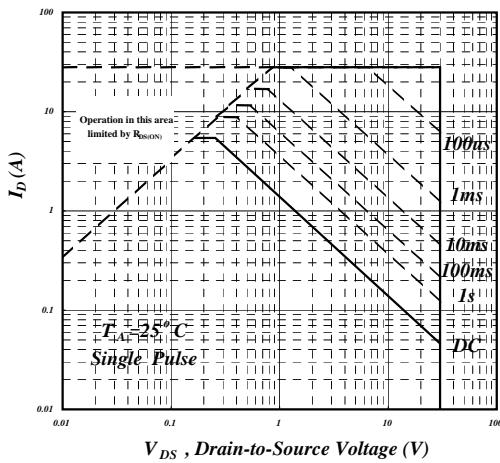


Fig 9. Maximum Safe Operating Area

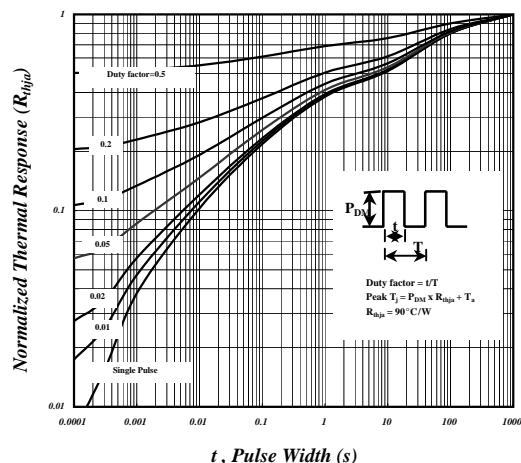


Fig 10. Effective Transient Thermal Impedance

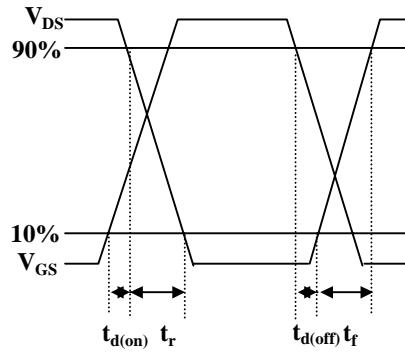


Fig 11. Switching Time Waveform

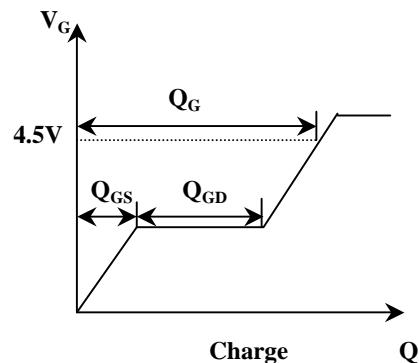


Fig 12. Gate Charge Waveform



## Typical P-channel Electrical Characteristics

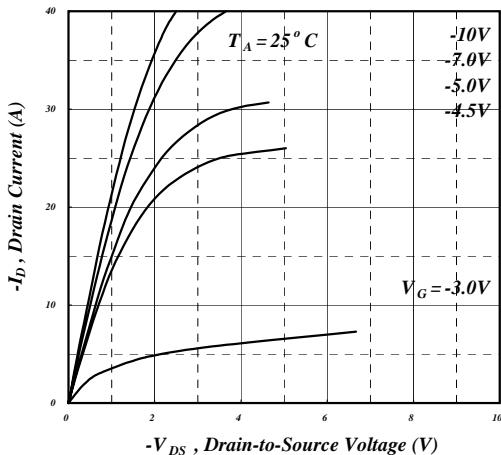


Fig 1. Typical Output Characteristics

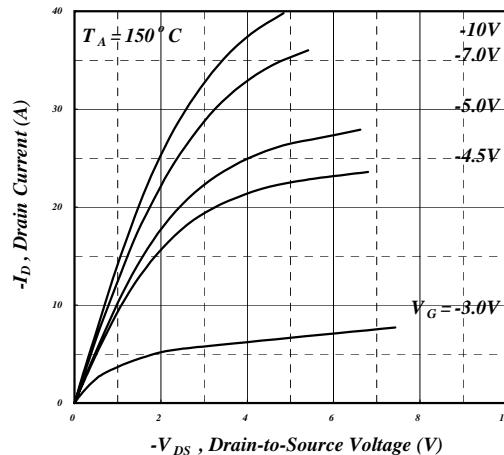


Fig 2. Typical Output Characteristics

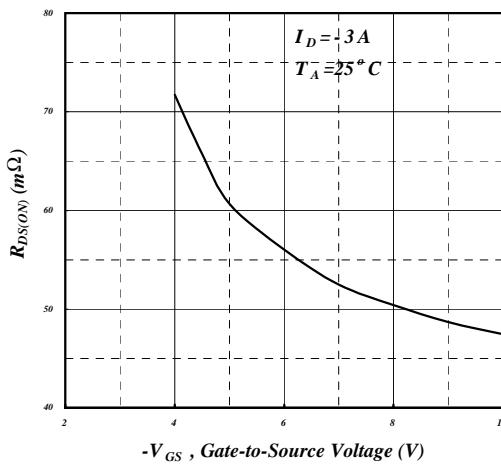


Fig 3. On-Resistance vs. Gate Voltage

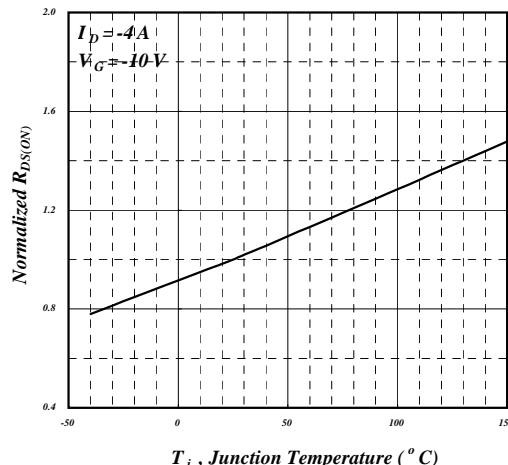


Fig 4. Normalized On-Resistance vs. Junction Temperature

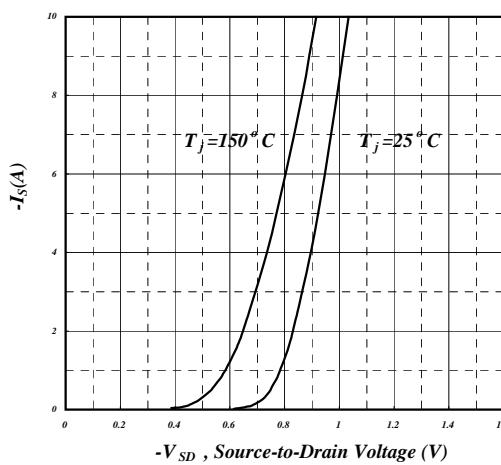


Fig 5. Forward Characteristic of Reverse Diode

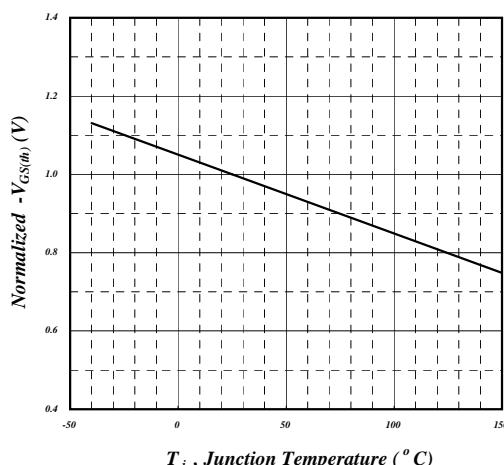


Fig 6. Gate Threshold Voltage vs. Junction Temperature



## Typical P-channel Electrical Characteristics (cont.)

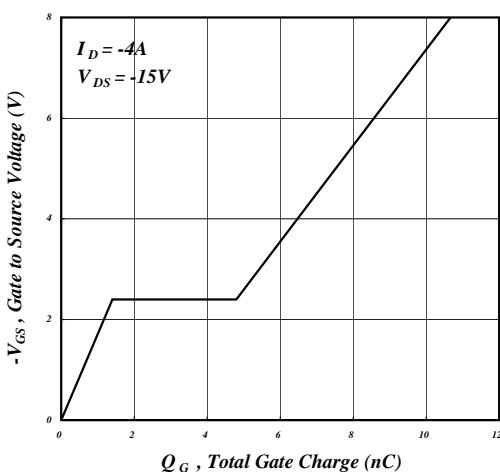


Fig 7. Gate Charge Characteristics

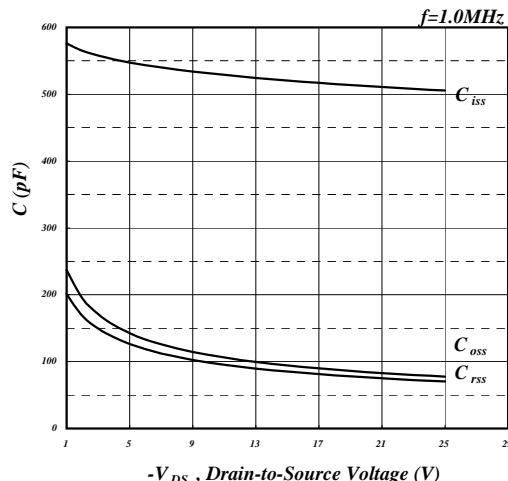


Fig 8. Typical Capacitance Characteristics

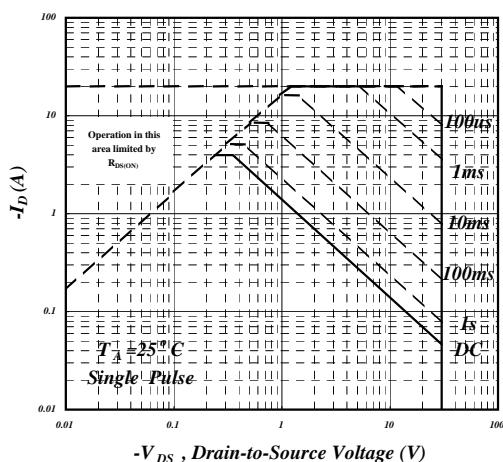


Fig 9. Maximum Safe Operating Area

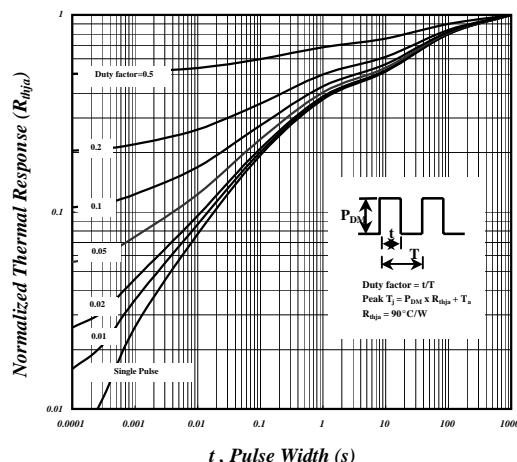


Fig 10. Effective Transient Thermal Impedance

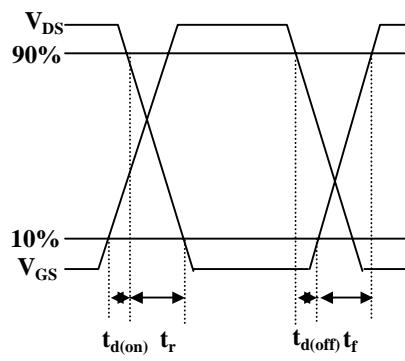


Fig 11. Switching Time Waveform

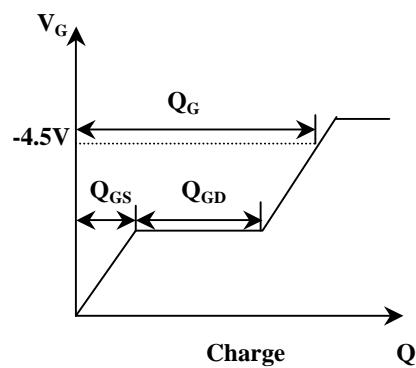
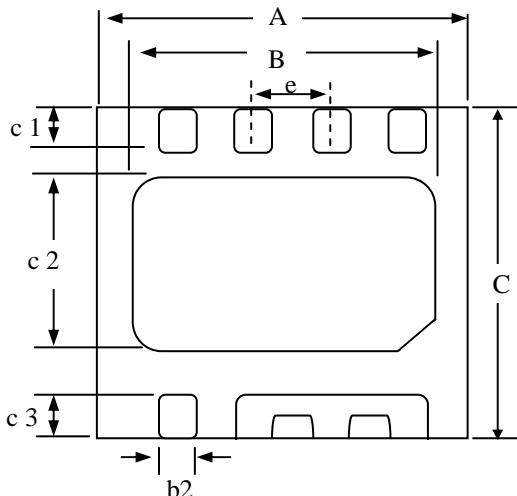


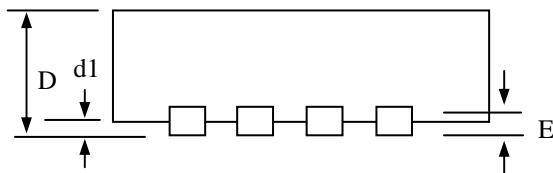
Fig 12. Gate Charge Waveform



## Package Dimensions: PMPAK®3x3



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	2.95	3.00	3.05
B	2.35	2.40	2.45
e		0.65 (ref.)	
b2	0.30	0.35	0.40
C	2.95	3.00	3.05
c1	0.37	0.42	0.47
c2	1.65	1.70	1.75
c3	0.37	0.42	0.47
D	0.80	0.85	0.95
d1	0.00	-	0.05
E	0.178	0.203	0.228



1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

## Marking Information:

