2A Sink/Source Bus Termination Regulator

Features

- Ideal for DDR-I, DDR-II and DDR-III V_{TT} Applications
- Sink and Source 2A Continuous Current
- Integrated Power MOSFETs
- Generates Termination Voltage for SSTL_2, SSTL_18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- Highly Accurate Output Voltage at Full-Load
- Output Adjustment using Two External Resistors
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- On-Chip Thermal Protection
- No Power Sequence Issue for V_{IN} and V_{CNTL}
- SO-8 with Exposed Pad
- RoHS/REACH-compliant, Halogen-free

Application

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses in DDR-I, DDR-II and DDR-III Memory Systems

Description

The AP1280MP-HF-3 is a simple and cost-effective high-speed linear regulator designed to generate termination voltages in double data rate (DDR) memory systems to comply with JEDEC SSTL_2 and SSTL_18, or other specific interfaces such as HSTL, SCSI-2 and SCSI-3.

The regulator is capable of actively sinking or sourcing up to 2A while regulating an output voltage to within 40mV. The output termination voltage can be tightly regulated to track $1/2V_{DDQ}$ by using two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The AP1280MP-HF-3 also incorporates a high-speed differential amplifier to provide ultra-fast response to line/load transients. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in both directions and on-chip thermal shut-down protection.

The AP1280MP-HF-3 is available in the ESOP-8 exposed-pad surface mount package.

Ordering Information

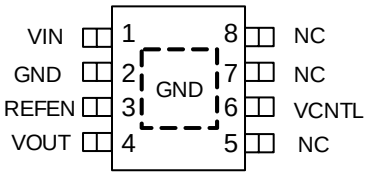
AP1280MP-HF-3TR

Supplied on tape and reel, 3000pcs per reel

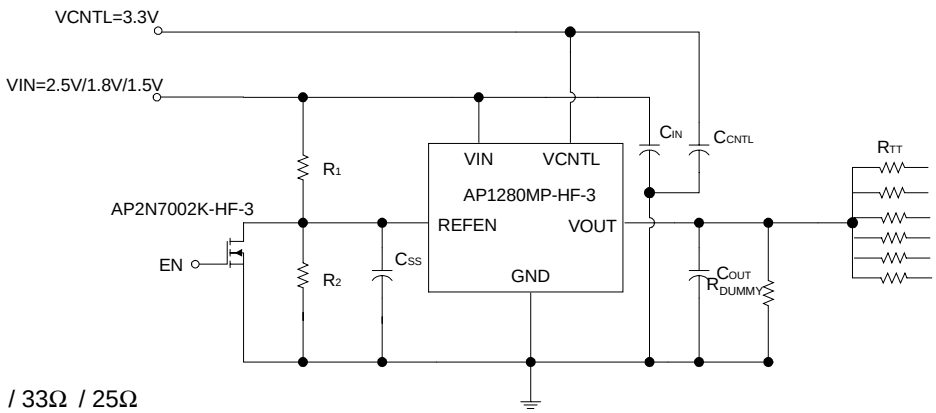
Pin Configuration

ESO-8 (MP)

(Top View)



Typical Application Circuit



$R_1 = R_2 = 100k\Omega$, $R_{TT} = 50\Omega$ / 33Ω / 25Ω

$C_{OUT,min} = 10\mu F$ (Ceramic) + $100\mu F$ under the worst case testing condition

$C_{SS} = 1\mu F$, $C_{IN} = 470\mu F$ (Low ESR), $C_{CNTL} = 47\mu F$

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	6	V
Control Voltage	V_{CNTL}	6	V
Power Dissipation	P_D	Internally Limited	--
Storage Temperature Range	T_S	-65 to 150	°C
Lead Temperature (Soldering, 5 sec.)	T_{LEAD}	260	°C
Package Thermal Resistance	Rth_{JC}	28	ºC/W

Recommended Operating Conditions

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	2.5 to 1.5 ±3%	V
Control Voltage	V_{CNTL}	5.5 or 3.3 ±5%	V
Ambient Temperature	T_A	-40 to +85	°C
Junction Temperature	T_J	-40 to +125	°C

Electrical Specifications

V_{IN}=1.8V, V_{CNTL}=3.3V, V_{REFEN}=0.9V, C_{OUT}=10µF (Ceramic)), T_A=25ºC, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input						
V_{CNTL} Operation Current	I_{CNTL}	I_{OUT}=0A	--	1	2.5	mA
Standby Current	I_{STBY}	V_{REFEN} < 0.2V (Shutdown), R_{LOAD} = 180Ω	--	50	90	µA
Output (DDR / DDR II / DDR III)						
Output Offset Voltage(Note2)	V_{OS}	I_{OUT}= 0A	-20	--	+20	mV
Load Regulation(Note3)	ΔV_{LOAD}	I_{OUT} =10mA to 2A	-20	--	+20	mV
		I_{OUT}= -10mA to -2A	-20	--	+20	mV
Protection						
Current limit	I_{LIM}		2.2	--	--	A
Thermal Shutdown Temperature	T_{SD}	3.3V ≤ V_{CNTL} ≤ 5V	130	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}	3.3V ≤ V_{CNTL} ≤ 5V	--	30	--	°C
REFEN Shutdown						
Shutdown Threshold	V_{IH}	Enable	0.65	--	--	V
	V_{IL}	Shutdown	--	--	0.2	V

Note 1: Exceeding the absolute maximum rating may damage the device.

Note 2: The device is not guaranteed to function outside its operating conditions.

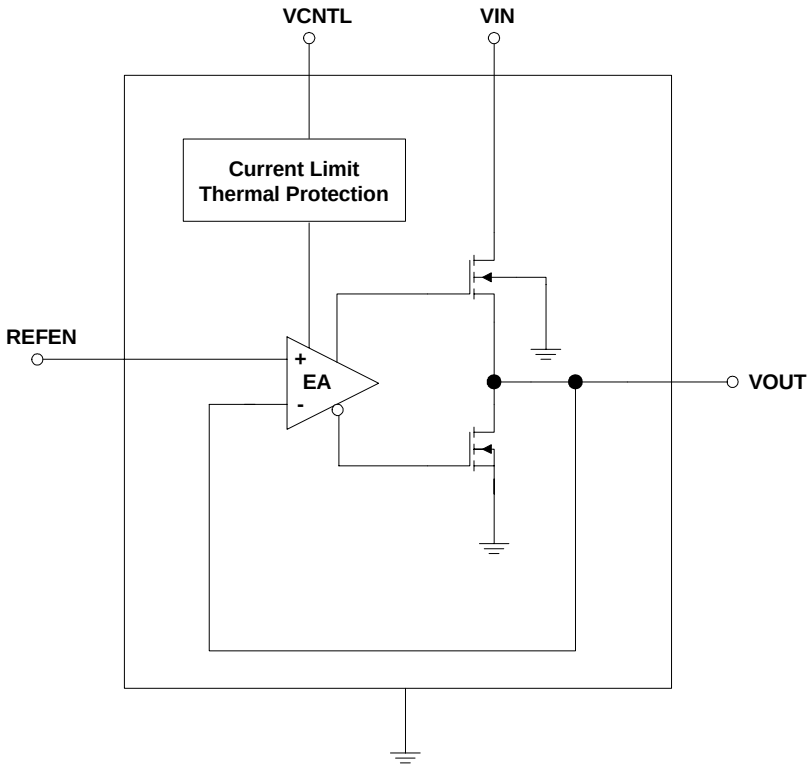
Note 3: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

Note 4: Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 2A.

Pin Descriptions

PIN SYMBOL	PIN DESCRIPTION
V_{IN}	Power Input Voltage.
GND	Ground Pin
V_{OUT}	Output Voltage
V_{CNTL}	Gate Drive Voltage
REFEN	Reference Voltage Input and Chip Enable

Block Diagram



Application Information

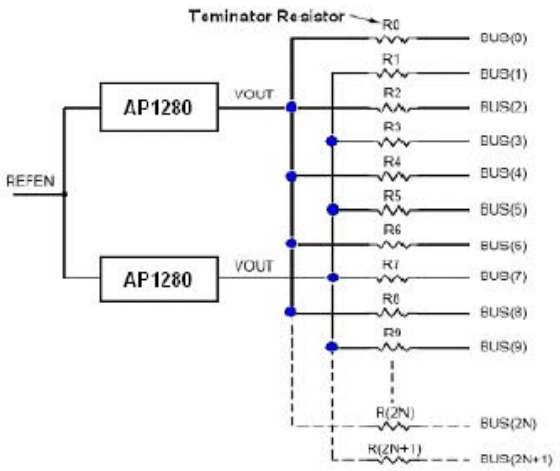
Input Capacitor and Layout Consideration

The input bypass capacitor should be placed as close as possible to the AP1280MP-HF-3. A low-ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance.

Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between the AP1280MP-HF-3 and the preceding power converter.

Design considerations for the resistances of the voltage divider

Make sure the sinking current capability of the pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V. In addition, the capacitor and voltage divider form the lowpass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



Thermal Consideration

AP1280MP-HF-3 regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continuous operation, do not exceed the maximum operation junction temperature of 125°C. The power dissipated in the device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, the rate of surrounding airflow and the temperature difference between junction and the ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / Rth_{JA}$$

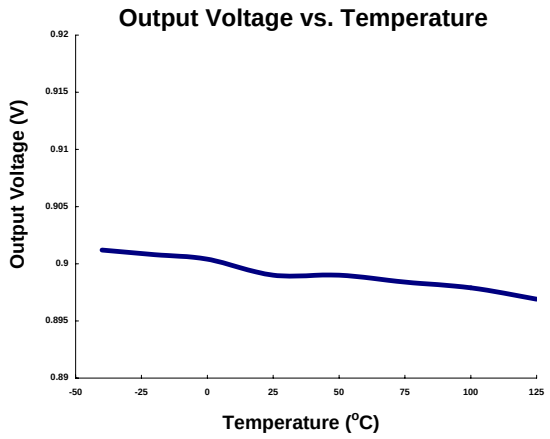
where $T_{J(MAX)}$ is the maximum operating junction temperature 125°C, T_A is the ambient temperature and Rth_{JA} is the junction-to-ambient thermal resistance. The junction-to-ambient thermal resistance, Rth_{JA}, is layout and package dependent, and for this ESOP-8 package is 75°C/W on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at T_A = 25°C can be calculated using the following formula:

$$P_{D(MAX)} = (125°C - 25°C) / 75°C/W = 1.33W$$

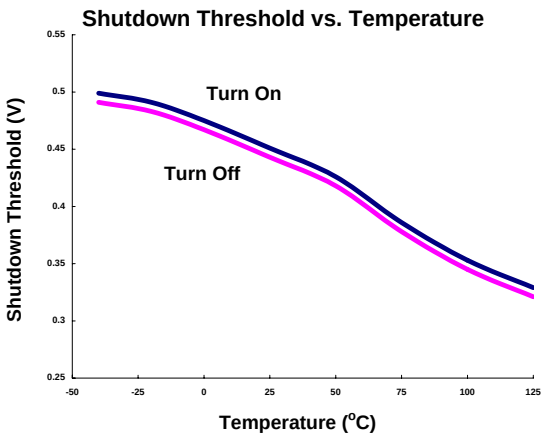
The thermal resistance, Rth_{JA}, of the ESOP-8 is determined by the package design and the PCB design. However, the package design is fixed.

It is possible where necessary to improve the thermal performance by changing the PCB design. The thermal resistance can be decreased by adding copper under the exposed pad of the ESOP-8 package.

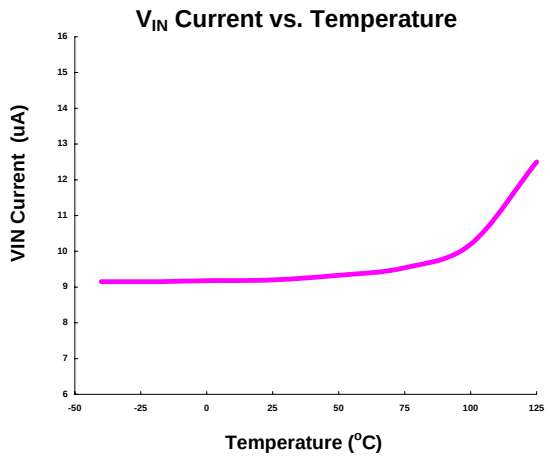
Typical Performance Characteristics



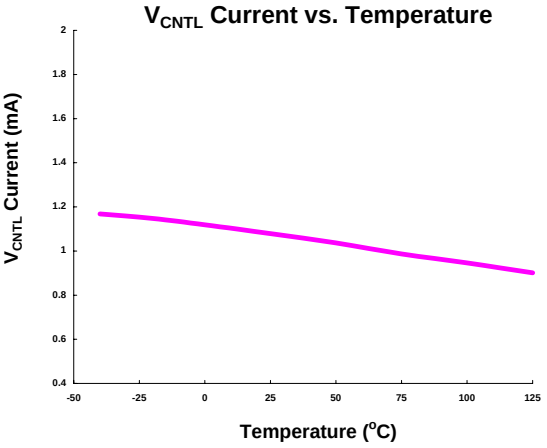
V_{IN} = 1.8V, V_{CNTL} = 3.3V



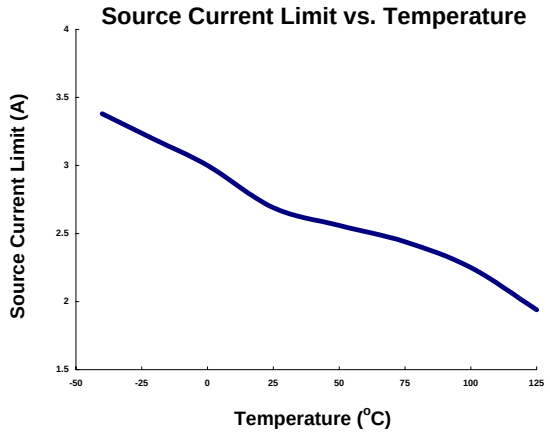
V_{IN} = 1.8V, V_{CNTL} = 3.3V



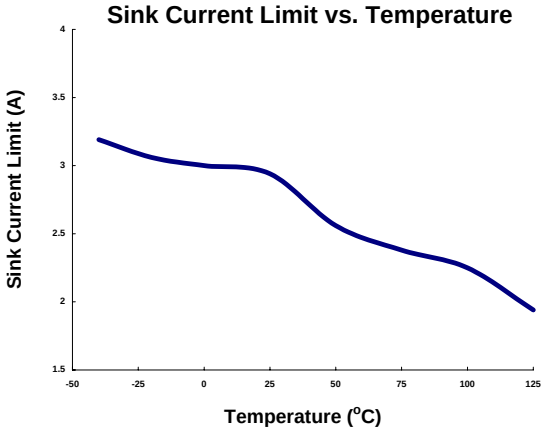
V_{IN} = 1.8V, V_{CNTL} = 3.3V



V_{IN} = 1.8V, V_{CNTL} = 3.3V



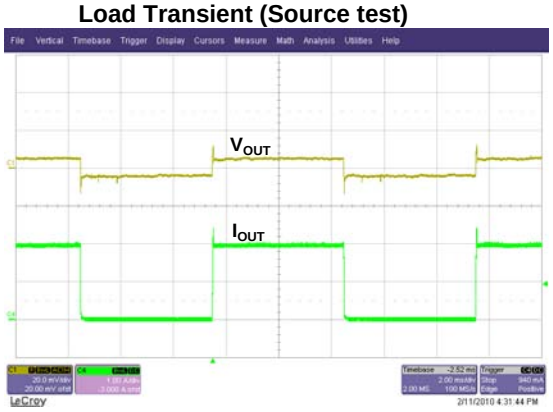
V_{IN} = 1.8V, V_{CNTL} = 3.3V



V_{IN} = 1.8V, V_{CNTL} = 3.3V

Typical Performance Characteristics (cont.)

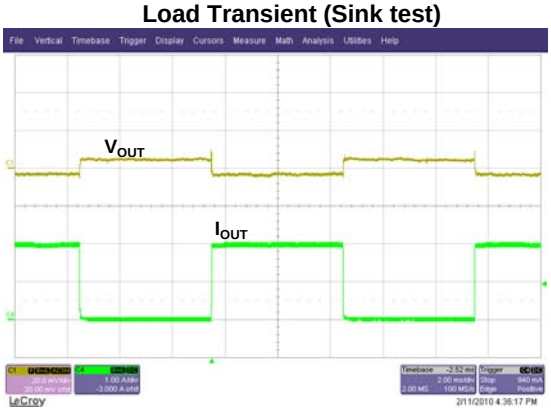
Load Transient (Source test)



V_{IN} = 1.8V, V_{CNTL} = 3.3V

V_{REF} = 0.9V Supplied by a regulator

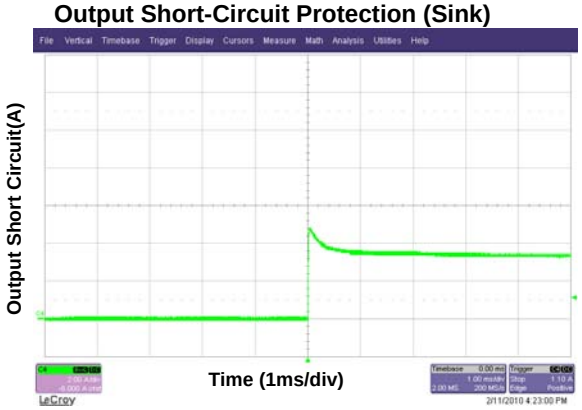
Load Transient (Sink test)



V_{IN} = 1.8V, V_{CNTL} = 3.3V

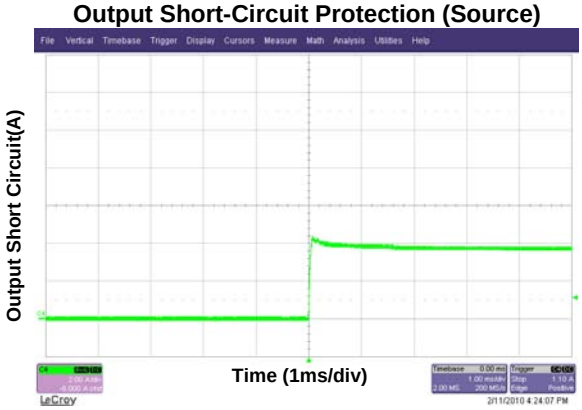
V_{REF} = 0.9V Supplied by a regulator

Output Short-Circuit Protection (Sink)



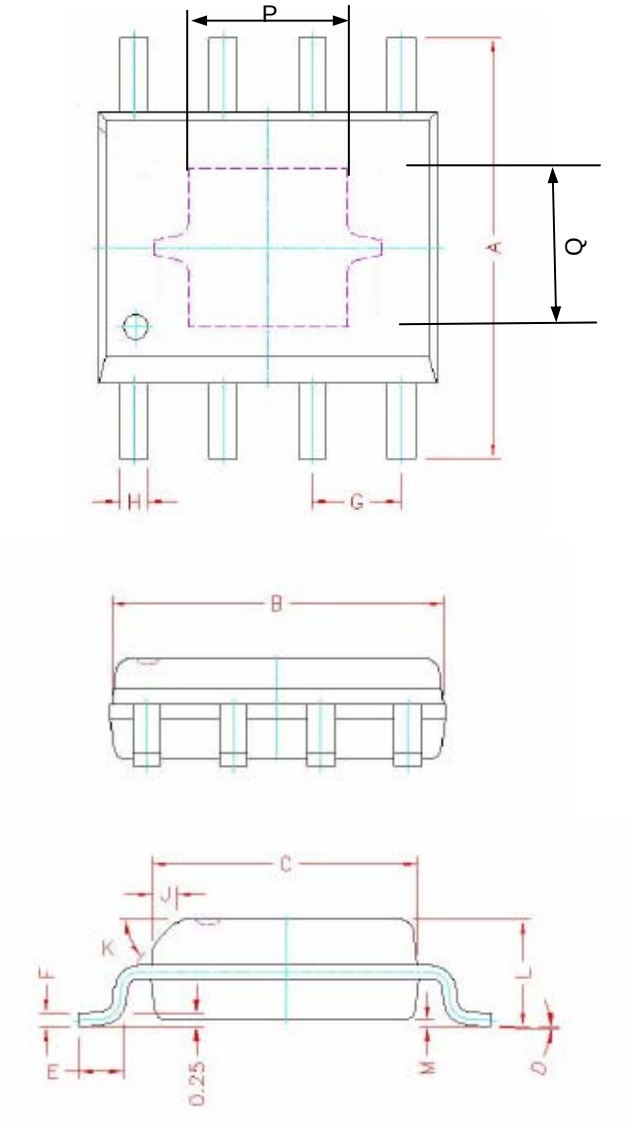
V_{IN} = 1.8V, V_{CNTL} = 3.3V

Output Short-Circuit Protection (Source)



V_{IN} = 1.8V, V_{CNTL} = 3.3V

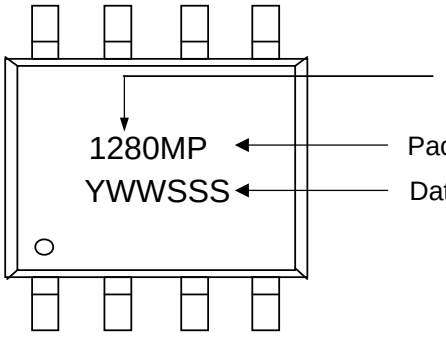
Package Dimensions: ESOP-8



	Millimeters		
SYMBOLS	MIN	NOM	MAX
A	5.80	6.00	6.20
B	4.80	4.90	5.00
C	3.80	3.90	4.00
D	0°	4°	8°
E	0.40	0.65	0.90
F	0.19	0.22	0.25
M	0.00	0.08	0.15
H	0.35	0.42	0.49
L	1.35	1.55	1.75
J	0.375 REF.		
K	45°		
G	1.27 TYP.		
P	2.15	2.25	2.35
Q	2.15	2.25	2.35

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information



Product : AP1280

Package code : MP = RoHS-compliant halogen-free ESOP-8

Date/lot code (YWWSSS)

Y: Last digit of the year
W: Work week
SSS: Lot code sequence