**CML Microcircuits** 

COMMUNICATION SEMICONDUCTORS

# **Product Preview**

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## **CMX994** Direct Conversion Receiver IC



## DCRx has the Edge!

A direct conversion receiver (DCRx) can also be referred to as a zero-IF receiver; the terms homodyne and synchrodyne are also sometimes applied but these are really separate concepts from the DCRx of today.

Until recently most radio systems used the superheterodyne (superhet) receiver, which uses one or more mix-down stages to fixed intermediate frequencies (IFs). Each non-zero IF stage requires fixed-frequency filters to reject the image and select the wanted signal. The filters are bulky and not suited to IC integration. Their fixed Bandwidth (BW) also limits receiver flexibility.

A DCRx mixes the wanted RF signal down to zero Hertz in a single stage using a local oscillator (LO) tuned to the wanted RF channel frequency. Selectivity filtering and gain can now take place at baseband with practical, low power, analogue and digital circuits. DCRx eliminates the need for an image reject filter.

DCRx enables on-chip integration, allowing a very small RF receiver to be realised with minimal external components. Improvements in semiconductor technologies have seen DCRx increasingly displace superhet as the technology choice for radio receivers in many applications.

The small size and flexibility of direct conversion make it a key element for the next generation of multichannel, multi-mode, software defined radios (SDR) for wireless data and digital two-way radio Applications.



## **CMX994 Brief Description**

The CMX994 is a direct conversion receiver IC. It includes a broadband LNA with gain control followed by a high dynamic range I/Q demodulator. The receiver baseband section includes amplifiers and precise baseband filter stages. LO generation is provided by an integer-N PLL and a VCO negative resistance amplifier; an external LO may also be used. LO dividers are provided for flexible multi-band operation.

The device operates from a single 3.3V supply over a temperature range of  $-40^{\circ}$ C to  $+85^{\circ}$ C and is available in a small 40-pin VQFN (Q4) package.

### **Features**

- Rx Direct Conversion Receiver
- Direct conversion eliminates image responses
- LNA with gain control
- 100MHz to 940MHz I/Q demodulator
- Extended operation down to 50MHz
- Precise filtering with bandwidth setting and 1:2:4 bandwidth modes
- Local Oscillator
- LO synthesiser
- VCO negative resistance amplifier
- LO divide by 2, 4 or 6 modes
- Tx LO Output
- 3.0 3.6V Low-power operation
- Small size 40-pin VQFN package

## **Applications**

- Analogue/digital multi-mode radio
- Software Defined Radio (SDR)
- Data telemetry modems
- Satellite communications
- Constant envelope and linear modulation
- Narrowband: e.g. 25kHz, 12.5kHz, 6.25kHz
- Wideband

## **Key Benefits**

- Highest integration for an RF Rx function
- Minimum of external components
- DCRx eliminates image responses
- Can be used in zero and low IF systems
- On-chip LNA with digital gain control
- Precise filtering for digital compensation
- On-chip filtering eases converter dynamic range requirement
- Overall lowest cost solution
- Smallest PCB area requirement
- Ideally suited to multi-band, multichannel bandwidth, SDR applications
- On-chip PLL
- On-chip VCO for up to 500MHz operation
- Single-ended RF connections (no baluns)
- Compatible with CMX998 FBL transmitter



#### System Diagram



## **General Description**

The CMX994 is a receiver IC featuring I/Q demodulators intended for use as a direct conversion receiver. The device has flexible LO inputs, integer-N PLL and an on-chip negative resistance amplifier which, with the addition of suitable external components, provides a VCO.

The receiver is fully integrated with a Low Noise Amplifier (LNA) preceding the down-converter section. The LNA may be configured with one of two possible output impedance settings ( $100\Omega$  or  $50\Omega$ ). With the  $50\Omega$  mode selected, gain of approximately 3dB higher will be achieved but the circuit will consume an additional 2mA of current. It should be noted that, as the output impedance is not the same for each setting, the required matching components between the LNA and mixer will be different for each case.

The high-linearity down-converting mixers are immediately followed by a baseband filter stage. The bandwidth of this section is set by external capacitors. This first stage of filtering is designed to remove off-channel blocking signals prior to baseband amplification. Following these filters, gain is applied via a variable gain amplifier. Further filtering is then applied and again the bandwidth of the filters is determined by external capacitors. A reference resistor must also be fitted; this is used to calibrate the internal filter circuits to ensure the cut-off point of the filters is accurately controlled. This system allows effective correction for the analogue response to be applied in signal processing following the CMX994. The output of the CMX994 is differential I/Q signals; these may be applied to analogue-to-digital converters such as those in the CMX981, CMX910, CMX7163 or the CMX7164 ICs.

The receiver I/Q chain includes the facility to correct for inherent dc offsets in the hardware. This process is intended to optimise the dynamic range of the system and must be controlled by the microprocessor or DSP that processes the I/Q signals from the CMX994. DC offsets are a well known issue with direct conversion receivers. In dynamic signal environments dc offset removal algorithms will be required to track and remove dc offsets generated by off-channel signals.

The receiver sections have a low-power mode which reduces the current drawn by the device. This mode may be used where degraded intermodulation performance can be accepted.

The Local Oscillator section features an integer-N Phase Locked Loop (PLL). This may be used with the on-chip VCO or with an external VCO. The on-chip VCO consists of a negative resistance amplifier and buffers, which allows an external inductor together with external varactor diodes to determine the operating frequency and tuning range. The use of external components allows optimum phase noise to be achieved. The Rx LO signal may be divided by 2, 4 or 6. There is also a Tx LO output provided and the Tx LO signal may be divided by 1, 2, 4 or 6. Alternatively the on-chip PLL and VCO can be disabled and an external LO source supplied.

All the features of the CMX994 may be controlled by the C-BUS control interface.



#### **Pin-out**

Pin No	Pin Name	Туре	Pin Function
1	IFLT2N	IP	I channel 2 <sup>nd</sup> filter capacitor negative
2	IFLT1P	IP	I channel 1 <sup>st</sup> filter capacitor positive
3	IFLT1N	IP	I channel 1 <sup>st</sup> filter capacitor negative
4	VCCRXIF	PWR	Supply for baseband circuits
5	VCCLNA	PWR	Supply for LNA
6	LNAIN	IP	LNA input
7	LNAOUT	OP	LNA output
8	VCCRF	PWR	Supply for RF circuits
9	MIXIN	IP	Rx mixer input
10	TXLO	OP	LO output for Tx
11	VCCLO	PWR	Supply for LO sections
12	LOP	IP	PLL LO positive input
13	LON	IP	PLL LO negative input
14	VCOP1	IP	PLL VCO positive input 1
15	VCOP2	IP	PLL VCO positive- input 2
16	VCON1	IP	PLL VCO1 negative input 1
17	VCON2	IP	PLL VCO1 negative input 2
18	VCCSYNTH	PWR	Supply to Integer N PLL
19	FREF	IP	Reference frequency input
20	DO	OP	PLL Charge Pump output
21	DGND	PWR	Digital ground
22	TXEN	IP	Tx Enable
23	RXEN	IP	Rx Enable
24	CSN	IP	C-BUS Chip Select
25	RDATA	TSOP	C-BUS Data output
26	SCLK	IP	C-BUS Clock input
27	CDATA	IP	C-BUS Data input
28	RESETN	IP	C-BUS/Device Reset (Reset when pin Low)
29	DVDD	PWR	Supply to digital circuits
30	VDDIO	PWR	Supply to C-BUS circuits
31	RREF	IP	Reference resistor for I/Q Filters
32	QFLT1N	IP	Q channel 1 <sup>st</sup> filter capacitor negative
33	QFLT1P	IP	Q channel 1 <sup>st</sup> filter capacitor positive
34	QFLT2N	IP	Q channel 2 <sup>nd</sup> filter capacitor negative
35	QFLT2P	IP	Q channel 2 <sup>nd</sup> filter capacitor positive
36	RXQP	OP	RXQ positive output
37	RXQN	OP	RXQ negative output
38	RXIP	OP	RXI positive output
39	RXIN	OP	RXI negative output
40	IFLT2P	IP	I channel 2 <sup>nd</sup> filter capacitor positive
Exposed Metal Pad	AGND	PWR	The exposed metal pad must be electrically connected to analogue ground



## **Evaluation Support**

The CMX994 can be evaluated with the EV9942; CMX994 evaluation kit. Interfacing to a PC can be achieved with our PE0002 universal interface board, with GUI and scripts available to assist product evaluation. Alternatively any microcontroller evaluation/emulator kit can be used to drive the CMX994's serial bus.



## **Electrical Specification Summary**

Operating Limits	Min	Max	Unit
$AV_{DD}$ and $DV_{DD}$	3.0	3.6	V
IO Supply (VDD <sub>IO</sub> )	1.6	3.6	v
Operating Temperature	-40	+85	°C

DC Parameter - Supply Current	Min	Тур	Max	Unit
Total Current Consumption				
Powersave Mode		25		μΑ
V <sub>BIAS</sub> Only		1.7		mA
Operating Currents				
Rx Only		66		mA
Rx Only, Low Power Mode		56		mA
Tx Only		22		mA
Stage Currents				
LNA Only		9		mA
LNA in 50 $\Omega$ Output Mode		11		mA
I/Q Demodulator		41		mA
Baseband I/Q		13		mA
VCO and Buffer		10		mA
LO Input		5		mA
PLL		5.5		mA
Current from VDDIO			600	μΑ

## **Package Options**



## **Typical Performance**

CMX994 testing on EV9942 evaluation kit (4-FSK modulation, 25kHz channels, 3kHz deviation, 19200bps, 448MHz)

- Intermodulation (EN 300 113 Method) = 65dB
- Sensitivity (1% BER) = -116dBm
- Blocking (EN 300 113 Method) = 90dB
- Adjacent Channel Rejection (EN 300 113, LO = EV9942 VCO/PLL) = 66 dB
- Adjacent Channel Rejection (EN 300 113, LO = Signal generator) = 73dB

Input Level (dBm)	BER
-114	2.29E-06
-116	3.89E-05
-118	5.68E-04
-120	3.94E-03
-121	8.77E-03
-122	1.55E-02

**Q4 Mechanical Outline:** 

Order as part no. CMX994Q4

Comprehensive technical datasheet and support material is available from the CML website.

Click here to link to the CML website or search for: CMX994

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