# Ultra-Low On-Resistance 4A Load Switch

## Features

- Integrated 4A Single Channel Load Switch
- Input Voltage Range: 0.8V to 5.5V
- Ultra-low On-Resistance
  RON=22mΩ at Vin=5V (VBIAS=5V)
  RON=22mΩ at Vin=1.8V (VBIAS=5V)
- Low Threshhold Control Input
- Adjustable Rise Time
- Integrated Quick Output Discharge
- ESD Level: 2kV for HBM, 1kV for CDM
- RoHS-Compliant, halogen-free

## Applications

- Telecom Systems
- Industrial Systems
- Set-Top Boxes
- Consumer Electronics
- Handheld Products

## Description

The APE8937-HF-3 is a small single load switch with ultra-low RON of 22mΩ and controlled turn-on, using an N-channel MOSFET that can operate over an input voltage range of 0.8V to 5.5V and support maximum continuous current up to 4A.

The switch is controlled by an on/off input (EN), which is capable of interfacing directly with low-voltage control signals.

Additional features include a 300Ω on-chip load resistor for output quick discharge when the switch is turned off. In order to avoid inrush current, the rise time is adjustable using an external ceramic capacitor on the CT pin.

The APE8937-HF-3 is available in an ultra-small, space-saving 2mmx2mm 8-pin DFN package with a thermal pad.

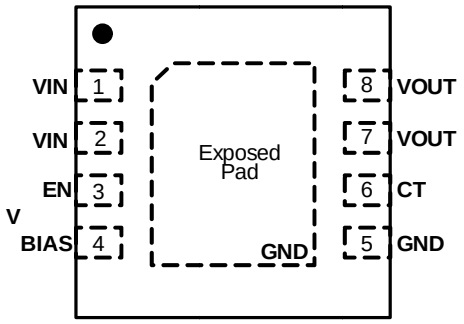
## Ordering Information

**APE8937GN2-HF-3TR**

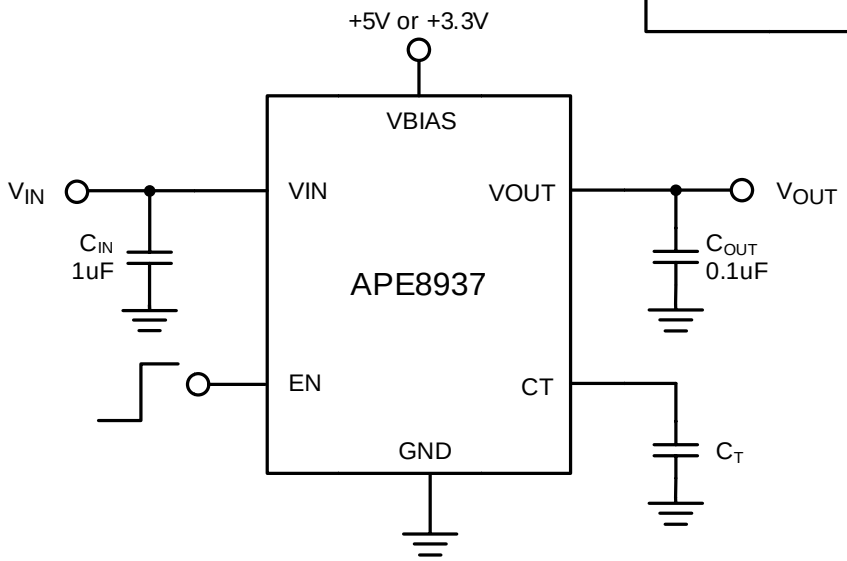
Package Type
GN2 : DFN2x2-8L

## Pin Configuration

Top View
DFN2x2-8L




## Typical Application Circuit



## Absolute Maximum Ratings (Note 1) at $T_A$= 25°C

| | |
|---|---|
| VIN | -0.3V to 6V |
| VOUT | VIN+0.3V |
| EN, CT | -0.3V to 6V |
| VBIAS | -0.3+6V |
| $I_{MAX}$ | 4A |
| Storage Temperature Range ($T_{ST}$) | -65 to +150°C |
| Junction Temperature ($T_J$) | 150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Thermal Resistance from Junction to Ambient, Rth(ja) | |
| DFN-8L (2mmX2mm) | 100°C/W |
| Thermal Resistance from Junction to Case (thermal pad), Rth(jc) | |
| DFN-8L (2mmX2mm) | 20°C/W |
| Electrostatic Discharge (ESD) | |
| HBM (MIL-STD 883G Method 3015.7) | 2kV |
| CDM (JESD22-C101-C) | 1kV |

## Recommended Operating Conditions

| | |
|---|---|
| VIN | 0.8V to 5.5V |
| VBIAS | 2.5V to 5.5V (VBIAS > VIN) |
| VOUT | VIN1 |
| CIN | >0.1uF |
| Junction Temperature ($T_J$) | 125°C |
| Operating Temperature Range | -40°C to +85°C |

**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be guaranteed. For guaranteed specifications and test conditions see the Electrical Specifications.

**Note2:** The maximum power dissipation is a function of the maximum junction temperature, $T_{Jmax}$, total thermal resistance, $R_{th(ja)}$ and ambient temperature $T_A$. The maximum allowable power dissipation at any ambient temperature is $(T_{jmax} - T_A) / R_{th(ja)}$.

**Note3:** Low duty pulse techniques are used during test to maintain a junction temperature as close to ambient as possible.

## Electrical Specifications

(VIN=0.8V to 5.5V, VBIAS=5V, CIN=1uF, COUT=0.1uF, TA=25°C, unless otherwise specified)

| PARAMETER | SYM | TEST CONDITION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Quiescent Current | $I_{BIAS}$ | $V_{BIAS}=V_{IN}=V_{EN}=5V$, $I_{OUT}=0A$ | | | 50 | 75 | uA |
| | | $V_{BIAS}=V_{IN}=V_{EN}=2.5V$, $I_{OUT}=0A$ | | | 30 | 50 | uA |
| Shutdown Current | $I_{SD}$ | $V_{EN}$=GND | | | | 1 | uA |
| ON Resistance(Note2) | $R_{ON}$ | $V_{BIAS}=V_{IN}=V_{EN}=5V$, $I_{OUT}$=200mA | $T_A$=25°C | | 22 | 26 | mΩ |
| | | | -40~85°C(NOTE1) | | | 33 | |
| | | $V_{BIAS}=V_{IN}=V_{EN}=2.5V$, $I_{OUT}$=200mA | $T_A$=25°C | | 23 | 27 | mΩ |
| | | | -40~85°C(NOTE1) | | | 34 | |
| Output Pull Down Resistance | $R_{OPD}$ | $V_{BIAS}$=5V, $V_{EN}$=0V | | | 300 | 350 | Ω |
| EN Input Leakage Current | $I_{ON}$ | $V_{EN}$=5V or GND | | | | 1 | uA |
| EN Threshold | $V_{ENH}$ | on | | 1.2 | | | V |
| | $V_{ENL}$ | off | | | | 0.5 | V |

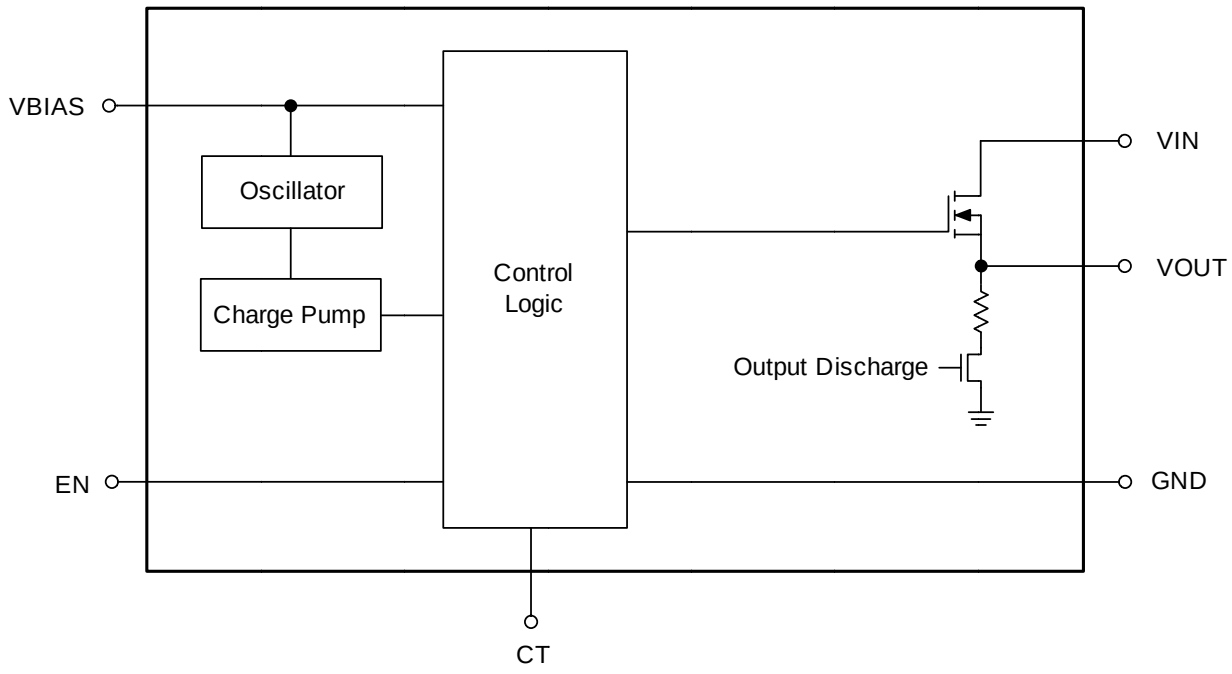
Note1: Guaranteed by design, not production tested

Note2: Make sure $V_{BIAS} \geqq V_{IN}$ for optimum $R_{ON}$ performance.

## Pin Descriptions

| PIN No. | PIN SYMBOL | PIN DESCRIPTION |
|---|---|---|
| 1, 2 | VIN | Input power supply; bypass this input with a ceramic capacitor to ground. |
| 3 | EN | Enable control input, active high. Do not leave floating. |
| 4 | VBIAS | Bias voltage. |
| 5 | GND | Ground. |
| 6 | CT | A capacitor to ground set the rise time of VOUT. |
| 7, 8 | VOUT | Switch output |
| Exposed pad | GND | Tie to ground to alleviate thermal stress. |

## Block Diagram



## Timing Specifications

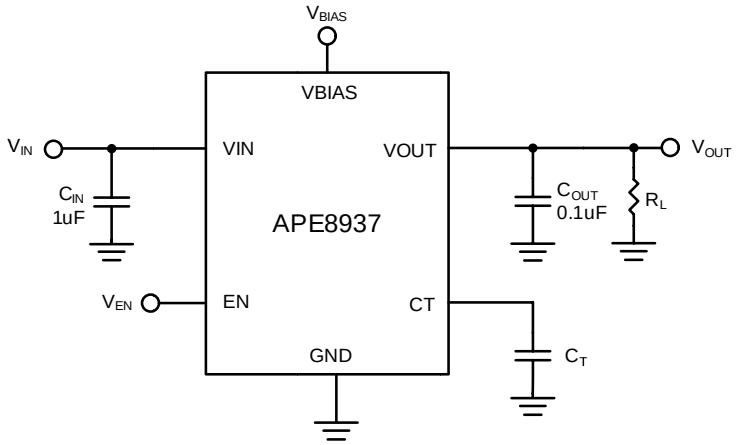



Fig.1 Test Circuit

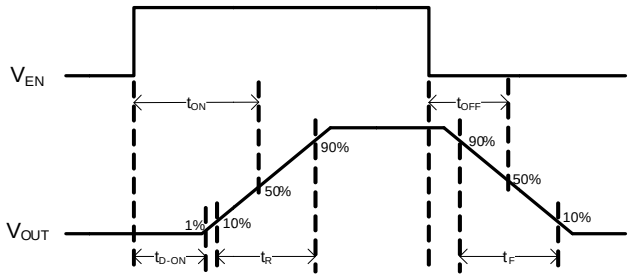



Fig.2 ON/OFF Waveforms

| PARAMETER | SYM | TEST CONDITION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Turn-on Time | $t_{ON}$ | $V_{BIAS}$=$V_{EN}$=5V, $C_T$=1nF, $R_L$=10Ω | $V_{IN}$=5V | | 1480 | | us |
| | | | $V_{IN}$=0.8V | | 520 | | us |
| Turn-off Time | $t_{OFF}$ | $V_{BIAS}$=$V_{EN}$=5V, $C_T$=1nF, $R_L$=10Ω | $V_{IN}$=5V | | 1 | | us |
| | | | $V_{IN}$=0.8V | | 1 | | us |
| VOUT Rise Time | $t_R$ | $V_{BIAS}$=$V_{EN}$=5V, $C_T$=1nF, $R_L$=10Ω | $V_{IN}$=5V | | 1910 | | us |
| | | | $V_{IN}$=0.8V | | 290 | | us |
| VOUT Fall Time | $t_F$ | $V_{BIAS}$=$V_{EN}$=5V, $C_T$=1nF, $R_L$=10Ω | $V_{IN}$=5V | | 1.9 | | us |
| | | | $V_{IN}$=0.8V | | 1.6 | | us |
| VOUT Turn-on Delay Time | $t_{D-ON}$ | $V_{BIAS}$=$V_{EN}$=5V, $C_T$=1nF, $R_L$=10Ω | $V_{IN}$=5V | | 310 | | us |
| | | | $V_{IN}$=0.8V | | 270 | | us |

## Typical Performance Characteristics

Condition: $V_{BIAS}$=5V, $V_{EN}$=3.3V, CT=1nF, $C_{IN}$=1µF, $C_{OUT}$=0.1µF, Io=4A, ch1:EN, ch2:$V_{OUT}$, ch4:$I_{IN}$

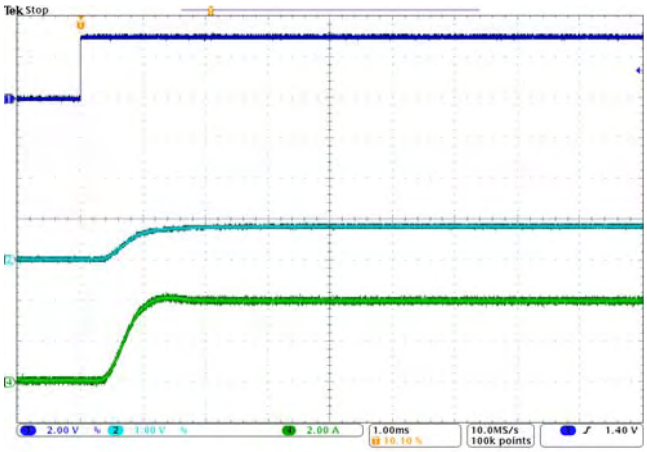


Fig.3 Start-up Waveform, VIN=0.8V

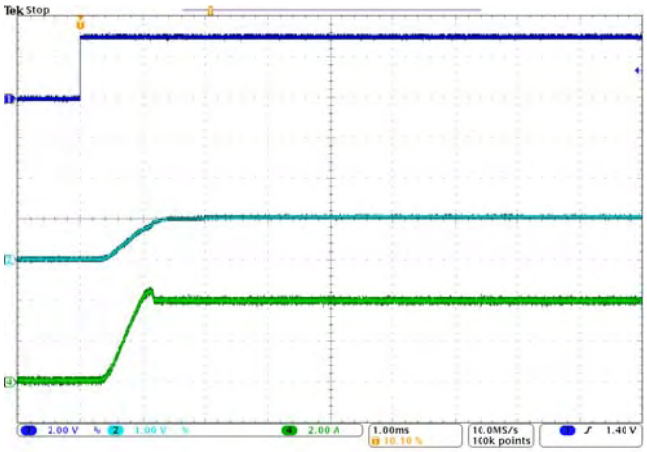


Fig.4 Start-up Waveform, VIN=1.05V

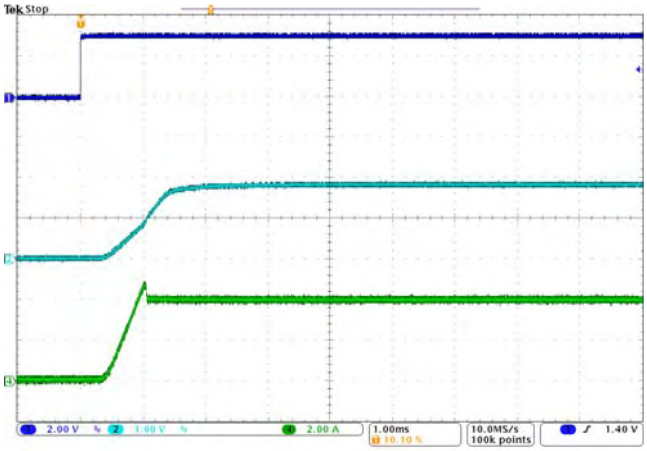


Fig.5 Start-up Waveform, VIN=1.8V

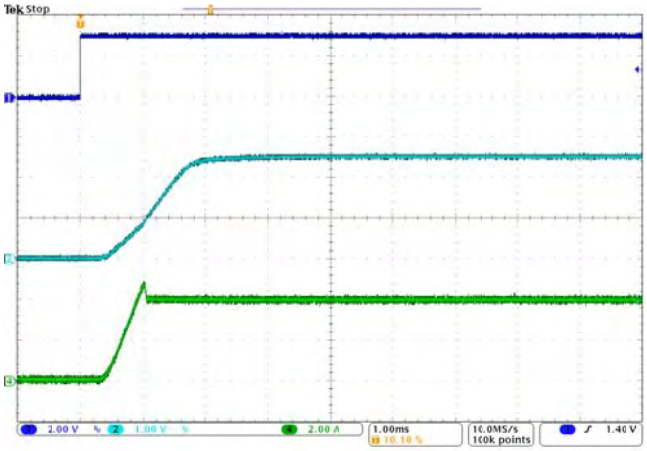


Fig.6 Start-up Waveform, VIN=2.5V

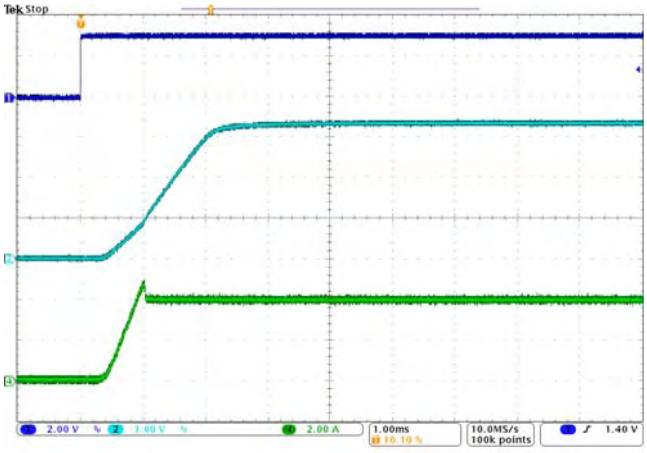


Fig.7 Start-up Waveform, VIN=3.3V

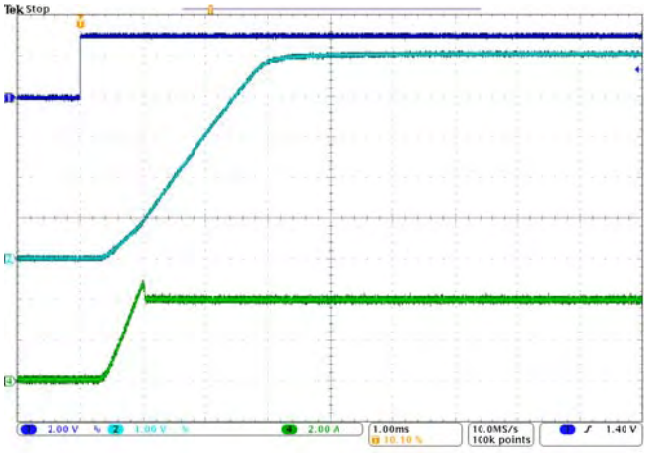


Fig.8 Start-up Waveform, VIN=5.0V

## Typical Performance Characteristics (continued)

Condition: $V_{BIAS}$=$V_{EN}$=3.3V, CT=1nF, $C_{IN}$=1µF, $C_{OUT}$=0.1µF, Io=4A, ch1:EN, ch2:$V_{OUT}$, ch4:$I_{IN}$

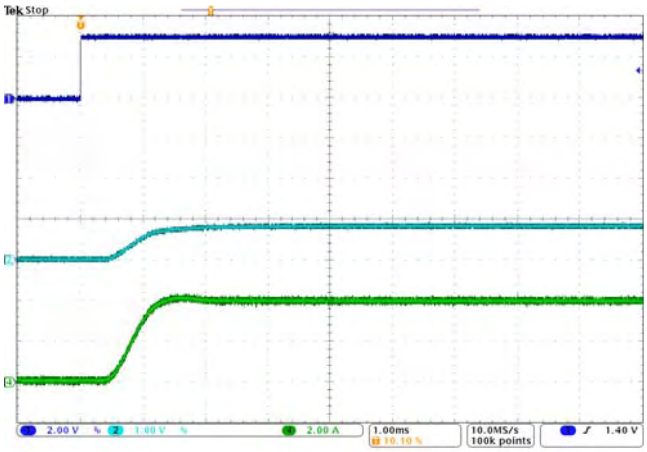


Fig.9 Start-up Waveform, VIN=0.8V

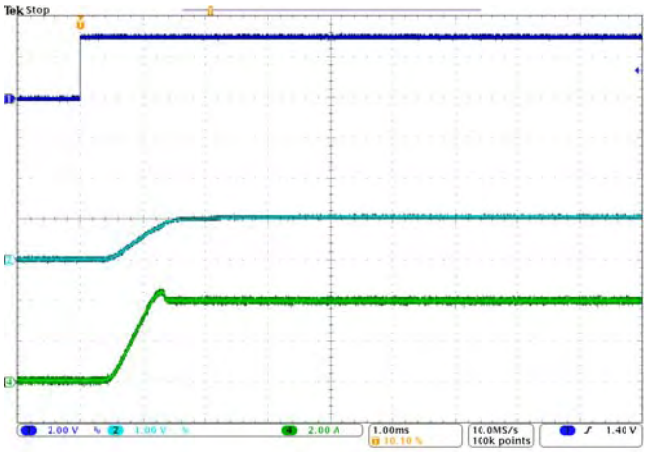


Fig.10 Start-up Waveform, VIN=1.05V

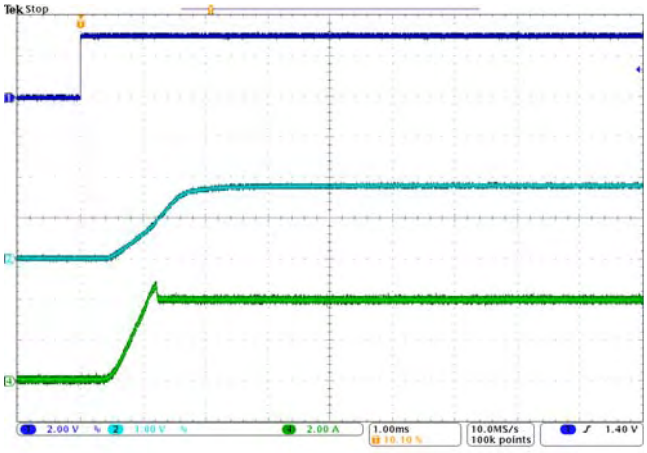


Fig.11 Start-up Waveform, VIN=1.8V

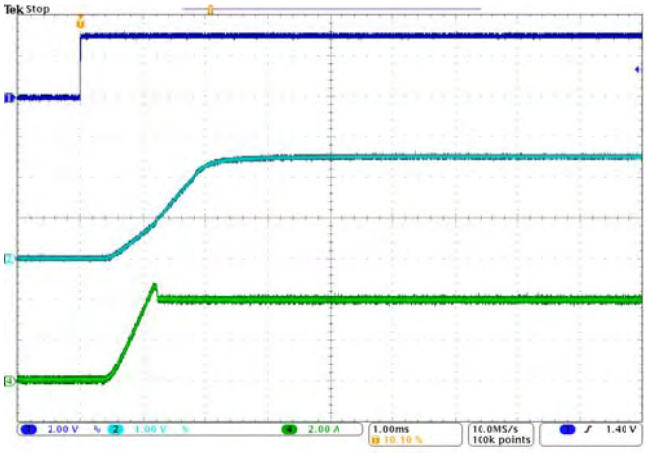


Fig.12 Start-up Waveform, VIN=2.5V

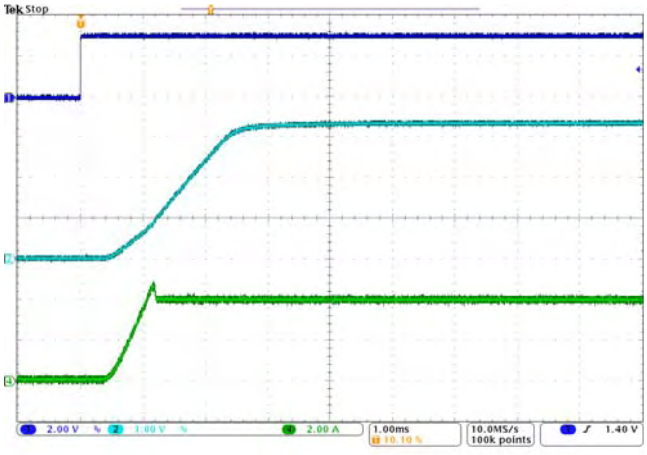


Fig.13 Start-up Waveform, VIN=3.3V

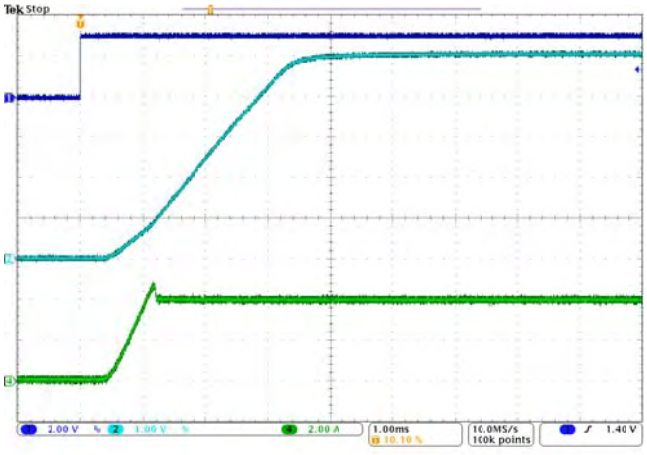


Fig.14 Start-up Waveform, VIN=5.0V

## Typical Performance Characteristics (continued)

Condition: $V_{BIAS}$=$V_{EN}$=5V, CT=1nF, $C_{IN}$=1μF, $C_{OUT}$=0.1μF, RL=10Ω, ch1:EN, ch2:$V_{OUT}$

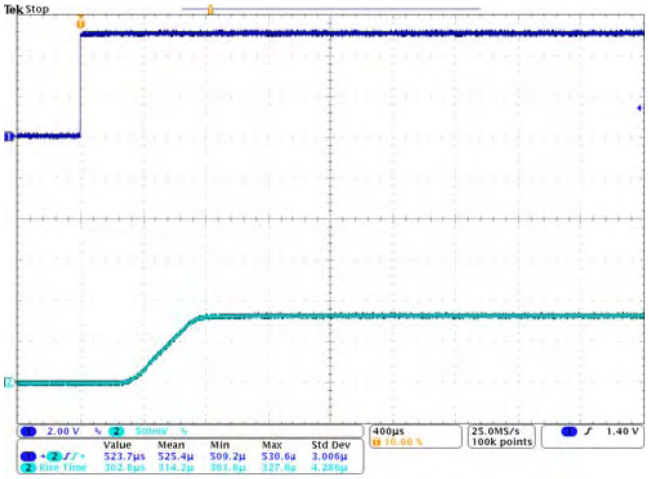


Fig.15 Turn-on Response Time, VIN=0.8V

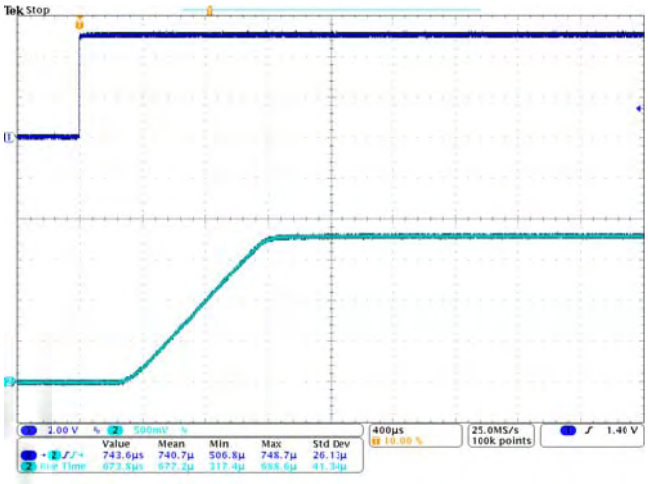


Fig.16 Turn-on Response Time, VIN=1.8V

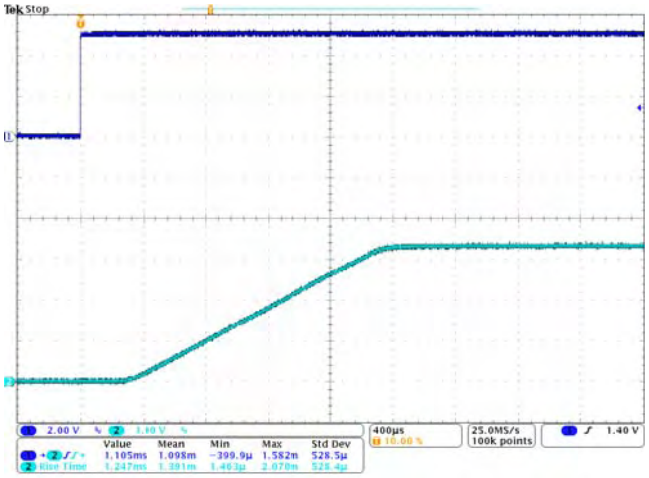


Fig.17 Turn-on Response Time, VIN=3.3V

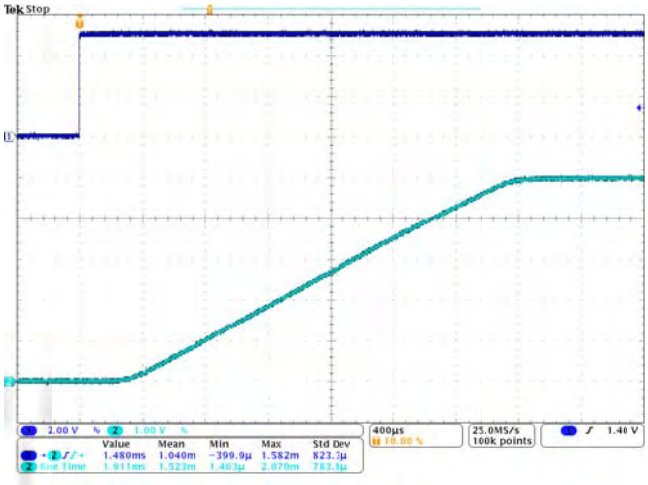


Fig.18 Turn-on Response Time, VIN=5V

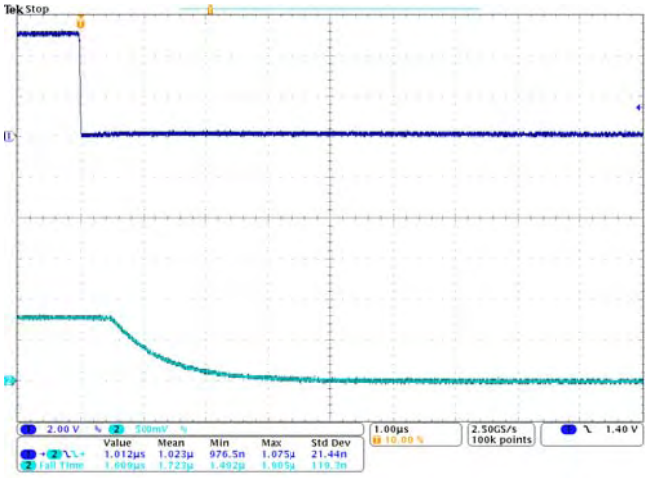


Fig.19 Turn-off Response Time, VIN=0.8V

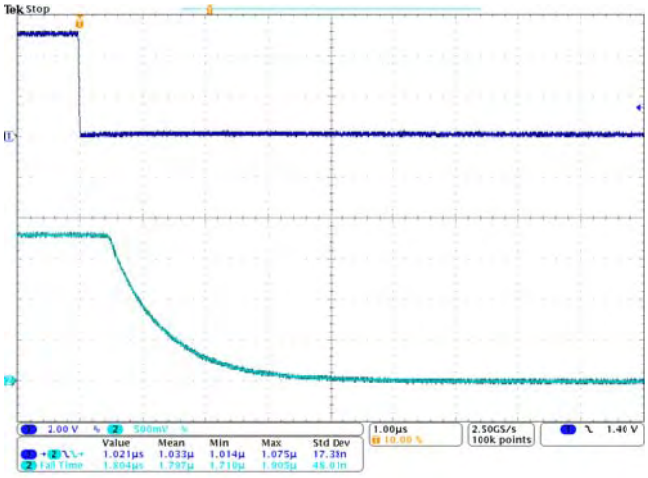


Fig.20 Turn-off Response Time, VIN=1.8V

## Typical Performance Characteristics (continued)

Condition: $V_{BIAS}$=$V_{EN}$=5V, CT=1nF, $C_{IN}$=1µF, $C_{OUT}$=0.1µF, RL=10Ω, ch1:EN, ch2:$V_{OUT}$

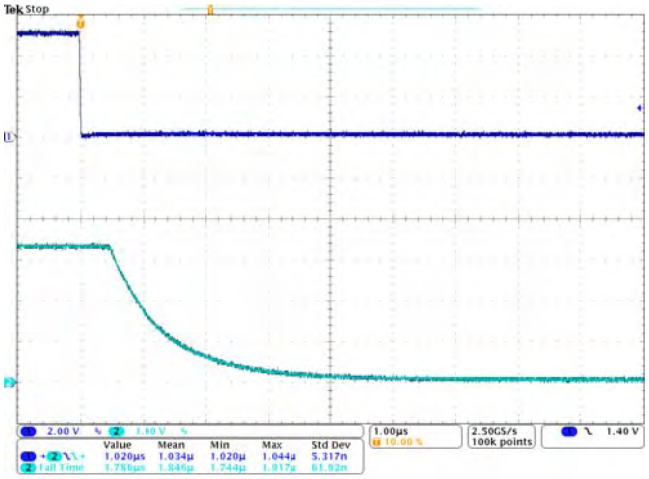


Fig.21 Turn-off Response Time, VIN=3.3V

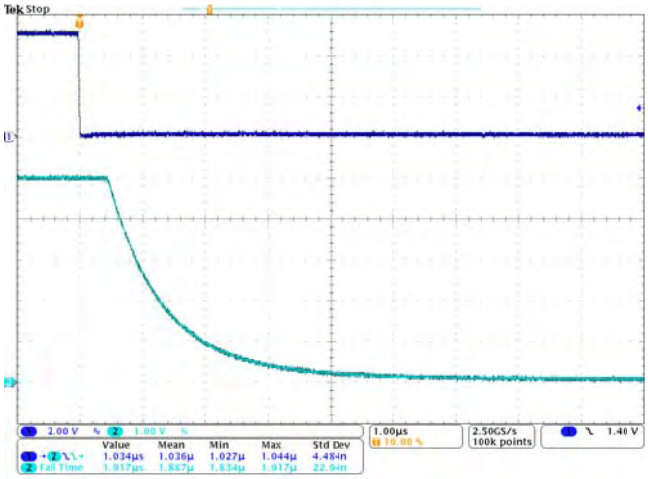


Fig.22 Turn-off Response Time, VIN=5V

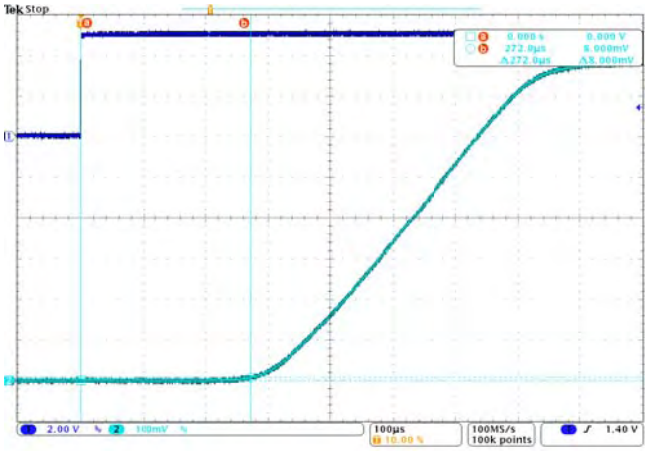


Fig.23 Turn-on Delay Time, VIN=0.8V

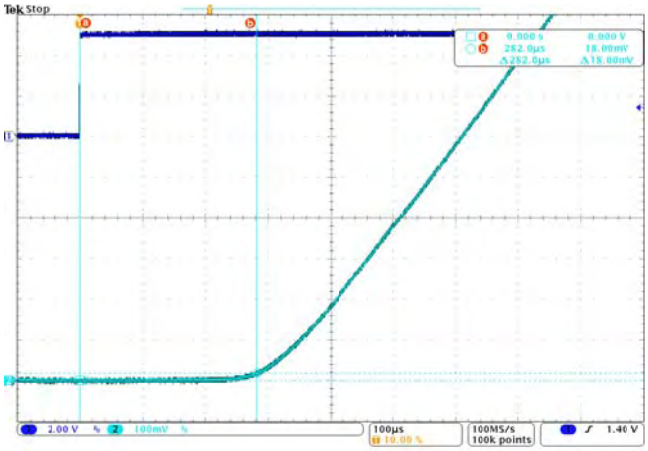


Fig.24 Turn-on Delay Time, VIN=1.8V

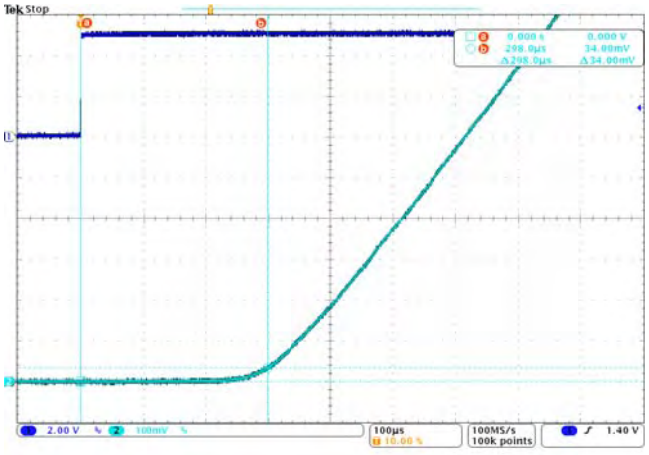


Fig.25 Turn-on Delay Time, VIN=3.3V

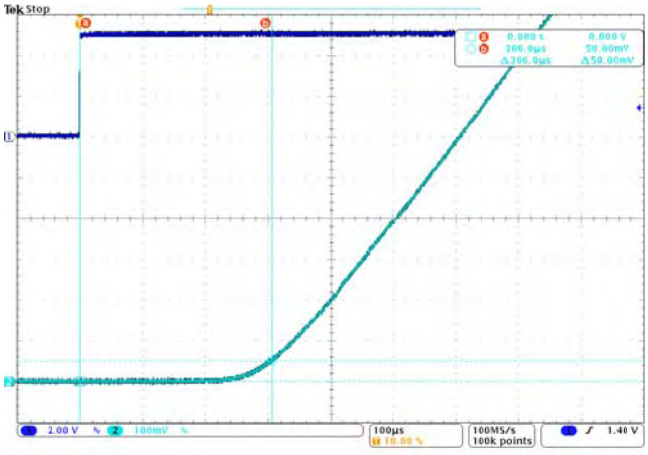


Fig.26 Turn-on Delay Time, VIN=5V

## Typical Performance Characteristics (continued)

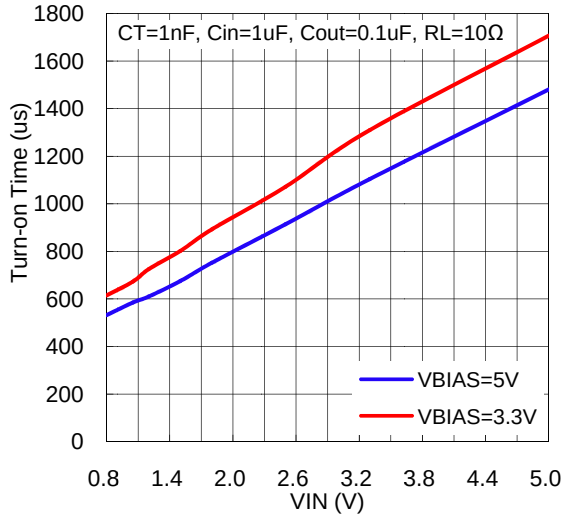



Fig.27 $t_{ON}$ vs. VIN

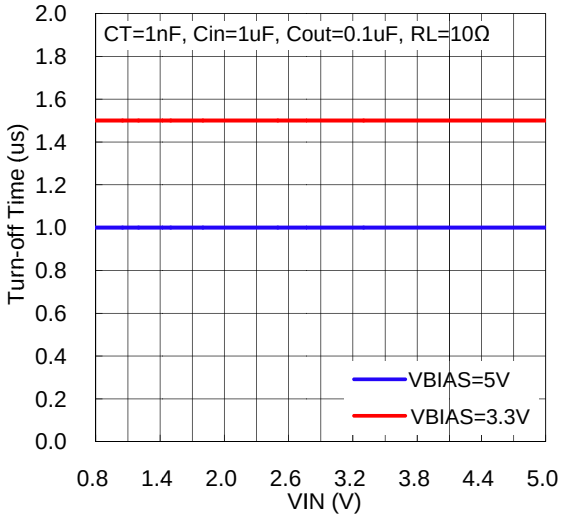



Fig.28 $t_{OFF}$ vs. VIN

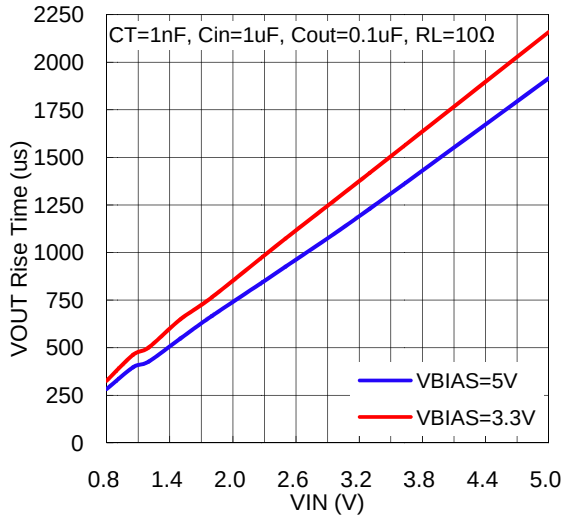



Fig.29 $t_R$ vs. VIN

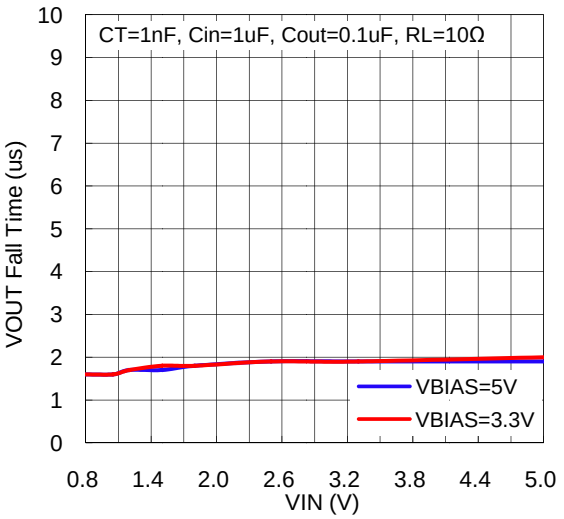



Fig.30 $t_F$ vs. VIN

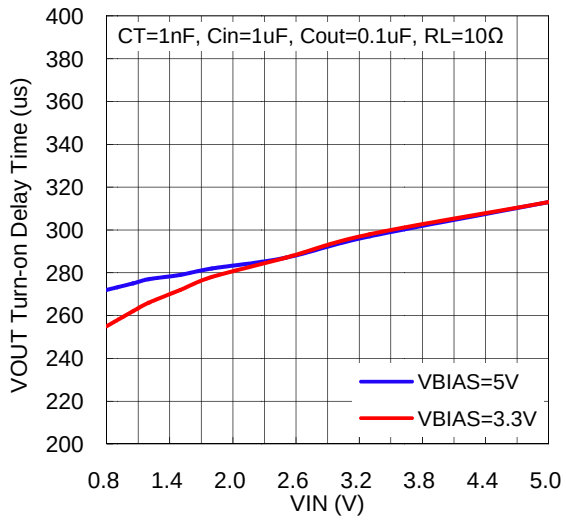



Fig.31 $t_{D\text{-}ON}$ vs. VIN

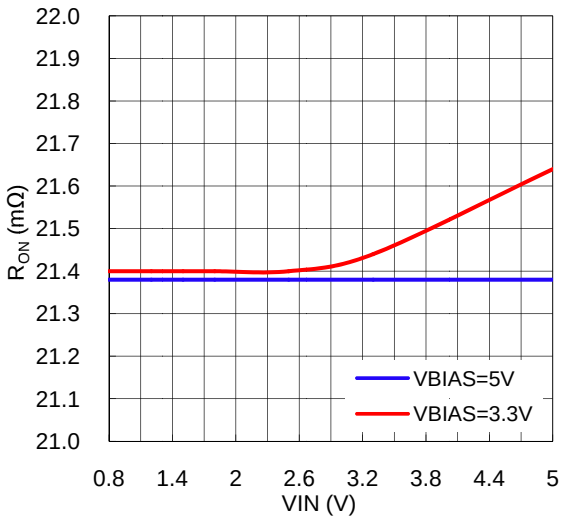



Fig.32 $R_{ON}$ vs. VIN

## Typical Performance Characteristics (continued)

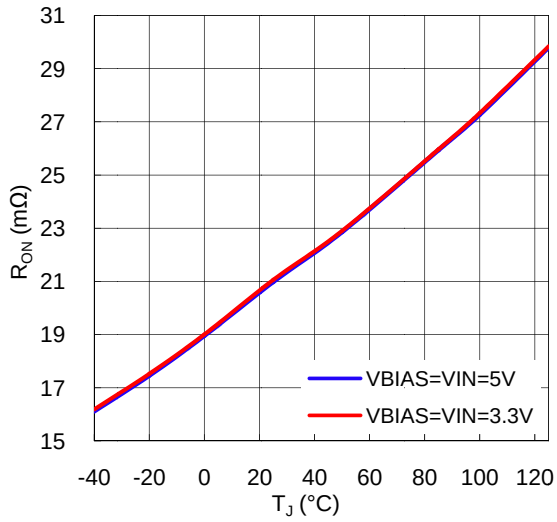



Fig.33 $R_{ON}$ vs. Temperature

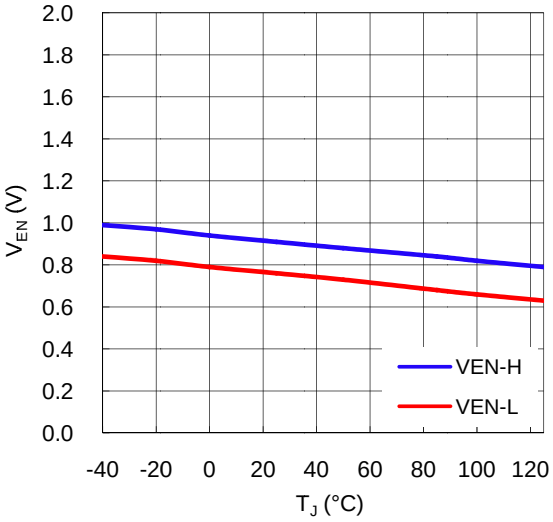



Fig.34 EN Threshold vs. Temperature

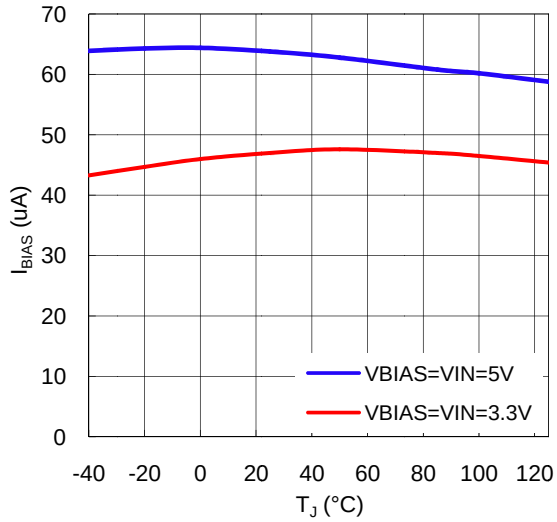



Fig.35 Quiescent Current vs. Temperature

## Application Information

**On/Off Control**

The load switch is controlled by the EN pin. The EN pin is active high and has a low threshold making it capable of interfacing with low voltage signals. The EN pin can be used with standard 1.2V, 1.8V, 2.5V or 3.3V GPIO logic threshold. Do not leave the EN pin floating.

**Output Rise Time Control**

The rise time of VOUT is adjustable by an external capacitor on the CT pin. The rise time shown in the table below is the typical measured value. Please refer to it for determining rise time.

| $C_T$ (nF) | VOUT Rise Time, $t_R$(µs), 10%~90%, $V_{BIAS}$=$V_{EN}$=5V, $C_{IN}$=1uF, $C_{OUT}$=0.1µF, $R_L$=10Ω | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | VIN=0.8V | VIN=1.05V | VIN=1.2V | VIN=1.5V | VIN=1.8V | VIN=2.5V | VIN=3.3V | VIN=5V |
| 0 | 29 | 38 | 40 | 48 | 53 | 63 | 76 | 100 |
| 0.22 | 85 | 114 | 125 | 168 | 190 | 260 | 329 | 501 |
| 0.47 | 151 | 208 | 218 | 287 | 334 | 435 | 601 | 946 |
| 1 | 302 | 397 | 427 | 548 | 673 | 926 | 1247 | 1911 |
| 2.2 | 610 | 865 | 924 | 1227 | 1448 | 1979 | 2736 | 4176 |
| 4.7 | 1228 | 1723 | 1872 | 2450 | 3000 | 4043 | 5583 | 8681 |
| 10 | 2227 | 3418 | 3624 | 4894 | 5689 | 8159 | 10830 | 16910 |

<Table 1>

**Input Capacitor**

An input capacitor is recommended to be placed between VIN and GND to limit the voltage drop on the input supply during high current application.

**Output Capacitor**

Setting a $C_{IN}$ greater than the $C_{OUT}$ is highly recommended. Since the internal body diode is in the NMOS switch, this prevents the current flows through the body diode from VOUT to VIN when the system supply is removed.

## Application Information (continued)

### Input Capacitor

An input capacitor is recommended to be placed between VIN and GND to limit the voltage drop on the input supply during high current applications.

### Output Capacitor

Setting a $C_{IN}$ greater than the $C_{OUT}$ is highly recommended. Since the MOSFET switch has an internal body diode, this prevents the flow of current through the body diode from VOUT to VIN when the system supply is removed.

### Layout Considerations

The figure below shows the suggested layout for the APE8937-HF-3. The list below will help with layout.

1. Keep the high current paths (VIN, VOUT and GND; blue circle) wide and short to obtain the best effect.
2. The input and output capacitors should be as close to the device as possible to minimize any parasitic trace inductances.
3. Place thermal vias under the exposed pad of the device (green circle). This helps with thermal diffusion away from the device.

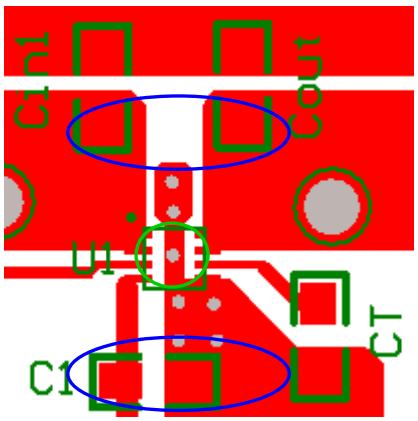
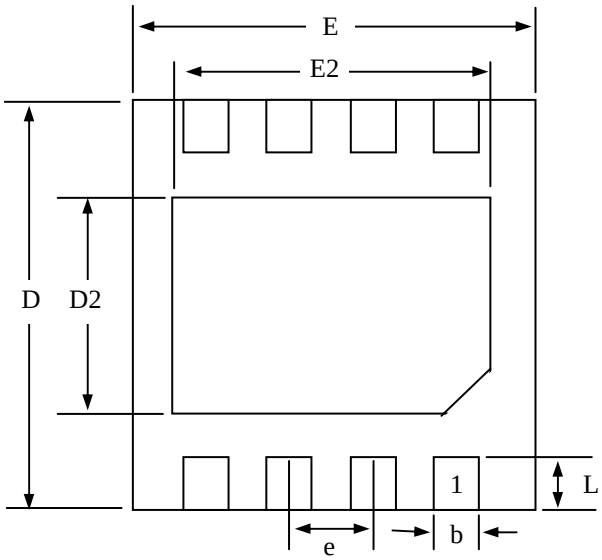


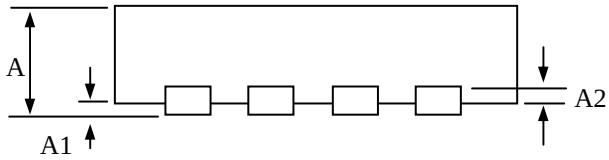

Fig.36 APE8937 Reference Layout

## Package Dimensions: DFN2X2-8L



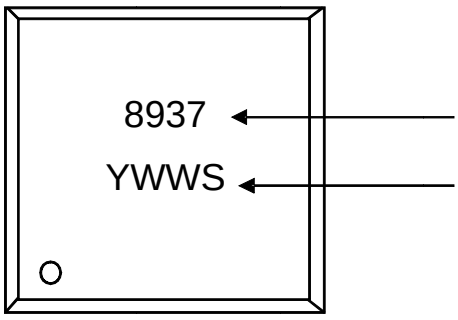

| SYMBOLS | Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.005 | 0.030 | 0.060 |
| A2 | 0.145 | 0.170 | 0.190 |
| b | 0.20 | 0.25 | 0.30 |
| D | 1.95 | 2.00 | 2.05 |
| D2 | 0.80 | 0.90 | 1.00 |
| E | 1.95 | 2.00 | 2.05 |
| E2 | 1.50 | 1.60 | 1.70 |
| e | 0.50 | | |
| L | 0.20 | 0.30 | 0.40 |

**BOTTOM VIEW**




1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

## Marking Information




Product : APE8937

Date/lot code (YWWS)

Y: Last digit of the year

WW: Work week

S: Lot code sequence